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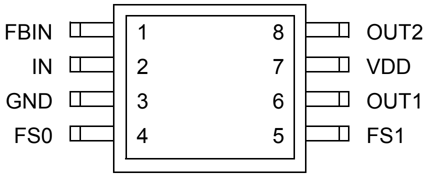
Pinouts

Figure 1. 8-pin SOIC pinout



Pin Definitions

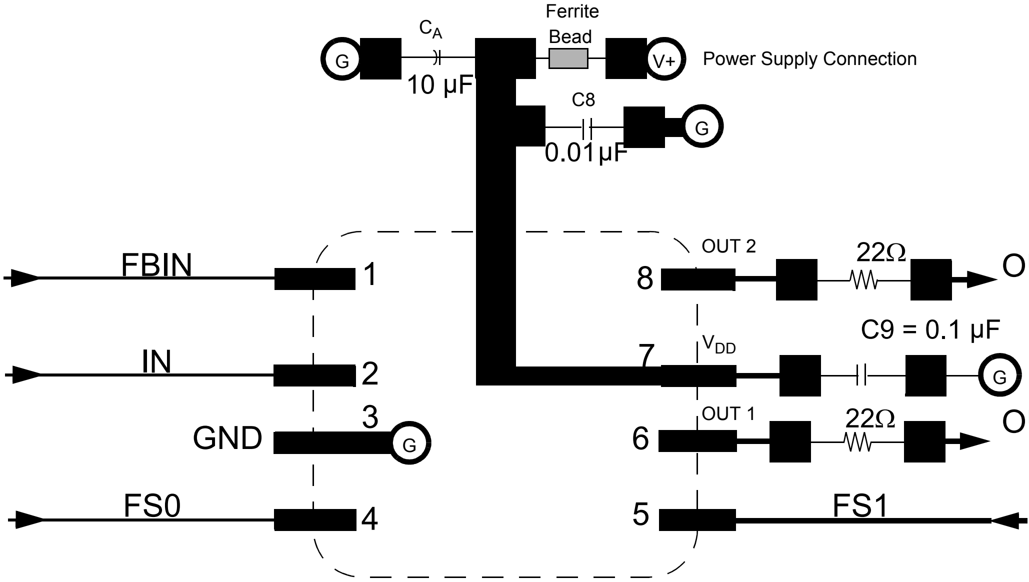
Pin Name	Pin No.	Pin Type	Pin Description
IN	2	I	Reference Input: The output signals are synchronized to this signal.
FBIN	1	I	Feedback Input: This input must be fed by one of the outputs (OUT1 or OUT2) to ensure proper functionality. If the trace between FBIN and the output pin being used for feedback is equal in length to the traces between the outputs and the signal destinations, then the signals received at the destinations are synchronized to the REF signal input (IN).
OUT1	6	O	Output 1: The frequency of the signal provided by this pin is determined by the feedback signal connected to FBIN, and the FS0:1 inputs (see Configuration Options on page 1).
OUT2	8	O	Output 2: The frequency of the signal provided by this pin is one-half of the frequency of OUT1. See Configuration Options on page 1.
VDD	7	P	Power Connections: Connect to 3.3 V or 5 V. This pin should be bypassed with a 0.1-µF decoupling capacitor. Use ferrite beads to help reduce noise for optimal jitter performance.
GND	3	P	Ground Connection: Connect all grounds to the common system ground plane.
FS0:1	4, 5	I	Function Select Inputs: Tie to V_{DD} (HIGH, 1) or GND (LOW, 0) as desired per Configuration Options on page 1.

Overview

The CY2302 is a two-output zero delay buffer and frequency multiplier. It provides an external feedback path allowing maximum flexibility when implementing the Zero Delay feature. This is explained further in the sections of this datasheet titled, How to Implement Zero Delay, and Inserting Other Devices in Feedback Path.

The CY2302 is a pin-compatible upgrade of the Cypress W42C70-01. The CY2302 addresses some application dependent problems experienced by users of the older device.

Figure 2. Schematic/Suggested Layout



How to Implement Zero Delay

Typically, Zero Delay Buffers (ZDBs) are used because a designer wants to provide multiple copies of a clock signal in phase with each other. The whole concept behind ZDBs is that the signals at the destination chips are all going HIGH at the same time as the input to the ZDB. In order to achieve this, layout must compensate for trace length between the ZDB and the target devices. The method of compensation is described as follows.

External feedback is the trait that allows for this compensation. The PLL on the ZDB causes the feedback signal to be in phase with the reference signal. When laying out the board, match the trace lengths between the output being used for feedback and the FBIN input to the PLL.

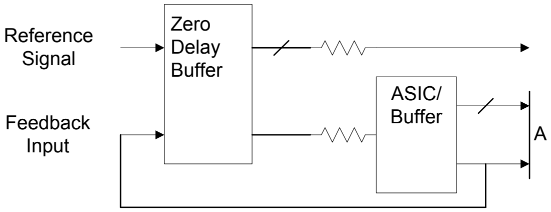
If it is desirable to either add a little delay, or slightly precede the input signal, this may also be implemented by either making the trace to the FBIN pin a little shorter or a little longer than the traces to the devices being clocked.

Inserting Other Devices in Feedback Path

Another nice feature available due to the external feedback is the ability to synchronize signals to the signal coming from some other device. This implementation can be applied to any device (ASIC, multiple output clock buffer/driver, etc.) that is put into the feedback path.

Referring to Figure 2, if the traces between the ASIC/Buffer and the destination of the clock signal(s) (A) are equal in length to the trace between the buffer and the FBIN pin, the signals at the destination(s) device is driven HIGH at the same time when the Reference clock provided to the ZDB goes HIGH. Synchronizing the other outputs of the ZDB to the outputs from the ASIC/Buffer is more complex however, as any propagation delay from the ZDB output to the ASIC/Buffer output must be accounted for.

Figure 3. Six Output Buffer in the Feedback Path



Phase Alignment

In cases where OUT1 (i.e., the higher frequency output) is connected to FBIN input pin the output OUT2 rising edges may be either 0 or 180° phase aligned to the IN input waveform (as set randomly when the input and/or power is supplied). If OUT2 is desired to be rising-edge aligned to the IN input's rising edge, then connect the OUT2 (i.e., the lowest frequency output) to the FBIN pin. This set-up provides a consistent input-output phase relationship.

Absolute Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Parameter	Description	Rating	Unit
V_{DD}, V_{IN}	Voltage on any pin with respect to GND	–0.5 to +7.0	V
T_{STG}	Storage temperature	–65 to +150	°C
T_A	Ambient operating temperature, commercial	0 to +70	°C
	Ambient operating temperature, industrial	–40 to +85	°C
T_B	Ambient temperature under bias	–55 to +125	°C
P_D	Power dissipation	0.5	W

DC Electrical Characteristics

T_A = 0 °C to 70 °C or –40 °C to 85 °C, V_{DD} = 3.3 V ± 5%

Parameter	Description	Test Condition	Min	Typ	Max	Unit
I_{DD}	Supply current	Unloaded, 100 MHz	–	17	35	mA
V_{IL}	Input low voltage	–	–	–	0.8	V
V_{IH}	Input high voltage	–	2.0	–	–	V
V_{OL}	Output low voltage	I_{OL} = 12 mA	–	–	0.4	V
V_{OH}	Output high voltage	I_{OH} = –12 mA	2.4	–	–	V
I_{IL}	Input low current	V_{IN} = 0V	–40	–	5	µA
I_{IH}	Input high current	V_{IN} = V_{DD}	–	–	5	µA

DC Electrical Characteristics

T_A = 0 °C to 70 °C or –40 °C to 85 °C, V_{DD} = 5 V ± 10%

Parameter	Description	Test Condition	Min	Typ	Max	Unit
I_{DD}	Supply current	Unloaded, 100 MHz	–	37	50	mA
V_{IL}	Input low voltage	–	–	–	0.8	V
V_{IH}	Input high voltage	–	2.0	–	–	V
V_{OL}	Output low voltage	I_{OL} = 12 mA	–	–	0.4	V
V_{OH}	Output high voltage	I_{OH} = –12 mA	2.4	–	–	V
I_{IL}	Input low current	V_{IN} = 0 V	–80	–	5	µA
I_{IH}	Input high current	V_{IN} = V_{DD}	–	–	5	µA

Thermal Resistance

Parameter [1]	Description	Test Conditions	8-pin SOIC	Unit
θ_{JA}	Thermal resistance (junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, in accordance with EIA/JESD51.	132	°C/W
θ_{JC}	Thermal resistance (junction to case)		43	°C/W

Note

1. These parameters are guaranteed by design and are not tested.

AC Electrical Characteristics

T_A = 0 °C to +70 °C or –40 °C to 85 °C, V_{DD} = 3.3 V ± 5% [2]

Parameter	Description	Test Condition	Min	Typ	Max	Unit
f_{IN}	Input Frequency [3]	–	5	–	133	MHz
f_{OUT}	Output Frequency	OUT1 15 pF load	10	–	133	MHz
t_R	Output Rise Time	0.8 V to 2.0 V, 15 pF load	–	–	3.5	ns
t_F	Output Fall Time	2.0 V to 0.8 V, 15 pF load	–	–	2.5	ns
t_{ICLKR}	Input Clock Rise Time [4]	–	–	–	10	ns
t_{ICLKF}	Input Clock Fall Time [4]	–	–	–	10	ns
t_D	Duty Cycle	15-pF load[5]	40	50	60	%
t_{LOCK}	PLL Lock Time	Power supply stable	–	–	1.0	ms
t_{JC}	Jitter, Cycle-to-Cycle	OUT1, f_{OUT} >30 MHz	–	200	300	ps
		OUT2, f_{OUT} >30 MHz	–	90	300	ps
t_{DC}	Die Out Time[6]	–	100	–	–	Clock Cycles
t_{SKEW}	Output-output Skew[7]	–	–	65	250	ps
t_{PD}	Propagation Delay[7]	–	–350	90	350	ps

Notes

[2] All AC specifications are measured with a 50Ω transmission line, load terminated with 50 Ω to 1.4 V.

[3] Input frequency is limited by output frequency range and input to output frequency multiplication factor (which is determined by circuit configuration).

[4] Longer input rise and fall time degrades skew and jitter performance.

[5] Duty cycle is measured at 1.4 V.

[6] 33 MHz reference input suddenly stopped (0 MHz). Number of cycles provided prior to output falling to <16 MHz.

[7] Skew is measured at 1.4 V on rising edges.

AC Electrical Characteristics

T_A = 0 °C to +70 °C or –40 °C to 85 °C, V_{DD} = 5.0 V ± 10% [8]

Parameter	Description	Test Condition	Min	Typ	Max	Unit
f_{IN}	Input Frequency [9]	–	5	–	133	MHz
f_{OUT}	Output Frequency	OUT1 15 pF load	10	–	133	MHz
t_R	Output Rise Time	0.8 V to 2.0 V, 15 pF load	–	–	2.5	ns
t_F	Output Fall Time	2.0 V to 0.8 V, 15 pF load	–	–	1.5	ns
t_{ICLKR}	Input Clock Rise Time [10]	–	–	–	10	ns
t_{ICLKF}	Input Clock Fall Time [10]	–	–	–	10	ns
t_D	Duty Cycle	15-pF load [11, 12]	40	50	60	%
t_{LOCK}	PLL Lock Time	Power supply stable	–	–	1.0	ms
t_{JC}	Jitter, Cycle-to-Cycle	OUT1, f_{OUT} >30 MHz	–	200	300	ps
		OUT2, f_{OUT} >30 MHz	–	90	300	ps
t_{DC}	Die out time [13]	–	100	–	–	Clock cycles
t_{SKEW}	Output-output Skew [14]	–	–	65	250	ps
t_{PD}	Propagation Delay [14]	–	–350	90	350	ps

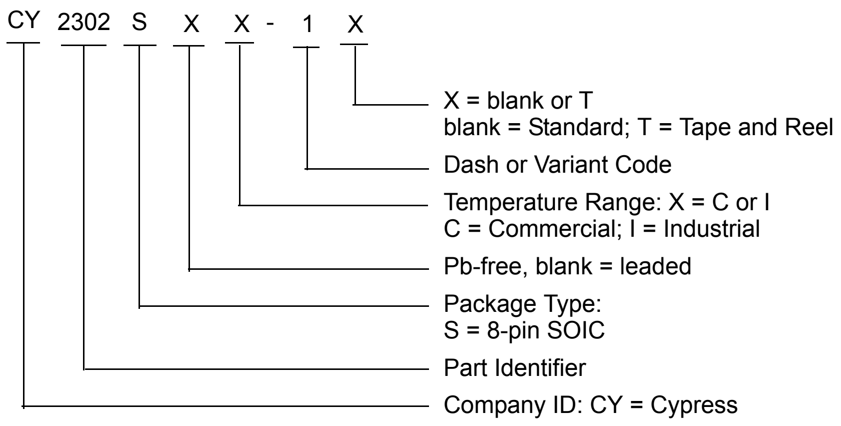
Notes

8. All AC specifications are measured with a 50Ω transmission line, load terminated with 50 Ω to 1.4 V.
9. Input frequency is limited by output frequency range and input to output frequency multiplication factor (which is determined by circuit configuration).
10. Longer input rise and fall time degrades skew and jitter performance.
11. Duty cycle is measured at 1.4 V.
12. Duty Cycle measured at 120 MHz. For 133 MHz, degrades to 35/65 worst case.
13. 33 MHz reference input suddenly stopped (0 MHz). Number of cycles provided prior to output falling to <16 MHz.
14. Skew is measured at 1.4 V on rising edges.

Ordering Information

Ordering Code	Package Type	Temperature Grade
Pb-free		
CY2302SXC-1	8-pin SOIC	Commercial (0 °C to 70 °C)
CY2302SXC-1T	8-pin SOIC – Tape and Reel	Commercial (0 °C to 70 °C)
CY2302SXI-1	8-pin SOIC	Industrial (–40 °C to 85 °C)
CY2302SXI-1T	8-pin SOIC – Tape and Reel	Industrial (–40 °C to 85 °C)

Ordering Code Definitions



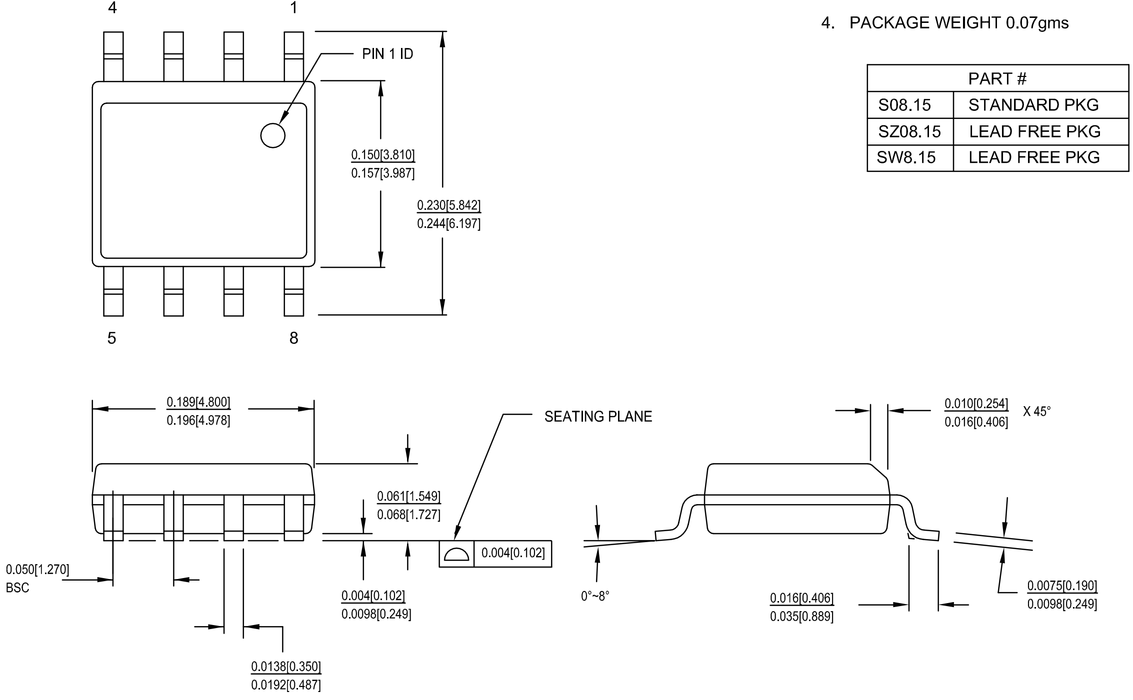
X = blank or T
blank = Standard; T = Tape and Reel
Dash or Variant Code
Temperature Range: X = C or I
C = Commercial; I = Industrial
Pb-free, blank = leaded
Package Type:
S = 8-pin SOIC
Part Identifier
Company ID: CY = Cypress

Package Diagram

Figure 4. 8-pin SOIC (150 Mils) S0815/SZ815/SW815 Package Outline, 51-85066

1. DIMENSIONS IN INCHES[MM] MIN.
   MAX.
2. PIN 1 ID IS OPTIONAL,
   ROUND ON SINGLE LEADFRAME
   RECTANGULAR ON MATRIX LEADFRAME
3. REFERENCE JEDEC MS-012
4. PACKAGE WEIGHT 0.07gms

PART #	
S08.15	STANDARD PKG
SZ08.15	LEAD FREE PKG
SW8.15	LEAD FREE PKG



51-85066 *H

Acronyms

Acronym	Description
FBK	Feedback
PLL	Phase Locked Loop
MUX	Multiplexer

Document Conventions

Units of Measure

Symbol	Unit of Measure	Symbol	Unit of Measure
°C	degree Celsius	µW	microwatt
dB	decibel	mA	milliampere
fC	femtocoulomb	mm	millimeter
fF	femtofarad	ms	millisecond
Hz	hertz	mV	millivolt
KB	1024 bytes	nA	nanoampere
Kbit	1024 bits	ns	nanosecond
kHz	kilohertz	nV	nanovolt
kΩ	kilohm	Ω	ohm
MHz	megahertz	ppm	parts per million
MΩ	megaohm	pA	picoampere
µA	microampere	pF	picofarad
µF	microfarad	pp	peak-to-peak
µH	microhenry	ps	picosecond
µs	microsecond	sps	samples per second
µV	microvolt	σ	sigma: one standard deviation
µVrms	microvolts root-mean-square		

Document History Page

Document Title: CY2302, Frequency Multiplier and Zero Delay Buffer **Document Number: 38-07154**				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	110264	SZV	12/18/01	Change from Spec number: 38-00794 to 38-07154
*A	394695	RGL	See ECN	Added typical char data Added Pb-free devices Added phase alignment paragraph
*B	2761988	KVM	09/10/09	Added temperature values to Absolute Maximum Ratings table. Removed CY2302SI-1T from the Ordering Information table. Added temperature values to Ordering Information table.
*C	2894970	KVM	03/23/2010	Updated Ordering Information: Removed inactive parts. Updated Package Diagram.
*D	2907904	KVM	04/08/2010	Updated Ordering Information: Removed inactive parts.
*E	3204657	BASH	03/24/2011	Added Ordering Code Definitions under Ordering Information. Added Acronyms and Units of Measure.
*F	4348705	CINM	04/16/2014	Updated Package Diagram: spec 51-85066 – Changed revision from *D to *F. Updated to new template. Completing Sunset Review.
*G	4578443	AJU	11/25/2014	Updated Functional Description: Added “For a complete list of related documentation, click here.” at the end.
*H	5275750	PSR	05/18/2016	Added Thermal Resistance. Updated Package Diagram: spec 51-85066 – Changed revision from *F to *H. Updated to new template.

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