Absolute Maximum Ratings

Stresses beyond the limits listed below may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

V_S .... 0V to +6V

V_{IN} .... $-V_S$ - 0.5V to $+V_S$ +0.5V

Operating Conditions

Supply Voltage Range ....2.5 to 5.5V

Operating Temperature Range ....-40°C to 85°C

Junction Temperature .... 150°C

Storage Temperature Range.............................-65°C to 150°C

Lead Temperature (Soldering, 10s) ....260°C

Package Thermal Resistance

θ_{JA} (SOIC-8) ....150°C/W

θ_{JA} (MSOP-8) .... 200°C/W

θ_{JA} (TSOT23-5) ....215°C/W

θ_{JA} (TSOT23-6) ....192°C/W

Package thermal resistance (θ_{JA}), JEDEC standard, multi-layer test boards, still air.

ESD Protection

SOIC-8 (HBM) 2.5kV

ESD Rating for HBM (Human Body Model) and CDM (Charged Device Model).

Electrical Characteristics at +2.7V

T_A = 25°C, V_S = +2.7V, R_f = 2kΩ, R_L = 2kΩ to V_S/2; G = 2; unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Frequency Domain Response						
GBWP	-3dB Gain Bandwidth Product			86		MHz
UGBW	Unity Gain Bandwidth(1)	G = +1, V_{OUT} = 0.05V_{pp}		215		MHz
BW_{SS}	-3dB Bandwidth	G = +2, V_{OUT} = 0.2V_{pp}		85		MHz
BW_{LS}	Large Signal Bandwidth	G = +2, V_{OUT} = 2V_{pp}		36		MHz
Time Domain						
t_R, t_F	Rise and Fall Time (1)	V_{OUT} = 0.2V step; (10% to 90%)		3.7		ns
t_S	Settling Time to 0.1%	V_{OUT} = 1V step		40		ns
OS	Overshoot	V_{OUT} = 0.2V step		9		%
SR	Slew Rate	G = -1, 2.7V step		130		V/μs
Distortion/Noise Response						
HD2	2nd Harmonic Distortion (1)	5MHz, V_{OUT} = 1V_{pp}		79		dBc
HD3	3rd Harmonic Distortion (1)	5MHz, V_{OUT} = 1V_{pp}		82		dBc
THD	Total Harmonic Distortion (1)	5MHz, V_{OUT} = 1V_{pp}		77		dB
e_n	Input Voltage Noise	>1MHz		16		nV/√Hz
i_n	Input Current Noise	>1MHz		1.3		pA/√Hz
X_{TALK}	Crosstalk(1)	CLC2005, 10MHz		65		dB
DC Performance						
V_{IO}	Input Offset Voltage			-1.6		mV
dV_{IO}	Average Drift			10		μV/°C
I_B	Input Bias Current			3		μA
dI_B	Average Drift			7		nA/°C
I_{OS}	Input Offset Current			0.1		μA
PSRR	Power Supply Rejection Ratio	DC	52	57		dB
A_{OL}	Open Loop Gain			75		dB
I_S	Supply Current			3.9		mA
Disable Characteristics (CLC1015)						
T_{ON}	Turn On Time			150		ns
T_{OFF}	Turn Off Time			25		ns
OFF_{ISO}	Off Isolation	5MHz, R_L = 100Ω		75		dB
I_{SD}	Disable Supply Current	$\overline{DIS}$ tied to GND		58	100	μA
Input Characteristics						
R_{IN}	Input Resistance			4.3		MΩ
C_{IN}	Input Capacitance			1.8		pF
CMIR	Common Mode Input Range			-0.3 to 1.5		V
CMRR	Common Mode Rejection Ratio	DC, V_{CM} = 0 to V_S - 1.5V		87		dB
Output Characteristics						
V_{OUT}	Output Swing	R_L = 10kΩ to V_S / 2		0.023 to 2.66		V
		R_L = 2kΩ to V_S / 2		0.025 to 2.653		V
		R_L = 150Ω to V_S / 2		0.065 to 2.55		V
I_{OUT}	Output Current			±55		mA
		-40°C to +85°C		±50		mA
I_{SC}	Short Circuit Current	V_{OUT} = V_S / 2		±85		mA
V_S	Power Supply Operating Range		2.5	2.7	5.5	V

Notes:

1. R_f = 1kΩ was used for optimal performance. (For G = +1, R_f = 0)

Electrical Characteristics at +5V

T_A = 25°C, V_S = +5V, R_f = 2kΩ, R_L = 2kΩ to V_S/2; G = 2; unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Frequency Domain Response						
GBWP	-3dB Gain Bandwidth Product			90		MHz
UGBW	Unity Gain Bandwidth[(1)]	G = +1, V_{OUT} = 0.05V_{pp}		260		MHz
BW_{SS}	-3dB Bandwidth	G = +2, V_{OUT} = 0.2V_{pp}		90		MHz
BW_{LS}	Large Signal Bandwidth	G = +2, V_{OUT} = 2V_{pp}		40		MHz
Time Domain						
t_R, t_F	Rise and Fall Time [(1)]	V_{OUT} = 0.2V step		3.6		ns
t_S	Settling Time to 0.1%	V_{OUT} = 2V step		40		ns
OS	Overshoot	V_{OUT} = 0.2V step		7		%
SR	Slew Rate	G = -1, 5V step		145		V/µs
Distortion/Noise Response						
HD2	2nd Harmonic Distortion [(1)]	5MHz, V_{OUT} = 2V_{pp}		71		dBc
HD3	3rd Harmonic Distortion [(1)]	5MHz, V_{OUT} = 2V_{pp}		78		dBc
THD	Total Harmonic Distortion [(1)]	5MHz, V_{OUT} = 2V_{pp}		70		dB
DG	Differential Gain	NTSC (3.85MHz), AC-Coupled, R_L = 150Ω		0.06		%
		NTSC (3.85MHz), DC-Coupled, R_L = 150Ω		0.08		%
DP	Differential Phase	NTSC (3.85MHz), AC-Coupled, R_L = 150Ω		0.07		°
		NTSC (3.85MHz), DC-Coupled, R_L = 150Ω		0.06		°
e_n	Input Voltage Noise	>1MHz		16		nV/√Hz
i_n	Input Current Noise	>1MHz		1.3		pA/√Hz
X_{TALK}	Crosstalk[(1)]	CLC2005, 10MHz		62		dB
DC Performance						
V_{IO}	Input Offset Voltage		-8	1.4	8	mV
d_{VIO}	Average Drift			10		µV/°C
I_B	Input Bias Current		-8	3	8	µA
dI_B	Average Drift			7		nA/°C
I_{OS}	Input Offset Current		-0.8	0.1	0.8	µA
PSRR	Power Supply Rejection Ratio	DC	52	57		dB
A_{OL}	Open Loop Gain		68	78		dB
I_S	Supply Current			4.2	5.2	mA
Disable Characteristics (CLC1015)						
T_{ON}	Turn On Time			150		ns
T_{OFF}	Turn Off Time			25		ns
OFF_{ISO}	Off Isolation	5MHz, R_L = 100Ω		75		dB
I_{SD}	Disable Supply Current	$\overline{DIS}$ tied to GND		127	170	µA
Input Characteristics						
R_{IN}	Input Resistance			4.3		MΩ
C_{IN}	Input Capacitance			1.8		pF
CMIR	Common Mode Input Range			-0.3 to 3.8		V
CMRR	Common Mode Rejection Ratio	DC, V_{CM} = 0 to V_S - 1.5V	72	87		dB

Electrical Characteristics at +5V Continued

T_A = 25°C, V_S = +5V, R_f = 2kΩ, R_L = 2kΩ to V_S/2; G = 2; unless otherwise noted.

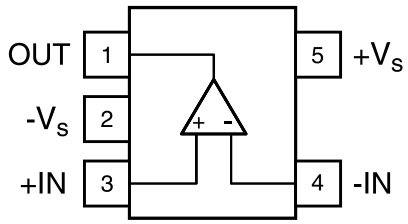
Symbol	Parameter	Conditions	Min	Typ	Max	Units
Output Characteristics						
V_{OUT}	Output Swing	R_L = 10kΩ to V_S / 2		0.027 to 4.97		V
		R_L = 2kΩ to V_S / 2		0.036 to 4.953		V
		R_L = 150Ω to V_S / 2	0.3	0.12 to 4.8	4.625	V
I_{OUT}	Output Current			±55		mA
		-40°C to +85°C		±50		mA
I_{SC}	Short Circuit Current	V_{OUT} = V_S / 2		±85		mA
V_S	Power Supply Operating Range		2.5	5	5.5	V

Notes:

1. R_f = 1kΩ was used for optimal performance. (For G = +1, R_f = 0)

CLC1005 Pin Configurations

TSOT-5

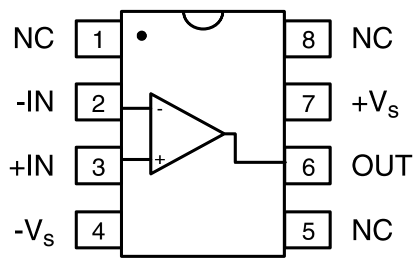


CLC1005 Pin Assignments

TSOT-5

Pin No.	Pin Name	Description
1	OUT	Output
2	$-V_S$	Negative supply
3	+IN	Positive input
4	-IN	Negative input
5	$+V_S$	Positive supply

SOIC-8

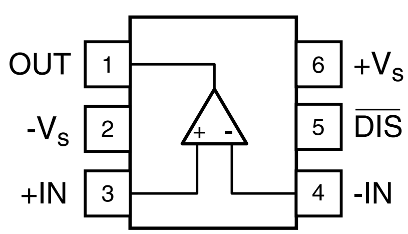


SOIC-8

Pin No.	Pin Name	Description
1	NC	No Connect
2	-IN	Negative input
3	+IN	Positive input
4	$-V_S$	Negative supply
5	NC	No Connect
6	OUT	Output
7	$+V_S$	Positive supply
8	NC	No Connect

CLC1015 Pin Configurations

TSOT-6



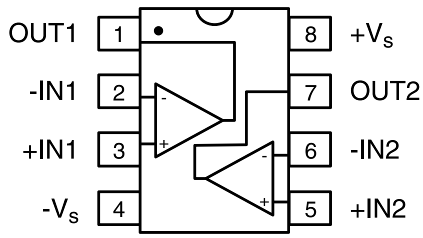
CLC1015 Pin Assignments

TSOT-6

Pin No.	Pin Name	Description
1	OUT	Output
2	$-V_S$	Negative supply
3	+IN	Positive input
4	-IN	Negative input
5	$\overline{DIS}$	Disable pin. Enabled if pin is left open or tied to $+V_S$, disabled if pin is tied to $-V_S$ (which is GND in a single supply application.)
6	$+V_S$	Positive supply

CLC2005 Pin Configuration

SOIC-8 / MSOP-8



CLC2005 Pin Assignments

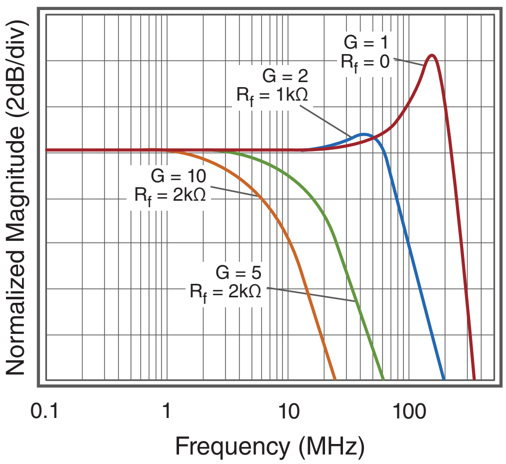
SOIC-8 / MSOP-8

Pin No.	Pin Name	Description
1	OUT1	Output, channel 1
2	-IN1	Negative input, channel 1
3	+IN1	Positive input, channel 1
4	$-V_S$	Negative supply
5	+IN2	Positive input, channel 2
6	-IN2	Negative input, channel 2
7	OUT2	Output, channel 2
8	$+V_S$	Positive supply

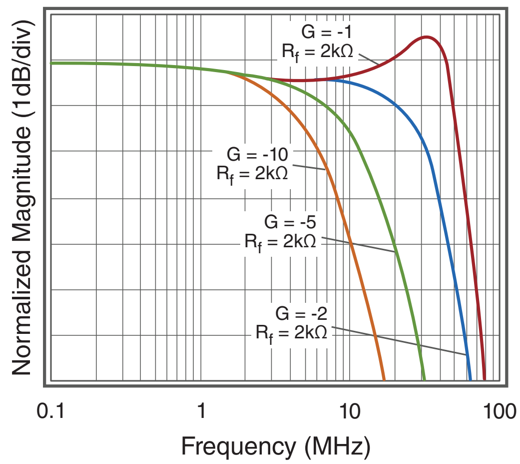
Typical Performance Characteristics

T_A = 25°C, V_S = +5V, R_L = 2kΩ to V_S/2, G = +2, R_F = 2kΩ; unless otherwise noted.

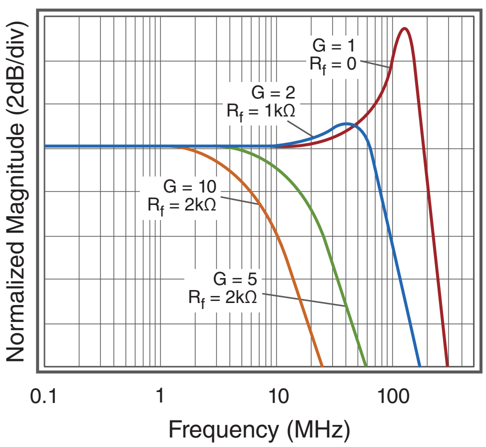
Non-Inverting Frequency Response V_S = +5V



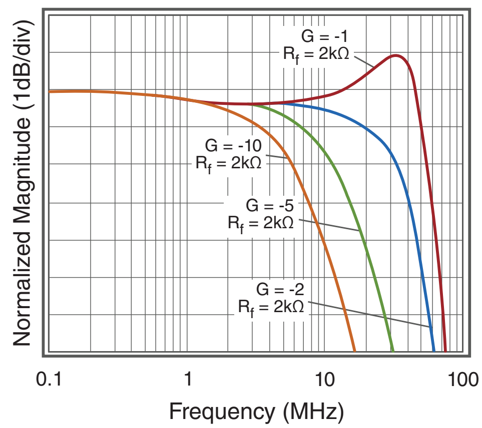
Inverting Frequency Response V_S = +5V



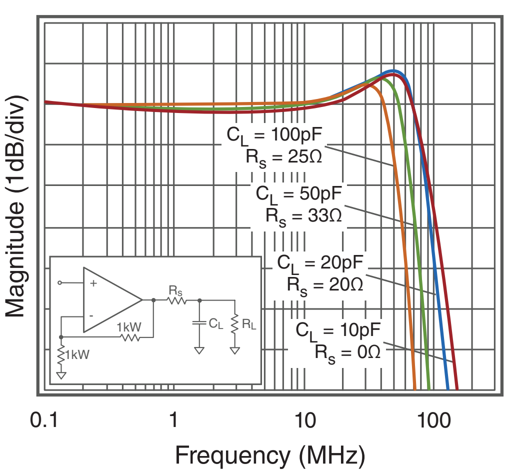
Non-Inverting Frequency Response V_S = +2.7V



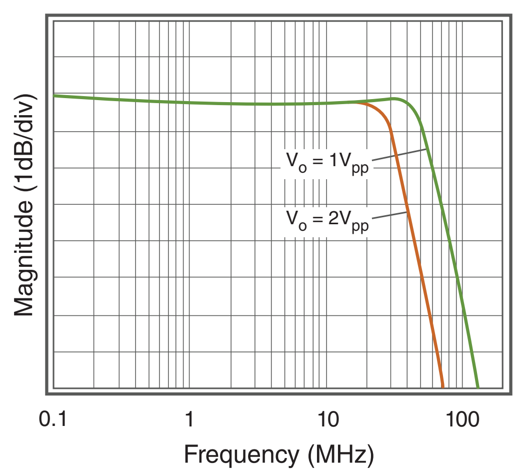
Inverting Frequency Response V_S = +2.7V



Frequency Response vs C_L



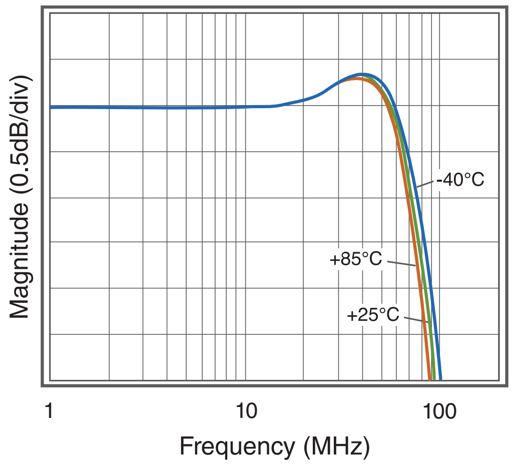
Large Signal Frequency Response



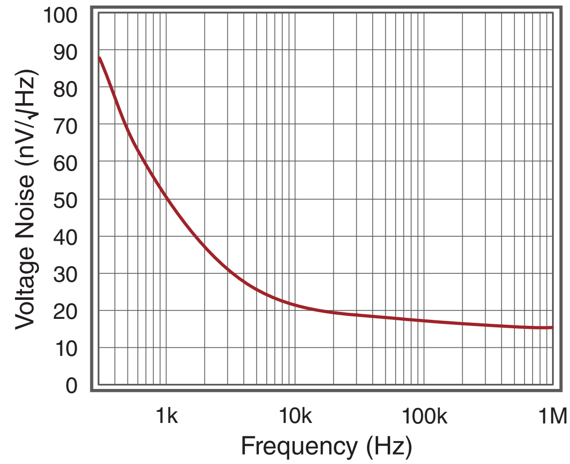
Typical Performance Characteristics

T_A = 25°C, V_S = +5V, R_L = 2kΩ to V_S/2, G = +2, R_F = 2kΩ; unless otherwise noted.

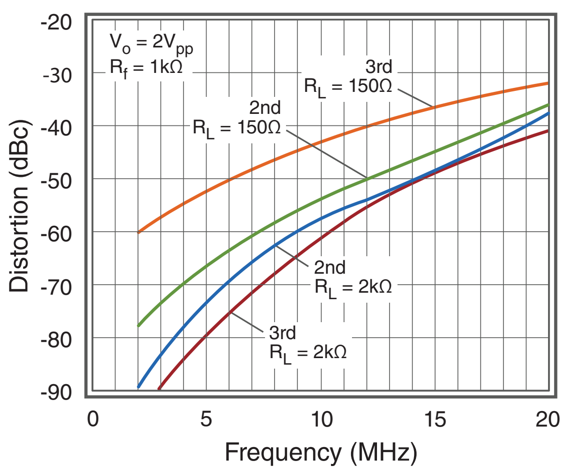
Frequency Response vs. Temperature



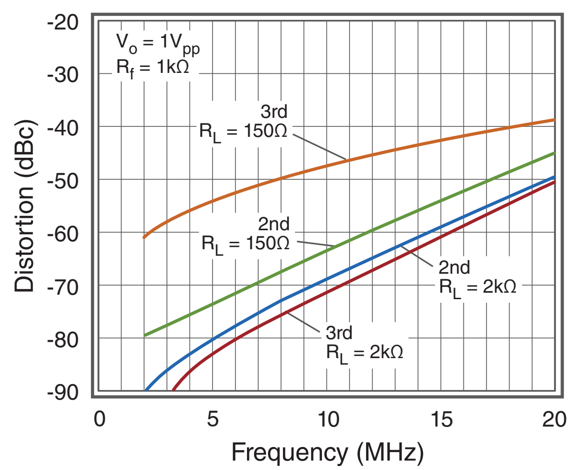
Input Voltage Noise vs Frequency



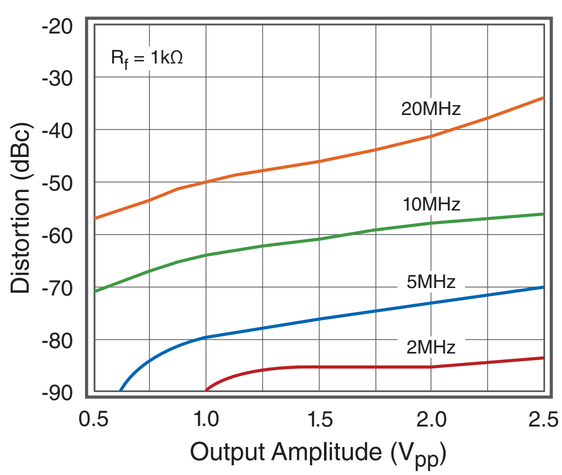
2nd & 3rd Harmonic Distortion V_S = +5V



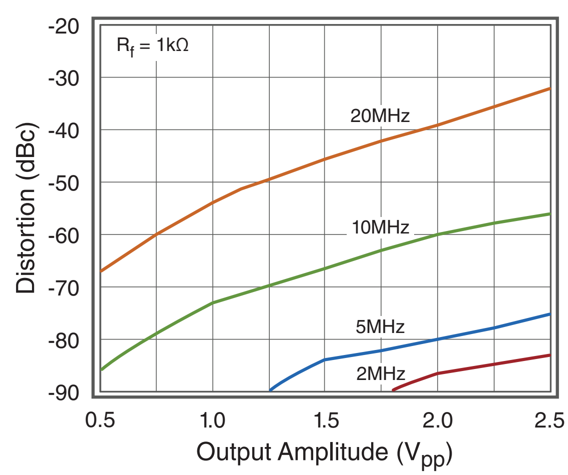
2nd & 3rd Harmonic Distortion V_S = +2.7V



2nd Harmonic Distortion vs V_O



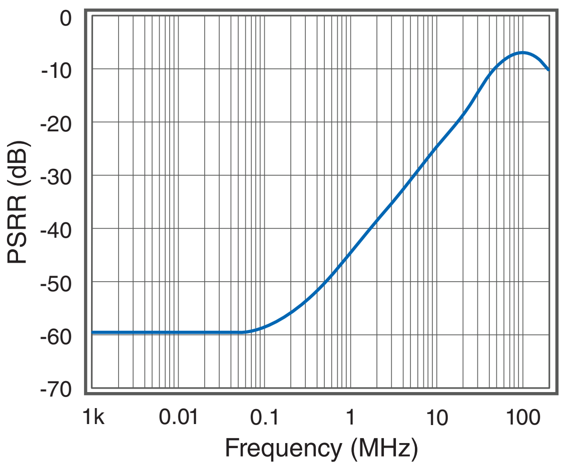
3rd Harmonic Distortion vs V_O



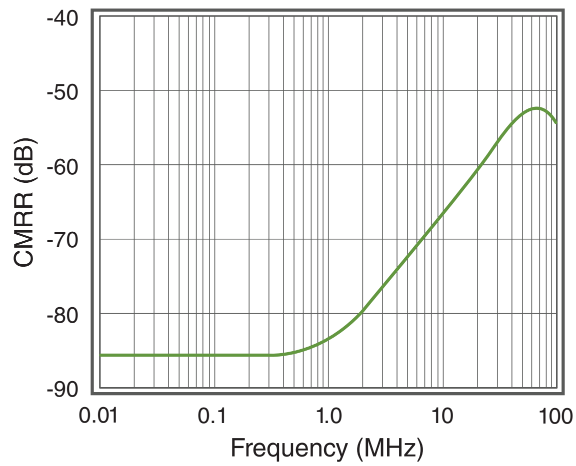
Typical Performance Characteristics

T_A = 25°C, V_S = +5V, R_L = 2kΩ to V_S/2, G = +2, R_F = 2kΩ; unless otherwise noted.

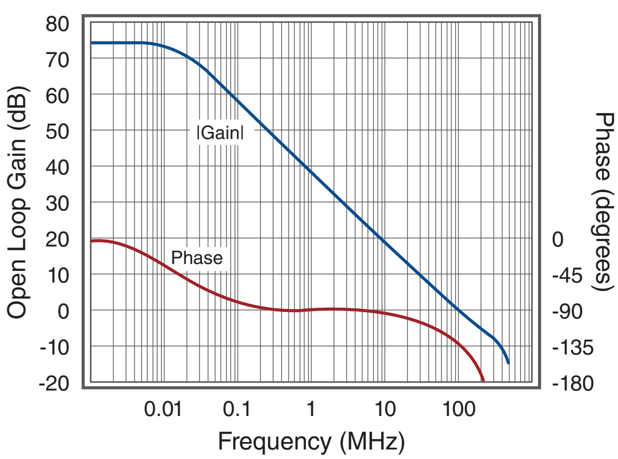
PSRR



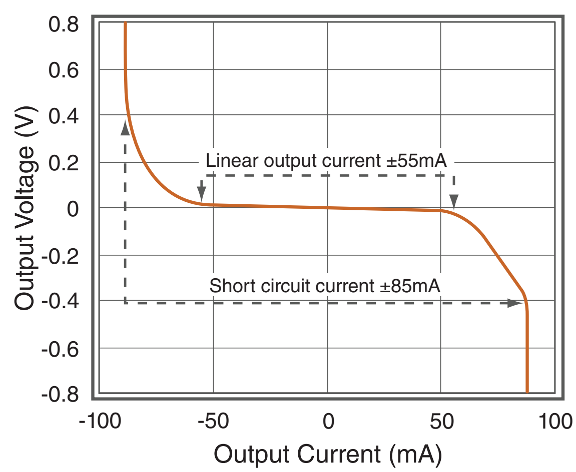
CMRR



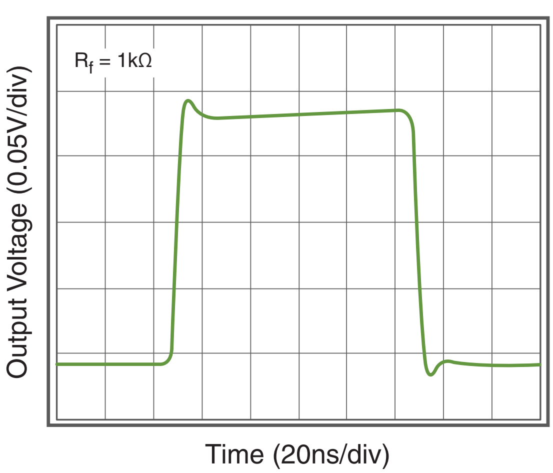
Open Loop Gain & Phase vs. Frequency



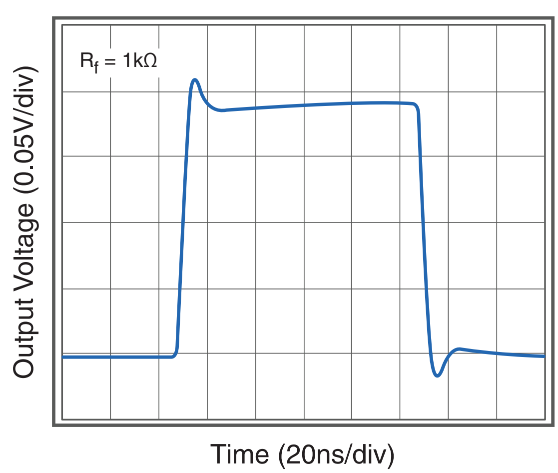
Output Current



Small Signal Pulse Response V_S = +5V



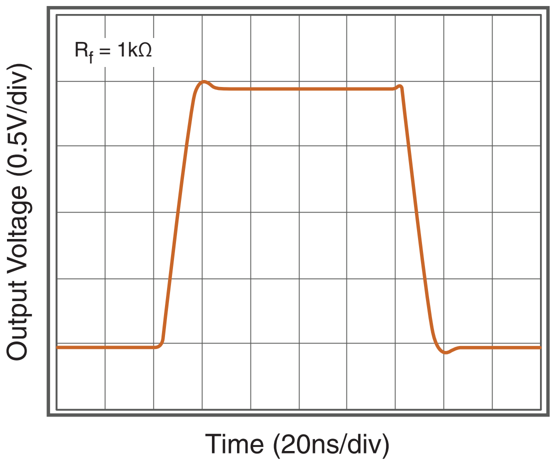
Small Signal Pulse Response V_S = +2.7V



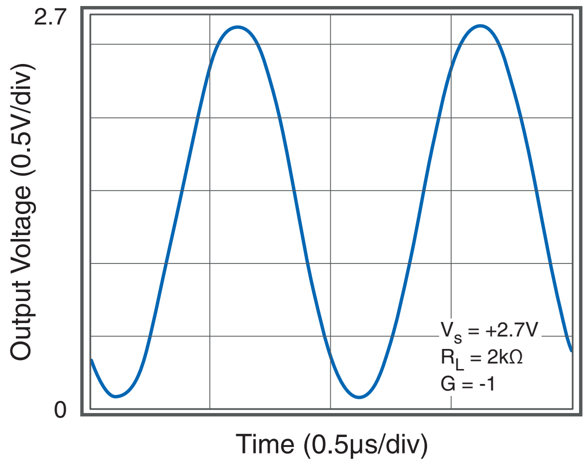
Typical Performance Characteristics

T_A = 25°C, V_S = +5V, R_L = 2kΩ to V_S/2, G = +2, R_F = 2kΩ; unless otherwise noted.

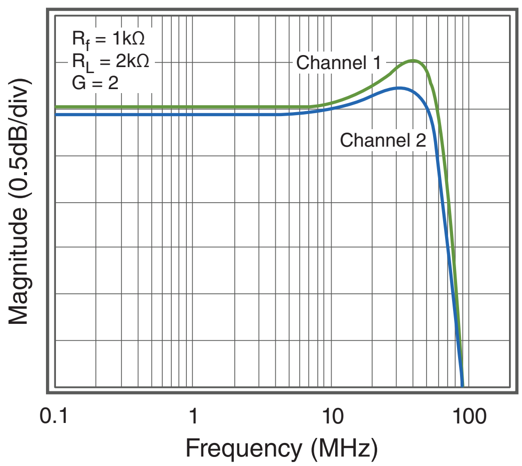
Large Signal Pulse Response V_S = +5V



Output Swing



Channel Matching V_S = +5V



Application Information

General Description

The CLC1005, CLC1015, and CLC2005 are single supply, general purpose, voltage-feedback amplifiers fabricated on a complementary bipolar process using a patented topography. They feature a rail-to-rail output stage and are unity gain stable. Both gain bandwidth and slew rate are insensitive to temperature.

The common mode input range extends to 300mV below ground and to 1.2V below V_S. Exceeding these values will not cause phase reversal. However, if the input voltage exceeds the rails by more than 0.5V, the input ESD devices will begin to conduct. The output will stay at the rail during this overdrive condition.

The design is short circuit protected and offers "soft" saturation protection that improves recovery time.

Figures 1, 2, and 3 illustrate typical circuit configurations for non-inverting, inverting, and unity gain topologies for dual supply applications. They show the recommended bypass capacitor values and overall closed loop gain equations. Figure 4 shows the typical non-inverting gain circuit for single supply applications.

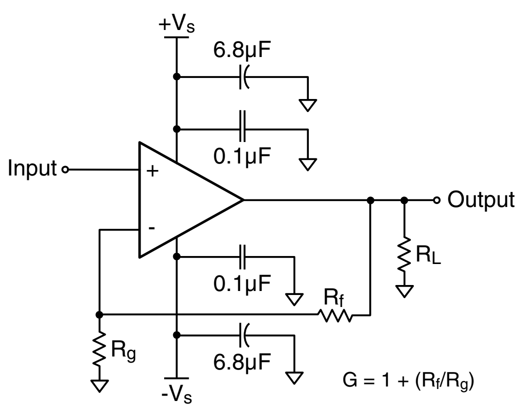


Figure 1: Typical Non-Inverting Gain Circuit

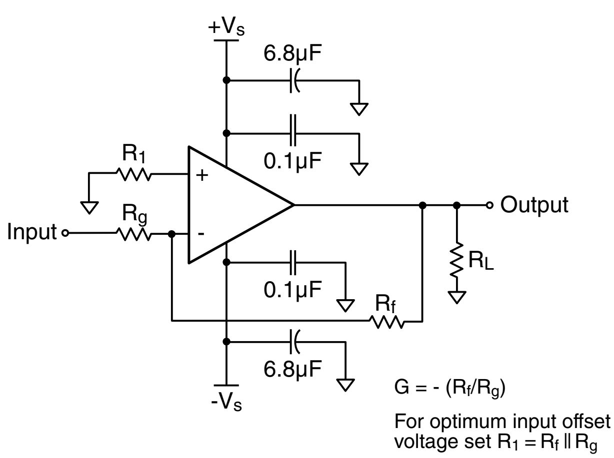


Figure 2: Typical Inverting Gain Circuit

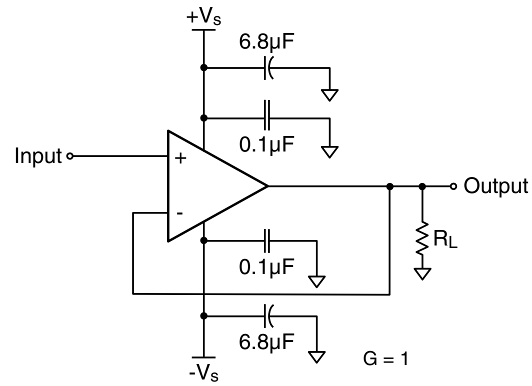


Figure 3: Unity Gain Circuit

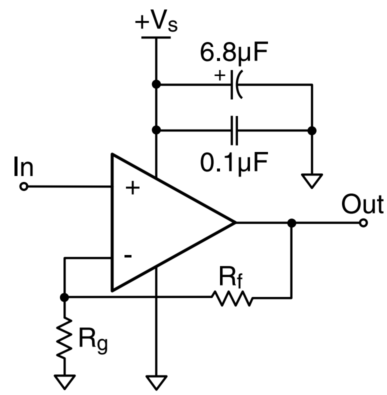


Figure 4: Single Supply Non-Inverting Gain Circuit

At non-inverting gains other than G = +1, keep R_g below 1kΩ to minimize peaking; thus for optimum response at a gain of +2, a feedback resistor of 1kΩ is recommended. Figure 5 illustrates the CLC1005, CLC1015 and CLC2005 frequency response with both 1kΩ and 2kΩ feedback resistors.

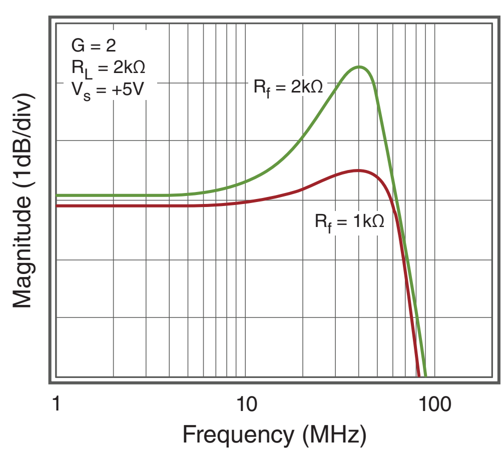


Figure 5: Frequency Response vs. R_f

Overdrive Recovery

For an amplifier, an overdrive condition occurs when the output and/or input ranges are exceeded. The recovery time varies based on whether the input or output is overdriven and by how much the ranges are exceeded. The CLC1005, CLC1015, and CLC2005 will typically recover in less than 20ns from an overdrive condition. Figure 6 shows the CLC2005 in an overdriven condition.

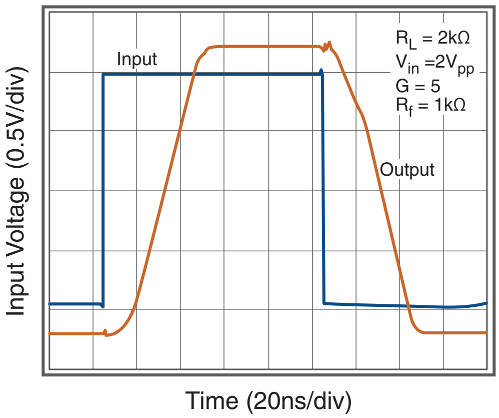


Figure 6: Overdrive Recovery

Enable/Disable Function

The CLC1015 offers an active-low disable pin that can be used to lower its supply current. Leave the pin floating to enable to part. Pull the disable pin to the negative supply (which is ground in a single supply application) to disable the output. During the disable condition, the nominal supply current will drop below 127μA and the output will be at a high impedance with about 2pF capacitance.

Power Dissipation

Power dissipation should not be a factor when operating under the stated 2kΩ load condition. However, applications with low impedance, DC coupled loads should be analyzed to ensure that maximum allowed junction temperature is not exceeded. Guidelines listed below can be used to verify that the particular application will not cause the device to operate beyond it's intended operating range.

Maximum power levels are set by the absolute maximum junction rating of 150°C. To calculate the junction temperature, the package thermal resistance value $Theta_{JA}$ (θ_{JA}) is used along with the total die power dissipation.

$$T_{Junction} = T_{Ambient} + (\theta_{JA} \times P_D)$$

Where $T_{Ambient}$ is the temperature of the working environment.

In order to determine P_D, the power dissipated in the load needs to be subtracted from the total power delivered by the supplies.

$$P_D = P_{supply} - P_{load}$$

Supply power is calculated by the standard power equation.

$$P_{supply} = V_{supply} \times I_{RMSsupply}$$

$$V_{supply} = V_{S+} - V_{S-}$$

Power delivered to a purely resistive load is:

$$P_{load} = ((V_{load})_{RMS^2})/Rload_{eff}$$

The effective load resistor ($Rload_{eff}$) will need to include the effect of the feedback network. For instance,

$Rload_{eff}$ in Figure 3 would be calculated as:

$$R_L \parallel (R_f + R_g)$$

These measurements are basic and are relatively easy to perform with standard lab equipment. For design purposes however, prior knowledge of actual signal levels and load impedance is needed to determine the dissipated power. Here, P_D can be found from

$$P_D = P_{Quiescent} + P_{Dynamic} - P_{load}$$

Quiescent power can be derived from the specified I_S values along with known supply voltage, V_{supply}. Load power can be calculated as above with the desired signal amplitudes using:

$$(V_{load})_{RMS} = V_{peak} / \sqrt{2}$$

$$(I_{load})_{RMS} = (V_{load})_{RMS} / Rload_{eff}$$

The dynamic power is focused primarily within the output stage driving the load. This value can be calculated as:

$$P_{Dynamic} = (V_{S+} - V_{load})_{RMS} \times (I_{load})_{RMS}$$

Assuming the load is referenced in the middle of the power rails or $V_{supply}/2$.

The CLC1015 is short circuit protected. However, this may not guarantee that the maximum junction temperature (+150°C) is not exceeded under all conditions. Figure 7 shows the maximum safe power dissipation in the package vs. the ambient temperature for the packages available.

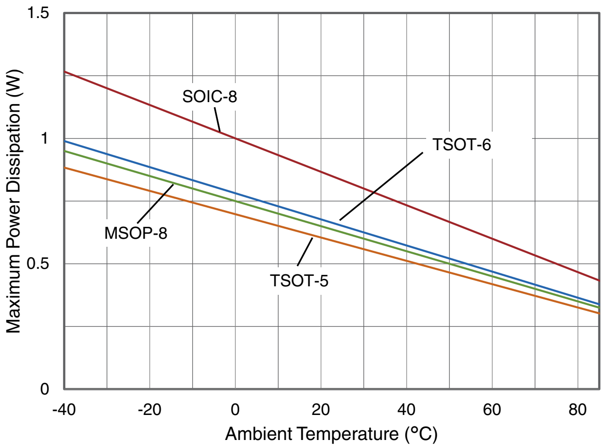


Figure 7. Maximum Power Derating

Driving Capacitive Loads

Increased phase delay at the output due to capacitive loading can cause ringing, peaking in the frequency response, and possible unstable behavior. Use a series resistance, R_S, between the amplifier and the load to help improve stability and settling performance. Refer to Figure 8.

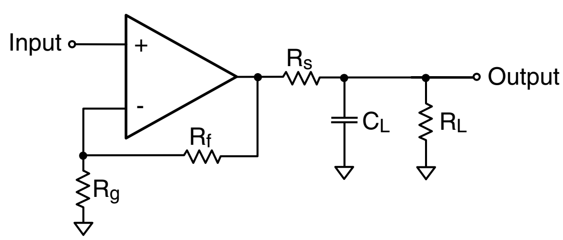


Figure 8. Addition of R_S for Driving Capacitive Loads

Table 1 provides the recommended R_S for various capacitive loads. The recommended R_S values result in approximately <1dB peaking in the frequency response.

C_L (pF)	R_S (Ω)	-3dB BW (MHz)
22pF	0	118
47pF	15	112
100pF	15	91
492pF	6.5	59

Table 1: Recommended R_S vs. C_L

For a given load capacitance, adjust R_S to optimize the tradeoff between settling time and bandwidth. In general, reducing R_S will increase bandwidth at the expense of additional overshoot and ringing.

Layout Considerations

General layout and supply bypassing play major roles in high frequency performance. Resurgent has evaluation boards to use as a guide for high frequency layout and as an aid in device testing and characterization. Follow the steps below as a basis for high frequency layout:

- Include 6.8μF and 0.1μF ceramic capacitors for power supply decoupling
- Place the 6.8μF capacitor within 0.75 inches of the power pin
- Place the 0.1μF capacitor within 0.1 inches of the power pin
- Remove the ground plane under and around the part, especially near the input and output pins to reduce parasitic capacitance
- Minimize all trace lengths to reduce series inductances

Refer to the evaluation board layouts below for more information.

Evaluation Board Information

The following evaluation boards are available to aid in the testing and layout of these devices:

Evaluation Board #	Products
CEB002	CLC1005 and CLC1015 in TSOT
CEB003	CLC1005 in SOIC
CEB006	CLC2005 in SOIC
CEB010	CLC2005 in MSOP

Evaluation Board Schematics

Evaluation board schematics and layouts are shown in Figures 9-18. These evaluation boards are built for dual-supply operation. Follow these steps to use the board in a single-supply application:

1. Short $-V_S$ to ground.
2. Use C3 and C4, if the $-V_S$ pin of the amplifier is not directly connected to the ground plane.

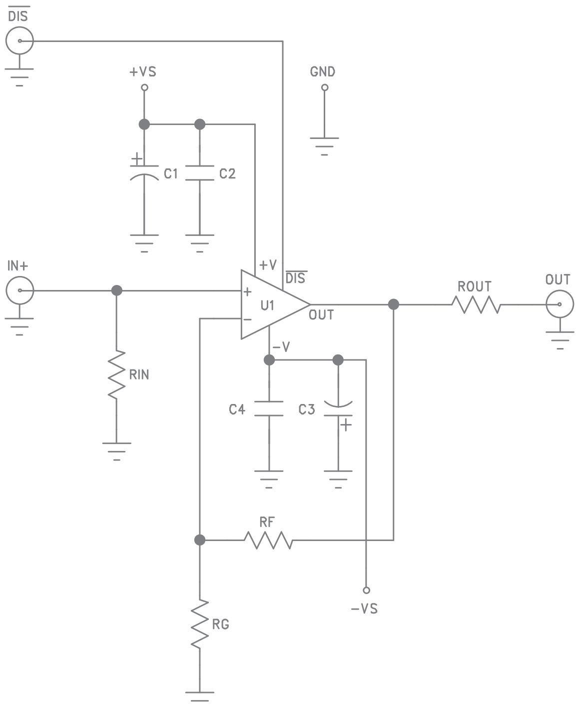


Figure 9. CEB002 and CEB003 Schematic

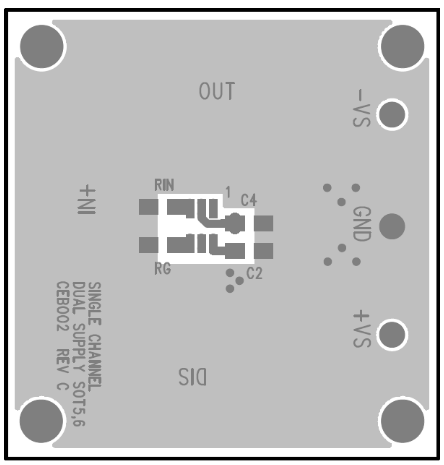


Figure 10. CEB002 Top View

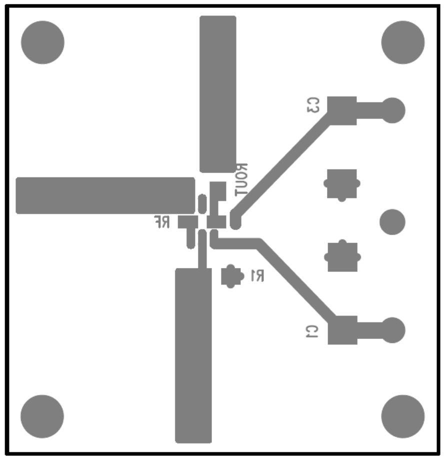


Figure 11. CEB002 Bottom View

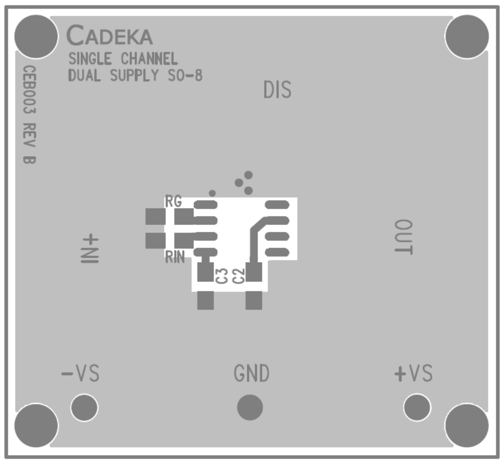


Figure 12. CEB003 Top View

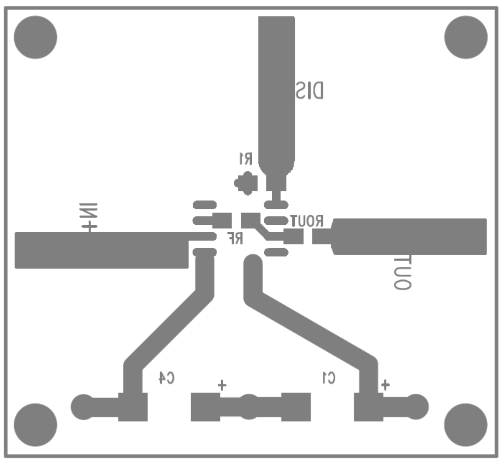


Figure 13. CEB003 Bottom View

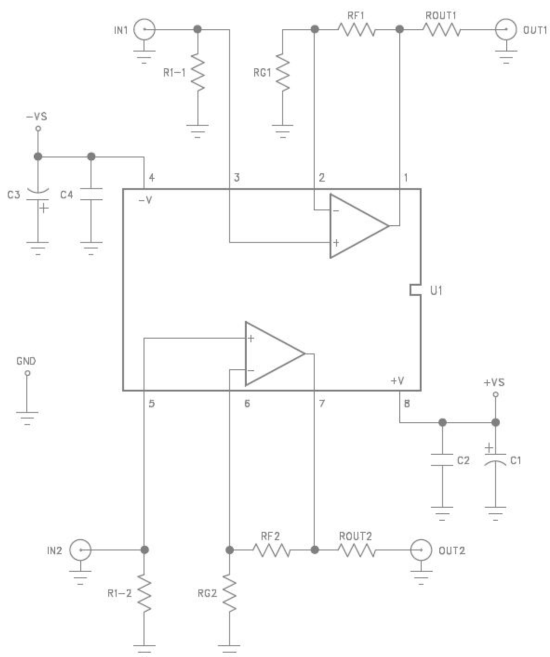


Figure 14. CEB006 & CEB010 Schematic

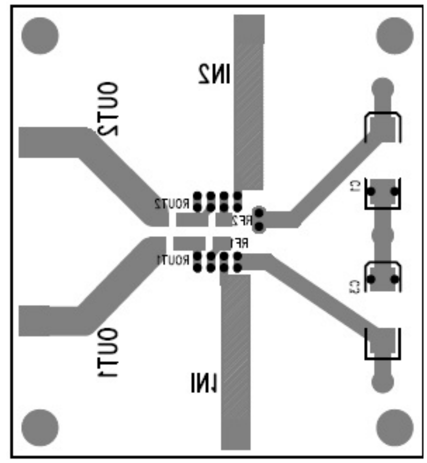


Figure 16. CEB006 Bottom View

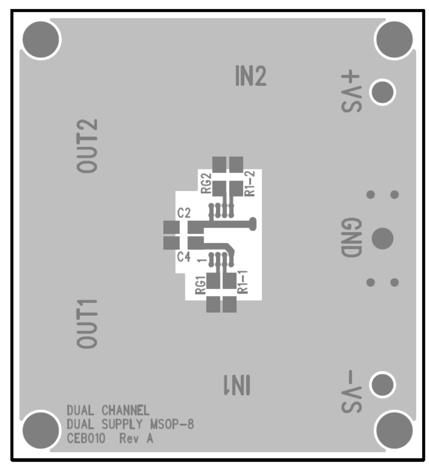


Figure 17. CEB010 Top View

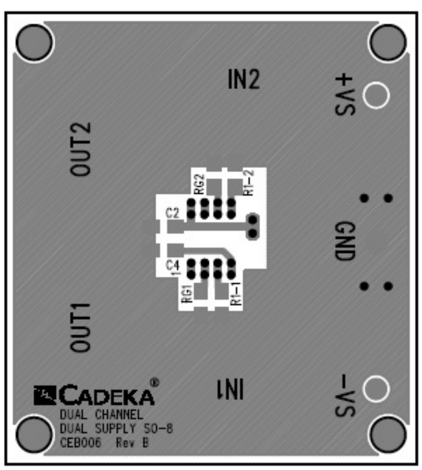


Figure 15. CEB006 Top View

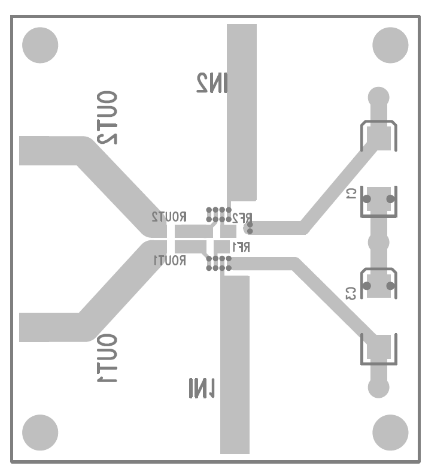
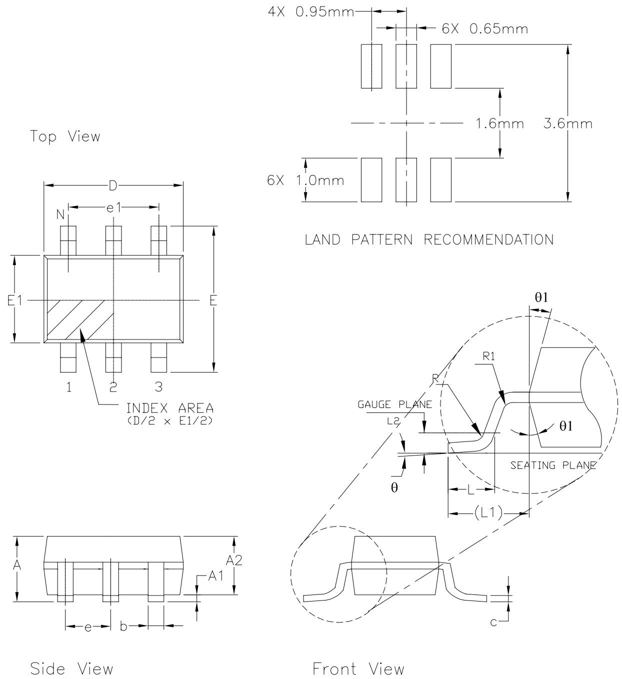


Figure 18. CEB010 Bottom View

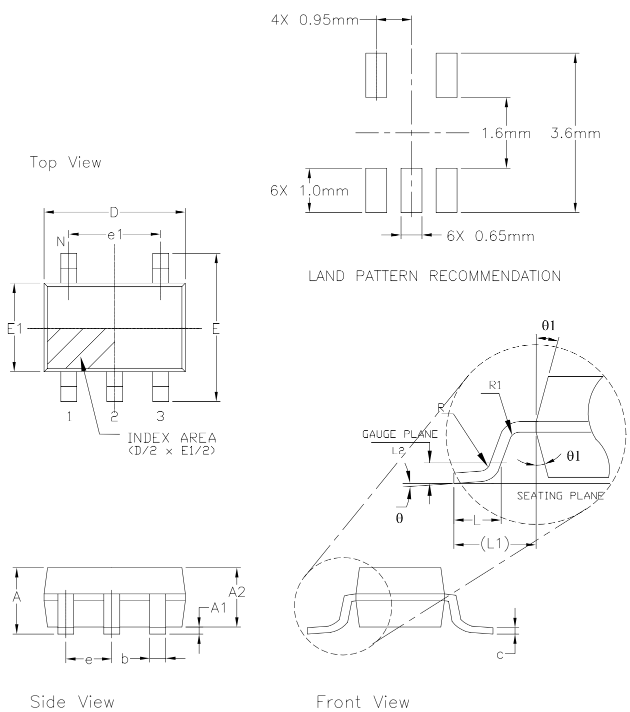
Mechanical Dimensions

TSOT-6 Package



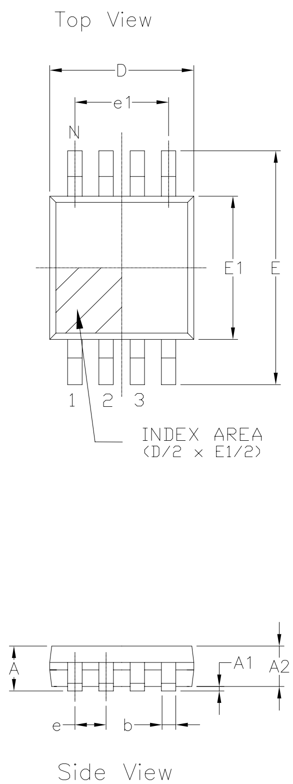
6 PIN TSOT (OPTION 2)						
SYMBOLS	DIMENSION IN MM (Control Unit)			DIMENSION IN INCH (Reference Unit)		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.75	—	0.80	0.030	—	0.031
A1	0.00	—	0.05	0.000	—	0.002
A2	0.70	0.75	0.78	0.028	0.036	0.031
b	0.35	—	0.50	0.012	—	0.020
c	0.10	—	0.20	0.003	—	0.008
D	2.90 BSC			0.114 BSC		
E	2.80 BSC			0.110 BSC		
E1	1.60 BSC			0.063 BSC		
e	0.95 BSC			0.038 BSC		
e1	1.90 BSC			0.075 BSC		
L	0.37	0.45	0.60	0.012	0.018	0.024
L1	0.60 REF			0.024 REF		
L2	0.25 BSC			0.010 BSC		
R	0.10	—	—	0.004	—	—
R1	0.10	—	0.25	0.004	—	0.010
θ	0°	4°	8°	0°	4°	8°
θ1	4°	10°	12°	4°	10°	12°
N	6			6		

TSOT-5 Package

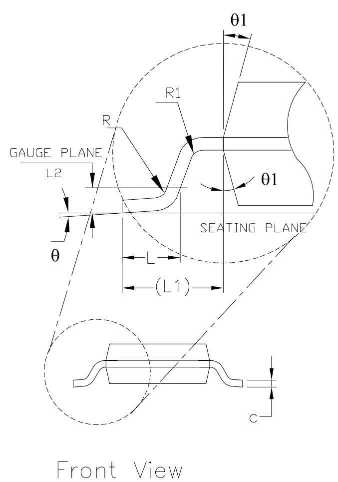


5 Pin TSOT (OPTION 2)						
SYMBOLS	DIMENSION IN MM (Control Unit)			DIMENSION IN INCH (Reference Unit)		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.75	—	0.80	0.030	—	0.031
A1	0.00	—	0.05	0.000	—	0.002
A2	0.70	0.75	0.78	0.028	0.030	0.031
b	0.35	—	0.50	0.012	—	0.020
c	0.10	—	0.20	0.003	—	0.008
D	2.90 BSC			0.114 BSC		
E	2.80 BSC			0.110 BSC		
E1	1.60 BSC			0.063 BSC		
e	0.95 BSC			0.038 BSC		
e1	1.90 BSC			0.075 BSC		
L	0.37	0.45	0.60	0.012	0.018	0.024
L1	0.60 REF			0.024 REF		
L2	0.25 BSC			0.010 BSC		
R	0.10	—	—	0.004	—	—
R1	0.10	—	0.25	0.004	—	0.010
θ	0°	4°	8°	0°	4°	8°
θ1	4°	10°	12°	4°	10°	12°
N	5			5		

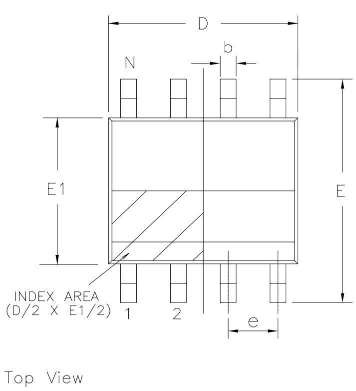
MSOP-8 Package

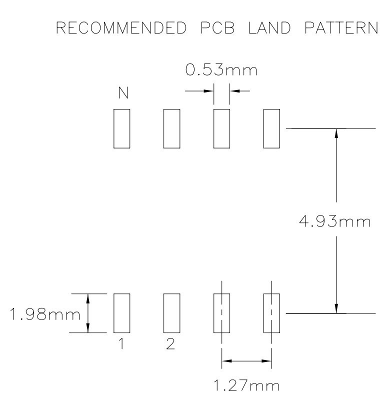


8 Pin MSOP JEDEC MO-187 Variation AA						
SYMBOLS	DIMENSIONS IN MM (Control Unit)			DIMENSIONS IN INCH (Reference Unit)		
	MIN	NOM	MAX	MIN	NOM	MAX
A	—	—	1.10	—	—	0.043
A1	0.00	—	0.15	0.000	—	0.006
A2	0.75	0.85	0.95	0.030	0.033	0.037
b	0.22	—	0.38	0.009	—	0.015
c	0.08	—	0.23	0.003	—	0.009
E	4.90 BSC			0.193 BSC		
E1	3.00 BSC			0.118 BSC		
e	0.65 BSC			0.026 BSC		
e1	1.95 BSC			0.077 BSC		
L	0.40	0.60	0.80	0.016	0.024	0.031
L1	0.95 REF			0.037 REF		
L2	0.25 BSC			0.010 BSC		
R	0.07	—	—	0.003	—	—
R1	0.07	—	—	0.003	—	—
θ	0°	—	8°	0°	—	8°
θ1	5°	—	15°	5°	—	15°
D	3.00 BSC			0.118 BSC		
N	8			8		

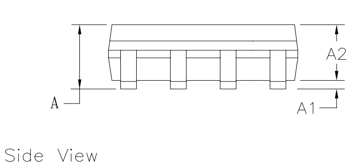


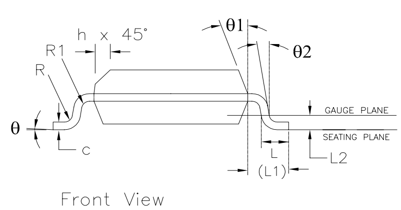
SOIC-8 Package





8 Pin SOICN JEDEC MS-012 Variation AA						
SYMBOLS	DIMENSIONS IN MM (Control Unit)			DIMENSIONS IN INCH (Reference Unit)		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.35	—	1.75	0.053	—	0.069
A1	0.10	—	0.25	0.004	—	0.010
A2	1.25	—	1.65	0.049	—	0.065
b	0.31	—	0.51	0.012	—	0.020
c	0.17	—	0.25	0.007	—	0.010
E	6.00 BSC			0.236 BSC		
E1	3.90 BSC			0.154 BSC		
e	1.27 BSC			0.050 BSC		
h	0.25	—	0.50	0.010	—	0.020
L	0.40	—	1.27	0.016	—	0.050
L1	1.04 REF			0.041 REF		
L2	0.25 BSC			0.010 BSC		
R	0.07	—	—	0.003	—	—
R1	0.07	—	—	0.003	—	—
θ	0°	—	8°	0°	—	8°
θ1	5°	—	15°	5°	—	15°
θ2	0°	—	—	0°	—	—
D	4.90 BSC			0.193 BSC		
N	8			8		





Ordering Information

Part Number	Package	Green	Operating Temperature Range	Packaging
CLC1005 Ordering Information				
CLC1005IST5X	TSOT-5	Yes	-40°C to +85°C	Tape & Reel
CLC1005IST5MTR	TSOT-5	Yes	-40°C to +85°C	Mini Tape & Reel
CLC1005IST5EVB	Evaluation Board	N/A	N/A	N/A
CLC1005ISO8X	SOIC-8	Yes	-40°C to +85°C	Tape & Reel
CLC1005ISO8MTR	SOIC-8	Yes	-40°C to +85°C	Mini Tape & Reel
CLC1005ISO8EVB	Evaluation Board	N/A	N/A	N/A
CLC1015 Ordering Information				
CLC1015IST6X	TSOT-6	Yes	-40°C to +85°C	Tape & Reel
CLC1015IST6MTR	TSOT-6	Yes	-40°C to +85°C	Mini Tape & Reel
CLC1015IST6EVB	Evaluation Board	N/A	N/A	N/A
CLC2005 Ordering Information				
CLC2005ISO8X*	SOIC-8	Yes	-40°C to +85°C	Tape & Reel
CLC2005ISO8MTR*	SOIC-8	Yes	-40°C to +85°C	Mini Tape & Reel
CLC2005ISO8EVB*	Evaluation Board	N/A	N/A	N/A
CLC2005IMP8X*	MSOP-8	Yes	-40°C to +85°C	Tape & Reel
CLC2005IMP8MTR*	MSOP-8	Yes	-40°C to +85°C	Mini Tape & Reel
CLC2005IMP8EVB*	Evaluation Board	N/A	N/A	N/A

Moisture sensitivity level for all parts is MSL-1. Mini tape and reel quantity is 250.

*Contact Resurgent Semiconductor for availability.

Revision History

Revision	Date	Description
2D (ECN 1513-01)	March 2015	Reformat into Exar data sheet template. Updated ordering information table to include MTR and EVB part numbers. Updated thermal resistance numbers and package outline drawings. Added CLC1015 back into data sheet.
2D.R	July 2018	Updated to Resurgent Semiconductor.

For Further Assistance:

www.resurgentsemi.net

RESURGENT SEMICONDUCTOR

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