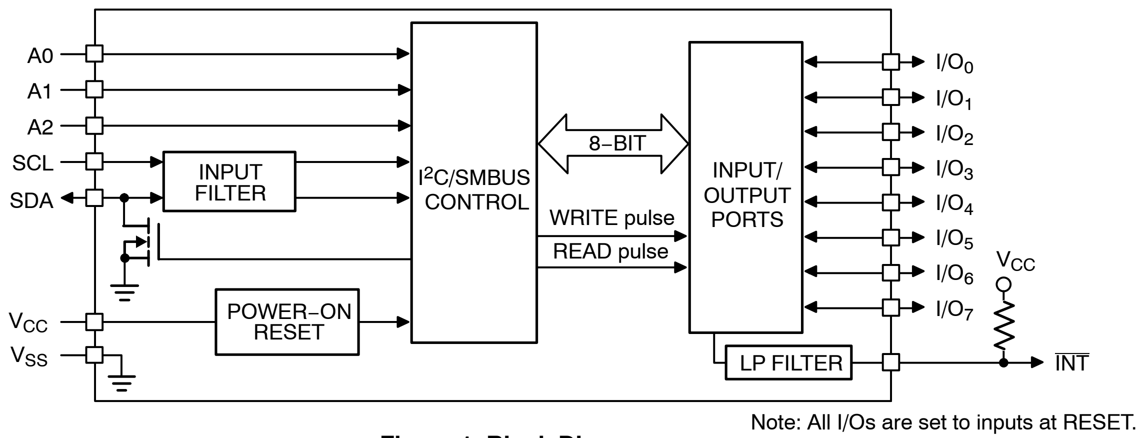


Figure 1. Block Diagram

Table 1. PIN DESCRIPTION

SOIC / TSSOP	TQFN	Pin Name	Function
1	15	A0	Address Input 0
2	16	A1	Address Input 1
3	1	A2	Address Input 2
4−7	2−5	I/O_{0-3}	Input/Output Port 0 to Input/Output Port 3
8	6	V_{SS}	Ground
9−12	7−10	I/O_{4-7}	Input/Output Port 4 to Input/Output Port 7
13	11	$\overline{INT}$	Interrupt Output (open drain)
14	12	SCL	Serial Clock
15	13	SDA	Serial Data
16	14	V_{CC}	Power Supply

Table 2. ABSOLUTE MAXIMUM RATINGS

Parameters	Ratings	Units
V_{CC} with Respect to Ground	−0.5 to +6.5	V
Voltage on Any Pin with Respect to Ground	−0.5 to +5.5	V
DC Current on I/O_0 to I/O_7	±50	mA
DC Input Current	±20	mA
V_{CC} Supply Current	85	mA
V_{SS} Supply Current	100	mA
Package Power Dissipation Capability (T_A = 25°C)	1.0	W
Junction Temperature	+150	°C
Storage Temperature	−65 to +150	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Table 3. RELIABILITY CHARACTERISTICS

Symbol	Parameter	Reference Test Method	Min	Units
V_{ZAP} (Note 1)	ESD Susceptibility	JEDEC Standard JESD 22	2000	Volts
I_{LTH} (Notes 1, 2)	Latch−up	JEDEC Standard 17	100	mA

1. This parameter is tested initially and after a design or process change that affects the parameter.
2. Latch−up protection is provided for stresses up to 100 mA on address and data pins from −1 V to V_{CC} +1 V.

Table 4. D.C. OPERATING CHARACTERISTICS (V_{CC} = 2.3 to 5.5 V; T_A = −40°C to +85°C, unless otherwise specified.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
SUPPLIES						
V_{CC}	Supply voltage		2.3	–	5.5	V
I_{CC}	Supply current	Operating mode; V_{CC} = 5.5 V; no load; f_{SCL} = 100 kHz	–	104	175	μA
I_{stbl}	Standby current	Standby mode; V_{CC} = 5.5 V; no load; $V_I = V_{SS}$; f_{SCL} = 0 kHz; I/O = inputs	–	0.25	3	μA
I_{stbh}	Standby current	Standby mode; V_{CC} = 5.5 V; no load; $V_I = V_{CC}$; f_{SCL} = 0 kHz; I/O = inputs	–	0.25	1	μA
V_{POR}	Power−on reset voltage	No load; $V_I = V_{CC}$ or V_{SS}	–	1.5	1.65	V
SCL, SDA, $\overline{INT}$						
V_{IL} (Note 3)	Low level input voltage		−0.5	–	0.3 x V_{CC}	V
V_{IH} (Note 3)	High level input voltage		0.7 x V_{CC}	–	5.5	V
I_{OL}	Low level output current	V_{OL} = 0.4 V	3	–	–	mA
I_L	Leakage current	$V_I = V_{CC}$ or V_{SS}	−1	–	+1	μA
C_I (Note 4)	Input capacitance	$V_I = V_{SS}$	–	–	6	pF
C_O (Note 4)	Output capacitance	$V_O = V_{SS}$	–	–	8	pF
A0, A1, A2						
V_{IL} (Note 3)	Low level input voltage		−0.5	–	0.8	V
V_{IH} (Note 3)	High level input voltage		2.0	–	5.5	V
I_{LI}	Input leakage current		−1	–	1	μA
I/Os						
V_{IL}	Low level input voltage		−0.5	–	0.8	V
V_{IH}	High level input voltage		2.0	–	5.5	V
I_{OL}	Low level output current	V_{OL} = 0.5 V; V_{CC} = 2.3 V (Note 5)	8	10	–	mA
		V_{OL} = 0.7 V; V_{CC} = 2.3 V (Note 5)	10	13	–	mA
		V_{OL} = 0.5 V; V_{CC} = 4.5 V (Note 5)	8	17	–	mA
		V_{OL} = 0.7 V; V_{CC} = 4.5 V (Note 5)	10	24	–	mA
		V_{OL} = 0.5 V; V_{CC} = 3.0 V (Note 5)	8	14	–	mA
		V_{OL} = 0.7 V; V_{CC} = 3.0 V (Note 5)	10	19	–	mA
V_{OH}	High level output voltage	I_{OH} = −8 mA; V_{CC} = 2.3 V (Note 6)	1.8	–	–	V
		I_{OH} = −10 mA; V_{CC} = 2.3 V (Note 6)	1.7	–	–	V
		I_{OH} = −8 mA; V_{CC} = 3.0 V (Note 6)	2.6	–	–	V
		I_{OH} = −10 mA; V_{CC} = 3.0 V (Note 6)	2.5	–	–	V
		I_{OH} = −8 mA; V_{CC} = 4.75 V (Note 6)	4.1	–	–	V
		I_{OH} = −10 mA; V_{CC} = 4.75 V (Note 6)	4.0	–	–	V
I_L	Input leakage current	V_{CC} = 3.6 V; $V_I = V_{CC}$	–	–	1	μA
C_I (Note 4)	Input capacitance		–	–	5	pF
C_O (Note 4)	Output capacitance		–	–	8	pF

3. $V_{IL\ min}$ and $V_{IH\ max}$ are reference values only and are not tested.
4. This parameter is characterized initially and after a design or process change that affects the parameter. Not 100% tested.
5. The total current sunk by all I/Os must be limited to 100 mA and each I/O limited to 25 mA maximum.
6. The total current sourced by all I/Os must be limited to 85 mA.

Table 5. A.C. CHARACTERISTICS (V_{CC} = 2.3 to 5.5 V; T_A = −40°C to +85°C, unless otherwise specified.) (Note 7)

Symbol	Parameter	Standard I²C		Fast I²C		Units
		Min	Max	Min	Max	
F_{SCL}	Clock Frequency		100		400	kHz
$t_{HD:STA}$	START Condition Hold Time	4		0.6		μs
t_{LOW}	Low Period of SCL Clock	4.7		1.3		μs
t_{HIGH}	High Period of SCL Clock	4		0.6		μs
$t_{SU:STA}$	START Condition Setup Time	4.7		0.6		μs
$t_{HD:DAT}$	Data In Hold Time	0		0		μs
$t_{SU:DAT}$	Data In Setup Time	250		100		ns
t_R (Note 8)	SDA and SCL Rise Time		1000		300	ns
t_F (Note 8)	SDA and SCL Fall Time		300		300	ns
$t_{SU:STO}$	STOP Condition Setup Time	4		0.6		μs
t_{BUF} (Note 8)	Bus Free Time Between STOP and START	4.7		1.3		μs
t_{AA}	SCL Low to Data Out Valid		3.5		0.9	μs
t_{DH}	Data Out Hold Time	100		50		ns
T_i (Note 8)	Noise Pulse Filtered at SCL and SDA Inputs		100		100	ns

Symbol	Parameter	Min	Max	Units
PORT TIMING				
t_{PV}	Output Data Valid		200	ns
t_{PS}	Input Data Setup Time	100		ns
t_{PH}	Input Data Hold Time	1		μs
INTERRUPT TIMING				
t_{IV}	Interrupt Valid		4	μs
t_{IR}	Interrupt Reset		4	μs

7. Test conditions according to “AC Test Conditions” table.
8. This parameter is characterized initially and after a design or process change that affects the parameter. Not 100% tested.

Table 6. A.C. TEST CONDITIONS

Input Rise and Fall time	≤ 10 ns
CMOS Input Voltages	0.2 V_{CC} to 0.8 V_{CC}
CMOS Input Reference Voltages	0.3 V_{CC} to 0.7 V_{CC}
TTL Input Voltages	0.4 V to 2.4 V
TTL Input Reference Voltages	0.8 V, 2.0 V
Output Reference Voltages	0.5 V_{CC}
Output Load: SDA, $\overline{INT}$	Current Source I_{OL} = 3 mA; C_L = 100 pF
Output Load: I/Os	Current Source: I_{OL}/I_{OH} = 10 mA; C_L = 50 pF

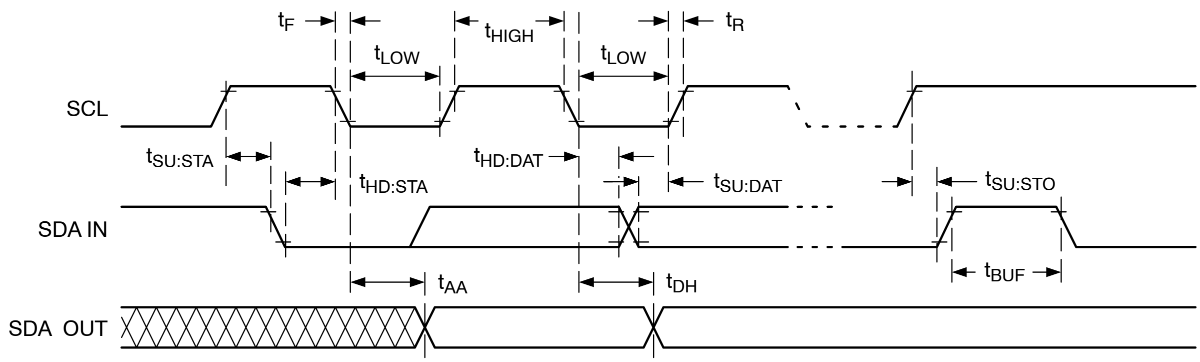


Figure 2. I²C Serial Interface Timing

Pin Description

SCL: Serial Clock

The serial clock input clocks all data transferred into or out of the device. The SCL line requires a pull−up resistor if it is driven by an open drain output.

SDA: Serial Data/Address

The bidirectional serial data/address pin is used to transfer all data into and out of the device. The SDA pin is an open drain output and can be wire−ORed with other open drain or open collector outputs. A pull−up resistor must be connected from SDA line to V_{CC}. The value of the pull−up resistor, R_P, can be calculated based on minimum and maximum values from Figure 3 and Figure 4 (see Note).

A0, A1, A2: Device Address Inputs

These inputs are used for extended addressing capability. The A0, A1, A2 pins should be hardwired to V_{CC} or V_{SS}. When hardwired, up to eight CAT9534s may be addressed on a single bus system. The levels on these inputs are compared with corresponding bits, A2, A1, A0, from the slave address byte.

I/O_0 to I/O_7: Input / Output Ports

Any of these pins may be configured as input or output. The simplified schematic of I/O_0 to I/O_7 is shown in Figure 5. When an I/O is configured as an input, the Q1 and Q2 output transistors are off creating a high impedance input. If the I/O pin is configured as an output, the push−pull output stage is enabled. Care should be taken if an external voltage is applied to an I/O pin configured as an output due to the low impedance paths that exist between the pin and either V_{CC} or V_{SS}.

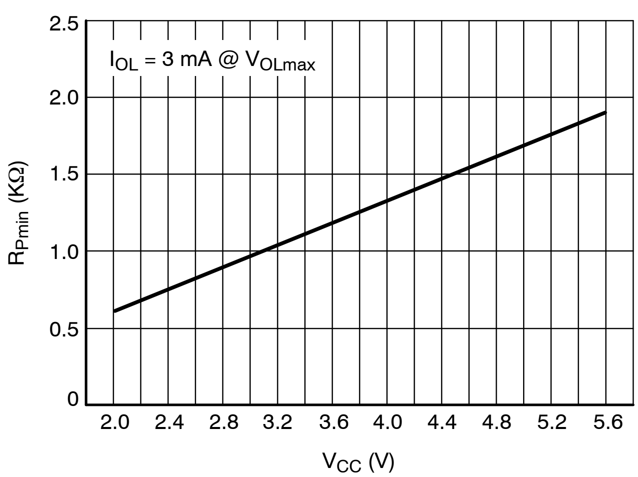


Figure 3. Minimum R_P Value vs. Supply Voltage

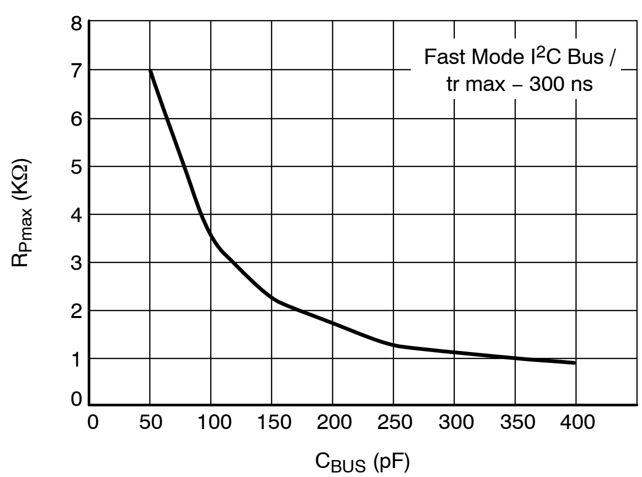


Figure 4. Maximum R_P Value vs. Bus Capacitance

NOTE: According to the Fast Mode I²C bus specification, for bus capacitance up to 200 pF, the pull up device can be a resistor. For bus loads between 200 pF and 400 pF, the pull−up device can be a current source (Imax = 3 mA) or a switched resistor circuit.

$\overline{\text{INT}}$: Interrupt Output

The open−drain interrupt output is activated when one of the port pins configured as an input changes state (differs from the corresponding input port register bit state). The interrupt is deactivated when the input returns to its previous state or the input port register is read. Changing an I/O from an output to an input may cause a false interrupt if the state of the pin does not match the contents of the input port register.

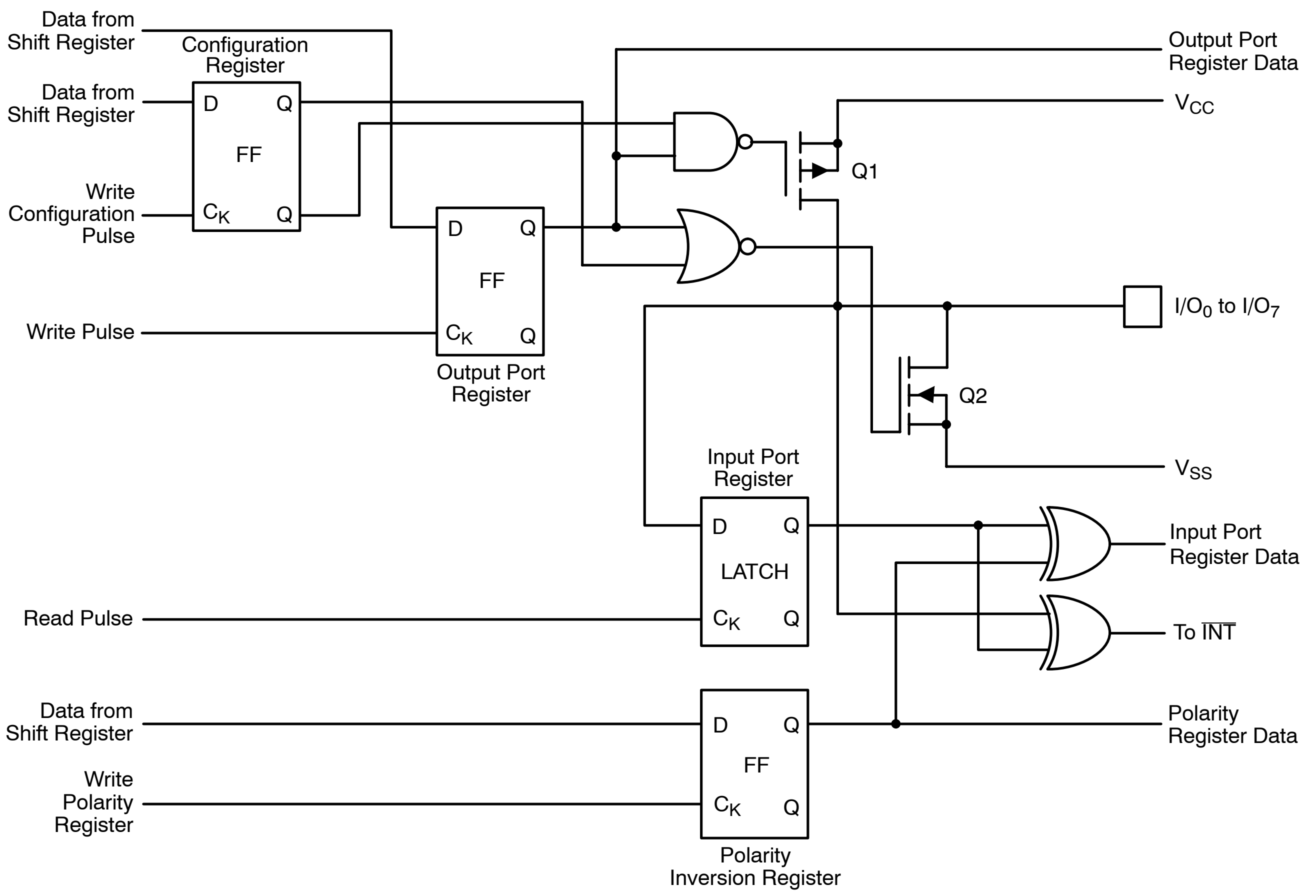


Figure 5. Simplified Schematic of I/O$_0$ to I/O$_7$

Functional Description

CAT9534's general purpose input/ output (GPIO) peripherals provide up to eight I/O ports, controlled through an I^{2}C compatible serial interface.

The CAT9534 supports the I^{2}C Bus data transmission protocol. This I^{2}C Bus protocol defines any device that sends data to the bus to be a transmitter and any device receiving data to be a receiver. The transfer is controlled by the Master device which generates the serial clock and all START and STOP conditions for bus access. The CAT9534 operates as a Slave device. Both the Master device and Slave device can operate as either transmitter or receiver, but the Master device controls which mode is activated.

I^{2}C Bus Protocol

The features of the I^{2}C bus protocol are defined as follows:

1. Data transfer may be initiated only when the bus is not busy.
2. During a data transfer, the data line must remain stable whenever the clock line is high. Any changes in the data line while the clock line is high will be interpreted as a START or STOP condition (Figure 6).

START and STOP Conditions

The START Condition precedes all commands to the device, and is defined as a HIGH to LOW transition of SDA when SCL is HIGH. The CAT9534 monitors the SDA and SCL lines and will not respond until this condition is met.

A LOW to HIGH transition of SDA when SCL is HIGH determines the STOP condition. All operations must end with a STOP condition.

Device Addressing

After the bus Master sends a START condition, a slave address byte is required to enable the CAT9534 for a read or write operation. The four most significant bits of the slave address are fixed as binary 0100 and the next three bits are its individual address bits (Figure 7).

The address bits A2, A1 and A0 are used to select which device is accessed from maximum eight devices on the same bus. These bits must compare to their hardwired input pins. The 8th bit following the 7−bit slave address is the R/$\overline{W}$ bit that specifies whether a read or write operation is to be performed. When this bit is set to "1", a read operation is initiated, and when set to "0", a write operation is selected.

Following the START condition and the slave address byte, the CAT9534 monitors the bus and responds with an acknowledge (on the SDA line) when its address matches the transmitted slave address. The CAT9534 then performs a read or a write operation depending on the state of the R/$\overline{W}$ bit.

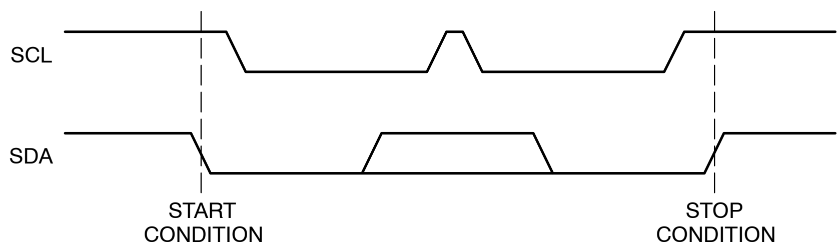


Figure 6. START/STOP Condition

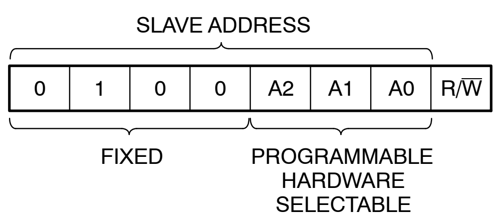


Figure 7. CAT9534 Slave Address

Acknowledge

After a successful data transfer, each receiving device is required to generate an acknowledge. The acknowledging device pulls down the SDA line during the ninth clock cycle, signaling that it received the 8 bits of data. The SDA line remains stable LOW during the HIGH period of the acknowledge related clock pulse (Figure 6).

The CAT9534 responds with an acknowledge after receiving a START condition and its slave address. If the device has been selected along with a write operation, it responds with an acknowledge after receiving each 8−bit byte.

When the CAT9534 begins a READ mode it transmits 8 bits of data, releases the SDA line, and monitors the line for an acknowledge. Once it receives this acknowledge, the CAT9534 will continue to transmit data. If no acknowledge is sent by the Master, the device terminates data transmission and waits for a STOP condition. The master must then issue a STOP condition to return the CAT9534 to the standby power mode and place the device in a known state.

Registers and Bus Transactions

The CAT9534 consists of an input port register, an output port register, a polarity inversion register and a configuration register. Table 7 shows the register address table. Tables 8 to 11 list Register 0 through Register 3 information.

Table 7. REGISTER COMMAND BYTE

Command (hex)	Protocol	Function
0x00	Read byte	Input port register
0x01	Read/write byte	Output port register
0x02	Read/write byte	Polarity inversion register
0x03	Read/write byte	Configuration register

The command byte is the first byte to follow the device address byte during a write/read bus transaction. The register command byte acts as a pointer to determine which register will be written or read.

The input port register is a read only port. It reflects the incoming logic levels of the I/O pins, regardless of whether the pin is defined as an input or an output by the configuration register. Writes to the input port register are ignored.

Table 8. REGISTER 0 – INPUT PORT REGISTER

bit	I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0
default	1	1	1	1	1	1	1	1

Table 9. REGISTER 1 – OUTPUT PORT REGISTER

bit	O_7	O_6	O_5	O_4	O_3	O_2	O_1	O_0
default	1	1	1	1	1	1	1	1

Table 10. REGISTER 2 – POLARITY INVERSION REGISTER

bit	N_7	N_6	N_5	N_4	N_3	N_2	N_1	N_0
default	0	0	0	0	0	0	0	0

Table 11. REGISTER 3 – CONFIGURATION REGISTER

bit	C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0
default	1	1	1	1	1	1	1	1

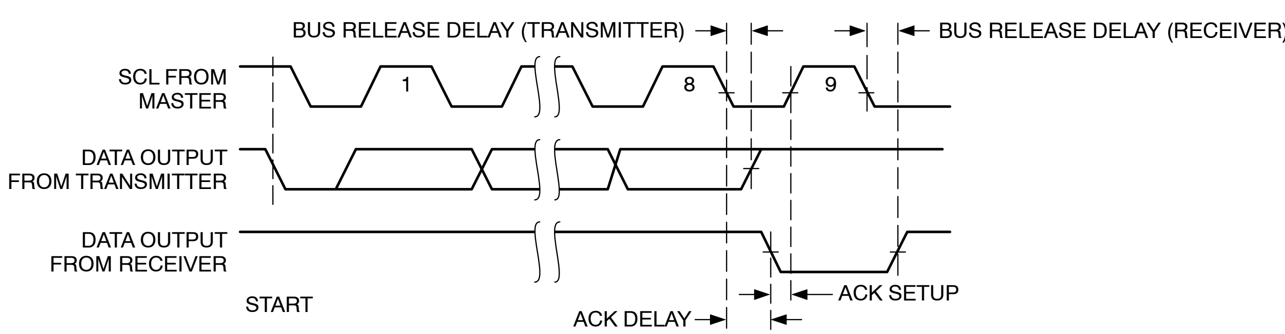


Figure 8. Acknowledge Timing

The output port register sets the outgoing logic levels of the I/O ports, defined as outputs by the configuration register. Bit values in this register have no effect on I/O pins defined as inputs. Reads from the output port register reflect the value that is in the flip−flop controlling the output, not the actual I/O pin value.

The polarity inversion register allows the user to invert the polarity of the input port register data. If a bit in this register is set (“1”) the corresponding input port data is inverted. If a bit in the polarity inversion register is cleared (“0”), the original input port polarity is retained.

The configuration register sets the directions of the ports. Set the bit in the configuration register to enable the corresponding port pin as an input with a high impedance output driver. If a bit in this register is cleared, the corresponding port pin is enabled as an output. At power−up, the I/Os are configured as inputs with a weak pull−up resistor to V_{CC}.

Data is transmitted to the CAT9534’s registers using the write mode shown in Figure 9 and Figure 10.

The CAT9534’s registers are read according to the timing diagrams shown in Figure 11 and Figure 12. Once a command byte has been sent, the register which was addressed will continue to be accessed by reads until a new command byte will be sent.

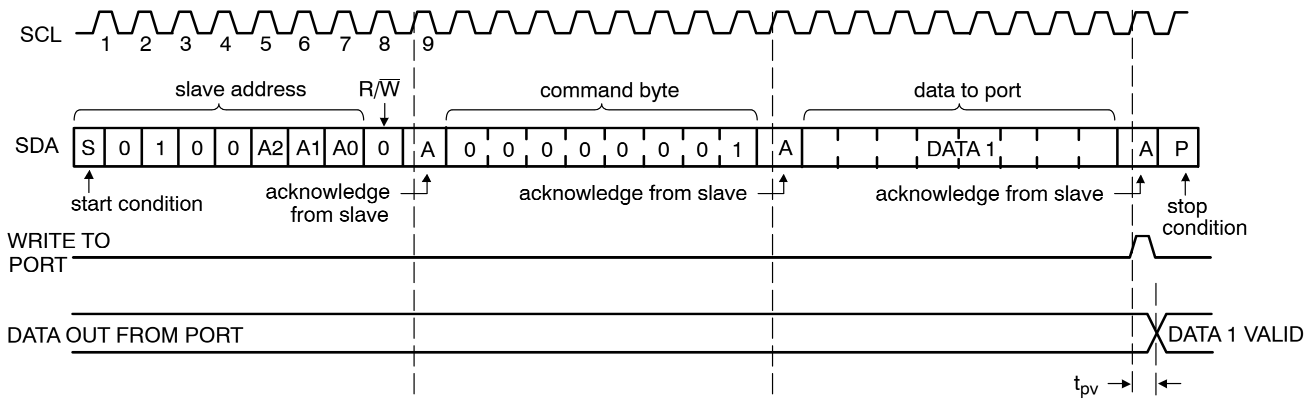


Figure 9. Write to Output Port Register

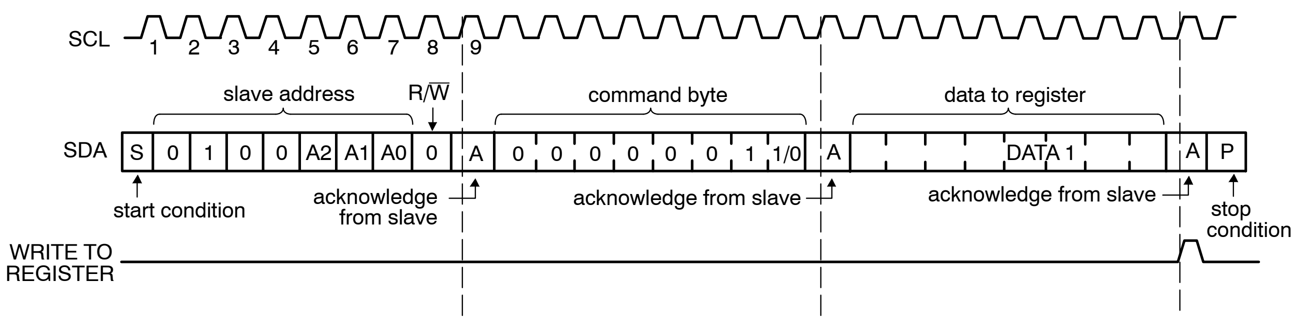


Figure 10. Write to Configuration or Polarity Inversion Register

Interrupt Output

CAT9534's interrupt otuput is an active LOW open−drain output that is activated when any port pin configured as an input changes state. The interrupt output is reset when the input returns to its previous state or the Input Port Register is read.

Note that changing an I/O from an output to an input may cause a false interrupt to occur if the state of the pin does not match the contents of the Input Port register.

Power−On Reset Operation

When the power supply is applied to V_{CC} pin, an internal power−on reset pulse holds the CAT9534 in a reset state until V_{CC} reaches V_{POR} level. At this point, the reset condition is released and the internal state machine and the CAT9534's registers are initialized to their default state.

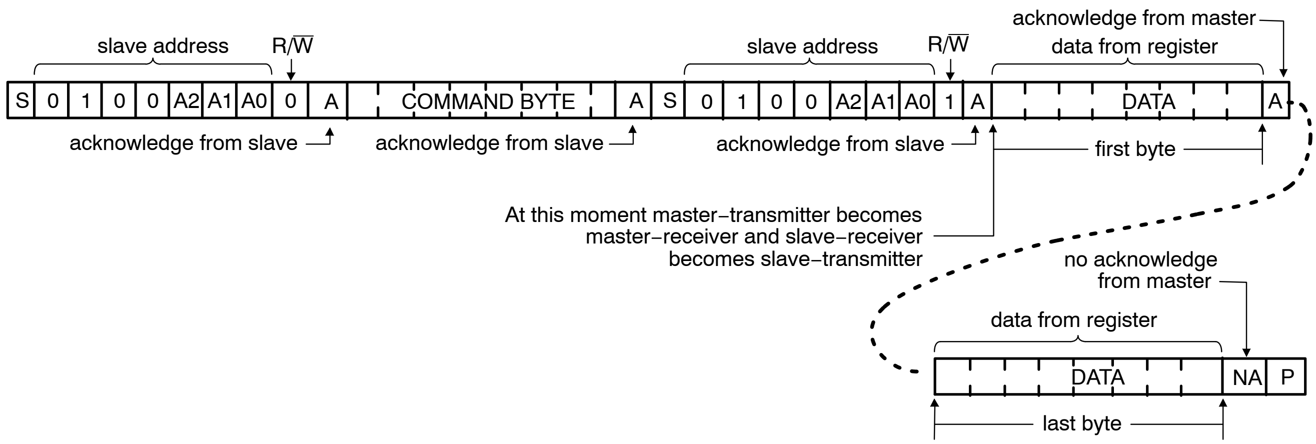


Figure 11. Read from Register

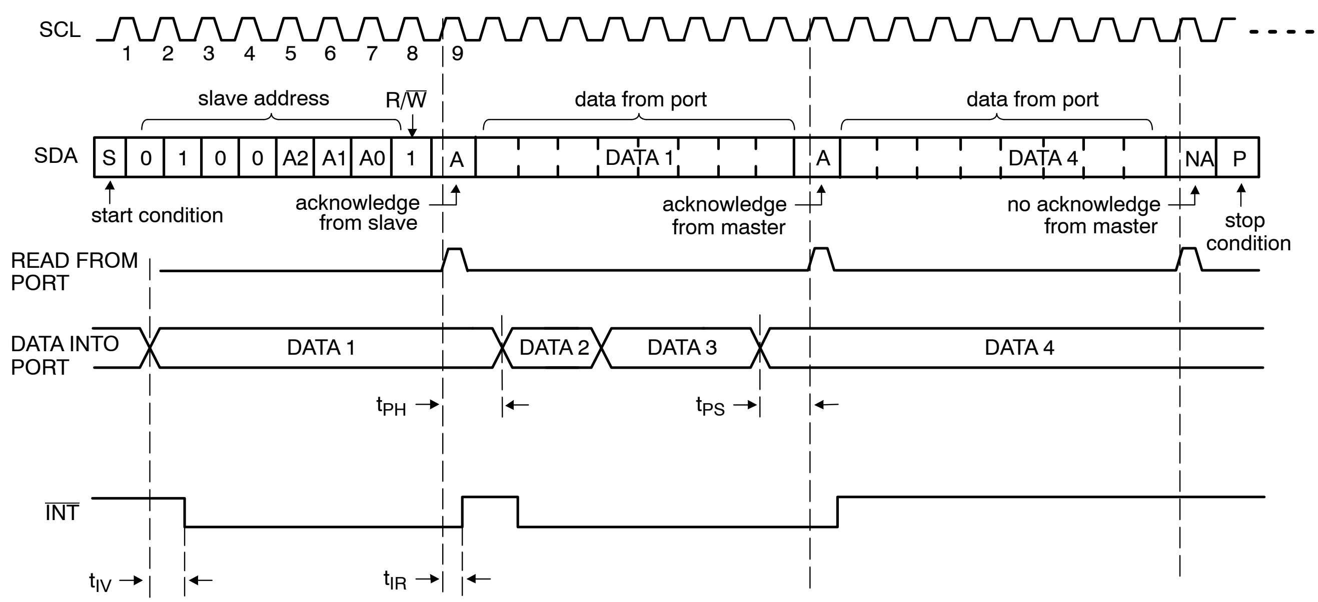
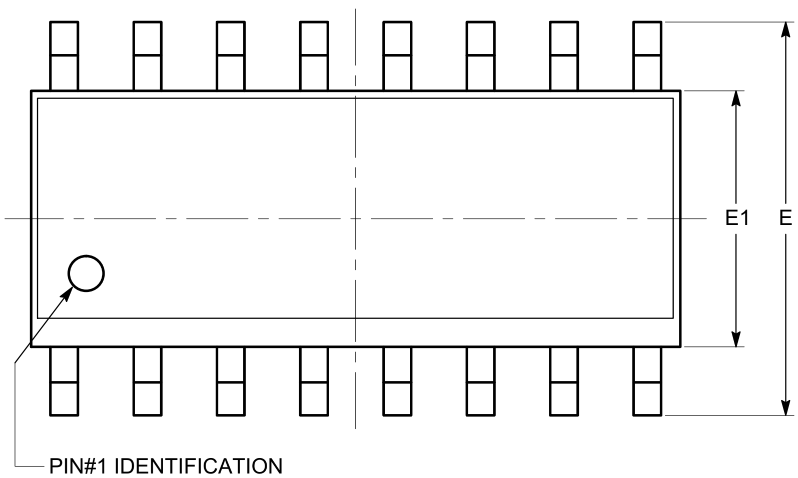


Figure 12. Read Input Port Register

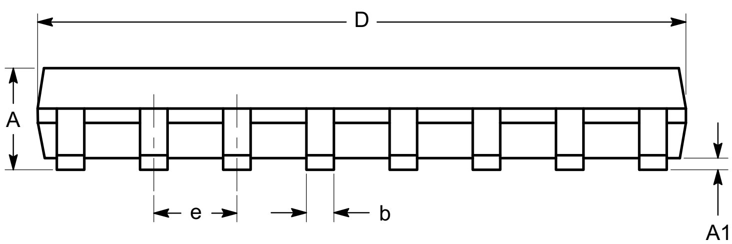
PACKAGE DIMENSIONS

SOIC−16, 150 mils
CASE 751BG−01
ISSUE O

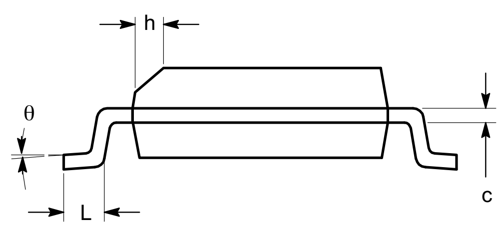


SYMBOL	MIN	NOM	MAX
A	1.35		1.75
A1	0.10		0.25
b	0.33		0.51
c	0.19		0.25
D	9.80	9.90	10.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27 BSC		
h	0.25		0.50
L	0.40		1.27
θ	0º		8º

TOP VIEW



SIDE VIEW

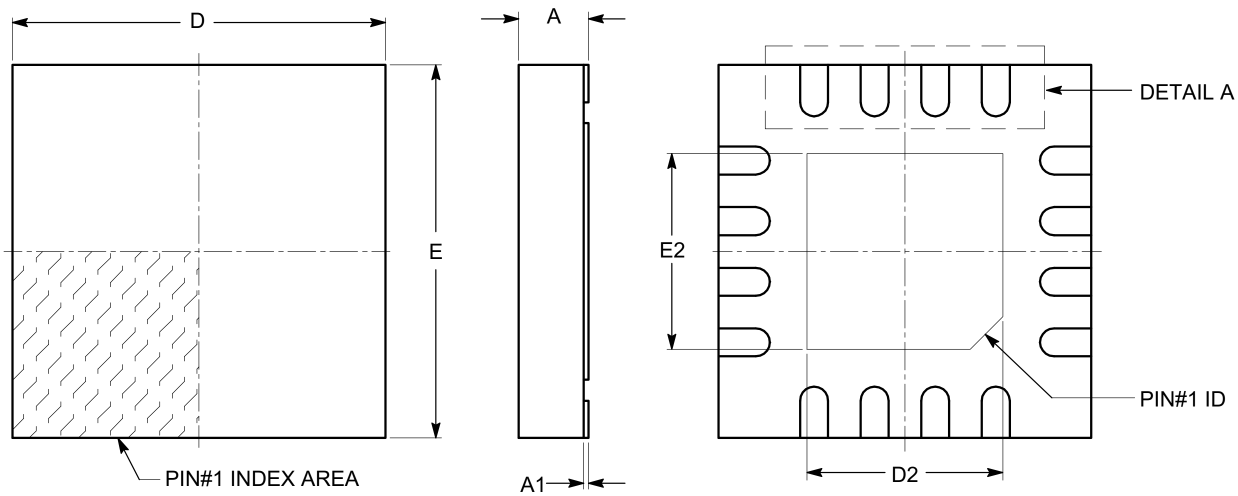


END VIEW

Notes:
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MS-012.

PACKAGE DIMENSIONS

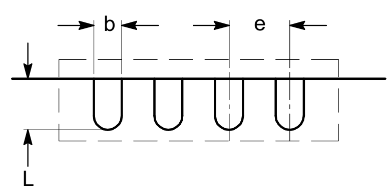
TQFN16, 4x4
CASE 510AE−01
ISSUE A



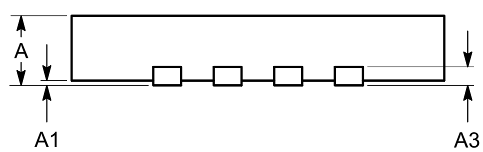
TOP VIEW **SIDE VIEW** **BOTTOM VIEW**

SYMBOL	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	0.20 REF		
b	0.25	0.30	0.35
D	3.90	4.00	4.10
D2	2.00	−−−	2.25
E	3.90	4.00	4.10
E2	2.00	−−−	2.25
e	0.65 BSC		
L	0.45	−−−	0.65

Notes:
(1) All dimensions are in millimeters.
(2) Complies with JEDEC MO-220.



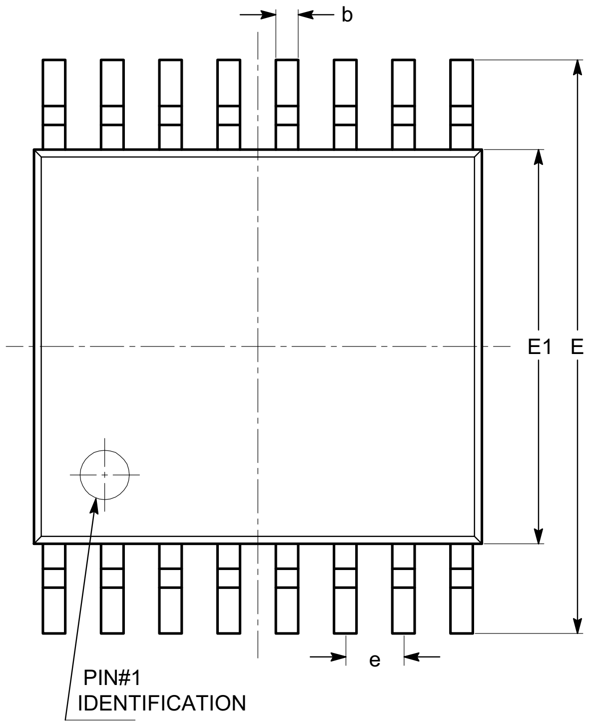
DETAIL A



FRONT VIEW

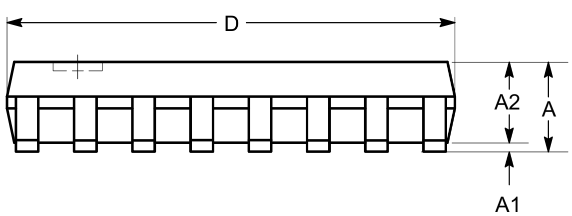
PACKAGE DIMENSIONS

TSSOP16, 4.4x5
CASE 948AN−01
ISSUE O

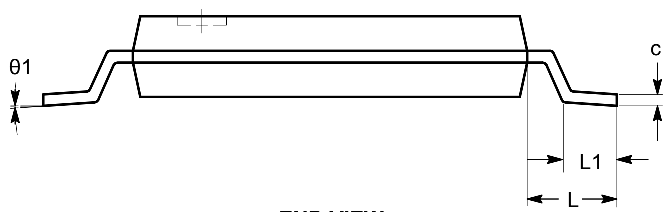


TOP VIEW

SYMBOL	MIN	NOM	MAX
A			1.10
A1	0.05		0.15
A2	0.85		0.95
b	0.19		0.30
c	0.13		0.20
D	4.90		5.10
E	6.30		6.50
E1	4.30		4.50
e	0.65 BSC		
L	1.00 REF		
L1	0.45		0.75
θ	0º		8º



SIDE VIEW



END VIEW

Notes:
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MO-153.

Example of Ordering Information (Note 11)

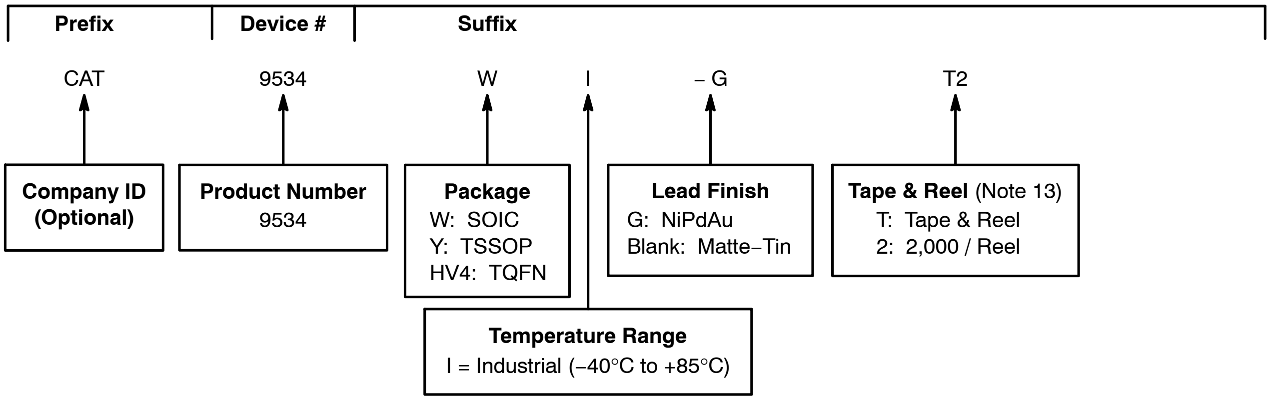


Table 12. ORDERING INFORMATION

Part Number	Package	Lead Finish
CAT9534WI−GT2	SOIC	NiPdAu
CAT9534YI−GT2	TSSOP	NiPdAu
CAT9534HV4I−GT2	TQFN	NiPdAu

9. All packages are RoHS−compliant (Lead−free, Halogen−free).
10. The standard lead finish is NiPdAu.
11. The device used in the above example is a CAT9534WI−GT2 (SOIC, Industrial Temperature, NiPdAu, Tape & Reel, 2,000/Reel).
12. For additional package and temperature options, please contact your nearest ON Semiconductor Sales office.
13. For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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