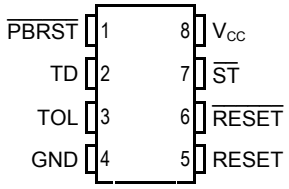
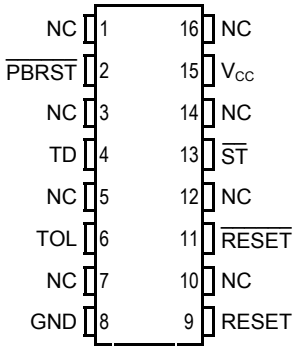
PIN CONFIGURATION

SOIC 8 Lead
MSOP 8 Lead
PDIP 8 Lead



SOIC 16 Lead



PIN DESCRIPTION

Pin Number 8-Lead Package	Pin Number 16-Lead Package	Name	Function
1	2	$\overline{\text{PBRST}}$	Debounced manual pushbutton reset input
2	4	TD	Watchdog typical time delay selection: a) t_{TD} = 150 ms for TD = GND b) t_{TD} = 600 ms for TD = Open c) t_{TD} = 1200 ms for TD = V_{CC}
3	6	TOL	CAT1232LP TOL selects 5% (TOL = GND) or 10% (TOL = V_{CC}) trip point tolerance. CAT1832 TOL selects 10% (TOL = GND) or 20% TOL = V_{CC}) trip point tolerance.
4	8	GND	Ground
5	9	RESET	Active HIGH reset output. RESET is active 1. If V_{CC} falls below the reset voltage trip point 2. If $\overline{\text{PBRST}}$ is low 3. If $\overline{\text{ST}}$ is not strobed low before the timeout period set by TD expires. 4. During power-up.
6	11	RESET	Active LOW reset output. (See RESET)
7	13	$\overline{\text{ST}}$	Strobe Input
8	15	V_{CC}	Power Supply
	1, 3. 5, 7, 10, 12, 14, 16	NC	No internal connection

ABSOLUTE MAXIMUM RATINGS (*)

Parameters	Ratings	Units
Voltage on V_{CC}	-0.5 to 7.0	V
Voltage on $\overline{\text{ST}}$ and TD	-0.5 to V_{CC} + 0.5	V
Voltage on $\overline{\text{PBRST}}$, $\overline{\text{RESET}}$and RESET	-0.5 to V_{CC} + 0.5	V

Parameters	Ratings	Units
Maximum Junction Temperature	125	ºC
Storage Temperature Range	-65 to +150	ºC
Lead Soldering Temperature (10s)	300	ºC
Operating Temperature Range	-40 to +85	ºC

Note:

* Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

ELECTRICAL CHARACTERISTICS

Unless otherwise stated, 1.0 V - V_{CC} - 5.5 V and over the operating temperature range of -40ºC to +85ºC.
All voltages are referenced to ground.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{CC}	Supply Voltage		1.0		5.5	V
I_{CC1}	Supply Current	V_{CC} = 5.5 V, CAT1232LP		35	50	µA
		V_{CC} = 3.6 V, CAT1832		20	35	
V_{IH}	ST and $\overline{PBRST}$ Input High Level	(5)	2		V_{CC} + 0.3 V	V
		(6)	V_{CC} - 0.4 V			
V_{IL}	ST and $\overline{PBRST}$ Input Low Level	V_{CC} = 5.5 V, CAT1232LP	-0.3		0.8	V
		V_{CC} = 3.6 V, CAT1832			0.5	
V_{CCTP}	V_{CC} Trip Point (TOL = GND)	CAT1232LP	4.50	4.62	4.74	V
V_{CCTP}	V_{CC} Trip Point (TOL = V_{CC})	CAT1232LP	4.25	4.37	4.49	V
V_{CCTP}	V_{CC} Trip Point (TOL = GND)	CAT1832	2.80	2.88	2.97	V
V_{CCTP}	V_{CC} Trip Point (TOL = V_{CC})	CAT1832	2.47	2.55	2.64	V
t_{TD}	Watchdog Time-Out Period	TD = GND	62.5	150	250	ms
t_{TD}	Watchdog Time-Out Period	TD = V_{CC}	500	1200	2000	ms
t_{TD}	Watchdog Time-Out Period	TD floating	250	600	1000	ms
V_{OH}	Output Voltage	I = -500 µA (3)	V_{CC} -0.5 V	V_{CC} -0.1 V		V
I_{OH}	Output Current	Output = 2.4 V (2)		-350		µA
I_{OL}	Output Current	Output = 0.4 V	10			mA
I_{IL}	Input Leakage	(1)	-1.0		1.0	µA
R_{PU}	Internal Pull-Up Resistor	(1)	32	40	55	kΩ
C_{IN}	Input Capacitance				5	pF
C_{OUT}	Output Capacitance				7	pF
t_{PB}	$\overline{PBRST}$ Manual Reset Minimum Low Time	$\overline{PBRST}$ = V_{IL}	20			ms
t_{RST}	Reset Active Time		250	600	1000	ms
t_{ST}	$\overline{ST}$ Pulse Width	(4)	20			ns
t_{RPD}	V_{CC} Fail Detect to RESET or $\overline{RESET}$			5	8	µs
t_F	V_{CC} Slew Rate		20			µs
t_{PDLY}	$\overline{PBRST}$ Stable LOW to RESET and $\overline{RESET}$ Active				20	ms
t_{RPU}	V_{CC} Detect to RESET or $\overline{RESET}$ Inactive	t_{RISE} = 5 µs	250	600	1000	ms
t_R	V_{CC} Slew Rate	4.25 V to 4.75 V	0			ns

Notes:

(1) $\overline{PBRST}$ is internally pulled HIGH to V_{CC} through a nominal 40 kΩ resistor (RPU).

(2) $\overline{RESET}$ is an open drain output on the CAT1232LP.

(3) RESET remains within 0.5 V of V_{CC} on power-down until V_{CC} falls below 2 V. RESET remains within 0.5 V of ground on power-down until V_{CC} falls below 2.0 V.

(4) Must not exceed the minimum watchdog time-out period (t_{TD}). The watchdog circuit cannot be disabled. To avoid a reset, $\overline{ST}$ must be strobed.

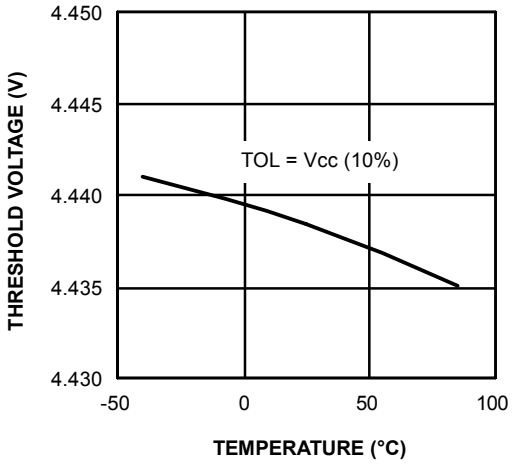
(5) Measured with $V_{CC} \geq 2.7$ V.

(6) Measured with $V_{CC} < 2.7$ V.

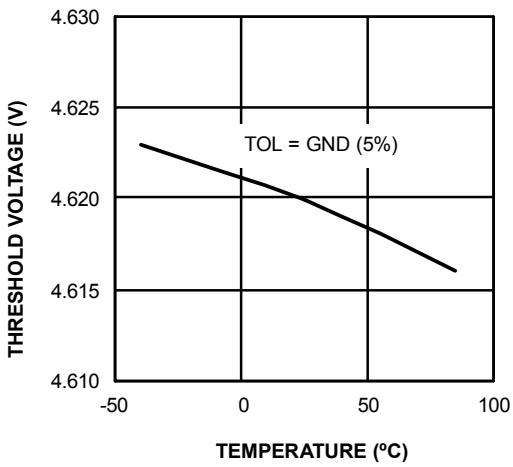
TYPICAL CHARACTERISTICS

For the CAT1232LP, V_{CC} = 5 V and T_{AMB} = 25ºC unless otherwise stated.

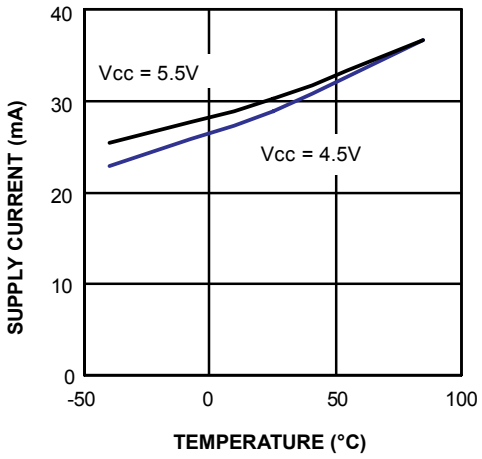
Threshold Voltage vs. Temperature (10% TOL)



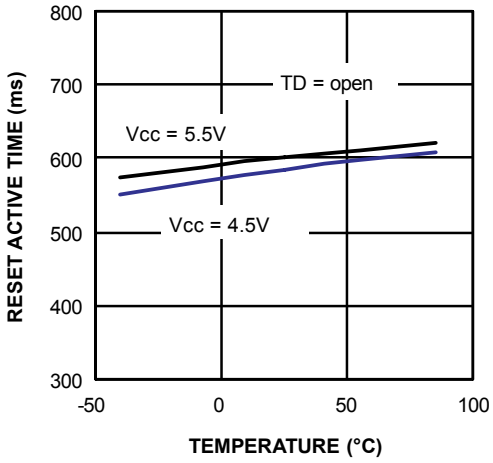
Threshold Voltage vs. Temperature (5% TOL)



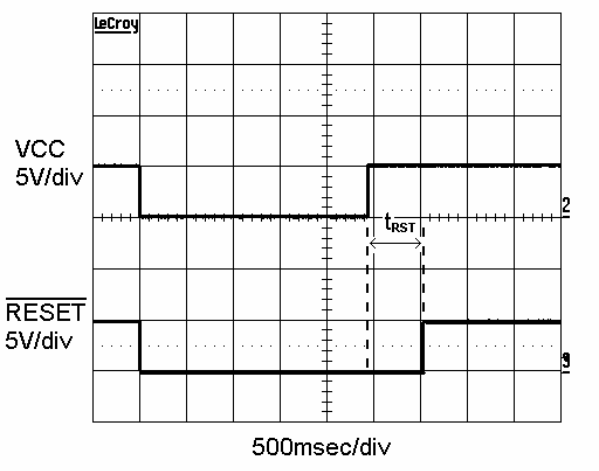
Supply Current vs. Temperature



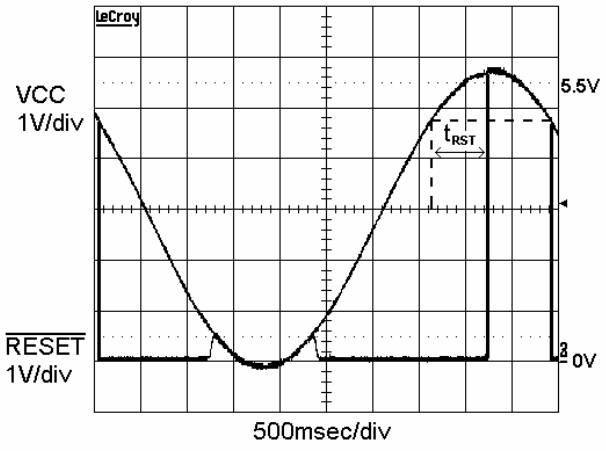
Reset Active Time vs. Temperature



Reset Active Time Waveform



Transient Response



APPLICATION INFORMATION

SUPPLY VOLTAGE MONITOR

Reset Signal Polarity and Output Stage Structure

$\overline{\text{RESET}}$ is an active LOW signal. It is developed with an open drain driver in the CAT1232LP. A pull-up resistor is required, typical values are 10 kΩ to 50 kΩ. The CAT1832 uses a CMOS push-pull output stage for the $\overline{\text{RESET}}$.

RESET is an active High signal developed by a CMOS push-pull output stage and is the logical opposite to $\overline{\text{RESET}}$.

Trip Point Tolerance Selection

The TOL input is used to select the V_{CC} trip point threshold. This selection is made connecting the TOL input to ground or V_{CC}. Connecting TOL to Ground makes the V_{CC} trip threshold 4.62 V for the CAT1232LP and 2.88 V for the CAT1832.

Connecting TOL to V_{CC} makes the V_{CC} trip threshold 4.37 V for the CAT1232LP and 2.55 V for the CAT1832.

After V_{CC} has risen above the trip point set by TOL, RESET and $\overline{\text{RESET}}$remain active for a minimum time period of 250 ms.

On power-down, once V_{CC} falls below the reset threshold the RESET outputs will remain active and are guaranteed valid down to a V_{CC} level of 1.0 V.

Tolerance Select Voltage	Trip Point Tolerance	Trip Point Voltage (V)		
		Min	Nominal	Max
CAT1232LP TOL = V_{CC}	10 %	4.25	4.37	4.49
CAT1232LP TOL = GND	5 %	4.50	4.62	4.74
CAT1832 TOL = V_{CC}	20 %	2.47	2.55	2.64
CAT1832 TOL = GND	10 %	2.80	2.88	2.97

Manual Reset Operation

Push-button input, $\overline{\text{PBRST}}$, allows the user to issue reset signals. The pushbutton input is debounced and is pulled high through an internal 40 kΩ resistor.

When $\overline{\text{PBRST}}$ is held low for the minimum time of 20 ms, both resets become active and remain active for a minimum time period of 250 ms after PBRST returns high.

No external pull-up resistor is required, since $\overline{\text{PBRST}}$ is pulled high by an internal 40 kΩ resistor.

$\overline{\text{PBRST}}$ can be driven from a TTL or CMOS logic line or short-ed to ground with a mechanical switch.

Figure 1. Timing Diagram: Power Up

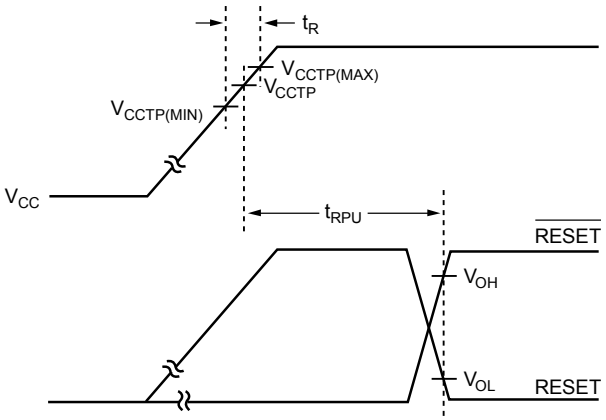
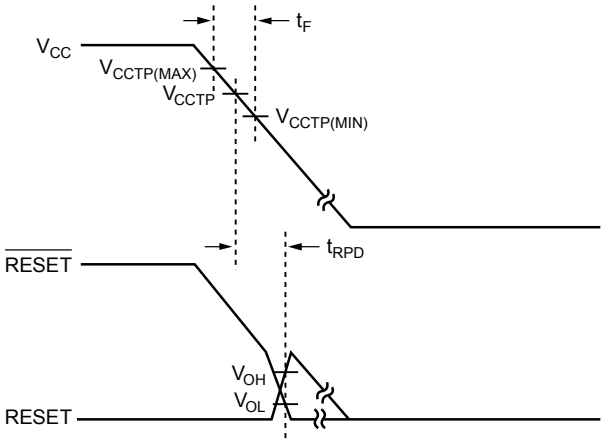


Figure 2. Timing Diagram: Power Down



WATCHDOG TIMER AND $\overline{ST}$ INPUT

A watchdog timer stops and restarts a microprocessor that has stopped proper operation or become “hung”. The watchdog performs this function by monitoring the $\overline{ST}$ input. After the reset outputs go inactive the $\overline{ST}$ input must be strobed with a high-to-low signal transition prior to the minimum watchdog timeout period. However if the $\overline{ST}$ input is not strobed with a high-to-low signal transition prior to a watchdog timeout the reset outputs will become active for TRST reseting and restarting the microprocessor. Once the resets return to the inactive state the watchdog timer restarts the process.

The TD input allows the user to select from three predetermined watchdog timeout periods. Always use the minimum timeout period to determine the required frequency of $\overline{ST}$ high-to-low transitions and the maximum to determine the time prior to the reset outputs becoming active. $\overline{ST}$ pulse widths must be 20 ns or greater.

The watchdog timer cannot be disabled. It must be strobed with a high-to-low signal transition to avoid a watchdog timeout and subsequent reset.

TD Voltage Level	Watchdog Time-out Period (ms)		
	Min	Nominal	Max
GND	62.5	150	250
Floating	250	600	1000
V_{CC}	500	1200	2000

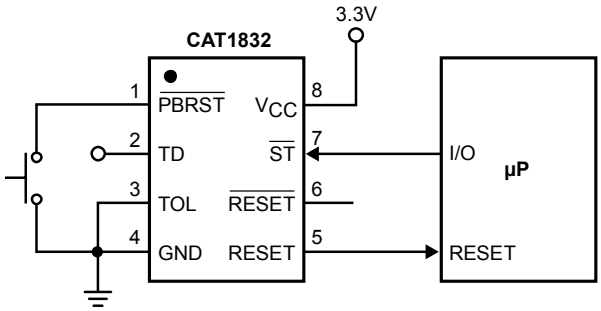


Figure 4. CAT1832 Application Circuit: Pushbutton Reset

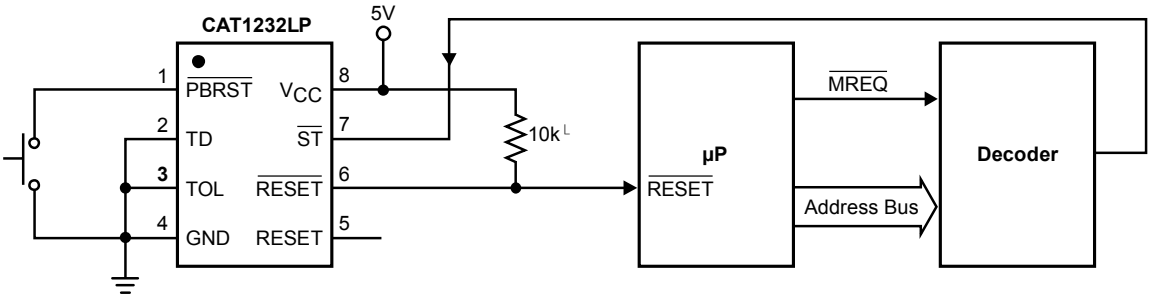


Figure 5. CAT1232LP Application Circuit: Watchdog Timer

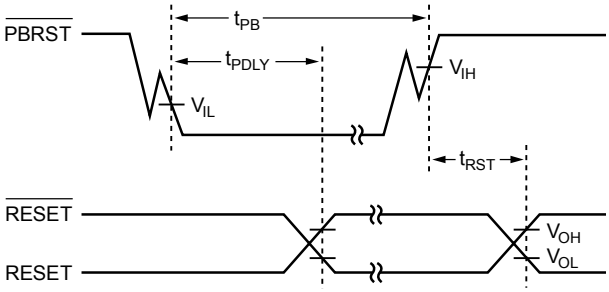
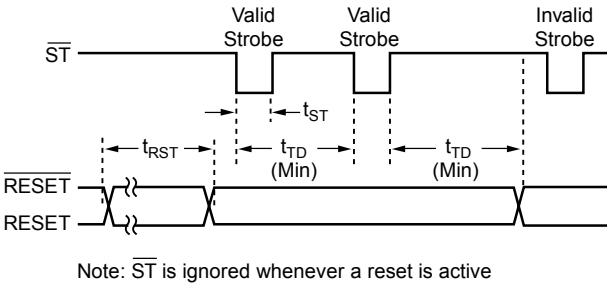


Figure 6. Timing Diagram: Pushbutton Reset

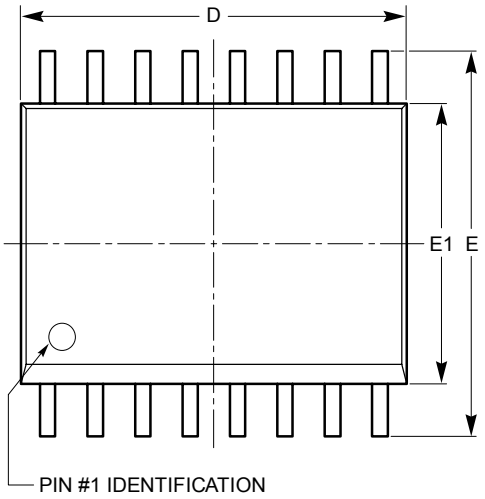


Note: $\overline{ST}$ is ignored whenever a reset is active

Figure 7. Timing Diagram: Strobe Input

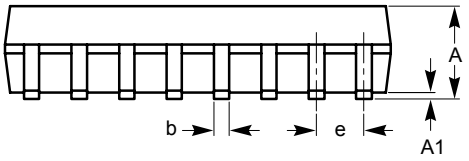
PACKAGE OUTLINE DRAWINGS

SOIC 16-Lead 300 mils (W)[1][2]

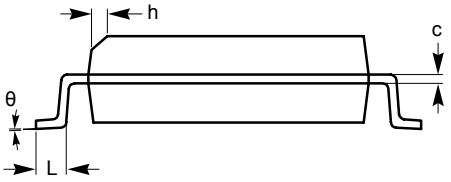


TOP VIEW

SYMBOL	MIN	NOM	MAX
A	2.36	2.49	2.64
A1	0.10		0.30
b	0.33	0.41	0.51
c	0.18	0.23	0.28
D	10.08	10.31	10.49
E	10.01	10.31	10.64
E1	7.39	7.49	7.59
e		1.27 BSC	
h	0.25		0.75
L	0.38	0.81	1.27
θ	0°		8°



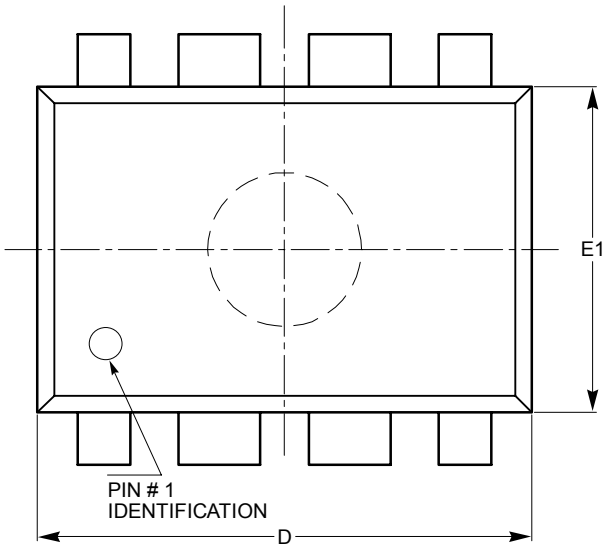
SIDE VIEW



END VIEW

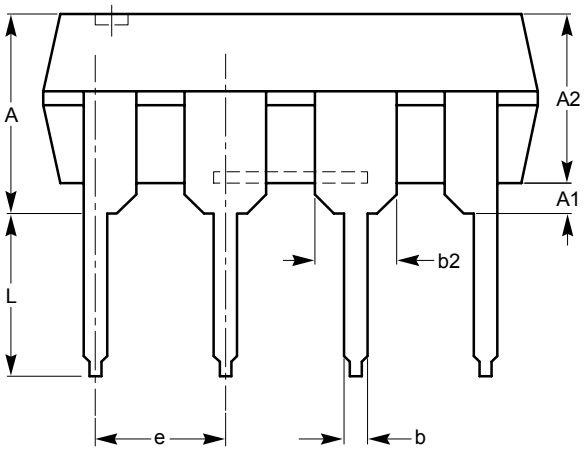
Notes:
(1) All dimensions are in millimeters.
(2) Complies with JEDEC MS-013.

PDIP 8-Lead 300mils (L)[1][2]

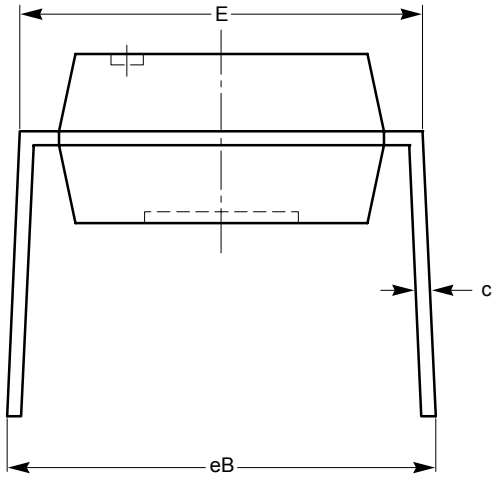


TOP VIEW

SYMBOL	MIN	NOM	MAX
A			5.33
A1	0.38		
A2	2.92	3.30	4.95
b	0.36	0.46	0.56
b2	1.14	1.52	1.78
c	0.20	0.25	0.36
D	9.02	9.27	10.16
E	7.62	7.87	8.25
e		2.54 BSC	
E1	6.10	6.35	7.11
eB	7.87		10.92
L	2.92	3.30	3.80



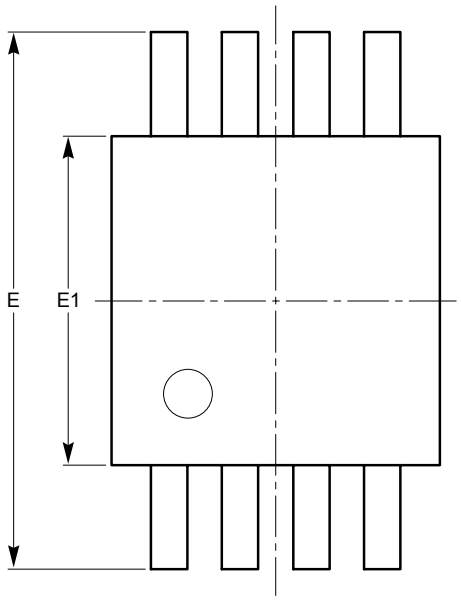
SIDE VIEW



END VIEW

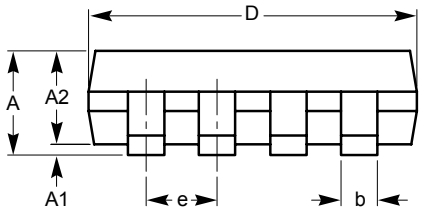
Notes:
(1) All dimensions are in millimeters.
(2) Complies with JEDEC MS-001.

MSOP 8-Lead (Z) [(1)(2)]

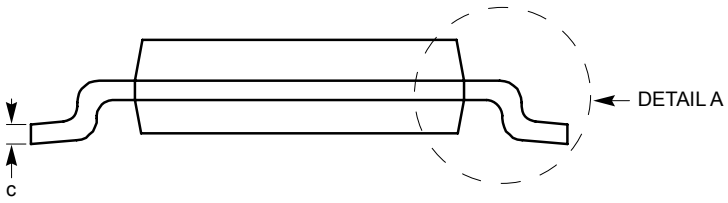


TOP VIEW

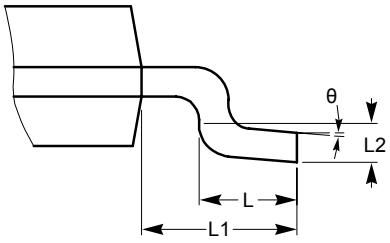
SYMBOL	MIN	NOM	MAX
A			1.10
A1	0.05	0.10	0.15
A2	0.75	0.85	0.95
b	0.22		0.38
c	0.13		0.23
D	2.90	3.00	3.10
E	4.80	4.90	5.00
E1	2.90	3.00	3.10
e	0.65 BSC		
L	0.40	0.60	0.80
L1	0.95 REF		
L2	0.25 BSC		
θ	0°		6°



SIDE VIEW



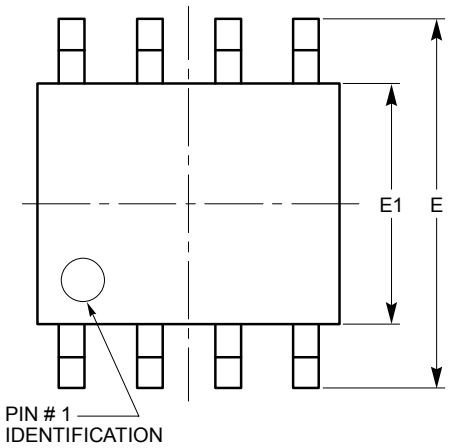
END VIEW



DETAIL A

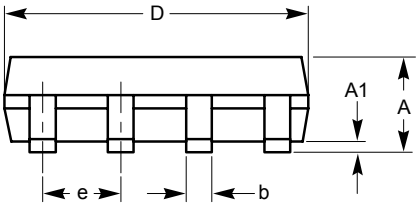
Notes:
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MO-187.

SOIC 8-Lead 150mils (V) [1][2]

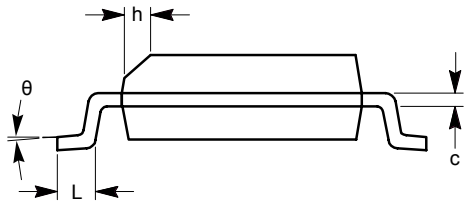


TOP VIEW

SYMBOL	MIN	NOM	MAX
A	1.35		1.75
A1	0.10		0.25
b	0.33		0.51
c	0.19		0.25
D	4.80		5.00
E	5.80		6.20
E1	3.80		4.00
e	1.27 BSC		
h	0.25		0.50
L	0.40		1.27
θ	0°		8°



SIDE VIEW



END VIEW

Notes:
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MS-012.

ORDERING INFORMATION

ORDERING PART NUMBER	Package	Parts per Tube	Parts Per Reel	Reel Size (inch)
CAT1232LPV-GT3*	8-lead, SOIC	—	3,000	13
CAT1232LPZ-GT3*	8-lead, MSOP	—	3,000	13
CAT1832L-G	8-lead, PDIP	50	—	—
CAT1832V-GT3	8-lead, SOIC	—	3,000	13
CAT1832Z-GT3	8-lead, MSOP	—	3,000	13

* Consult sales.

Notes:
(1) All packages are RoHS-compliant (Lead-free, Halogen-free).
(2) The standard lead finish is NiPdAu.
(3) The device used in the above example is a CAT1232LPV-GT3 (SOIC 8-Lead, NiPdAu, Tape & Reel).
(4) For additional package and temperature options, please contact your nearest ON Semiconductor Sales office.
(5) The SOIC 16-Lead package is only available in Matte-Tin finish.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 61312, Phoenix, Arizona 85082–1312 USA
Phone: 480–829–7710 or 800–344–3860 Toll Free USA/Canada
Fax: 480–829–7709 or 800–344–3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800–282–9855 Toll Free USA/Canada

Japan: ON Semiconductor, Japan Customer Focus Center
2–9–1 Kamimeguro, Meguro–ku, Tokyo, Japan 153–0051
Phone: 81–3–5773–3850

ON Semiconductor Website: http://onsemi.com

Order Literature: http://www.onsemi.com/litorder

For additional information, please contact your local Sales Representative.

CAT1232LP/D