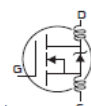


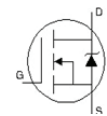
Static @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

| | Parameter | Min. | Typ. | Max. | Units | Conditions |
|---------------------------------|--------------------------------------|------|-------|------|------------|--|
| $V_{(BR)DSS}$ | Drain-to-Source Breakdown Voltage | 40 | — | — | V | $V_{GS} = 0V, I_D = 250\mu A$ |
| $\Delta V_{(BR)DSS}/\Delta T_J$ | Breakdown Voltage Temp. Coefficient | — | 0.032 | — | V/°C | Reference to 25°C , $I_D = 1mA$ |
| $R_{DS(on)}$ | Static Drain-to-Source On-Resistance | — | 4.3 | 5.5 | m Ω | $V_{GS} = 10V, I_D = 75A$ ③ |
| $V_{GS(th)}$ | Gate Threshold Voltage | 2.0 | — | 4.0 | V | $V_{DS} = V_{GS}, I_D = 250\mu A$ |
| g_{fs} | Forward Trans conductance | 63 | — | — | S | $V_{DS} = 10V, I_D = 75A$ |
| I_{DSS} | Drain-to-Source Leakage Current | — | — | 20 | μA | $V_{DS} = 40V, V_{GS} = 0V$ |
| | | — | — | 250 | | $V_{DS} = 40V, V_{GS} = 0V, T_J = 125^\circ\text{C}$ |
| I_{GSS} | Gate-to-Source Forward Leakage | — | — | 200 | nA | $V_{GS} = 20V$ |
| | Gate-to-Source Reverse Leakage | — | — | -200 | | $V_{GS} = -20V$ |

Dynamic Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

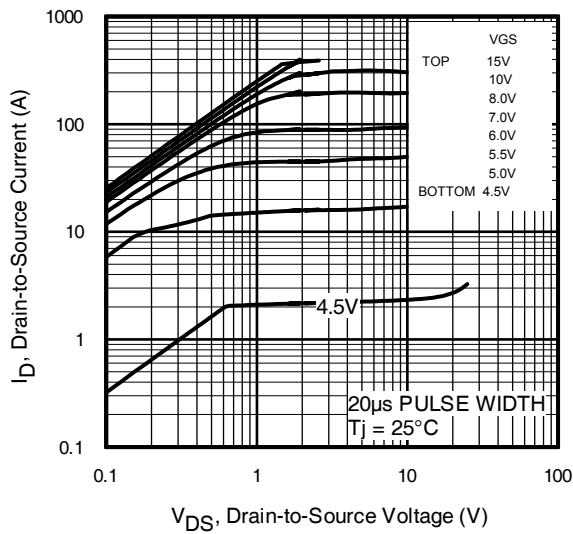
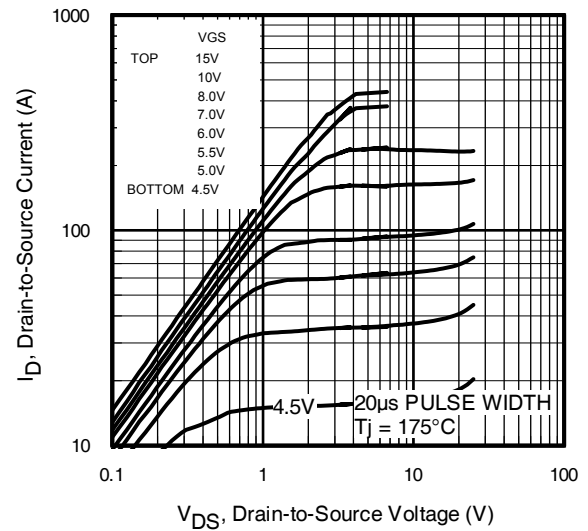
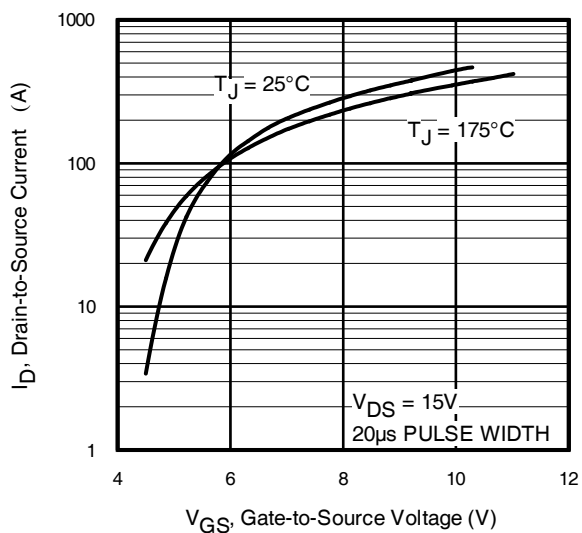
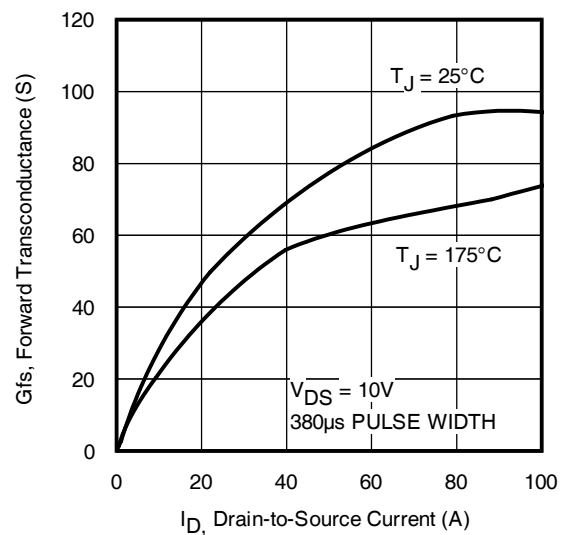
| | | | | | | |
|-----------------|------------------------------|---|------|-----|----|--|
| Q_g | Total Gate Charge | — | 68 | 100 | nC | $I_D = 75A$ |
| Q_{gs} | Gate-to-Source Charge | — | 21 | — | | $V_{DS} = 32V$ |
| Q_{gd} | Gate-to-Drain Charge | — | 27 | — | | $V_{GS} = 10V$ ③ |
| $t_{d(on)}$ | Turn-On Delay Time | — | 16 | — | ns | $V_{DD} = 20V$ |
| t_r | Rise Time | — | 130 | — | | $I_D = 75A$ |
| $t_{d(off)}$ | Turn-Off Delay Time | — | 38 | — | | $R_G = 6.8\Omega$ |
| t_f | Fall Time | — | 77 | — | | $V_{GS} = 10V$ ③ |
| L_D | Internal Drain Inductance | — | 4.5 | — | nH | Between lead, 6mm (0.25in.) from package and center of die contact :  |
| L_S | Internal Source Inductance | — | 7.5 | — | | |
| C_{iss} | Input Capacitance | — | 3000 | — | pF | $V_{GS} = 0V$ |
| C_{oss} | Output Capacitance | — | 660 | — | | $V_{DS} = 25V$ |
| C_{rss} | Reverse Transfer Capacitance | — | 380 | — | | $f = 1.0MHz$, See Fig. 5 |
| C_{oss} | Output Capacitance | — | 2160 | — | | $V_{GS} = 0V, V_{DS} = 1.0V, f = 1.0MHz$ |
| C_{oss} | Output Capacitance | — | 560 | — | | $V_{GS} = 0V, V_{DS} = 32V, f = 1.0MHz$ |
| $C_{oss\ eff.}$ | Effective Output Capacitance | — | 850 | — | | $V_{GS} = 0V, V_{DS} = 0V \text{ to } 32V$ ④ |

Diode Characteristics

| | Parameter | Min. | Typ. | Max. | Units | Conditions |
|----------|--|---|------|------|-------|--|
| I_S | Continuous Source Current (Body Diode) | — | — | 75 | A | MOSFET symbol showing the integral reverse p-n junction diode.  |
| I_{SM} | Pulsed Source Current (Body Diode) ① | — | — | 470 | | |
| V_{SD} | Diode Forward Voltage | — | — | 1.3 | V | $T_J = 25^\circ\text{C}, I_S = 75A, V_{GS} = 0V$ ③ |
| t_{rr} | Reverse Recovery Time | — | 23 | 35 | ns | $T_J = 25^\circ\text{C}, I_F = 75A, V_{DD} = 20V$ |
| Q_{rr} | Reverse Recovery Charge | — | 6.8 | 10 | nC | $di/dt = 100A/\mu s$ ③ |
| t_{on} | Forward Turn-On Time | Intrinsic turn-on time is negligible (turn-on is dominated by $L_S + L_D$) | | | | |

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)
- ② Limited by T_{Jmax} , starting $T_J = 25^\circ\text{C}$, $L = 0.04mH$, $R_G = 25\Omega$, $I_{AS} = 75A$, $V_{GS} = 10V$. Part not recommended for use above this value.
- ③ Pulse width $\leq 1.0ms$; duty cycle $\leq 2\%$.
- ④ $C_{oss\ eff.}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .
- ⑤ This value determined from sample failure population, $T_J = 25^\circ\text{C}$, $L = 0.04mH$, $R_G = 25\Omega$, $I_{AS} = 75A$, $V_{GS} = 10V$.
- ⑥ This is applied to D²Pak When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994
- ⑦ R_θ is measured at T_J of approximately 90°C
- ⑧ This is only applied to TO-220AB package.
- ⑨ Calculated continuous current based on maximum allowable junction temperature. Bond wire current limit is 75A. Note that current limitations arising from heating of the device leads may occur with some lead mounting arrangements. (Refer to AN-1140)


Fig. 1 Typical Output Characteristics

Fig. 2 Typical Output Characteristics

Fig. 3 Typical Transfer Characteristics

Fig. 4 Typical Forward Transconductance vs. Drain Current

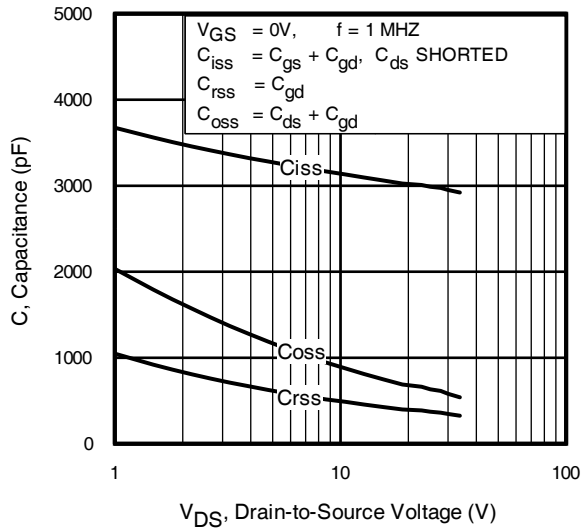


Fig 5. Typical Capacitance vs.
Drain-to-Source Voltage

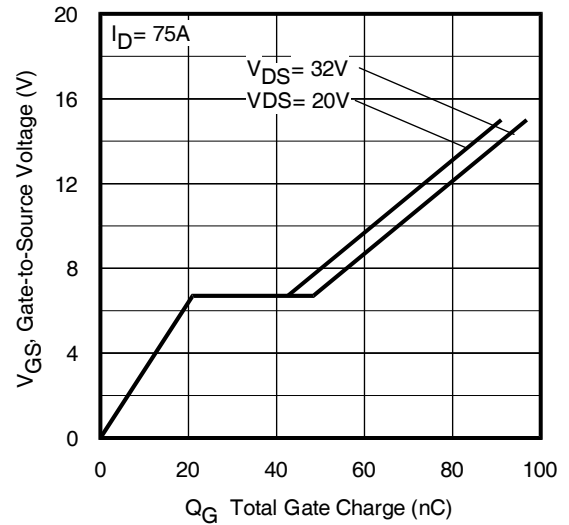


Fig 6. Typical Gate Charge vs.
Gate-to-Source Voltage

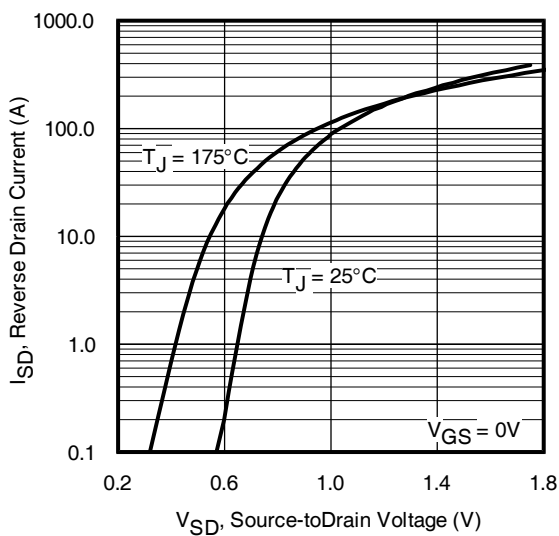


Fig. 7 Typical Source-to-Drain Diode
Forward Voltage

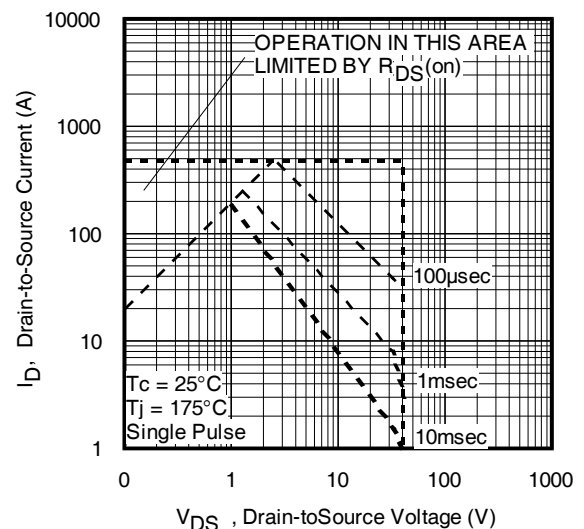
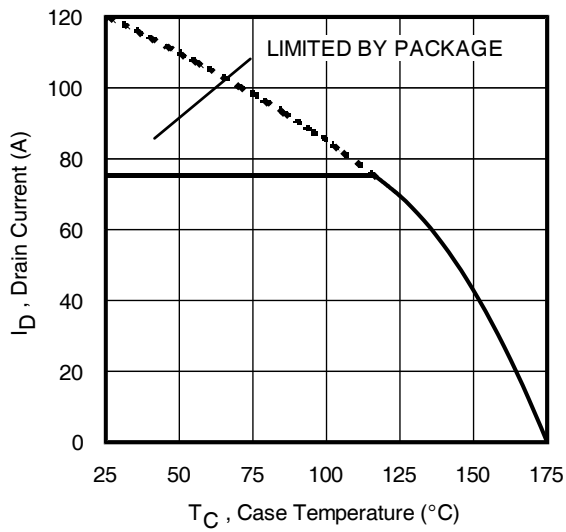
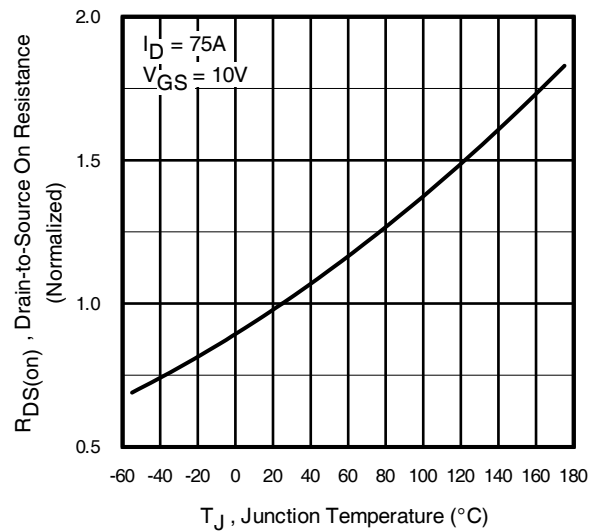
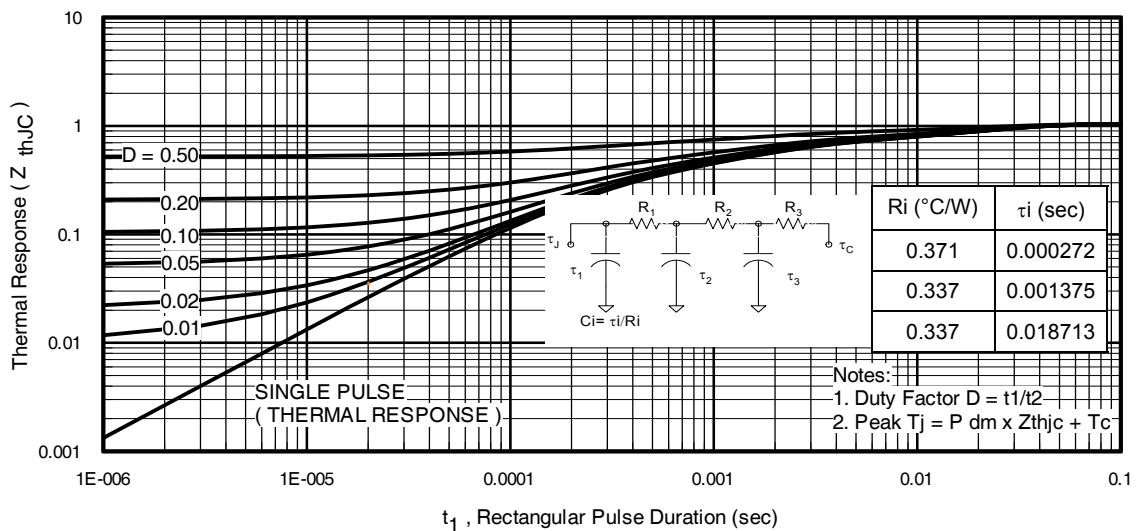
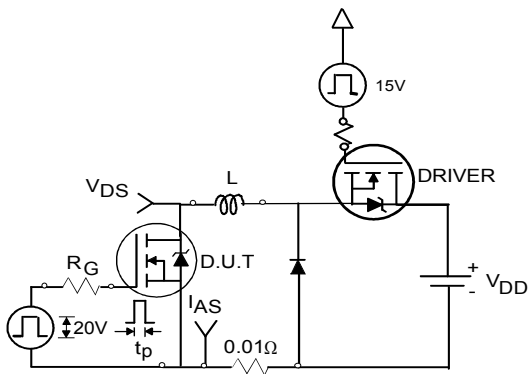
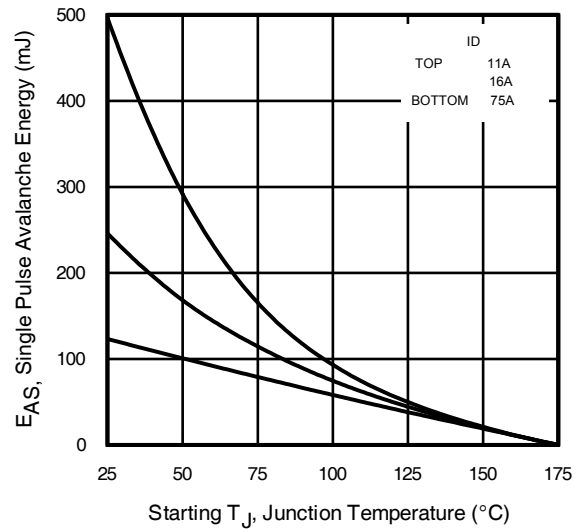
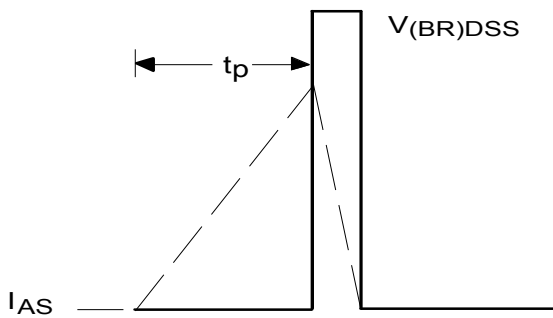
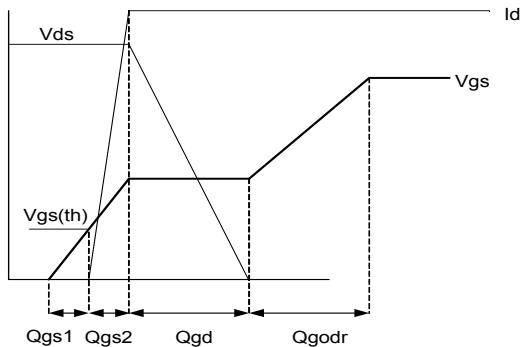
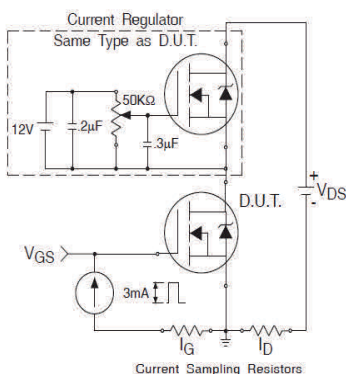
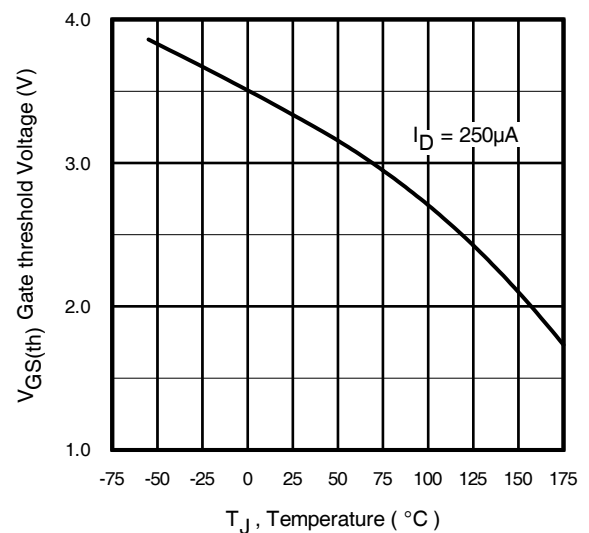


Fig 8. Maximum Safe Operating Area


Fig 9. Maximum Drain Current vs. Case Temperature

Fig 10. Normalized On-Resistance vs. Temperature

Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case


Fig 12a. Unclamped Inductive Test Circuit

Fig 12c. Maximum Avalanche Energy vs. Drain Current

Fig 12b. Unclamped Inductive Waveforms

Fig 13a. Gate Charge Waveform

Fig 13b. Gate Charge Test Circuit

Fig 14. Threshold Voltage vs. Temperature

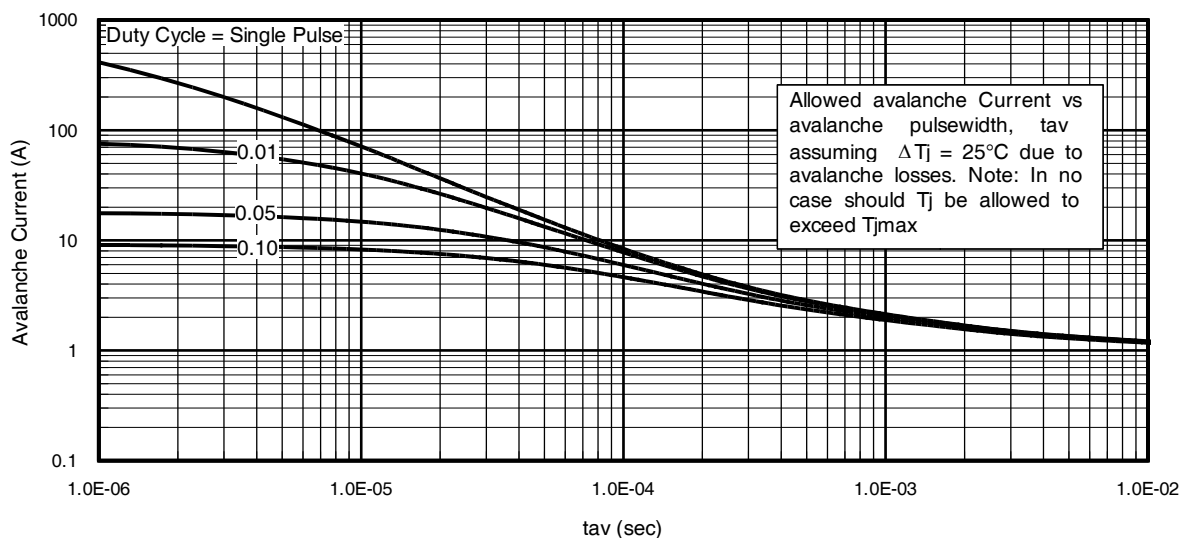


Fig 15. Typical Avalanche Current vs. Pulse width

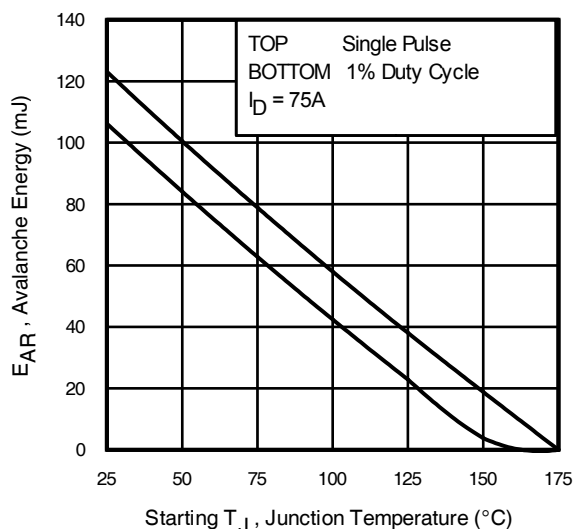


Fig 16. Maximum Avalanche Energy vs. Temperature

Notes on Repetitive Avalanche Curves , Figures 15, 16:
(For further info, see AN-1005 at www.infineon.com)

1. Avalanche failures assumption:
Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax} . This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as T_{jmax} is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 12a, 12b.
4. $P_{D(ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. I_{av} = Allowable avalanche current.
7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 15, 16).
 t_{av} = Average time in avalanche.
 D = Duty cycle in avalanche = $t_{av} \cdot f$
 $Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see Figures 13)

$$P_{D(ave)} = 1/2 (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$

$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{thJC}]$$

$$E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$$

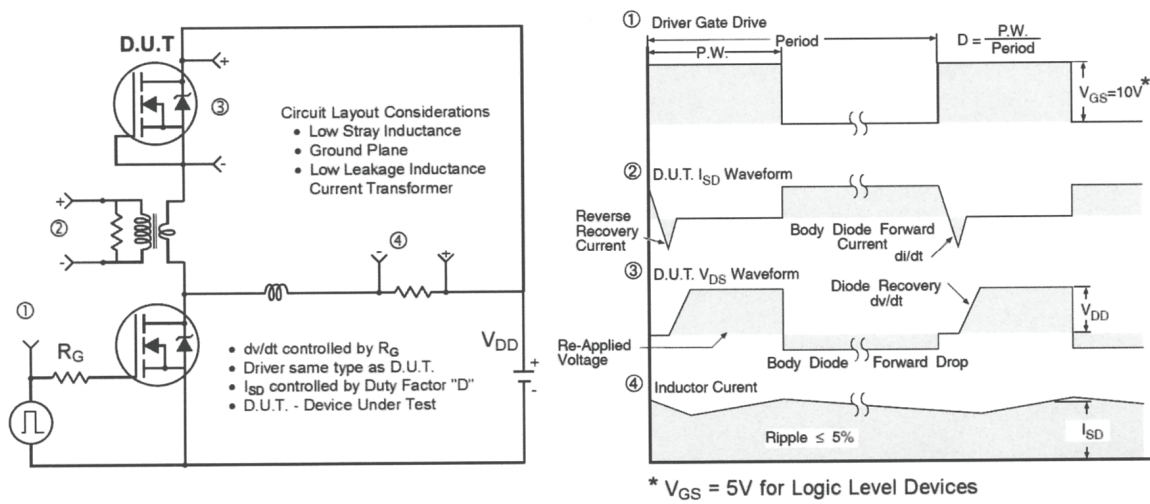


Fig 17. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

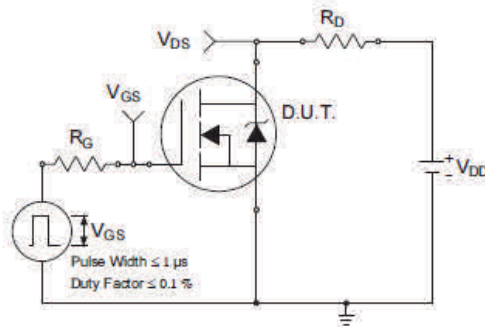


Fig 18a. Switching Time Test Circuit

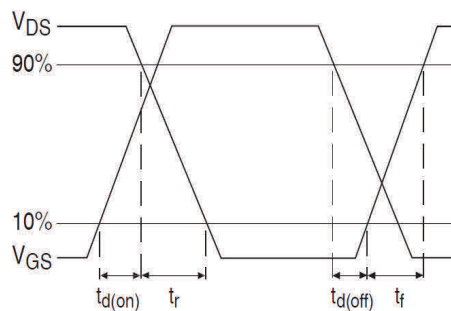
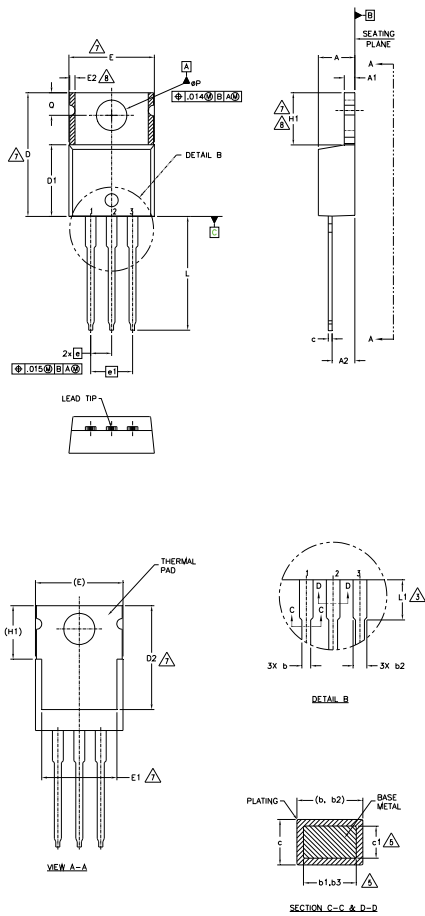



Fig 18b. Switching Time Waveforms

TO-220AB Package Outline (Dimensions are shown in millimeters (inches))



NOTES:

- 1.- DIMENSIONING AND TOLERANCING AS PER ASME Y14.5 M- 1994.
- 2.- DIMENSIONS ARE SHOWN IN INCHES [MILLIMETERS].
- 3.- LEAD DIMENSION AND FINISH UNCONTROLLED IN L1.
- 4.- DIMENSION D, D1 & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
- 5.-  DIMENSION b1, b3 & c1 APPLY TO BASE METAL ONLY.
- 6.- CONTROLLING DIMENSION : INCHES.
- 7.- THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS E1,H1,D2 & E1
- 8.- DIMENSION E2 X H1 DEFINE A ZONE WHERE STAMPING AND SINGULATION IRREGULARITIES ARE ALLOWED.
- 9.- OUTLINE CONFORMS TO JEDEC TO-220, EXCEPT A2 (max.) AND D2 (min.) WHERE DIMENSIONS ARE DERIVED FROM THE ACTUAL PACKAGE OUTLINE.

| SYMBOL | DIMENSIONS | | | | NOTES |
|--------|-------------|-------|----------|------|-------|
| | MILLIMETERS | | INCHES | | |
| | MIN. | MAX. | MIN. | MAX. | |
| A | 3.56 | 4.83 | .140 | .190 | 5 |
| A1 | 1.14 | 1.40 | .045 | .055 | |
| A2 | 2.03 | 2.92 | .080 | .115 | |
| b | 0.38 | 1.01 | .015 | .040 | |
| b1 | 0.38 | 0.97 | .015 | .038 | |
| b2 | 1.14 | 1.78 | .045 | .070 | 5 |
| b3 | 1.14 | 1.73 | .045 | .068 | |
| c | 0.36 | 0.61 | .014 | .024 | |
| c1 | 0.36 | 0.56 | .014 | .022 | 5 |
| D | 14.22 | 16.51 | .560 | .650 | 4 |
| D1 | 8.38 | 9.02 | .330 | .355 | 7 |
| D2 | 11.68 | 12.88 | .460 | .507 | |
| E | 9.65 | 10.67 | .380 | .420 | |
| E1 | 6.86 | 8.89 | .270 | .350 | 4, 7 |
| E2 | — | 0.76 | — | .030 | 7 |
| e | 2.54 BSC | | .100 BSC | | 8 |
| e1 | 5.08 BSC | | .200 BSC | | |
| H1 | 5.84 | 6.86 | .230 | .270 | 7, 8 |
| L | 12.70 | 14.73 | .500 | .580 | |
| L1 | 3.56 | 4.06 | .140 | .160 | 3 |
| øP | 3.54 | 4.08 | .139 | .161 | |
| Q | 2.54 | 3.42 | .100 | .135 | |

LEAD ASSIGNMENTS

- HEXFET
- 1.- GATE
 - 2.- DRAIN
 - 3.- SOURCE

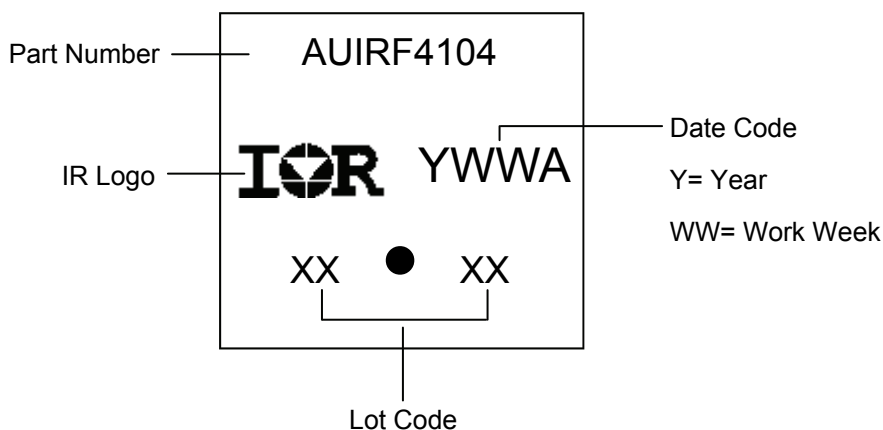
IGBTs, CoPACK

- 1.- GATE
- 2.- COLLECTOR
- 3.- EMITTER

DIODES

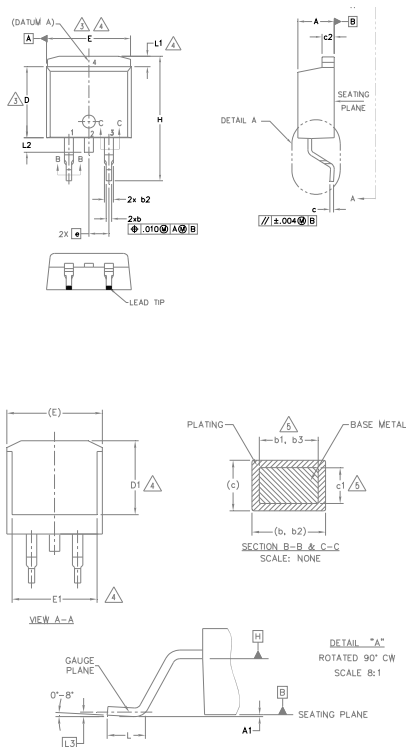
- 1.- ANODE
- 2.- CATHODE
- 3.- ANODE

TO-220AB Part Marking Information



TO-220AB package is not recommended for Surface Mount Application.

D²Pak (TO-263AB) Package Outline (Dimensions are shown in millimeters (inches))



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [0.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
4. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSION E, L1, D1 & E1.
5. DIMENSION b1, b3 AND c1 APPLY TO BASE METAL ONLY.
6. DATUM A & B TO BE DETERMINED AT DATUM PLANE H.
7. CONTROLLING DIMENSION: INCH.
8. OUTLINE CONFORMS TO JEDEC OUTLINE TO-263AB.

| SYMBOL | DIMENSIONS | | | | NOTES | |
|--------|-------------|-------|----------|------|-------|---|
| | MILLIMETERS | | INCHES | | | |
| | MIN. | MAX. | MIN. | MAX. | | |
| A | 4.06 | 4.83 | .160 | .190 | | |
| A1 | 0.00 | 0.254 | .000 | .010 | | |
| b | 0.51 | 0.99 | .020 | .039 | | |
| b1 | 0.51 | 0.89 | .020 | .035 | | 5 |
| b2 | 1.14 | 1.78 | .045 | .070 | | |
| b3 | 1.14 | 1.73 | .045 | .068 | 5 | |
| c | 0.38 | 0.74 | .015 | .029 | | |
| c1 | 0.38 | 0.58 | .015 | .023 | | 5 |
| c2 | 1.14 | 1.65 | .045 | .065 | | |
| D | 8.38 | 9.65 | .330 | .380 | 3 | |
| D1 | 6.86 | — | .270 | — | 4 | |
| E | 9.65 | 10.67 | .380 | .420 | 3,4 | |
| E1 | 6.22 | — | .245 | — | 4 | |
| e | 2.54 BSC | | .100 BSC | | 4 | |
| H | 14.61 | 15.88 | .575 | .625 | | |
| L | 1.78 | 2.79 | .070 | .110 | | |
| L1 | — | 1.68 | — | .066 | | |
| L2 | — | 1.78 | — | .070 | | |
| L3 | 0.25 BSC | | .010 BSC | | | |

LEAD ASSIGNMENTS

DIODES

- 1.- ANODE (TWO DIE) / OPEN (ONE DIE)
- 2.- CATHODE
- 3.- ANODE

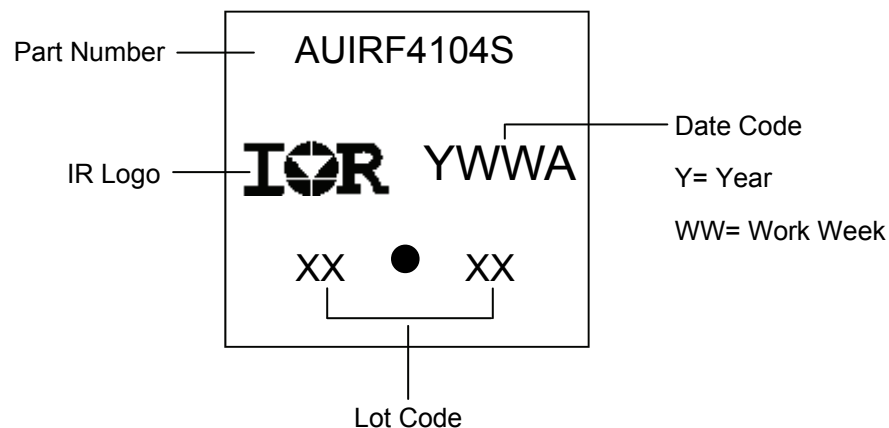
HEXFET

- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE

IGBTs, CoPACK

- 1.- GATE
- 2, 4.- COLLECTOR
- 3.- EMITTER

D²Pak (TO-263AB) Part Marking Information



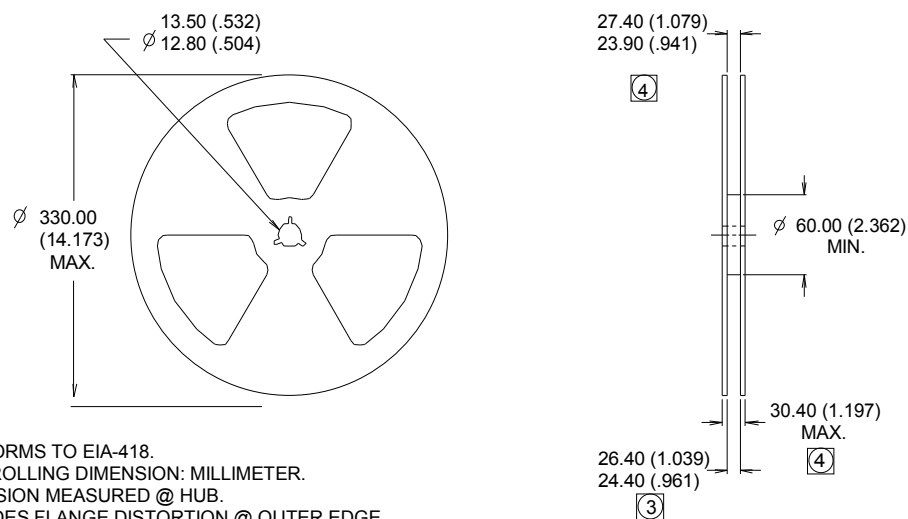
The figure shows two technical drawings of components, TRR and TRL, with their respective dimensions and feed directions.

TRR Component:

- Feed Direction:** Indicated by an arrow pointing right.
- Dimensions:**
 - Top: 1.60 (.063), 1.50 (.059)
 - Left: 4.10 (.161), 3.90 (.153)
 - Right: 1.60 (.063), 1.50 (.059)
 - Bottom: 11.60 (.457), 11.40 (.449)
 - Internal: 1.75 (.069), 1.25 (.049)
 - Overall: 16.10 (.634), 15.90 (.626)
 - Feed Direction: 1.85 (.073), 1.65 (.065)

TRL Component:

- Feed Direction:** Indicated by an arrow pointing right.
- Dimensions:**
 - Top: 0.368 (.0145), 0.342 (.0135)
 - Left: 15.42 (.609), 15.22 (.601)
 - Right: 24.30 (.957), 23.90 (.941)
 - Bottom: 4.72 (.136), 4.52 (.178)



NOTES :

1. COMFORMS TO EIA-418.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION MEASURED @ HUB.
4. INCLUDES FLANGE DISTORTION @ OUTER EDGE.

Qualification Information

| | | | |
|-----------------------------------|----------------------|---|------|
| Qualification Level | | Automotive (per AEC-Q101) | |
| | | Comments: This part number(s) passed Automotive qualification. Infineon's Industrial and Consumer qualification level is granted by extension of the higher Automotive level. | |
| Moisture Sensitivity Level | | TO-220AB | N/A |
| | | D ² -Pak | MSL1 |
| ESD | Machine Model | Class M4 [†] AEC-Q101-002 | |
| | Human Body Model | Class H1C [†] AEC-Q101-001 | |
| | Charged Device Model | Class C3 [†] AEC-Q101-005 | |
| RoHS Compliant | | Yes | |

† Highest passing voltage.

Revision History

| Date | Comments |
|------------|--|
| 09/30/2015 | <ul style="list-style-type: none"> Updated datasheet with corporate template Corrected ordering table on page 1. |
| 09/22/2017 | <ul style="list-style-type: none"> Corrected typo error on part marking on pages 9,10. |

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