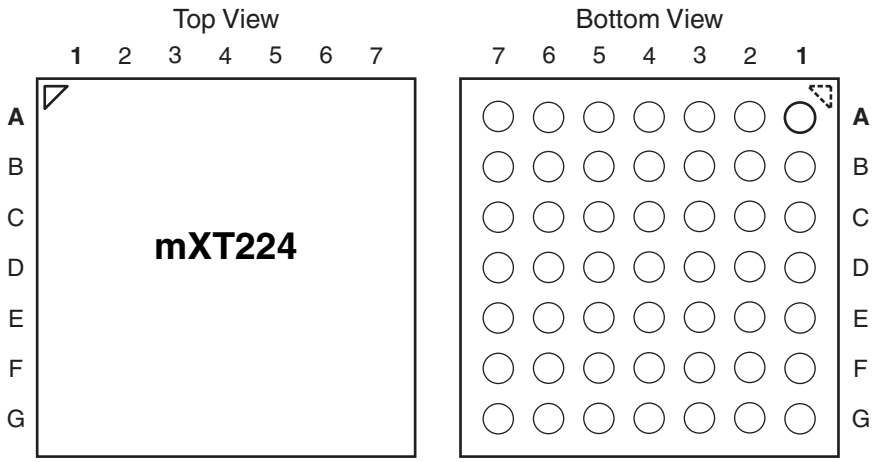
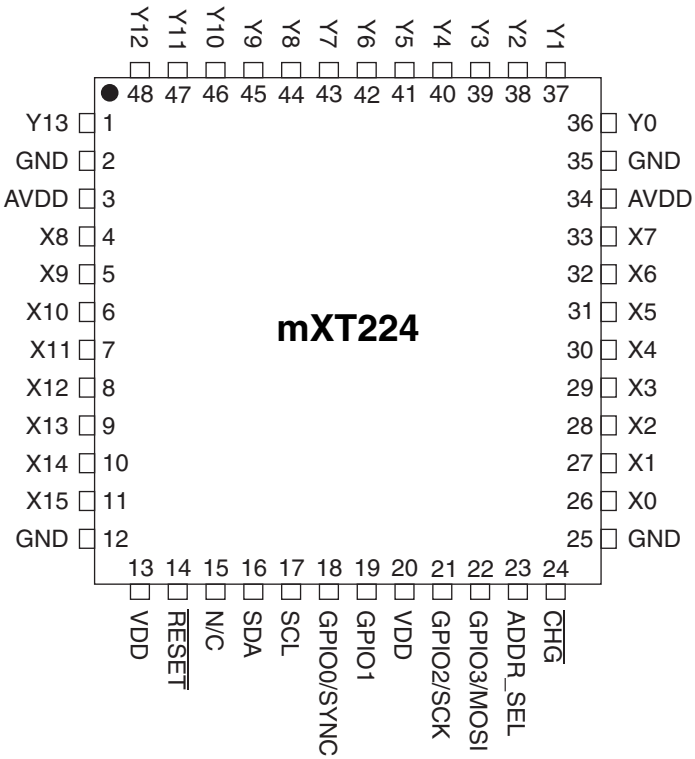
1. Pinout and Schematic

1.1 Pinout Configuration

1.1.1 49-ball UFBGA/VFBGA



1.1.2 48-pin QFN



1.2 Pinout Descriptions

1.2.1 49-ball UFBGA/VFBGA

Table 1-1. Pin Listing

Ball	Name	Type	Comments	If Unused, Connect To...
A1	AVDD	P	Analog power	–
A2	Y12	I/O	Y line connection or X line in extended mode	Leave open
A3	Y10	I/O	Y line connection or X line in extended mode	Leave open
A4	Y8	I	Y line connection	Leave open
A5	Y6	I	Y line connection	Leave open
A6	Y4	I	Y line connection	Leave open
A7	Y2	I	Y line connection	Leave open
B1	X8	O	X matrix drive line	Leave open
B2	GND	P	Ground	–
B3	Y11	I/O	Y line connection or X line in extended mode	Leave open
B4	Y9	I	Y line connection	Leave open
B5	Y5	I	Y line connection	Leave open
B6	Y1	I	Y line connection	Leave open
B7	Y0	I	Y line connection	Leave open
C1	X10	O	X matrix drive line	Leave open
C2	X9	O	X matrix drive line	Leave open
C3	Y13	I/O	Y line connection or X line in extended mode	Leave open
C4	Y7	I	Y line connection	Leave open
C5	Y3	I	Y line connection	Leave open
C6	GND	P	Ground	–
C7	AVDD	P	Analog power	–
D1	X12	O	X matrix drive line	Leave open
D2	X13	O	X matrix drive line	Leave open
D3	X11	O	X matrix drive line	Leave open
D4	GND	P	Ground	–
D5	X7	O	X matrix drive line	Leave open
D6	X5	O	X matrix drive line	Leave open
D7	X6	O	X matrix drive line	Leave open
E1	X14	O	X matrix drive line	Leave open
E2	X15	O	X matrix drive line	Leave open
E3	$\overline{\text{RESET}}$	I	Reset low; has internal 30 kΩ to 60 kΩ pull-up resistor	Vdd
E4	GPIO1	I/O	General purpose I/O	Input: GND Output: leave open

Table 1-1. Pin Listing (Continued)

Ball	Name	Type	Comments	If Unused, Connect To...
E5	X1	O	X matrix drive line	Leave open
E6	X3	O	X matrix drive line	Leave open
E7	X4	O	X matrix drive line	Leave open
F1	VDD	P	Digital power	–
F2	GND	P	Ground	–
F3	SCL	OD	Serial Interface Clock	–
F4	GPIO3/ MOSI	I/O	General purpose I/O / Debug data	Input: GND Output: leave open
F5	GND	P	Ground	–
F6	$\overline{\text{CHG}}$	OD	State change interrupt	–
F7	X2	O	X matrix drive line	Leave open
G1	N/C	–	No connection	Leave open
G2	SDA	OD	Serial Interface Data	–
G3	GPIO0/ SYNC	I/O	General purpose I/O External synchronization	Input: GND Output: leave open
G4	GPIO2/ SCK	I/O	General purpose I/O / Debug clock	Input: GND Output: leave open
G5	VDD	P	Digital power	–
G6	ADDR_SEL	I	I^2C-compatible address select	–
G7	X0	O	X matrix drive line	Leave open

I Input only
O Output only, push-pull
P Ground or power
I/O Input and output
OD Open drain output

1.2.2 48-pin QFN

Table 1-2. Pin Listing

Pin	Name	Type	Comments	If Unused, Connect To...
1	Y13	I/O	Y line connection or X line in extended mode	Leave open
2	GND	P	Ground	–
3	AVDD	P	Analog power	–
4	X8	O	X matrix drive line	Leave open
5	X9	O	X matrix drive line	Leave open
6	X10	O	X matrix drive line	Leave open
7	X11	O	X matrix drive line	Leave open
8	X12	O	X matrix drive line	Leave open
9	X13	O	X matrix drive line	Leave open
10	X14	O	X matrix drive line	Leave open
11	X15	O	X matrix drive line	Leave open
12	GND	P	Ground	–
13	VDD	P	Digital power	–
14	$\overline{\text{RESET}}$	I	Reset low; has internal 30 kΩ to 60 kΩ pull-up resistor	Vdd
15	N/C	–	No connection	Leave open
16	SDA	OD	Serial Interface Data	–
17	SCL	OD	Serial Interface Clock	–
18	GPIO0/ SYNC	I/O	General purpose I/O External synchronization	Input: GND Output: leave open
19	GPIO1	I/O	General purpose I/O	Input: GND Output: leave open
20	VDD	P	Digital power	–
21	GPIO2/ SCK	I/O	General purpose I/O / Debug clock	Input: GND Output: leave open
22	GPIO3/ MOSI	I/O	General purpose I/O / Debug data	Input: GND Output: leave open
23	ADDR_SEL	I	I^2C-compatible address select	–
24	$\overline{\text{CHG}}$	OD	State change interrupt	–
25	GND	P	Ground	–
26	X0	O	X matrix drive line	Leave open
27	X1	O	X matrix drive line	Leave open
28	X2	O	X matrix drive line	Leave open
29	X3	O	X matrix drive line	Leave open
30	X4	O	X matrix drive line	Leave open
31	X5	O	X matrix drive line	Leave open
32	X6	O	X matrix drive line	Leave open

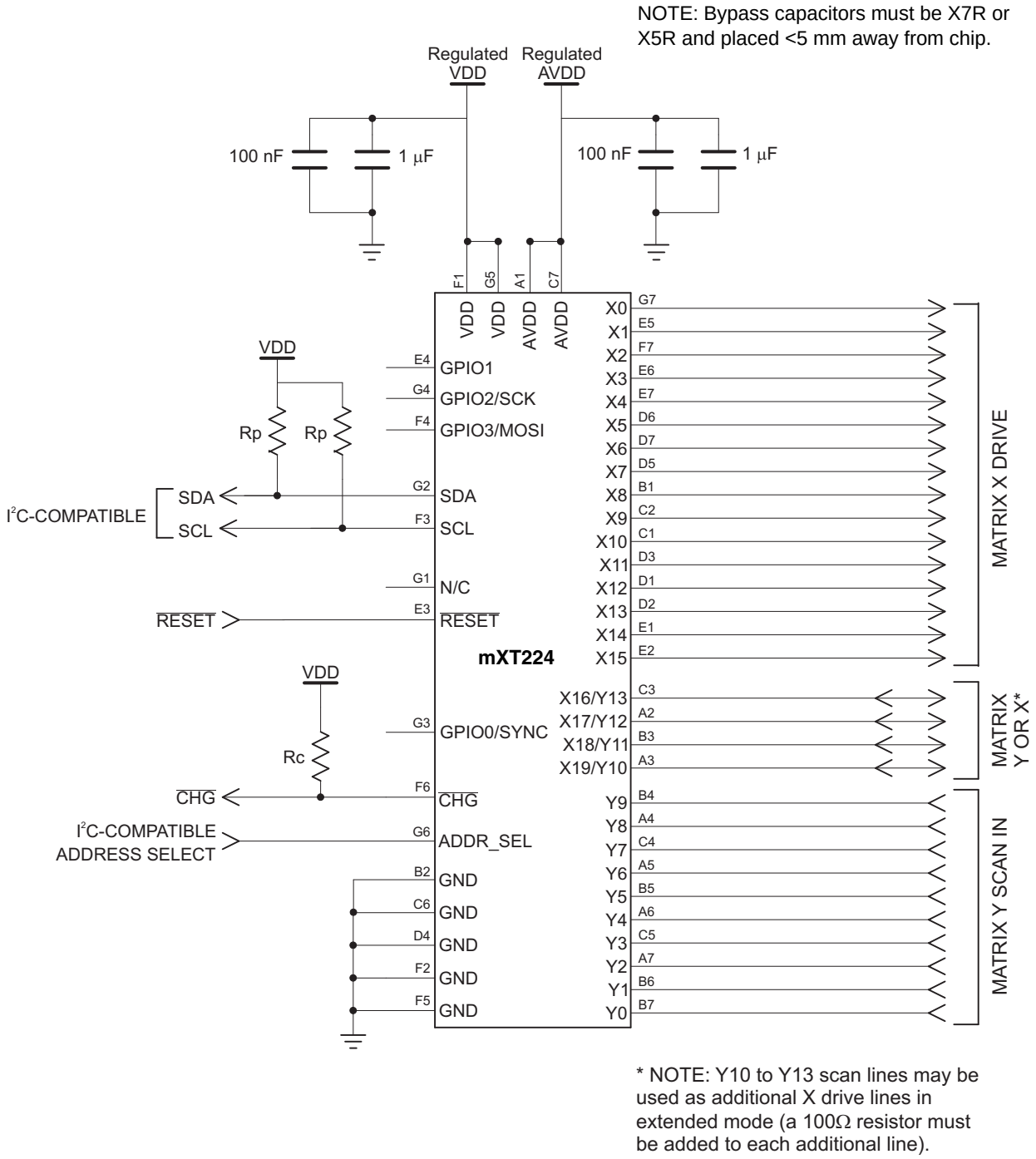
Table 1-2. Pin Listing (Continued)

Pin	Name	Type	Comments	If Unused, Connect To...
33	X7	O	X matrix drive line	Leave open
34	AVDD	P	Analog power	–
35	GND	P	Ground	–
36	Y0	I	Y line connection	Leave open
37	Y1	I	Y line connection	Leave open
38	Y2	I	Y line connection	Leave open
39	Y3	I	Y line connection	Leave open
40	Y4	I	Y line connection	Leave open
41	Y5	I	Y line connection	Leave open
42	Y6	I	Y line connection	Leave open
43	Y7	I	Y line connection	Leave open
44	Y8	I	Y line connection	Leave open
45	Y9	I	Y line connection	Leave open
46	Y10	I/O	Y line connection or X line in extended mode	Leave open
47	Y11	I/O	Y line connection or X line in extended mode	Leave open
48	Y12	I/O	Y line connection or X line in extended mode	Leave open

I Input only
O Output only, push-pull
P Ground or power
I/O Input and output
OD Open drain output

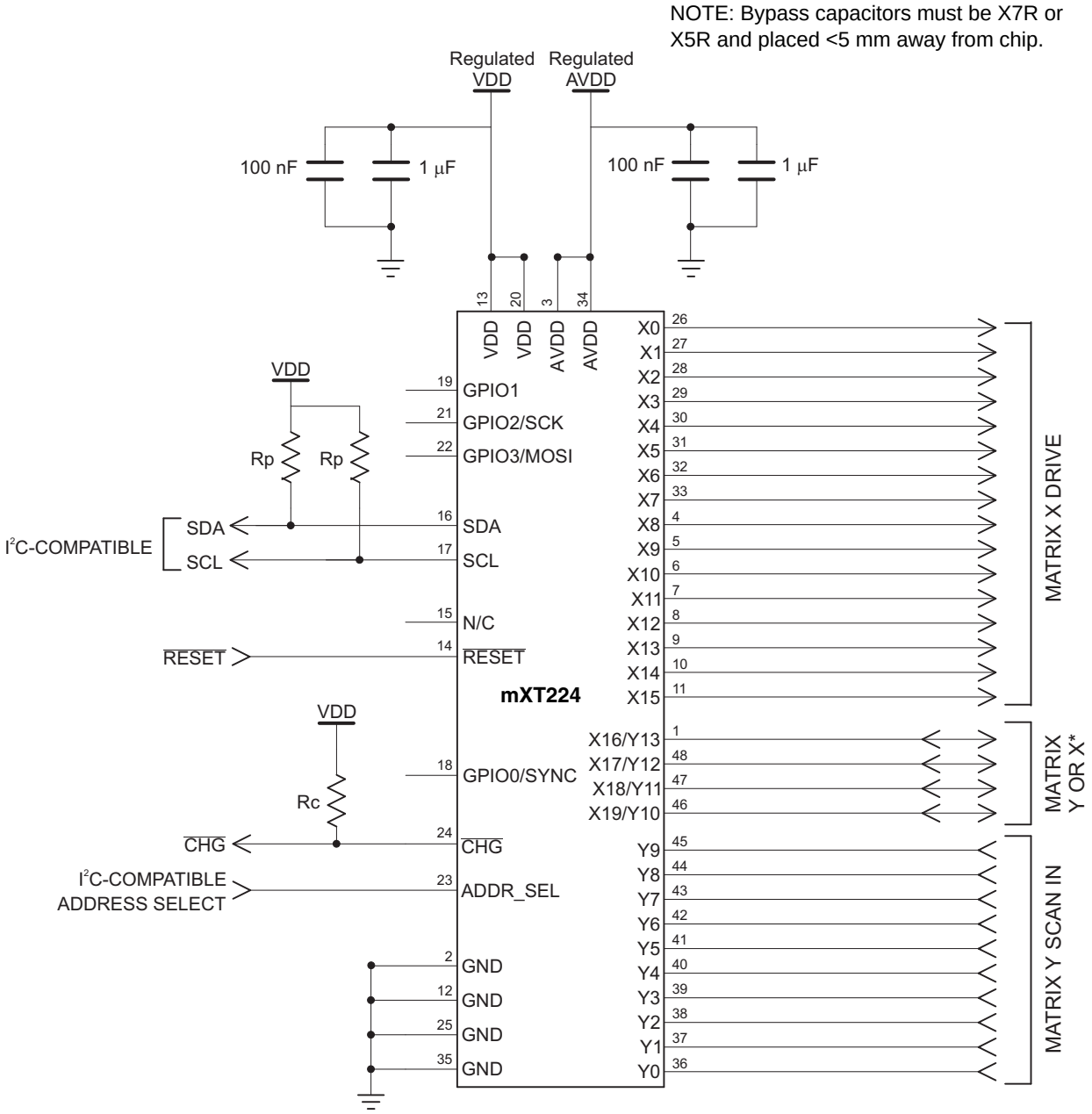
1.3 Schematic

1.3.1 49-ball UFBGA/VFBGA



* NOTE: Y10 to Y13 scan lines may be used as additional X drive lines in extended mode (a 100Ω resistor must be added to each additional line).

1.3.2 48-pin QFN



* NOTE: Y10 to Y13 scan lines may be used as additional X drive lines in extended mode (a 100Ω resistor must be added to each additional line).

2. Overview of the mXT224

2.1 Introduction

The mXT224 uses a unique charge-transfer acquisition engine to implement the QMatrix™ capacitive sensing method patented by Atmel®. This allows the measurement of up to 224 mutual capacitance nodes in under 1 ms. Coupled with a state-of-the-art XMEGA™ CPU, the entire touchscreen sensing solution can measure, classify and track a single finger touch every 4 ms if required.

The acquisition engine uses an optimal measurement approach to ensure almost complete immunity from parasitic capacitance on the receiver inputs (Y lines). The engine includes sufficient dynamic range to cope with touchscreen mutual capacitances spanning 0.5 pF to 5 pF. This allows great flexibility for use with Atmel's proprietary ITO pattern designs. One and two layer ITO sensors are possible using glass or PET substrates.

The main AVR® XMEGA CPU has two powerful, yet low power, microsequencer coprocessors under its control. These combine to allow the signal acquisition, preprocessing, postprocessing and housekeeping to be partitioned in an efficient and flexible way. This gives ample scope for sensing algorithms, touch tracking or advanced shape-based filtering. An in-circuit reflash can be performed over the chip's hardware-driven two-wire interface (I^2C-compatible).

The mXT224 represents a step improvement over competing technologies. It provides a near optimal mix of low power, small size and low part count with unrivalled true multitouch performance.

Revision History

Revision Number	History
Revision AS – September 2009	Initial release for chip revision 1.4
Revision BS – October 2009	QFN package details added
Revision CS – November 2009	Updated for chip revision 1.5

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9530CS–AT42–11/09