Pin Configurations

PDIP

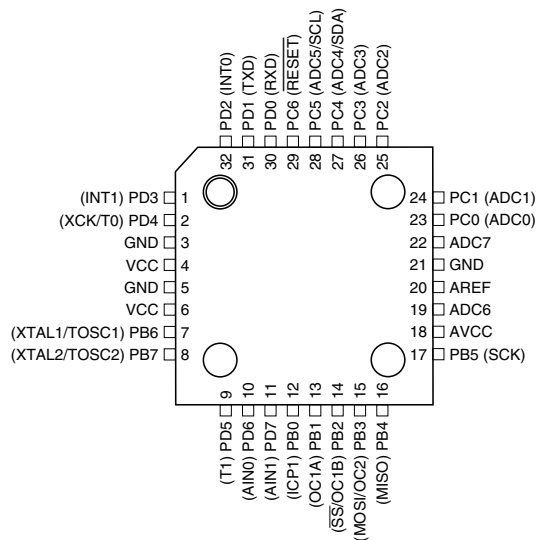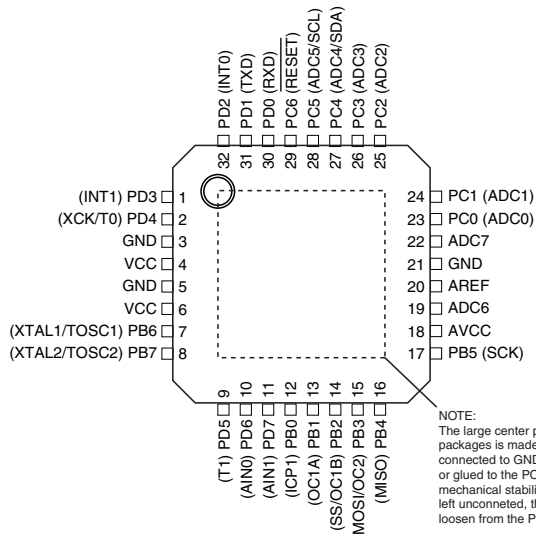|					
(RESET) PC6	1			28	PC5 (ADC5/SCL)
(RXD) PD0	2			27	PC4 (ADC4/SDA)
(TXD) PD1	3			26	PC3 (ADC3)
(INT0) PD2	4			25	PC2 (ADC2)
(INT1) PD3	5			24	PC1 (ADC1)
(XCK/T0) PD4	6			23	PC0 (ADC0)
VCC	7			22	GND
GND	8			21	AREF
(XTAL1/TOSC1) PB6	9			20	AVCC
(XTAL2/TOSC2) PB7	10			19	PB5 (SCK)
(T1) PD5	11			18	PB4 (MISO)
(AIN0) PD6	12			17	PB3 (MOSI/OC2)
(AIN1) PD7	13			16	PB2 (SS/OC1B)
(ICP1) PB0	14			15	PB1 (OC1A)
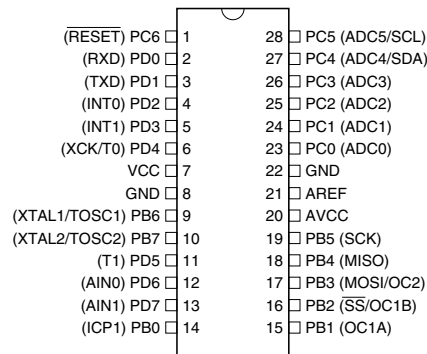
TQFP Top View

MLF Top View

NOTE:
The large center pad underneath the MLF packages is made of metal and internally connected to GND. It should be soldered or glued to the PCB to ensure good mechanical stability. If the center pad is left unconnected, the package might loosen from the PCB.

Atmel

Overview

The Atmel®AVR® ATmega8 is a low-power CMOS 8-bit microcontroller based on the AVR RISC architecture. By executing powerful instructions in a single clock cycle, the ATmega8 achieves throughputs approaching 1MIPS per MHz, allowing the system designer to optimize power consumption versus processing speed.

Block Diagram

Figure 1. Block Diagram
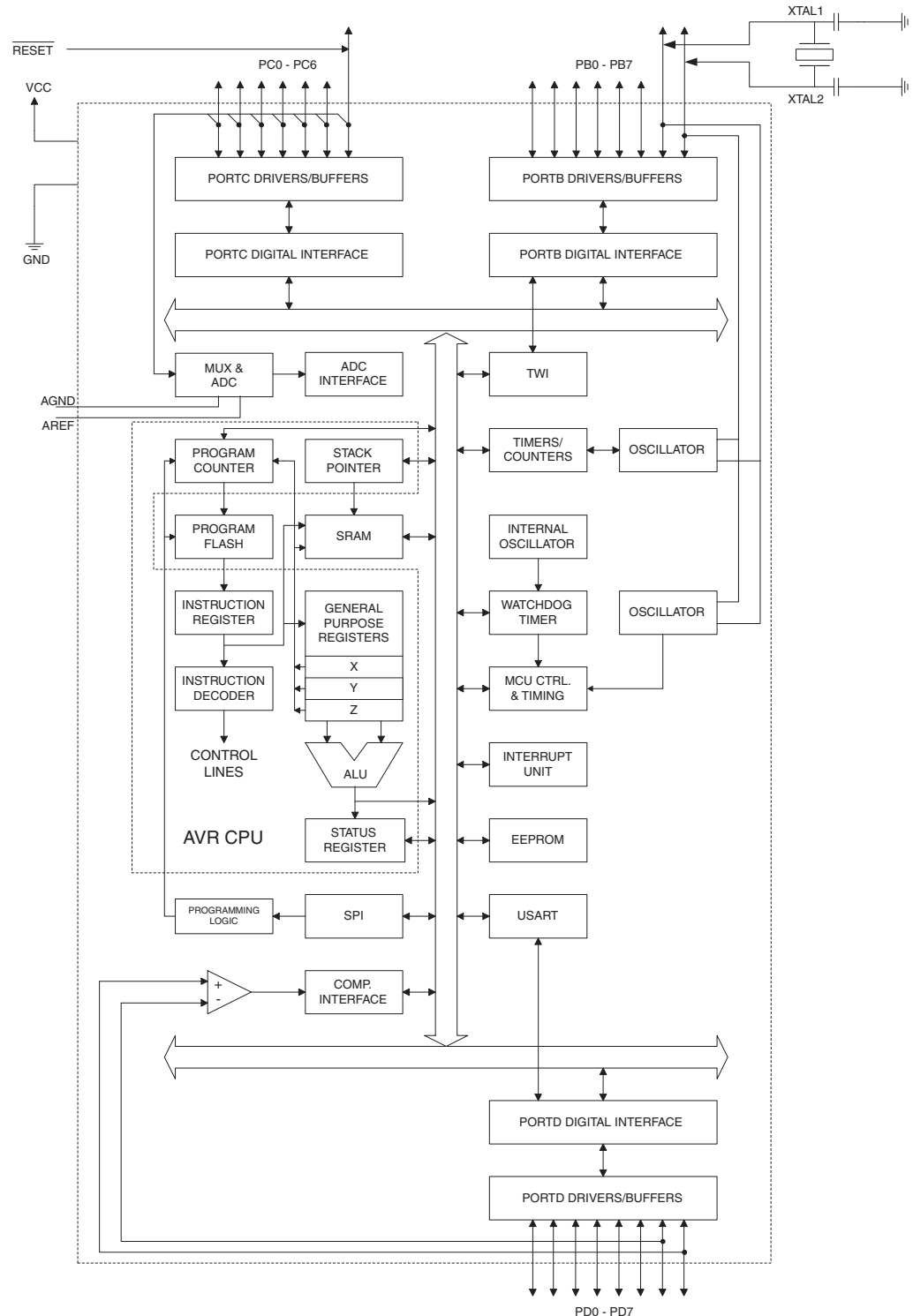
The Atmel®AVR® core combines a rich instruction set with 32 general purpose working registers. All the 32 registers are directly connected to the Arithmetic Logic Unit (ALU), allowing two independent registers to be accessed in one single instruction executed in one clock cycle. The resulting architecture is more code efficient while achieving throughputs up to ten times faster than conventional CISC microcontrollers.

The ATmega8 provides the following features: 8 Kbytes of In-System Programmable Flash with Read-While-Write capabilities, 512 bytes of EEPROM, 1 Kbyte of SRAM, 23 general purpose I/O lines, 32 general purpose working registers, three flexible Timer/Counters with compare modes, internal and external interrupts, a serial programmable USART, a byte oriented Two-wire Serial Interface, a 6-channel ADC (eight channels in TQFP and QFN/MLF packages) with 10-bit accuracy, a programmable Watchdog Timer with Internal Oscillator, an SPI serial port, and five software selectable power saving modes. The Idle mode stops the CPU while allowing the SRAM, Timer/Counters, SPI port, and interrupt system to continue functioning. The Power-down mode saves the register contents but freezes the Oscillator, disabling all other chip functions until the next Interrupt or Hardware Reset. In Power-save mode, the asynchronous timer continues to run, allowing the user to maintain a timer base while the rest of the device is sleeping. The ADC Noise Reduction mode stops the CPU and all I/O modules except asynchronous timer and ADC, to minimize switching noise during ADC conversions. In Standby mode, the crystal/resonator Oscillator is running while the rest of the device is sleeping. This allows very fast start-up combined with low-power consumption.

The device is manufactured using Atmel's high density non-volatile memory technology. The Flash Program memory can be reprogrammed In-System through an SPI serial interface, by a conventional non-volatile memory programmer, or by an On-chip boot program running on the AVR core. The boot program can use any interface to download the application program in the Application Flash memory. Software in the Boot Flash Section will continue to run while the Application Flash Section is updated, providing true Read-While-Write operation. By combining an 8-bit RISC CPU with In-System Self-Programmable Flash on a monolithic chip, the Atmel ATmega8 is a powerful microcontroller that provides a highly-flexible and cost-effective solution to many embedded control applications.

The ATmega8 is supported with a full suite of program and system development tools, including C compilers, macro assemblers, program simulators, and evaluation kits.

Disclaimer

Typical values contained in this datasheet are based on simulations and characterization of other AVR microcontrollers manufactured on the same process technology. Minimum and Maximum values will be available after the device is characterized.

Pin Descriptions

VCC   Digital supply voltage.

GND   Ground.

Port B (PB7..PB0)   Port B is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The
XTAL1/XTAL2/TOSC1/   Port B output buffers have symmetrical drive characteristics with both high sink and source
TOSC2   capability. As inputs, Port B pins that are externally pulled low will source current if the pull-up
                             resistors are activated. The Port B pins are tri-stated when a reset condition becomes active,
                             even if the clock is not running.

                             Depending on the clock selection fuse settings, PB6 can be used as input to the inverting Oscil-
                             lator amplifier and input to the internal clock operating circuit.

                             Depending on the clock selection fuse settings, PB7 can be used as output from the inverting
                             Oscillator amplifier.

                             If the Internal Calibrated RC Oscillator is used as chip clock source, PB7..6 is used as TOSC2..1
                             input for the Asynchronous Timer/Counter2 if the AS2 bit in ASSR is set.

                             The various special features of Port B are elaborated in "Alternate Functions of Port B" on page
                             58 and "System Clock and Clock Options" on page 25.

Port C (PC5..PC0)   Port C is an 7-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The
                             Port C output buffers have symmetrical drive characteristics with both high sink and source
                             capability. As inputs, Port C pins that are externally pulled low will source current if the pull-up
                             resistors are activated. The Port C pins are tri-stated when a reset condition becomes active,
                             even if the clock is not running.

PC6/$\overline{\text{RESET}}$ If the RSTDISBL Fuse is programmed, PC6 is used as an I/O pin. Note that the electrical char-
                             acteristics of PC6 differ from those of the other pins of Port C.

                             If the RSTDISBL Fuse is unprogrammed, PC6 is used as a Reset input. A low level on this pin
                             for longer than the minimum pulse length will generate a Reset, even if the clock is not running.
                             The minimum pulse length is given in Table 15 on page 38. Shorter pulses are not guaranteed to
                             generate a Reset.

                             The various special features of Port C are elaborated on page 61.

Port D (PD7..PD0)   Port D is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The
                             Port D output buffers have symmetrical drive characteristics with both high sink and source
                             capability. As inputs, Port D pins that are externally pulled low will source current if the pull-up
                             resistors are activated. The Port D pins are tri-stated when a reset condition becomes active,
                             even if the clock is not running.

                             Port D also serves the functions of various special features of the ATmega8 as listed on page
                             63.

$\overline{\text{RESET}}$ Reset input. A low level on this pin for longer than the minimum pulse length will generate a
                             reset, even if the clock is not running. The minimum pulse length is given in Table 15 on page
                             38. Shorter pulses are not guaranteed to generate a reset.

Ordering Information

| Speed (MHz)	Power Supply (V)	Ordering Code[2]	Package[1]	Operation Range
8	2.7 - 5.5	ATmega8L-8AU ATmega8L-8AUR[3] ATmega8L-8PU ATmega8L-8MU ATmega8L-8MUR[3]	32A 32A 28P3 32M1-A 32M1-A	Industrial (-40°C to 85°C)
16	4.5 - 5.5	ATmega8-16AU ATmega8-16AUR[3] ATmega8-16PU ATmega8-16MU ATmega8-16MUR[3]	32A 32A 28P3 32M1-A 32M1-A	
8	2.7 - 5.5	ATmega8L-8AN ATmega8L-8ANR[3] ATmega8L-8PN ATmega8L-8MN ATmega8L-8MUR[3]	32A 32A 28P3 32M1-A 32M1-A	Industrial (-40°C to 105°C)
16	4.5 - 5.5	ATmega8-16AN ATmega8-16ANR[3] ATmega8-16PN ATmega8-16MN ATmega8-16MUR[3]	32A 32A 28P3 32M1-A 32M1-A	

Notes: 1. This device can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information and minimum quantities
2. Pb-free packaging complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green
3. Tape & Reel
4. See characterization specification at 105°C

Package Type	
32A	32-lead, Thin (1.0mm) Plastic Quad Flat Package (TQFP)
28P3	28-lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
32M1-A	32-pad, 5 × 5 × 1.0 body, Lead Pitch 0.50mm Quad Flat No-Lead/Micro Lead Frame Package (QFN/MLF)

Packaging Information

32A

PIN 1 IDENTIFIER

PIN 1

PIN 1

e

B

E1

E

D1

D

C

0°~7°

A1

A2

A

L
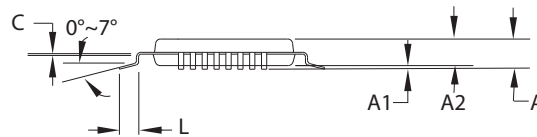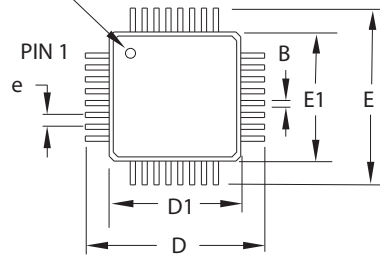
COMMON DIMENSIONS
(Unit of measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	1.20	
A1	0.05	–	0.15	
A2	0.95	1.00	1.05	
D	8.75	9.00	9.25	
D1	6.90	7.00	7.10	Note 2
E	8.75	9.00	9.25	
E1	6.90	7.00	7.10	Note 2
B	0.30	–	0.45	
C	0.09	–	0.20	
L	0.45	–	0.75	
e		0.80 TYP		

Notes:
1. This package conforms to JEDEC reference MS-026, Variation ABA.
2. Dimensions D1 and E1 do not include mold protrusion.   Allowable
   protrusion is 0.25mm per side. Dimensions D1 and E1 are maximum
   plastic body size dimensions including mold mismatch.
3. Lead coplanarity is 0.10mm maximum.

2010-10-20

	TITLE	DRAWING NO.	REV.
Atmel®	32A, 32-lead, 7 x 7mm body size, 1.0mm body thickness, 0.8mm lead pitch, thin profile plastic quad flat package (TQFP)	32A	C

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28P3
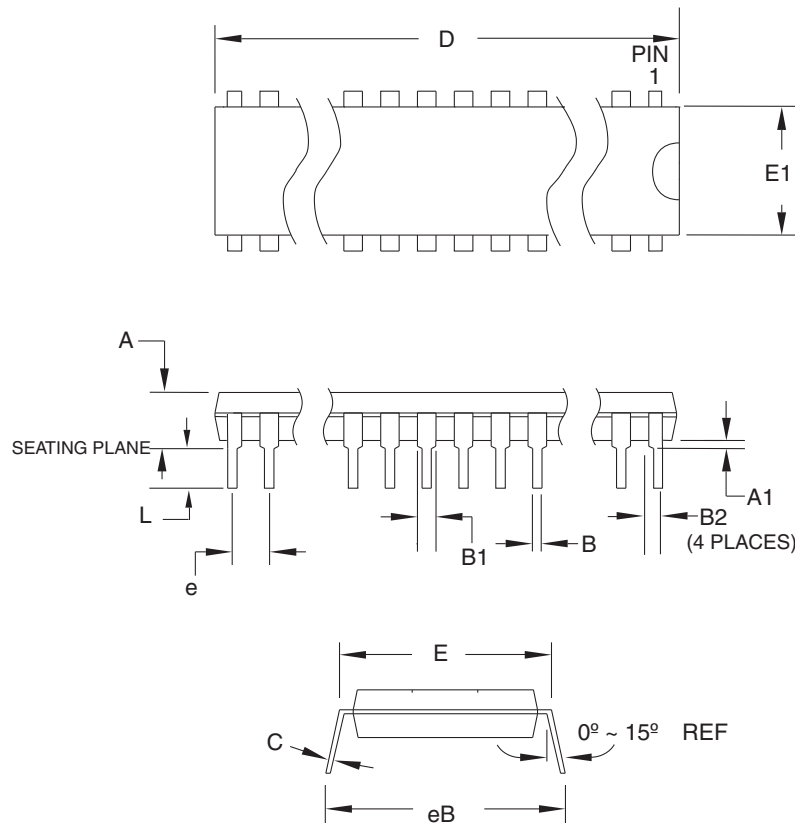
Note: 1. Dimensions D and E1 do not include mold Flash or Protrusion.
Mold Flash or Protrusion shall not exceed 0.25mm (0.010").

COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	4.5724	
A1	0.508	–	–	
D	34.544	–	34.798	Note 1
E	7.620	–	8.255	
E1	7.112	–	7.493	Note 1
B	0.381	–	0.533	
B1	1.143	–	1.397	
B2	0.762	–	1.143	
L	3.175	–	3.429	
C	0.203	–	0.356	
eB	–	–	10.160	
e	2.540 TYP			

09/28/01

	TITLE	DRAWING NO.	REV.
Atmel 2325 Orchard Parkway San Jose, CA 95131	**28P3**, 28-lead (0.300"/7.62mm Wide) Plastic Dual Inline Package (PDIP)	28P3	B

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32M1-A

TOP VIEW

SIDE VIEW

BOTTOM VIEW

Pin 1 ID

Pin #1 Notch
(0.20 R)

△ 0.08 C

Note: JEDEC Standard MO-220, Fig. 2 (Anvil Singulation), VHHD-2.
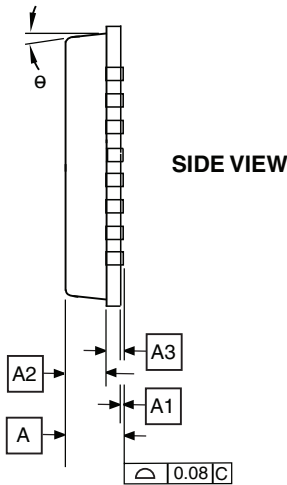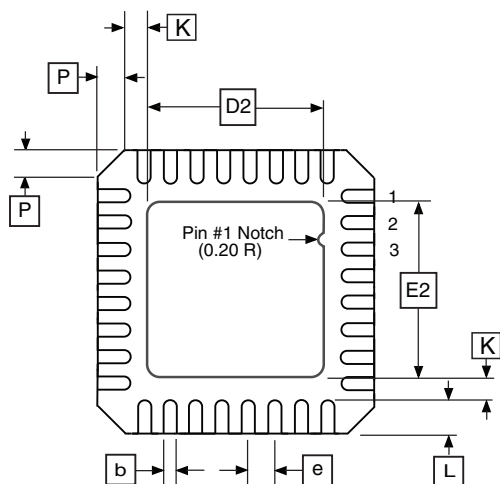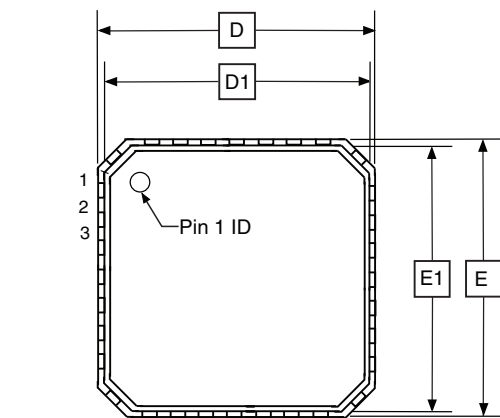
COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	0.80	0.90	1.00	
A1	–	0.02	0.05	
A2	–	0.65	1.00	
A3		0.20 REF		
b	0.18	0.23	0.30	
D	4.90	5.00	5.10	
D1	4.70	4.75	4.80	
D2	2.95	3.10	3.25	
E	4.90	5.00	5.10	
E1	4.70	4.75	4.80	
E2	2.95	3.10	3.25	
e		0.50 BSC		
L	0.30	0.40	0.50	
P	–	–	0.60	
θ	–	–	12°	
K	0.20	–	–	

5/25/06

		TITLE	DRAWING NO.	REV.
ATMEL	2325 Orchard Parkway San Jose, CA 95131	**32M1-A**, 32-pad, 5 x 5 x 1.0mm Body, Lead Pitch 0.50mm, 3.10mm Exposed Pad, Micro Lead Frame Package (MLF)	32M1-A	E

Errata

The revision letter in this section refers to the revision of the ATmega8 device.

**ATmega8
Rev. D to I, M**

- First Analog Comparator conversion may be delayed
- Interrupts may be lost when writing the timer registers in the asynchronous timer
- Signature may be Erased in Serial Programming Mode
- CKOPT Does not Enable Internal Capacitors on XTALn/TOSCn Pins when 32KHz Oscillator is Used to Clock the Asynchronous Timer/Counter2
- Reading EEPROM by using ST or STS to set EERE bit triggers unexpected interrupt request

1. **First Analog Comparator conversion may be delayed**

   If the device is powered by a slow rising V_{CC}, the first Analog Comparator conversion will take longer than expected on some devices.

   Problem Fix / Workaround

   When the device has been powered or reset, disable then enable theAnalog Comparator before the first conversion.

2. **Interrupts may be lost when writing the timer registers in the asynchronous timer**

   The interrupt will be lost if a timer register that is synchronized to the asynchronous timer clock is written when the asynchronous Timer/Counter register(TCNTx) is 0x00.

   Problem Fix / Workaround

   Always check that the asynchronous Timer/Counter register neither have the value 0xFF nor 0x00 before writing to the asynchronous Timer Control Register(TCCRx), asynchronous Timer Counter Register(TCNTx), or asynchronous Output Compare Register(OCRx).

3. **Signature may be Erased in Serial Programming Mode**

   If the signature bytes are read before a chiperase command is completed, the signature may be erased causing the device ID and calibration bytes to disappear. This is critical, especially, if the part is running on internal RC oscillator.

   Problem Fix / Workaround:

   Ensure that the chiperase command has exceeded before applying the next command.

4. **CKOPT Does not Enable Internal Capacitors on XTALn/TOSCn Pins when 32KHz Oscillator is Used to Clock the Asynchronous Timer/Counter2**

   When the internal RC Oscillator is used as the main clock source, it is possible to run the Timer/Counter2 asynchronously by connecting a 32KHz Oscillator between XTAL1/TOSC1 and XTAL2/TOSC2. But when the internal RC Oscillator is selected as the main clock source, the CKOPT Fuse does not control the internal capacitors on XTAL1/TOSC1 and XTAL2/TOSC2. As long as there are no capacitors connected to XTAL1/TOSC1 and XTAL2/TOSC2, safe operation of the Oscillator is not guaranteed.

   Problem Fix / Workaround

   Use external capacitors in the range of 20pF - 36pF on XTAL1/TOSC1 and XTAL2/TOSC2. This will be fixed in ATmega8 Rev. G where the CKOPT Fuse will control internal capacitors also when internal RC Oscillator is selected as main clock source. For ATmega8 Rev. G, CKOPT = 0 (programmed) will enable the internal capacitors on XTAL1 and XTAL2. Customers who want compatibility between Rev. G and older revisions, must ensure that CKOPT is unprogrammed (CKOPT = 1).

5. **Reading EEPROM by using ST or STS to set EERE bit triggers unexpected interrupt request.**

    Reading EEPROM by using the ST or STS command to set the EERE bit in the EECR register triggers an unexpected EEPROM interrupt request.

    Problem Fix / Workaround

    Always use OUT or SBI to set EERE in EECR.

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