Table 1. KEY PARAMETERS

Parameter		Typical Value
Optical Format		1/3-inch (5.8 mm) Note: Sensor optical format will also work with lenses designed for 1/3.2" format.
Active Pixels		2048 (H) x 1536 (V) (4:3, mode)
Pixel Size		2.2 µm x 2.2 µm
Color Filter Array		RGB Bayer
Shutter Type		Electronic rolling shutter and GRR
Input Clock Range		6 – 48 MHz
Output Clock Maximum		148.5 Mp/s (4-lane HiSPi) 74.25 Mp/s (Parallel)
Output	Serial	HiSPi 10-, 12-, 14-, or 16-bit
	Parallel	10-, 12-bit
Frame Rate	Full Resolution	30 fps
	1080p	60 fps
Responsivity		1.9 V/lux-sec
SNR_{MAX}		39 dB
Max Dynamic Range		Up to 100 dB
Supply Voltage	I/O	1.8 or 2.8 V
	Digital	1.8 V
	Analog	2.8 V
	HiSPi	0.3 V–0.6 V, 1.7 V–1.9 V
Power Consumption (Typical)		<780 mW
Operating Temperature (Ambient)		–30°C to +85° C
Package Options		10 x 10 mm 48 pin iLCC 9.5 x 9.5 mm 63-pin iBGA

ORDERING INFORMATION

Table 2. AVAILABLE PART NUMBERS

Part Number	Product Description	Orderable Product Attribute Description
AR0331SRSC00SHCA0-DRBR	48-pin iLCC HiSPi, 0° CRA	Dry Pack without Protective Film, Double Side BBAR Glass
AR0331SRSC00SHCAD3-GEVK	48-pin iLCC HiSPi, 0° CRA	Demo Kit 3
AR0331SRSC00SHCAD-GEVK	48-pin iLCC HiSPi, 0° CRA	Demo Kit
AR0331SRSC00SHCAH-GEVB	48-pin iLCC HiSPi, 0° CRA	Demo Board
AR0331SRSC00SUCA0-DPBR	48-pin iLCC Parallel, 0° CRA	Dry Pack with Protective Film, Double Side BBAR Glass
AR0331SRSC00SUCA0-DRBR	48-pin iLCC Parallel, 0° CRA	Dry Pack without Protective Film, Double Side BBAR Glass
AR0331SRSC00SUCAD3-GEVK	48-pin iLCC Parallel, 0° CRA	Demo Kit 3
AR0331SRSC00SUCAD-GEVK	48-pin iLCC Parallel, 0° CRA	Demo Kit
AR0331SRSC00SUCAH-GEVB	48-pin iLCC Parallel, 0° CRA	Demo Board
AR0331SRSC00XUEAD3-GEVK	63-pin iBGA	Demo Kit 3
AR0331SRSC00XUEAD-GEVK	63-pin iBGA	Demo Kit
AR0331SRSC00XUEAH-GEVB	63-pin iBGA	Demo Board
AR0331SRSC00XUEE0–BY–DRBR	63-pin iBGA, 0° CRA	Dry Pack without Protective Film, Double Side BBAR Glass
AR0331SRSC00XUEE0-DPBR	63-pin iBGA, 0° CRA	Dry Pack with Protective Film, Double Side BBAR Glass
AR0331SRSC00XUEE0-DRBR	63-pin iBGA, 0° CRA	Dry Pack without Protective Film, Double Side BBAR Glass
AR0331SRSC00XUEE0-DRBR1	63-pin iBGA, 0° CRA	Dry Pack without Protective Film, Double Side BBAR Glass

FUNCTIONAL OVERVIEW

The AR0331 is a progressive-scan sensor that generates a stream of pixel data at a constant frame rate. It uses an on-chip, phase-locked loop (PLL) that can be optionally enabled to generate all internal clocks from a single master input clock running between 6 and 48 MHz. The maximum output pixel rate is 148.5 Mp/s, corresponding to a clock rate of 74.25 MHz. Figure 1 shows a block diagram of the sensor.

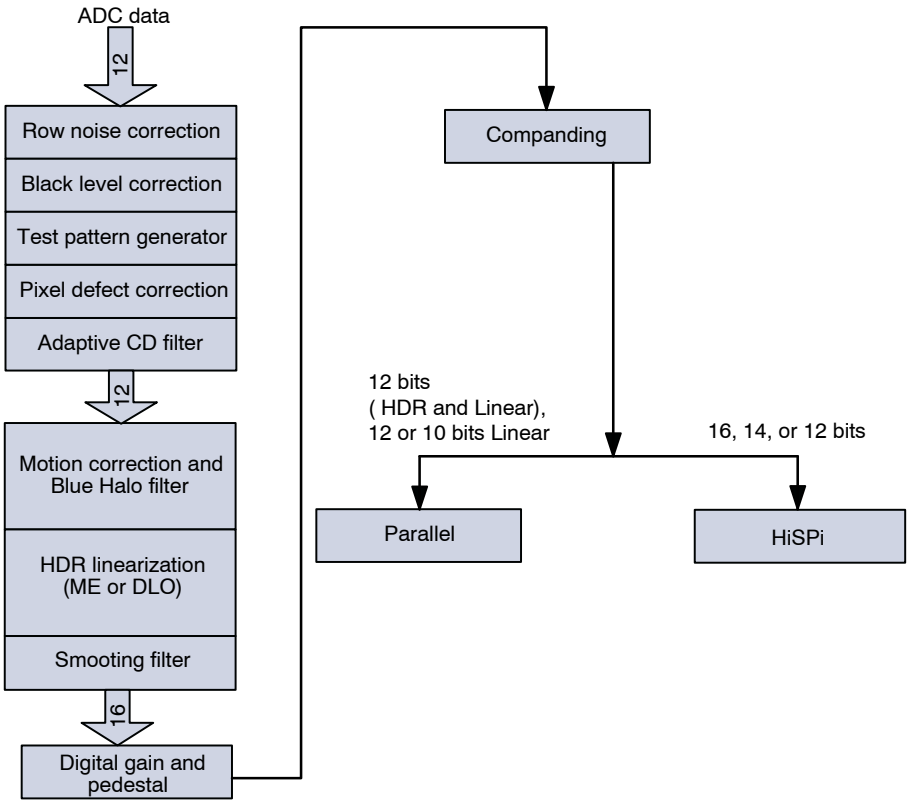
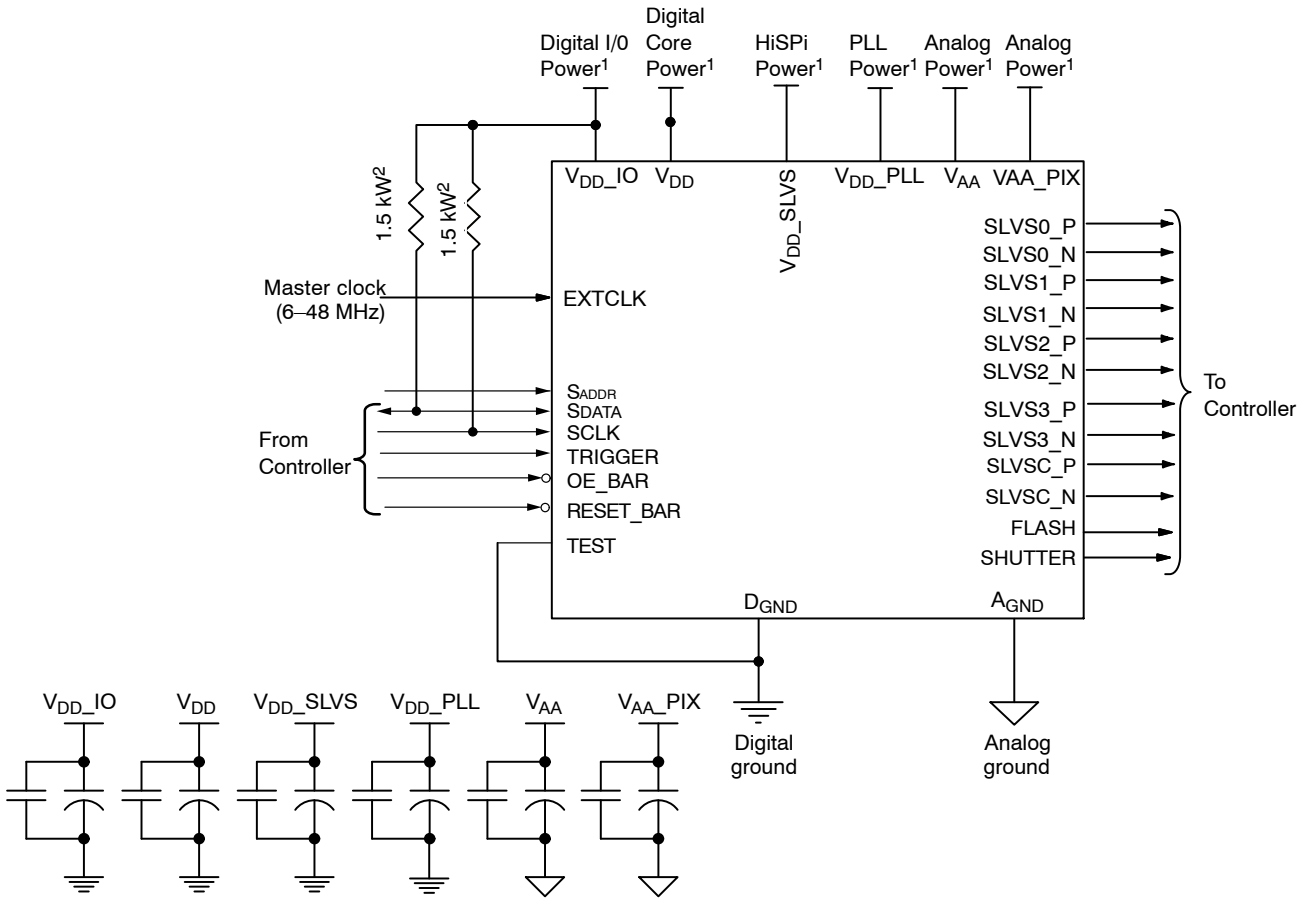


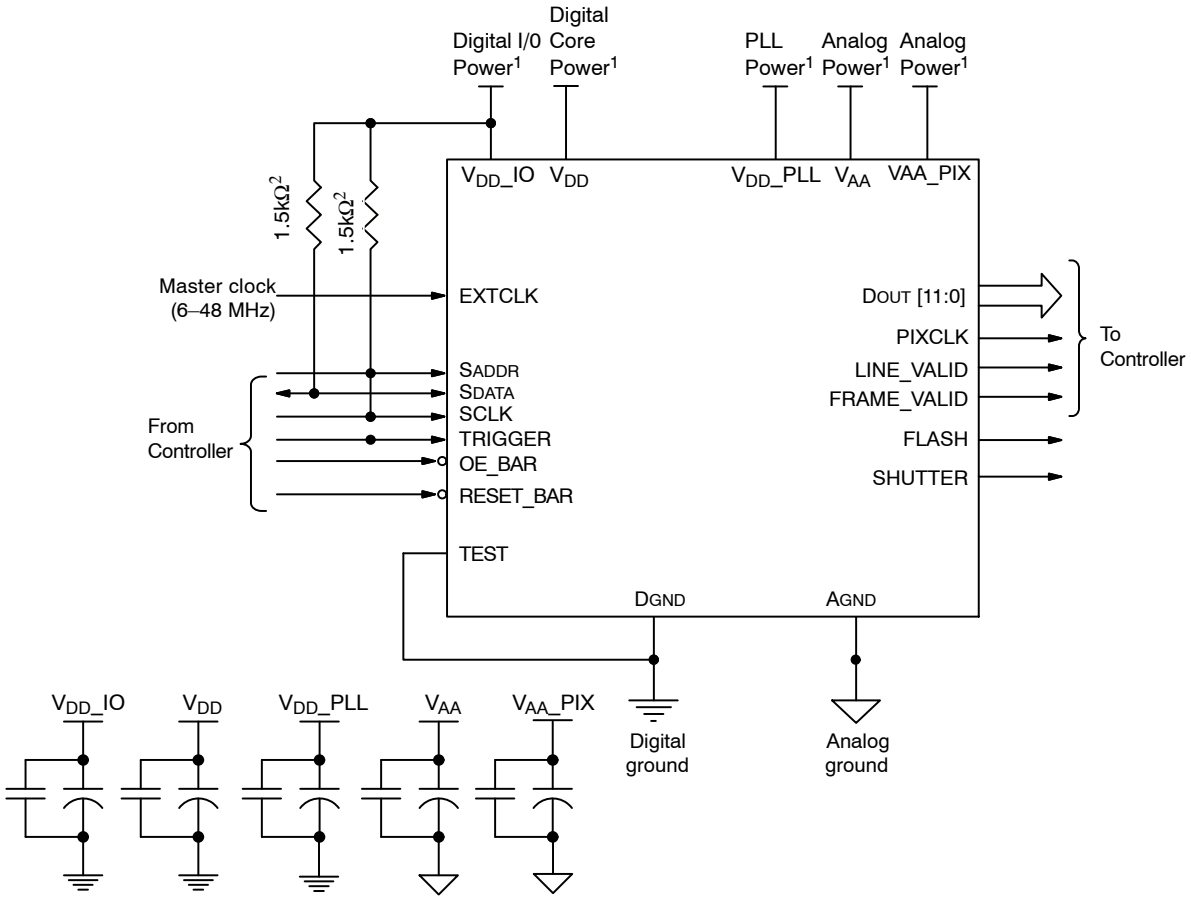
Figure 1. Block Diagram

User interaction with the sensor is through the two-wire serial bus, which communicates with the array control, analog signal chain, and digital signal chain. The core of the sensor is a 3.1 Mp Active-pixel Sensor array. The timing and control circuitry sequences through the rows of the array, resetting and then reading each row in turn. In the time interval between resetting a row and reading that row, the pixels in the row integrate incident light. The exposure is controlled by varying the time interval between reset and readout. Once a row has been read, the data from the columns is sequenced through an analog signal chain (providing offset correction and gain), and then through an analog-to-digital converter (ADC). The output from the ADC is a 12-bit value for each pixel in the array. The ADC output passes through a digital processing signal chain (which provides further data path corrections and applies digital gain). The sensor also offers a high dynamic range mode of operation where multiple images are combined on-chip to produce a single image at 16-bit per pixel value. A compression mode is further offered to allow the 16-bit pixel value to be transmitted to the host system as a 12-bit value with close to zero loss in image quality.



Notes:
1. All power supplies should be adequately decoupled.
2. ON Semiconductor recommends a resistor value of 1.5 kΩ, but a greater value may be used for slower two-wire speed.
3. The parallel interface output pads can be left unconnected if the serial output interface is used.
4. ON Semiconductor recommends that 0.1 μF and 10 μF decoupling capacitors for each power supply are mounted as close as possible to the pad. Actual values and results may vary depending on layout and design considerations. Refer to the AR0331 demo headboard schematics for circuit recommendations.
5. ON Semiconductor recommends that analog power planes are placed in a manner such that coupling with the digital power planes is minimized.
6. I/O signals voltage must be configured to match VDD_IO voltage to minimize any leakage currents.

Figure 2. Typical Configuration: Serial Four-Lane HiSPi Interface



Notes:
1. All power supplies should be adequately decoupled.
2. ON Semiconductor recommends a resistor value of 1.5 kΩ, but a greater value may be used for slower two-wire speed.
3. The serial interface output pads and VDDSLVS can be left unconnected if the parallel output interface is used.
4. ON Semiconductor recommends that 0.1 μF and 10 μF decoupling capacitors for each power supply are mounted as close as possible to the pad. Actual values and results may vary depending on layout and design considerations. Refer to the AR0331 demo headboard schematics for circuit recommendations.
5. ON Semiconductor recommends that analog power planes are placed in a manner such that coupling with the digital power planes is minimized.
6. I/O signals voltage must be configured to match VDD_IO voltage to minimize any leakage currents.
7. The EXTCLK input is limited to 6–48 MHz.

Figure 3. Typical Configuration: Parallel Pixel Data Interface

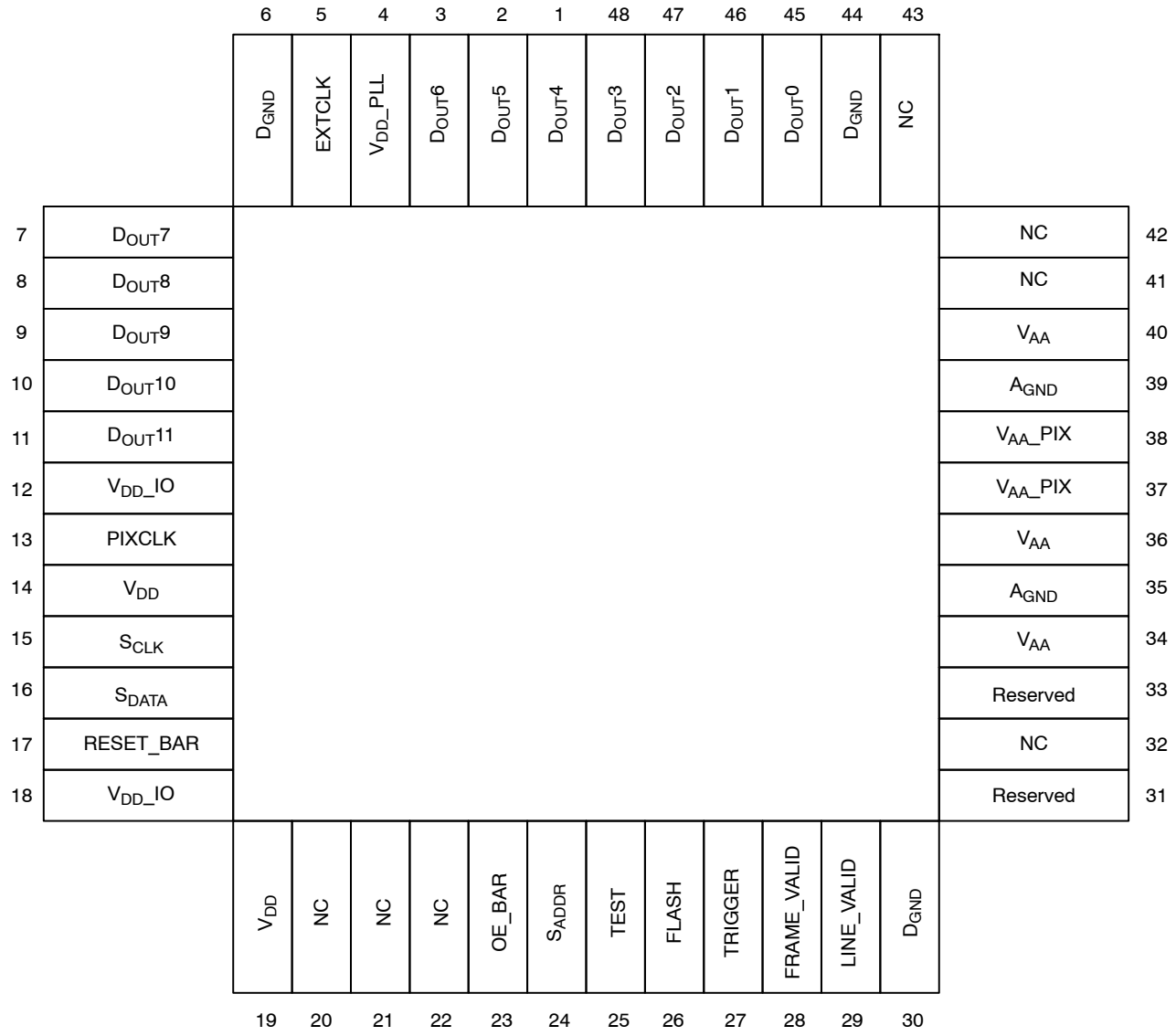


Figure 4. 48 iLCC Package, Parallel Output

Table 3. PIN DESCRIPTION

Pin Number	Name	Type	Description
1	DOUT4	Output	Parallel Pixel Data Output
2	DOUT5	Output	Parallel Pixel Data Output
3	DOUT6	Output	Parallel Pixel Data Output
4	VDD_PLL	Power	PLL Power
5	EXTCLK	Input	External Input Clock
6	DGND	Power	Digital Ground
7	DOUT7	Output	Parallel Pixel Data Output
8	DOUT8	Output	Parallel Pixel Data Output
9	DOUT9	Output	Parallel Pixel Data Output
10	DOUT10	Output	Parallel Pixel Data Output

Table 3. PIN DESCRIPTION (continued)

Pin Number	Name	Type	Description
11	DOUT11	Output	Parallel Pixel Data Output (MSB)
12	VDD_IO	Power	I/O Supply Power
13	PIXCLK	Output	Pixel Clock Out. DOUT is Valid on Rising Edge of this Clock
14	VDD	Power	Digital Power
15	SCLK	Input	Two-wire Serial Clock Input
16	SDATA	I/O	Two-wire Serial Data I/O
17	RESET_BAR	Input	Asynchronous Reset (Active LOW). All Settings are Restored to Factory Default
18	VDD_IO	Power	I/O Supply Power
19	VDD	Power	Digital Power
20	NC		
21	NC		
22	NC		
23	OE_BAR	Input	Output Enable (Active LOW)
24	SADDR	Input	Two-wire Serial Address Select. 0: 0x20. 1: 0x30
25	TEST	Input	Manufacturing Test Enable Pin (Connect to DGND)
26	FLASH	Output	Flash Output Control
27	TRIGGER	Input	Receives Slave Mode VD Signal for Frame Rate Synchronization and Trigger to Start a GRR Frame
28	FRAME_VALID	Output	Asserted when DOUT Frame Data is Valid
29	LINE_VALID	Output	Asserted when DOUT Line Data is Valid.
30	DGND	Power	Digital Ground
31	Reserved		
32	SHUTTER	Output	Control for External Mechanical Shutter. Can be Left Floating if not Used
33	Reserved		
34	VAA	Power	Analog Power
35	AGND	Power	Analog Ground
36	VAA	Power	Analog Power
37	VAA_PIX	Power	Pixel Power
38	VAA_PIX	Power	Pixel Power
39	AGND	Power	Analog Ground
40	VAA	Power	Analog Power
41	NC		
42	NC		
43	NC		
44	DGND	Power	Digital Ground
45	DOUT0	Output	Parallel Pixel Data Output (LSB)
46	DOUT1	Output	Parallel Pixel Data Output
47	DOUT2	Output	Parallel Pixel Data Output
48	DOUT3	Output	Parallel Pixel Data Output

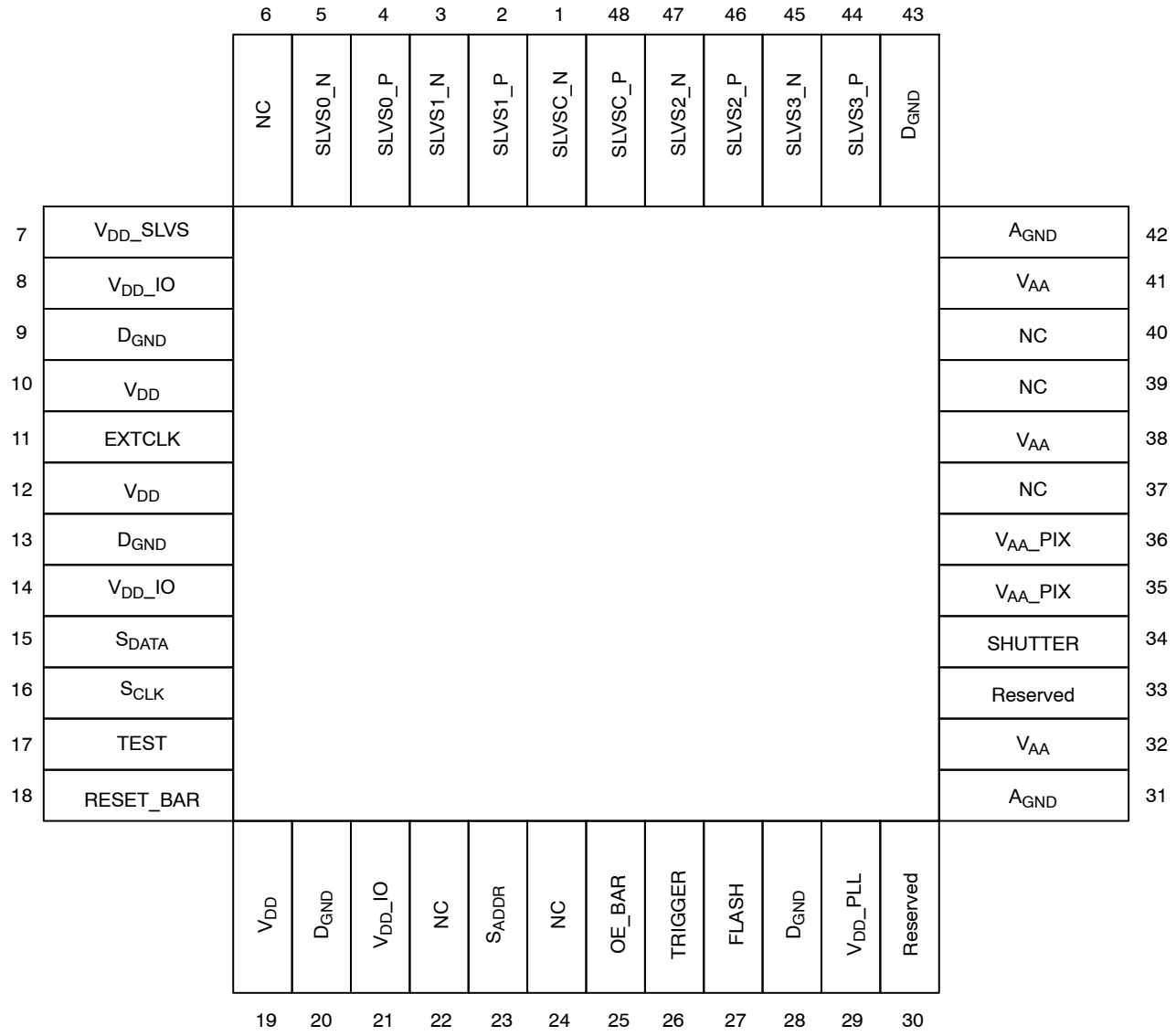


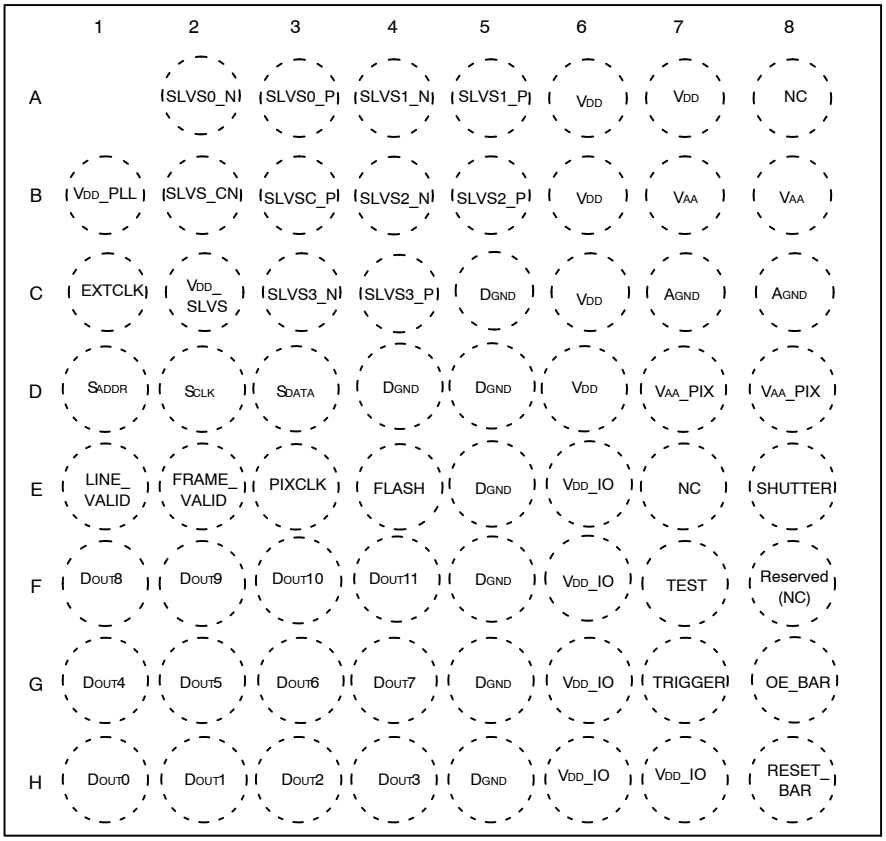
Figure 5. 48 iLCC Package, HiSPi Output

Table 4. PIN DESCRIPTION, 48 ILCC

Pin Number	Name	Type	Description
1	SLVSC_N	Output	HiSPi Serial DDR Clock Differential N
2	SLVS1_P	Output	HiSPi Serial Data, Lane 1, Differential P
3	SLVS1_N	Output	HiSPi Serial Data, Lane 1, Differential N
4	SLVS0_P	Output	HiSPi Serial Data, Lane 0, Differential P
5	SLVS0_N	Output	HiSPi Serial Data, Lane 0, Differential N
6	NC		
7	VDD_SLVS	Power	0.3 V−0.6 V or 1.7 V−1.9 V Port to HiSPi Output Driver. Set the High_VCM (R0x306E[9]) Bit to 1 when Configuring VDD_SLVS to 1.7−1.9 V
8	VDD_IO	Power	I/O Supply Power
9	DGND	Power	Digital Ground
10	VDD	Power	Digital Power

Table 4. PIN DESCRIPTION, 48 ILCC (continued)

Pin Number	Name	Type	Description
11	EXTCLK	Input	External Input Clock
12	VDD	Power	Digital Power
13	DGND		Digital Ground
14	VDD_IO	Power	I/O Supply Power
15	SDATA	I/O	Two-wire Serial Data I/O
16	SCLK	Input	Two-wire Serial Clock Input
17	TEST		Manufacturing Test Enable Pin (Connect to DGND)
18	RESET_BAR	Input	Asynchronous Reset (Active LOW). All Settings are Restored to Factory Default
19	VDD	Power	Digital Power
20	DGND	Power	Digital Ground
21	VDD_IO	Power	I/O Supply Power
22	NC		
23	SADDR	Input	Two-wire Serial Address Select. 0: 0x20. 1: 0x30
24	NC		
25	OE_BAR		Output Enable (active LOW)
26	TRIGGER	Input	Receives Slave Mode VD Signal for Frame Rate Synchronization and Trigger to Start a GRR Frame
27	FLASH	Output	Flash Output Control
28	DGND	Power	
29	VDD_PLL	Power	PLL Power
30	Reserved		
31	AGND	Power	Analog Ground
32	VAA	Power	Analog Power
33	Reserved		
34	SHUTTER	Output	Control for External Mechanical Shutter. Can be Left Floating if not Used
35	VAA_PIX	Power	Pixel Power
36	VAA_PIX	Power	Pixel Power
37	NC		
38	VAA	Power	Analog Power
39	NC		
40	NC		
41	VAA	Power	Analog Power
42	AGND	Power	Analog Ground
43	DGND	Power	Digital Ground
44	SLVS3_P	Output	HiSPi Serial Data, Lane 3, Differential P
45	SLVS3_N	Output	HiSPi Serial Data, Lane 3, Differential N
46	SLVS2_P	Output	HiSPi Serial Data, Lane 2, Differential P
47	SLVS2_N	Output	HiSPi Serial Data, Lane 2, Differential N
48	SLVSC_P	Output	HiSPi Serial DDR Clock Differential P



Top View
(Ball Down)

Figure 6. 9.5 x 9.5 mm 63−Ball IBGA Package

Table 5. PIN DESCRIPTIONS, 9.5 x 9.5 mm, 63-BALL IBGA

Name	iBGA Pin	Type	Description
SLVS0_N	A2	Output	HiSPi Serial Data, Lane 0, Differential N
SLVS0_P	A3	Output	HiSPi Serial Data, Lane 0, Differential P
SLVS1_N	A4	Output	HiSPi Serial Data, Lane 1, Differential N
SLVS1_P	A5	Output	HiSPi Serial Data, Lane 1, Differential P
VDD_PLL	B1	Power	PLL power.
SLVSC_N	B2	Output	HiSPi Serial DDR Clock Differential N
SLVSC_P	B3	Output	HiSPi Serial DDR Clock Differential P
SLVS2_N	B4	Output	HiSPi Serial Data, Lane 2, Differential N
SLVS2_P	B5	Output	HiSPi Serial Data, Lane 2, Differential P
VAA	B7, B8	Power	Analog Power
EXTCLK	C1	Input	External Input Clock.
VDD_SLVS	C2	Power	0.3 V−0.6 V or 1.7 V−1.9 V port to HiSPi Output Driver. Set the High_VCM (R0x306E[9]) bit to 1 when configuring VDD_SLVS to 1.7−1.9 V
SLVS3_N	C3	Output	HiSPi Serial Data, Lane 3, Differential N
SLVS3_P	C4	Output	HiSPi Serial Data, Lane 3, Differential P
DGND	C5, D4, D5, E5, F5, G5, H5	Power	Digital Ground

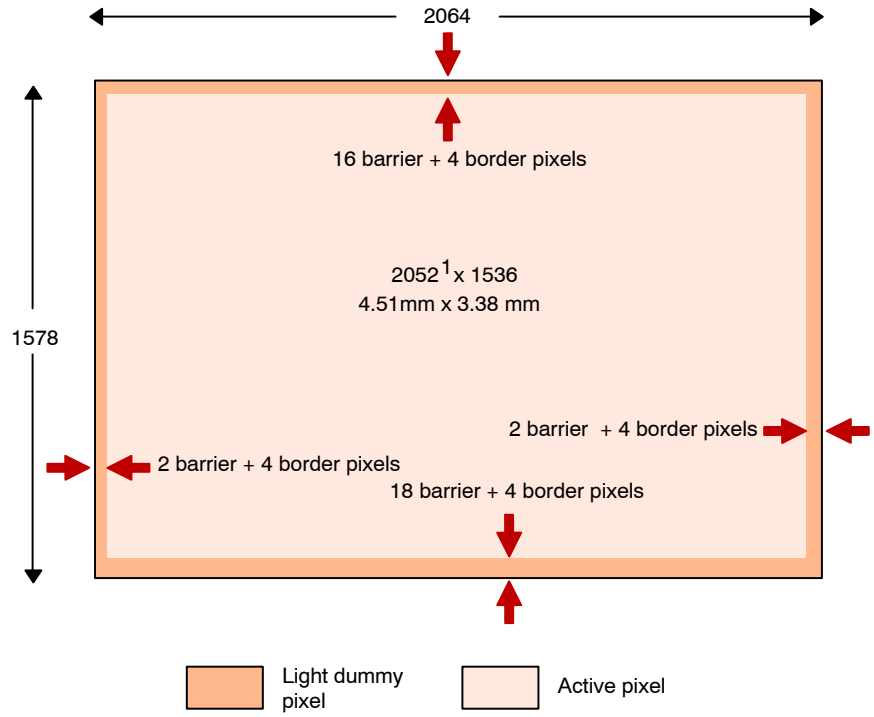
Table 5. PIN DESCRIPTIONS, 9.5 x 9.5 mm, 63-BALL IBGA (continued)

Name	iBGA Pin	Type	Description
VDD	A6, A7, B6, C6, D6	Power	Digital Power
AGND	C7, C8	Power	Analog Ground
SADDR	D1	Input	Two-wire Serial Address Select. 0: 0x20. 1: 0x30
SCLK	D2	Input	Two-wire Serial Clock Input
SDATA	D3	I/O	Two-Wire Serial Data I/O
VAA_PIX	D7, D8	Power	Pixel Power
LINE_VALID	E1	Output	Asserted when DOUT Line Data is Valid
FRAME_VALID	E2	Output	Asserted when DOUT Frame Data is Valid.
PIXCLK	E3	Output	Pixel Clock Out. DOUT is Valid on Rising Edge of this Clock.
VDD_IO	E6, F6, G6, H6, H7	Power	I/O Supply Power
DOUT8	F1	Output	Parallel Pixel Data Output
DOUT9	F2	Output	Parallel Pixel Data Output
DOUT10	F3	Output	Parallel Pixel Data Output
DOUT11	F4	Output	Parallel Pixel Data Output (MSB)
TEST	F7	Input.	Manufacturing Test Enable Pin (Connect to DGND)
DOUT4	G1	Output	Parallel Pixel Data Output
DOUT5	G2	Output	Parallel Pixel Data Output
DOUT6	G3	Output	Parallel Pixel Data Output
DOUT7	G4	Output	Parallel Pixel Data Output
TRIGGER	G7	Input	Exposure Synchronization Input
OE_BAR	G8	Input	Output Enable (Active LOW)
DOUT0	H1	Output	Parallel Pixel Data Output (LSB)
DOUT1	H2	Output	Parallel Pixel Data Output
DOUT2	H3	Output	Parallel Pixel Data Output
DOUT3	H4	Output	Parallel Pixel Data Output
RESET_BAR	H8	Input	Asynchronous reset (active LOW). All settings are restored to factory default
SHUTTER	E8	Output	Control for external mechanical shutter. Can be left floating if not used
FLASH	E4	Output	Flash Control Output
NC	A8, E7		
Reserved	F8		

PIXEL DATA FORMAT

Pixel Array Structure

While the sensor's format is 2048 x 1536, additional active columns and active rows are included for use when horizontal or vertical mirrored readout is enabled, to allow readout to start on the same pixel. The pixel adjustment is always performed for monochrome or color versions. The active area is surrounded with optically transparent dummy pixels to improve image uniformity within the active area. Not all dummy pixels or barrier pixels can be read out.



1. Maximum of 2048 columns is supported. Additional columns included for mirroring operations.

Figure 7. Pixel Array Description

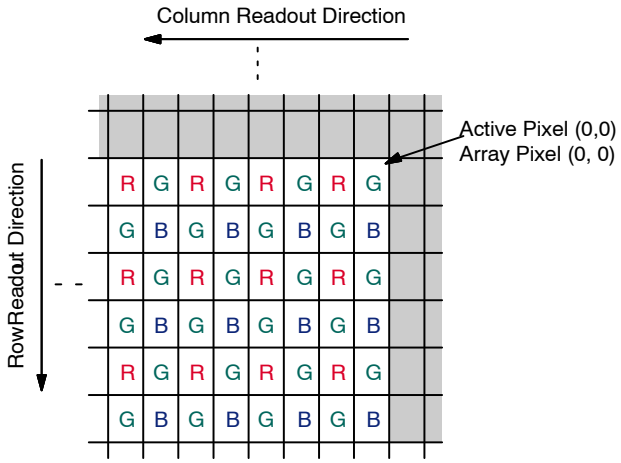


Figure 8. Pixel Color Pattern Detail (Top Right Corner)

Default Readout Order

By convention, the sensor core pixel array is shown with pixel (0,0) in the top right corner (see Figure 8). This reflects the actual layout of the array on the die. Also, the first pixel data read out of the sensor in default condition is that of pixel (0, 0).

When the sensor is imaging, the active surface of the sensor faces the scene as shown in Figure 9. When the image is read out of the sensor, it is read one row at a time, with the rows and columns sequenced as shown in Figure 9.

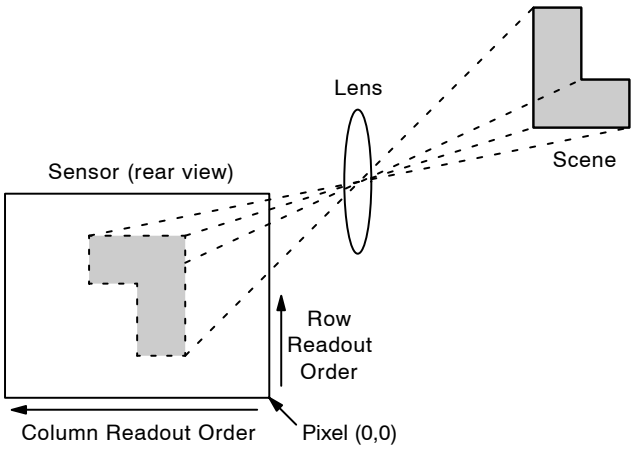


Figure 9. Imaging a Scene

PIXEL OUTPUT INTERFACES

Parallel Interface

The parallel pixel data interface uses these output-only signals:

- FRAME_VALID
- LINE_VALID
- PIXCLK
- DOUT[11:0]

The parallel pixel data interface is disabled by default at power up and after reset. It can be enabled by programming R0x301A. Table 7 shows the recommended settings.

When the parallel pixel data interface is in use, the serial data output signals can be left unconnected. Set reset_register [bit 12 (R0x301A[12] = 1)] to disable the serializer while in parallel output mode.

Output Enable Control

When the parallel pixel data interface is enabled, its signals can be switched asynchronously between the driven and High-Z under pin or register control, as shown in Table 6.

Table 6. OUTPUT ENABLE CONTROL

OE_BAR Pin	Drive Pins R0x301A[6]	Description
1	0	Interface High-Z
X	1	Interface Driven
0	X	Interface Driven

Configuration of the Pixel Data Interface

Fields in R0x301A are used to configure the operation of the pixel data interface. The supported combinations are shown in Table 7.

Table 7. CONFIGURATION OF THE PIXEL DATA INTERFACE

Serializer Disable R0x301 A[12]	Parallel Enable R0x301 A[7]	Description
0	0	Power up default Serial pixel data interface and its clocks are enabled. Transitions to soft standby are synchronized to the end of frames on the serial pixel data interface
1	1	Parallel pixel data interface, sensor core data output. Serial pixel data interface and its clocks disabled to save power. Transitions to soft standby are synchronized to the end of frames in the parallel pixel data interface

High Speed Serial Pixel Data Interface

The High Speed Serial Pixel (HiSPi) interface uses four data lanes and one clock as output.

- SLVSC_P
- SLVSC_N
- SLVS0_P
- SLVS0_N
- SLVS1_P
- SLVS1_N
- SLVS2_P
- SLVS2_N
- SLVS3_P
- SLVS3_N

The HiSPi interface supports three protocols, Streaming-S, Streaming-SP, and Packetized SP. The streaming protocols conform to a standard video application where each line of active or intra-frame blanking provided by the sensor is transmitted at the same length. The Packetized SP protocol will transmit only the active data ignoring line-to-line and frame-to-frame blanking data.

These protocols are further described in the High-Speed Serial Pixel (HiSPi) Interface Protocol Specification V1.50.00.

The HiSPi interface building block is a unidirectional differential serial interface with four data and one double data rate (DDR) clock lanes. One clock for every four serial data lanes is provided for phase alignment across multiple lanes. Figure 10 shows the configuration between the HiSPi transmitter and the receiver.

The HiSPi interface building block is a unidirectional differential serial interface with four data and one double data rate (DDR) clock lanes. One clock for every four serial data lanes is provided for phase alignment across multiple lanes. Figure 10 shows the configuration between the HiSPi transmitter and the receiver.

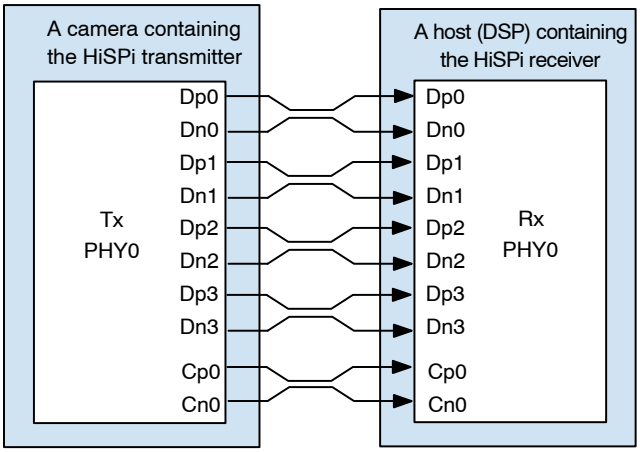


Figure 10. HiSPi Transmitter and Receiver Interface Block Diagram

HiSPi Physical Layer

The HiSPi physical layer is partitioned into blocks of four data lanes and an associated clock lane. Any reference to the PHY in the remainder of this document is referring to this minimum building block.

The PHY will serialize 10-, 12-, 14-, or 16-bit data words and transmit each bit of data centered on a rising edge of the clock, the second on the falling edge of the clock. Figure 11 shows bit transmission. In this example, the word is transmitted in order of MSB to LSB. The receiver latches data at the rising and falling edge of the clock.

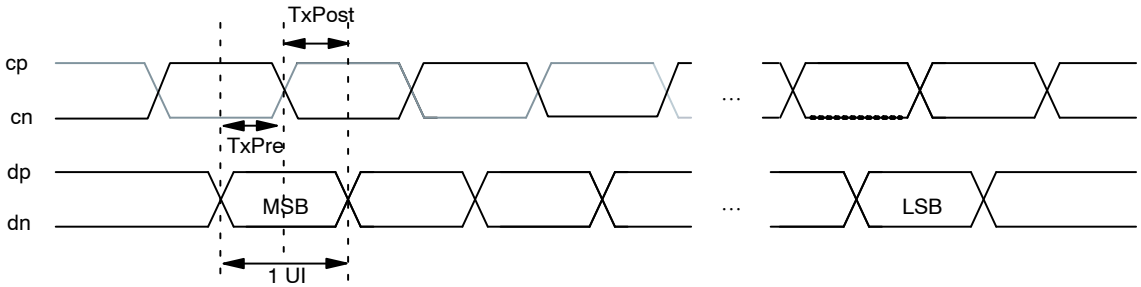


Figure 11. Timing Diagram

DLL Timing Adjustment

The specification includes a DLL to compensate for differences in group delay for each data lane. The DLL is connected to the clock lane and each data lane, which acts as a control master for the output delay buffers. Once the DLL has gained phase lock, each lane can be delayed in 1/8 unit interval (UI) steps. This additional delay allows the user to increase the setup or hold time at the receiver circuits and can be used to compensate for skew introduced in PCB design.

Delay compensation may be set for clock and/or data lines in the hispi_timing register R0x31C0. If the DLL timing adjustment is not required, the data and clock lane delay settings should be set to a default code of 0x000 to reduce jitter, skew, and power dissipation.

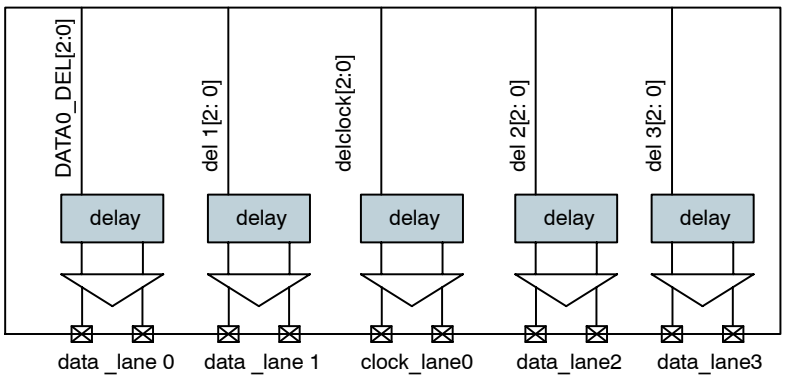


Figure 12. Block Diagram of DLL Timing Adjustment

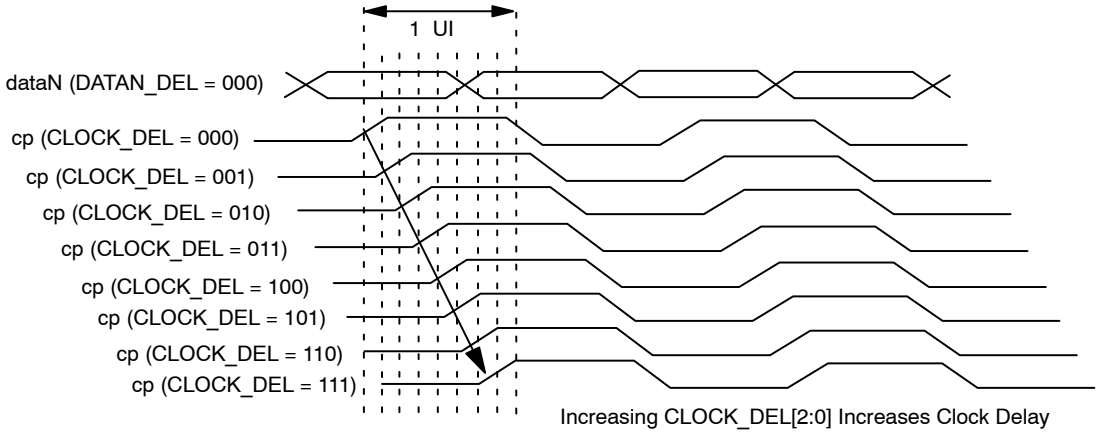


Figure 13. Delaying the Clock with Respect to Data

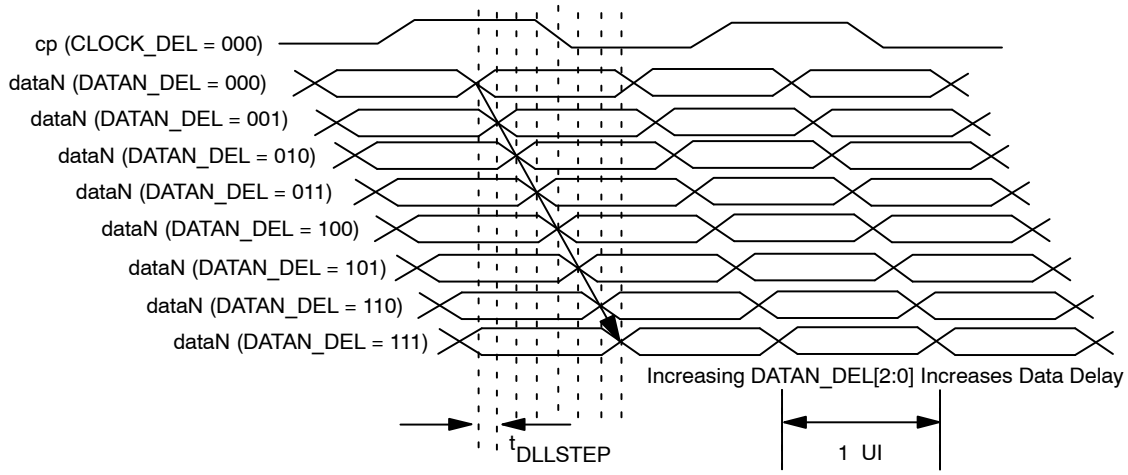


Figure 14. Delaying Data with Respect to the Clock

HiSPi Protocol Layer

The HiSPi protocol is described the HiSPi Protocol Specification document.

Serial Configuration

The serial format should be configured using R0x31AC. Refer to the AR0331 Register Reference document for more detail regarding this register.

The serial_format register (R0x31AE) controls which serial format is in use when the serial interface is enabled (reset_register[12] = 0). The following serial formats are supported:

- 0x0304 – Sensor supports quad-lane HiSPi operation
- 0x0302 – Sensor supports dual-lane HiSPi operation
- 0x0301 – Sensor supports single-lane HiSPi operation

PIXEL SENSITIVITY

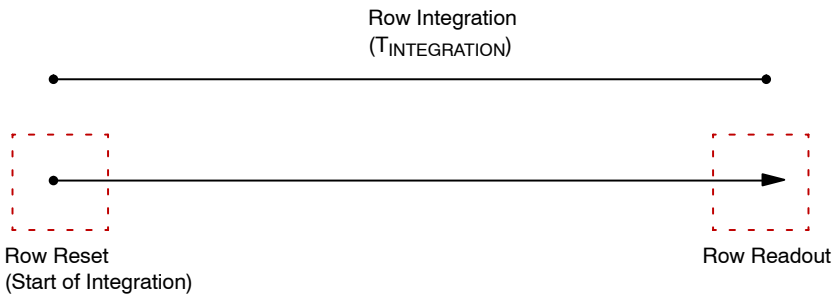


Figure 15. Integration Control in ERS Readout

A pixel's integration time is defined by the number of clock periods between a row's reset and read operation. Both the read followed by the reset operations occur within a row period (T_{ROW}) where the read and reset may be applied to different rows. The read and reset operations will be applied to the rows of the pixel array in a consecutive order.

The coarse integration time is defined by the number of row periods (T_{ROW}) between a row's reset and the row read. The row period is defined as the time between row read operations (see Sensor Frame Rate).

$$T_{COARSE} = T_{ROW} \times coarse\_integration\_time \quad \text{(eq. 1)}$$

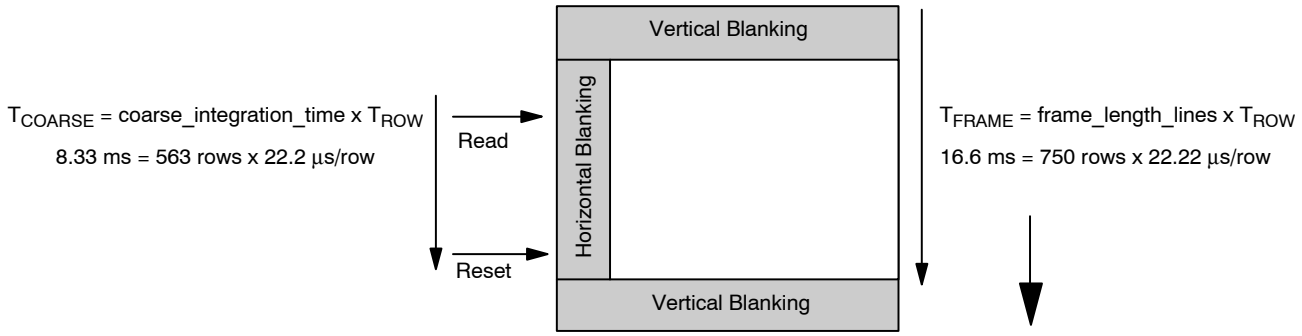


Figure 16. Example of 8.33 ms Integration in 16.6 ms Frame

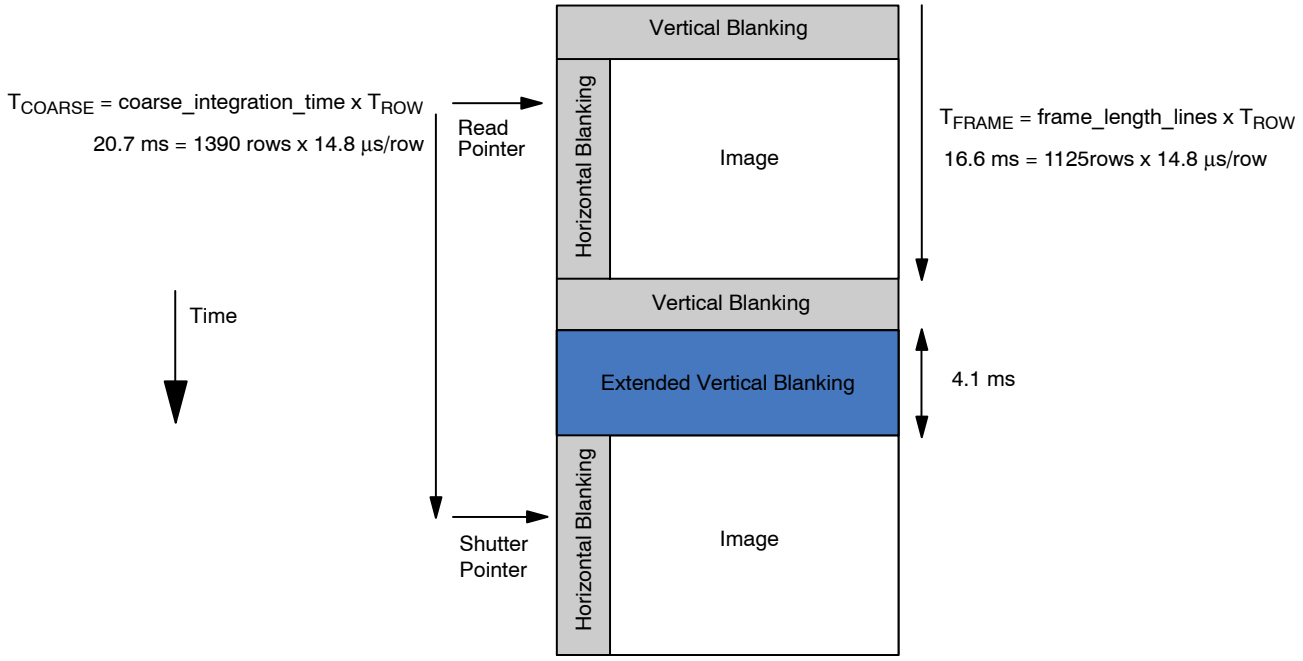


Figure 17. The Row Integration Time is Greater Than the Frame Readout Time

The minimum frame-time is defined by the number of row periods per frame and the row period. The sensor frame-time will increase if the coarse_integration_time is set to a value equal to or greater than the frame_length_lines.

GAIN STAGES

The analog gain stages of the AR0331 sensor are shown in Figure 18. The sensor analog gain stage consists of a variable ADC reference. The sensor will apply the same analog gain to each color channel. Digital gain can be configured to separate levels for each color channel.

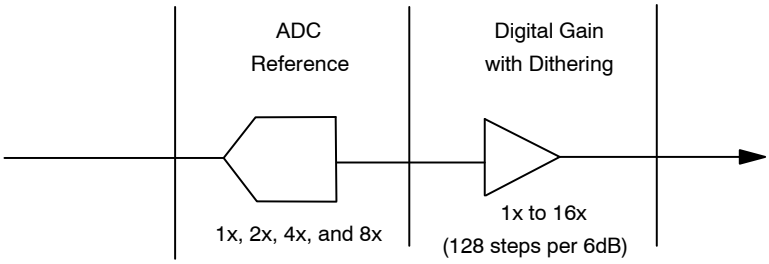


Figure 18. Gain Stages in AR0331 Sensor

The level of analog gain applied is controlled by the coarse_gain register. The recommended analog gain settings are listed in Table 8. A minimum analog gain of 1.23x is recommended. Changes to these registers should be done prior to streaming images.

Table 8. RECOMMENDED SENSOR GAIN

coarse_gain(0x3060[5:4])/ coarse_gain_cb (0x3060[13:12])	fine_gain (0x3060[3:0])/ fine_gain_cb (0x3060[11:8])	ADC Gain
0	6	1.23
0	7	1.28
0	8	1.34
0	9	1.39
0	10	1.45
0	11	1.52
0	12	1.60
0	13	1.69
0	14	1.78
0	15	1.88
1	0	2.00
1	2	2.14
1	4	2.28
1	6	2.47
1	8	2.67
1	10	2.91
1	12	3.20
1	14	3.56
2	0	4
2	4	4.56
2	8	5.34
2	12	6.41
3	0	8

Each digital gain can be configured from a gain of 0 to 15.992. The digital gain supports 128 gain steps per 6dB of gain. The format of each digital gain register is “xxxx.yyyyyyy” where “xxxx” refers an integer gain of 1 to 15 and “yyyyyyy” is a fractional gain ranging from 0/128 to 127/128.

The sensor includes a digital dithering feature to reduce quantization noise resulting from using digital gain. It can be disabled by setting R0x30BA[5] to 0. The default value is 1.

PEDESTALS

There are two types of constant offset pedestals that may be adjusted at the end of the datapath.

The data pedestal is a constant offset that is added to pixel values at the end of the datapath. The default offset when ALTM is disabled is 168 and is a 12-bit offset. This offset matches the maximum range used by the corrections in the digital readout path. The purpose of the data pedestal is to convert negative values generated by the digital datapath into positive output data. It is recommended that the data pedestal be set to 16 when ALTM is enabled.

The data pedestal value can be changed from its default value by adjusting register R0x301E.

The ALTM pedestal (R0x2450) is also located at the end of the datapath. The ALTM pedestal default offset is 0.

HIGH DYNAMIC RANGE MODE

By default, the sensor powers up in HDR Mode. The HDR scheme used is multi-exposure HDR. This allows the sensor to handle up to 100 dB of dynamic range. In HDR mode, the sensor sequentially captures two exposures by maintaining two separate read and reset pointers that are interleaved within the rolling shutter readout. The intermediate pixel values are stored in line buffers while waiting for the two exposure values to be present. As soon as a pixel's two exposure values are available, they are combined to create a linearized 16-bit value for each pixel's response. Depending on whether HiSPi or Parallel mode is selected, the full 16 bit value may be output, it can be compressed to 12 bits using Adaptive Local Tone Mapping (ALTM), or companded to 12 or 14 bits.

Adaptive Local Tone Mapping

Real- world scenes often have a very high dynamic range (HDR) that far exceeds the electrical dynamic range of the imager. Dynamic range is defined as the luminance ratio between the brightest and the darkest objects in a scene. Even though the AR0331 can capture full dynamic range images, the images are still limited by the low dynamic range of display devices. Today's typical LCD monitor has a contrast ratio around 1000:1 while it is not atypical for an HDR image having a contrast ratio of around 250000:1. Therefore, in order to reproduce HDR images on a low dynamic range display device, the captured high dynamic range must be compressed to the available range of the display device. This is commonly called tone mapping. The AR0331 has implemented an adaptive local tone mapping (ALTM) feature to reproduce visually appealing images that increase the local contrast and the visibility of the images. When ALTM is enabled, the gamma in the backend ISP should be set to 1 for proper display.

See the AR0331 Developer Guide for more information on ALTM.

Companding

The 16-bit linearized HDR image may be compressed to 12 bits using on-chip companding. Figure 19 illustrates the compression from 16- to 12-bits. Companding is enabled by setting R0x31D0. Table 10 shows the knee points for the different modes.

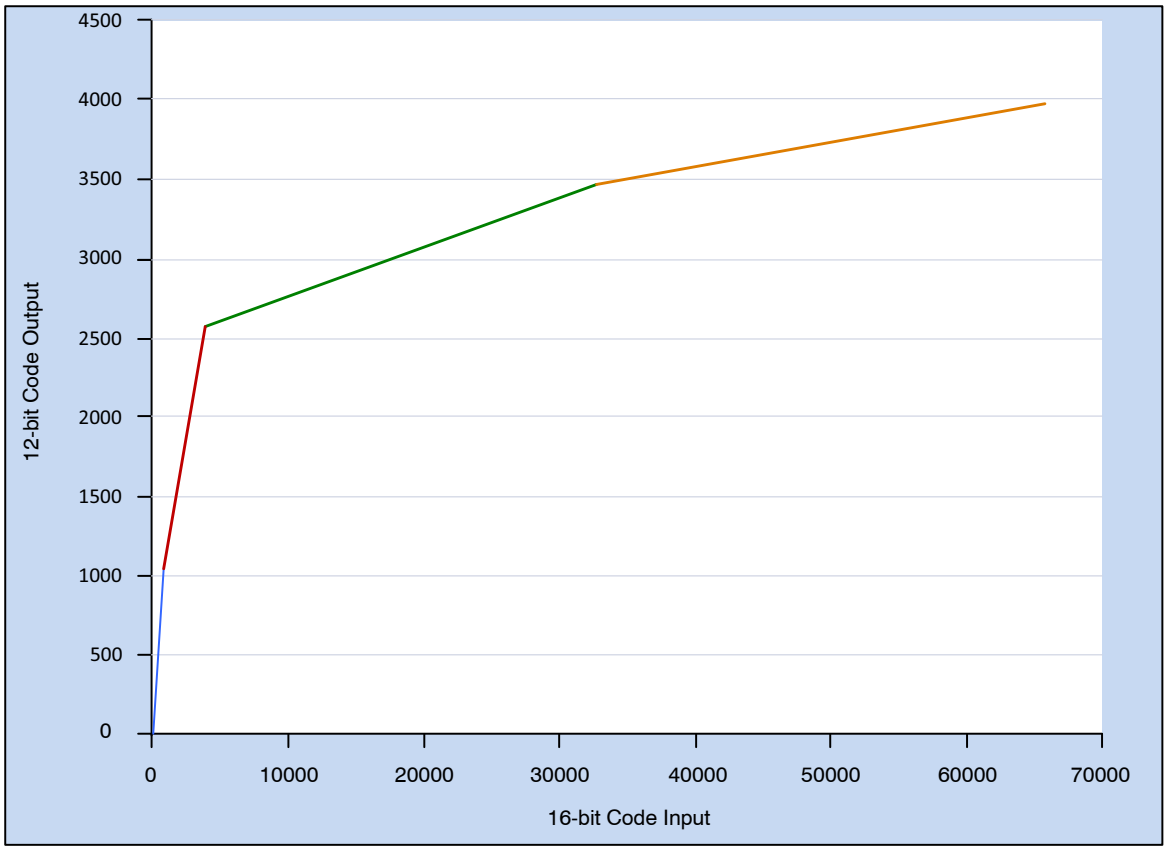


Figure 19. HDR Data Compression

Table 9. COMPANDING TABLE

	Segment 1	Segment 2	Segment 3	Segment 4
Input Code Range	0 to 1023	1024 to 4095	4096 to 32767	32768 to 65535
Output Code Range	0 to 1023	1024 to 2559	2560 to 3455	3456 to 3967
Companding Formula	$P_{out} = P_{in}$	$P_{out} = (P_{in} - 1024)/2 + 1024$	$P_{out} = (P_{in} - 4096)/32 + 2560$	$P_{out} = (P_{in} - 32768)/64 + 3456$
Decompanding Formula	$P_{out} = P_{in}$	$P_{out} = (P_{in} - 1024)*2 + 1024$	$P_{out} = (P_{in} - 2560)*32 + 4096$	$P_{out} = (P_{in} - 3456)*64 + 32768$

Table 9 illustrates the input and output codes as well as companding and decompanding formulas for each of the four colored segments in Figure 19.

Table 10. KNEE POINTS FOR COMPRESSION FROM 16 BITS TO 12 BITS

T1/T2 Exposure Ratio (R1) R0x3082[3:2]	P1	POUT1 = P1	P2	POUT2= (P2 – P1)/2 + 1024	P3	POUT3= (P3 – P2)/32 + 2560	PMAX	POUTMAX = (PMAX – P3)/64 + 3456
4x, 8x, 16x, 32x	2^{10}	1024	2^{12}	2560	2^{15}	3456	2^{16}	3968

As described in Table 10, the AR0331 companding block operates on 16-bit input only. For the exposure ratios that do not result in 16-bits, bit shifting occurs before the data enters the companding block. As a result of the bit shift, data needs to be unshifted after linearization in order to obtain the proper image. Table 11 provides the bit operation that should occur to the data after linearization.

Table 11. BIT OPERATION AFTER LINEARIZATION

ratio_t1_t2 (R0x3082[3:2])/ratio_t1_t2_cb (R0x3084[3:2])	Bit Shift Operation after Linearization
4x	Right Shift 2 Bits
8x	Right Shift 1 Bit
16x	No Shift
32x	Left Shift 1 Bit

HDR-Specific Exposure Settings

In HDR mode, pixel values are stored in line buffers while waiting for both exposures to be available for final pixel data combination. There are 70 line buffers used to store intermediate T1 data. Due to this limitation, the maximum coarse integration time possible for a given exposure ratio is equal to 70*T1/T2 lines.

For example, if R0x3082[3:2] = 2, the sensor is set to have T1/T2 ratio = 16x. Therefore the maximum number of integration lines is 70*16 = 1120 lines. If coarse integration time is greater than this, the T2 integration time will stay at 70. The sensor will calculate the ratio internally, enabling the linearization to be performed. If companding is being used, then relinearization would still follow the programmed ratio. For example if the T1/T2 ratio was programmed to 16x but coarse integration was increased beyond 1120 then one would still use the 16x relinearization formulas.

An additional limitation is the maximum number of exposure lines in relation to the frame_length_lines register. In linear mode, maximum coarse_integration_time = frame_length_lines – 1. However in HDR mode, since the coarse integration time register controls T1, the max coarse integration time is frame_length_lines – 71.

Putting the two criteria listed above together, the formula is as follows:

$$\text{maximum coarse\_integration\_time} = \text{minimum}\left(70 \times \frac{T1}{T2}, \text{frame\_length\_lines} - 71\right) \quad \text{(eq. 2)}$$

There is a limitation of the minimum number of exposure lines, which is one row time for linear mode. In HDR mode, the minimum number of rows required is half of the ratio T1/T2.

Motion Compensation

In typical multi-exposure HDR systems, motion artifacts can be created when objects move during the T1 or T2 integration time. When this happens, edge artifacts can potentially be visible and might look like a ghosting effect.

To correct this, the AR0331 has special 2D motion compensation circuitry that detects motion artifacts and corrects the image.

The motion compensation feature can be enabled by setting R0x318C[14] = 1. Additional parameters are available to control the extent of motion detection and correction as per the requirements of the specific application. For more information, refer to the AR0331 Register Reference document and the AR0331 Developer Guide.

RESET

The AR0331 may be reset by the RESET_BAR pin (active LOW) or the reset register.

Hard Reset of Logic

The RESET_BAR pin can be connected to an external RC circuit for simplicity. The recommended RC circuit uses a 10 kΩ resistor and a 0.1 μF capacitor. The rise time for the RC circuit is 1 μs maximum.

Soft Reset of Logic

Soft reset of logic is controlled by the R0x301A Reset register. Bit 0 is used to reset the digital logic of the sensor. Furthermore, by asserting the soft reset, the sensor aborts the current frame it is processing and starts a new frame. This bit is a self-resetting bit and also returns to “0” during two-wire serial interface reads.

SENSOR PLL

VCO

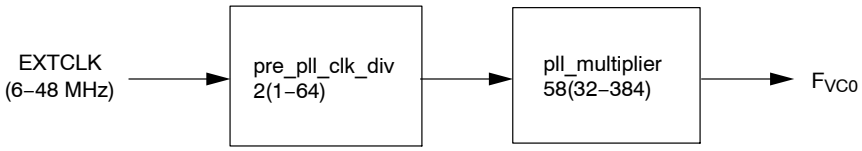


Figure 20. PLL Dividers Affecting VCO Frequency

The sensor contains a phase-locked loop (PLL) that is used for timing generation and control. The required VCO clock frequency is attained through the use of a pre-PLL clock divider followed by a multiplier. The PLL multiplier should be an even integer. If an odd integer (M) is programmed, the PLL will default to the lower (M−1) value to maintain an even multiplier value. The multiplier is followed by a set of dividers used to generate the output clocks required for the sensor array, the pixel analog and digital readout paths, and the output parallel and serial interfaces. Use of the PLL is required when using the HiSPi interface.

Dual Readout Paths

There are two readout paths within the sensor digital block. The sensor PLL should be configured such that the total pixel rate across both readout paths is equal to the output pixel rate. For example, if CLK_PIX is 74.25 MHz in a 4-lane HiSPi configuration, the CLK_OP should be equal to 37.125 MHz.

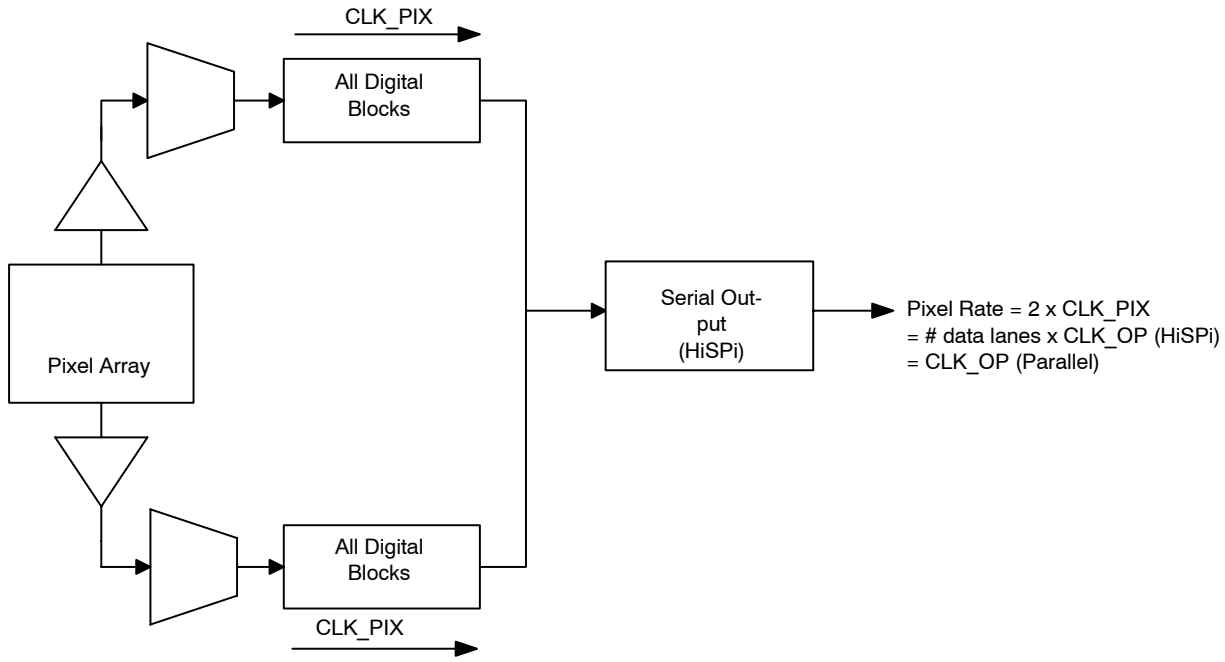


Figure 21. Sensor Dual Readout Paths

The sensor row timing calculation refers to each data-path individually. For example, the sensor default configuration uses 1100 clocks per row (line_length_pck) to output 1928 active pixels per row. The aggregate clocks per row seen by the receiver will be 2200 clocks (1100 x 2 readout paths).

Parallel PLL Configuration

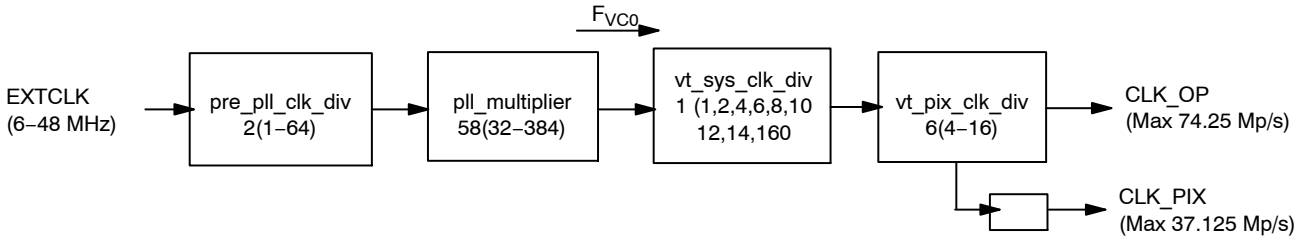


Figure 22. PLL for the Parallel Interface

The maximum output of the parallel interface is 74.25 MPixel/s. This will limit the readout clock (CLK_PIX) to 37.125 MPixel/s. The sensor will not use the F_{SERIAL}, F_{SERIAL_CLK}, or CLK_OP when configured to use the parallel interface.

Table 12. PLL PARAMETERS FOR THE PARALLEL INTERFACE

Parameter	Symbol	Min	Max	Unit
External Clock	EXTCLK	6	48	MHz
VCO Clock	F_{VCO}	384	768	MHz
Readout Clock	CLK_PIX		37.125	Mpixel/s
Output Clock	CLK_OP		74.25	Mpixel/s

Table 13. EXAMPLE PLL CONFIGURATION FOR THE PARALLEL INTERFACE

Parameter	Value	Output
F_{VCO}		445.5 MHz (Max)
vt_sys_clk_div	1	
vt_pix_clk_div	6	
CLK_PIX		37.125 MPixel/s (= 445.5 MHz / 12)
CLK_OP		74.25 MPixel/s (= 445.5 MHz / 6)
Output pixel rate		74.25 MPixel/s

Serial PLL Configuration

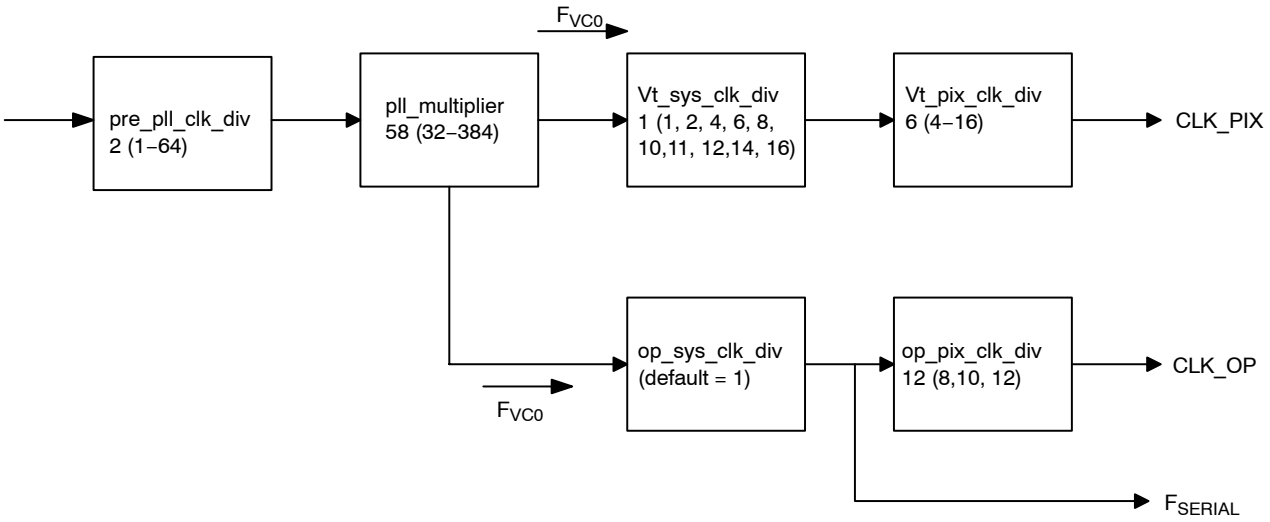


Figure 23. PLL for the Serial Interface

The PLL must be enabled when HiSPi mode is selected. The sensor will use op_sys_clk_div and op_pix_clk_div to configure the output clock per lane (CLK_OP). The configuration will depend on the number of active lanes (1, 2, or 4) configured. To configure the sensor protocol and number of lanes, refer to “Serial Configuration”.

Table 14. PLL PARAMETERS FOR THE SERIAL INTERFACE

Parameter	Symbol	Min	Max	Unit
External Clock	EXTCLK	6	48	MHz
External Clock	EXTCLK	6	48	MHz
VCO Clock	F_{VCO}	384	768	MHz
Readout Clock	CLK_PIX		74.25	Mpixel/s
Output Clock	CLK_OP		37.125	Mpixel/s
Output Serial Data Rate Per Lane	F_{SERIAL}	300 (HiSPi)	700 (HiSPi)	Mbps
Output Serial Clock Speed Per Lane	F_{SERIAL_CLK}	150 (HiSPi)	350 (HiSPi)	MHz

Configure the serial output so that it adheres to the following rules:

- The maximum data-rate per lane (F_{SERIAL}) is 700 Mbps/lane (HiSPi).
- Configure the output pixel rate per lane (CLK_OP) so that the sensor output pixel rate matches the peak pixel rate (2 x CLK_PIX).
  - 4-lane: 4 x CLK_OP = 2 x CLK_PIX = Pixel Rate (max: 148.5 Mpixel/s)
  - 2-lane: 2 x CLK_OP = 2 x CLK_PIX = Pixel Rate (max: 74.25 Mpixel/s)
  - 1-lane: 1 x CLK_OP = 2 x CLK_PIX = Pixel Rate (max: 37.125 Mpixel/s)

Table 15. EXAMPLE PLL CONFIGURATIONS FOR THE SERIAL INTERFACE

Parameter	4-lane				2-lane		1-lane	Units
	16-bit	14-bit	12-bit	10-bit	12-bit	10-bit	10-bit	
F_{VCO}	594	519.75	445.5	742.5	445.5	742.5	742.5	MHz
vt_sys_clk_div	1	1	1	2	1	2	4	
vt_pix_clk_div	8	7	6	5	12	10	10	
op_sys_clk_div	1	1	1	2	1	2	2	
op_pix_clk_div	16	14	12	10	12	10	10	
F_{SERIAL}	594	519.75	445.5	371.25	445.5	371.25	371.25	MHz
F_{SERIAL_CLK}	297	259.875	222.75	185.63	222.75	185.63	185.63	MHz
CLK_PIX	74.25	74.25	74.25	74.25	37.125	37.125	18.563	Mpixel/s
CLK_OP	37.125	37.125	37.125	37.125	37.125	37.125	37.125	Mpixel/s
Pixel Rate	148.5	148.5	148.5	148.5	74.25	74.25	37.125	Mpixel/s

Stream/Standby Control

The sensor supports a soft standby mode. In this mode, the external clock can be optionally disabled to further minimize power consumption. If this is done, then the "Power-Up Sequence" must be followed. When the external clock is disabled, the sensor will be unresponsive to register writes and other operations.

Soft Standby is a low-power state that is controlled through register R0x301A[2]. The sensor will go to Standby after completion of the current frame readout. When the sensor comes back from Soft Standby, previously written register settings are still maintained. Soft Standby will not occur if the Trigger pin is held high.

A specific sequence needs to be followed to enter and exit from Soft Standby.

Entering Soft Standby:

1. Set R0x301A[12] = 1 if serial mode was used
2. Set R0x301A[2] = 0 and drive Trigger pin low.
3. Turn off external clock to further minimize power consumption

Exiting Soft Standby:

1. Enable external clock if it was turned off
2. Set R0x301A[2] = 1 or drive Trigger pin high.
3. Set R0x301A[12] = 0 if serial mode is used

SENSOR READOUT

Image Acquisition Modes

The AR0331 supports two image acquisition modes:

- Electronic rolling shutter (ERS) mode:
  This is the normal mode of operation. When the AR0331 is streaming, it generates frames at a fixed rate, and each frame is integrated (exposed) using the ERS. When the ERS is in use, timing and control logic within the sensor sequences through the rows of the array, resetting and then reading each row in turn. In the time interval between resetting a row and subsequently reading that row, the pixels in the row integrate incident light. The integration (exposure) time is controlled by varying the time between row reset and row readout. For each row in a frame, the time between row reset and row readout is the same, leading to a uniform integration time across the frame. When the integration time is changed (by using the two-wire serial interface to change register settings), the timing and control logic controls the transition from old to new integration time in such a way that the stream of output frames from the AR0331 switches cleanly from the old integration time to the new while only generating frames with uniform integration. See “Changes to Integration Time” in the AR0331 Register Reference.
- Global reset mode:
  This mode can be used to acquire a single image at the current resolution. In this mode, the end point of the pixel integration time is controlled by an external electromechanical shutter, and the AR0331 provides control signals to interface to that shutter.

The benefit of using an external electromechanical shutter is that it eliminates the visual artifacts associated with ERS operation. Visual artifacts arise in ERS operation, particularly at low frame rates, because an ERS image effectively integrates each row of the pixel array at a different point in time.

Window Control

The sequencing of the pixel array is controlled by the x_addr_start, y_addr_start, x_addr_end, and y_addr_end registers.

Readout Modes

Horizontal Mirror

When the horiz_mirror bit (R0x3040[14]) is set in the read_mode register, the order of pixel readout within a row is reversed, so that readout starts from x_addr_end + 1 and ends at x_addr_start. Figure 24 shows a sequence of 6 pixels being read out with R0x3040[14] = 0 and R0x3040[14] = 1.

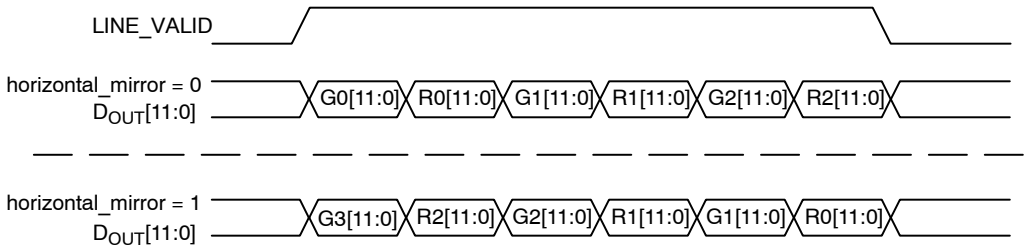


Figure 24. Effect of Horizontal Mirror on Readout Order

Vertical Flip

When the vert_flip bit (R0x3040[15]) is set in the read_mode register, the order in which pixel rows are read out is reversed, so that row readout starts from y_addr_end and ends at y_addr_start. Figure 30 shows a sequence of 6 rows being read out with R0x3040[15] = 0 and R0x3040[15] = 1.

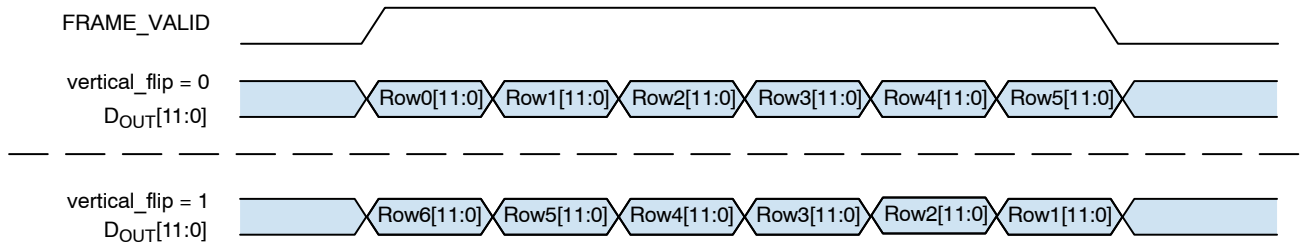


Figure 25. Effect of Vertical Flip on Readout Order

SUBSAMPLING

The AR0331 supports subsampling. Subsampling allows the sensor to read out a smaller set of active pixels by either skipping, binning, or summing pixels within the readout window. The following examples are configured to use either 2 x 2 or 3 x 3 subsampling.

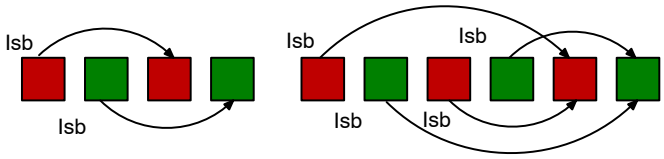


Figure 26. Horizontal Binning in the AR0331 Sensor

Horizontal binning is achieved either in the pixel readout or the digital readout. The sensor will sample the combined 2x or 3x adjacent pixels within the same color plane.

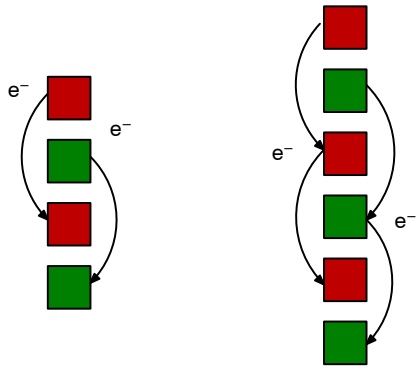


Figure 27. Vertical Row Binning in the AR0331 Sensor

Vertical row binning is applied in the pixel readout. Row binning can be configured as 2x or 3x rows within the same color plane.

Pixel skipping can be configured up to 2x and 3x in both the x-direction and y-direction. Skipping pixels in the x-direction will not reduce the row time. Skipping pixels in the y-direction will reduce the number of rows from the sensor effectively reducing the frame time. Skipping will introduce image artifacts from aliasing. Refer to the AR0331 Developer Guide for details on configuring skipping, binning, and summing modes for color and monochrome operation.

SENSOR FRAME RATE

The time required to read out an image frame (T_{FRAME}) can be derived from the number of clocks required to output each image and the pixel clock.

The frame-rate is the inverse of the frame period.

$$fps = \frac{1}{T_{FRAME}} \quad \text{(eq. 3)}$$

The number of clocks can be simplified further into the following parameters:

- The number of clocks required for each sensor row (line_length_pck)
  This parameter also determines the sensor row period when referenced to the sensor readout clock. (T_{ROW} = line_length_pck x 1/CLK_PIX)
- The number of row periods per frame (frame_length_lines)
- An extra delay between frames used to achieve a specific output frame period (extra_delay)

$$T_{FRAME} = \frac{1}{(CLK\_PIX)} \times [frame\_length\_lines \times line\_length\_pck + extra\_delay] \quad \text{(eq. 4)}$$

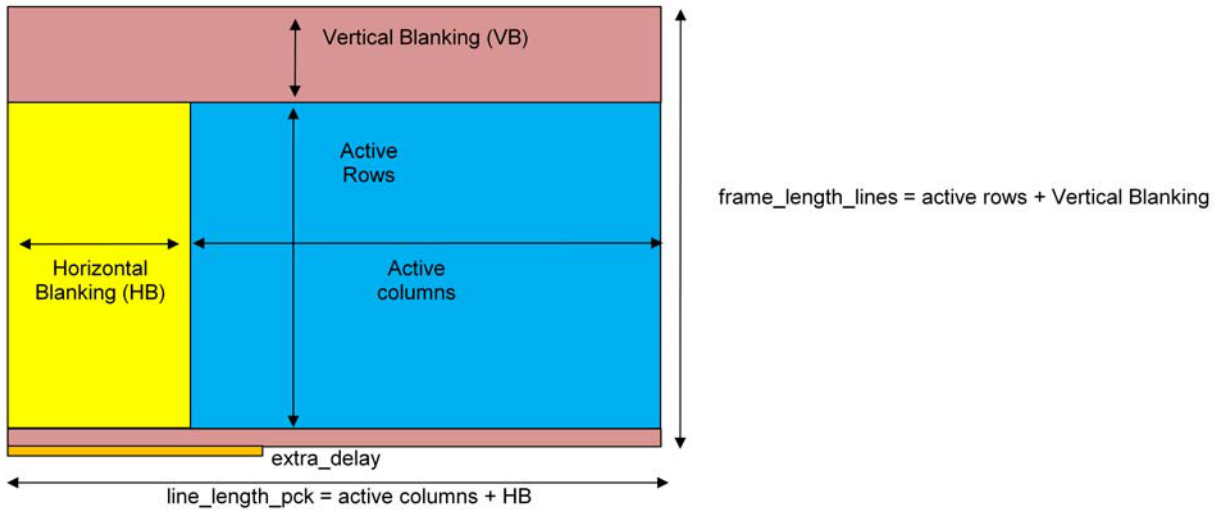


Figure 28. Frame Period Measured in Clocks

Row Period (T_{ROW})

line_length_pck will determine the number of clock periods per row and the row period (T_{ROW}) when combined with the sensor readout clock. line_length_pck includes both the active pixels and the horizontal blanking time per row. The sensor utilizes two readout paths, as seen in Figure 21, allowing the sensor to output two pixels during each pixel clock.

The minimum line_length_pck is defined as the maximum of the following three equations:

ADC Readout Limitation:

$$line\_length\_pck \geq 1100 \quad \text{(eq. 5)}$$

Digital Readout Limitation:

$$\frac{1}{3} \times \left[\frac{x\_addr\_end - x\_addr\_start + 1}{(x\_odd\_inc + 1) \times 0.5}\right] \quad \text{(eq. 6)}$$

Output Interface Limitations:

$$\frac{1}{2} \times \left[\frac{x\_addr\_end - x\_addr\_start + 1}{(x\_odd\_inc + 1) \times 0.5}\right] + 96 \quad \text{(eq. 7)}$$

Row Periods Per Frame

frame_length_lines determines the number of row periods (T_{ROW}) per frame. This includes both the active and blanking rows. The minimum vertical blanking value is defined by the number of OB rows read per frame, two embedded data rows, and two blank rows. A minimum number of idle rows equal to the T2 integration time should be added in HDR mode to allow for changes in integration time by an auto exposure algorithm. For example, if the coarse integration time is 320 lines and the exposure ratio is 16x, then the minimum vertical blanking would be 8 + 2 + 2 + 20 = 32 rows. The minimum (default) number of idle rows is 4.

$$Minimum\ frame\_length\_lines = \frac{y\_addr\_end - y\_addr\_start + 1}{\frac{(y\_odd\_inc + 1)}{2}} + min\_vertical\_blanking \quad \text{(eq. 8)}$$

The sensor is configured to output frame information in two embedded data rows by setting R0x3064[8] to 1 (default). If R0x3064[8] is set to 0, the sensor will instead output two blank rows. The data configured in the two embedded rows is defined in “Embedded Data and Statistics”.

Table 16. MINIMUM VERTICAL BLANKING CONFIGURATION

R0x3180[7:4]	OB Rows	min_vertical_blanking (Note 1)
0x8 (Default)	8 OB Rows	8 OB + 8 = 16
0x4	4 OB Rows	4 OB + 8 = 12
0x2	2 OB Rows	2 OB + 8 = 10

1. min_vertical_blanking includes the default number (4) of idle rows.

The locations of the OB rows, embedded rows, and blank rows within the frame readout are identified in Figure 29: “Slave Mode Active State and Vertical Blanking,” .

SLAVE MODE

The slave mode feature of the AR0331 supports triggering the start of a frame readout from a VD signal that is supplied from an external ASIC. The slave mode signal allows for precise control of frame rate and register change updates. The VD signal is an edge triggered input to the trigger pin and must be at least 3 PIXCLK cycles wide.

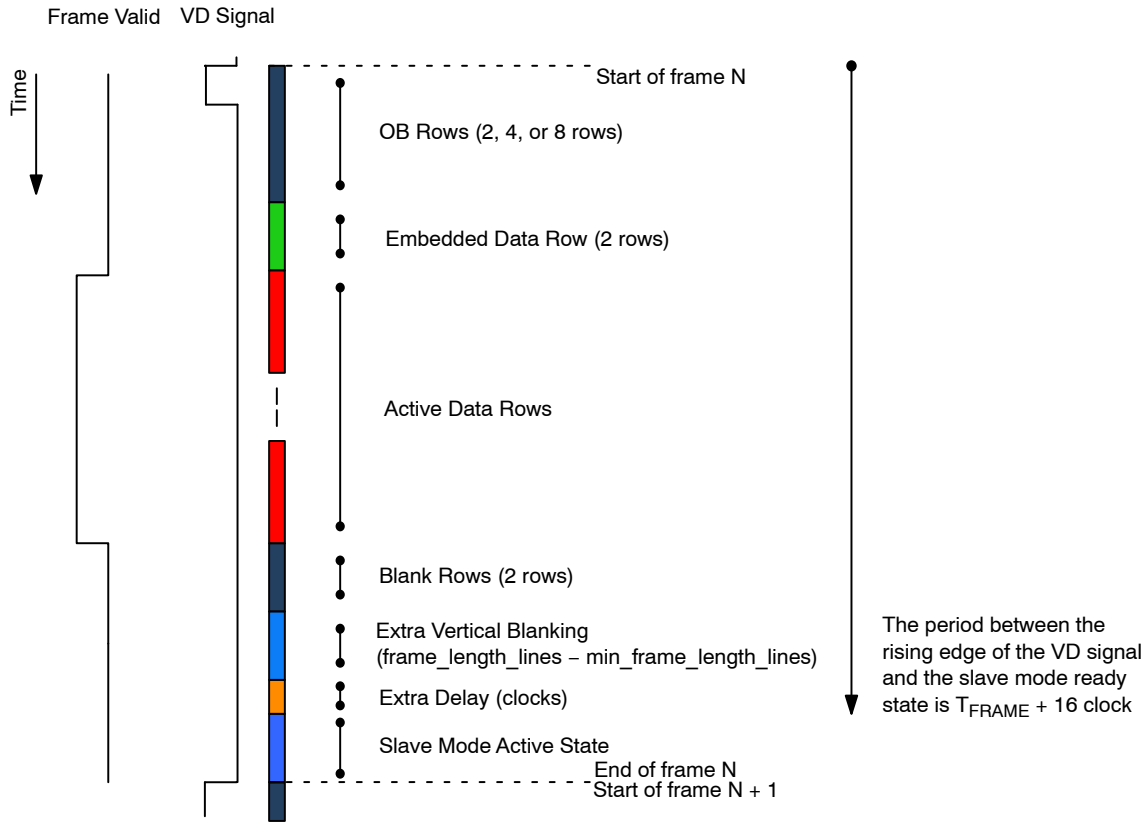
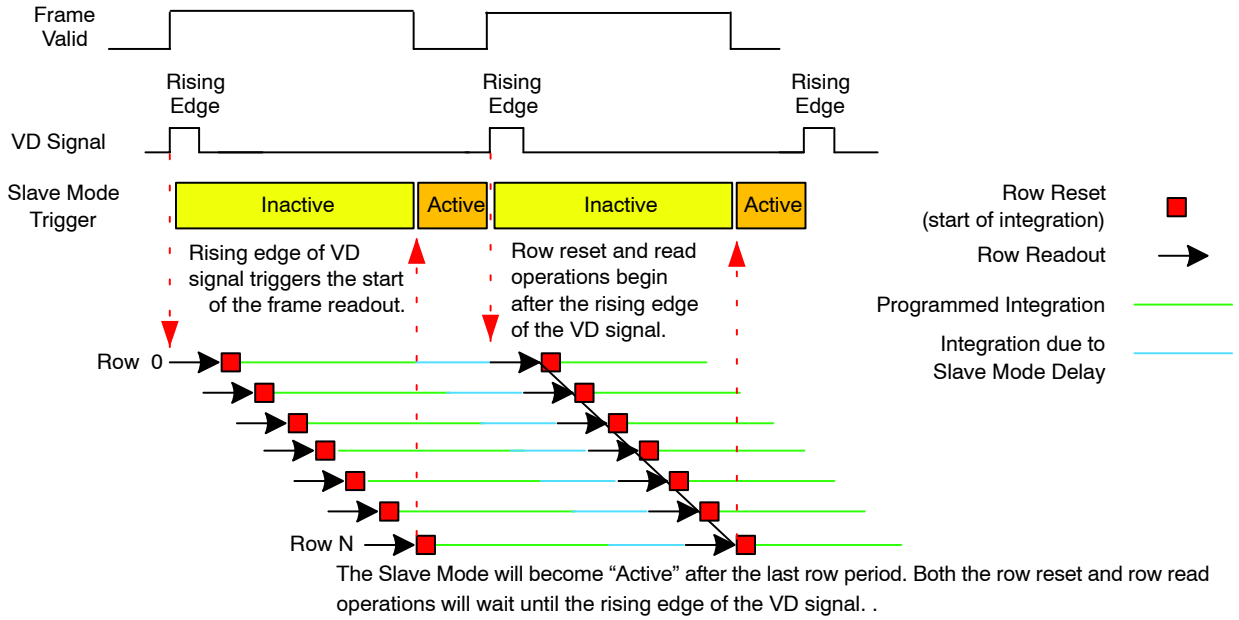


Figure 29. Slave Mode Active State and Vertical Blanking

If the slave mode is disabled, the new frame will begin after the extra delay period is finished.

The slave mode will react to the rising edge of the input VD signal if it is in an active state. When the VD signal is received, the sensor will begin the frame readout and the slave mode will remain inactive for the period of one frame time plus 16 clock periods (T_{FRAME} + (16 / CLK_PIX)). After this period, the slave mode will re-enter the active state and will respond to the VD signal.

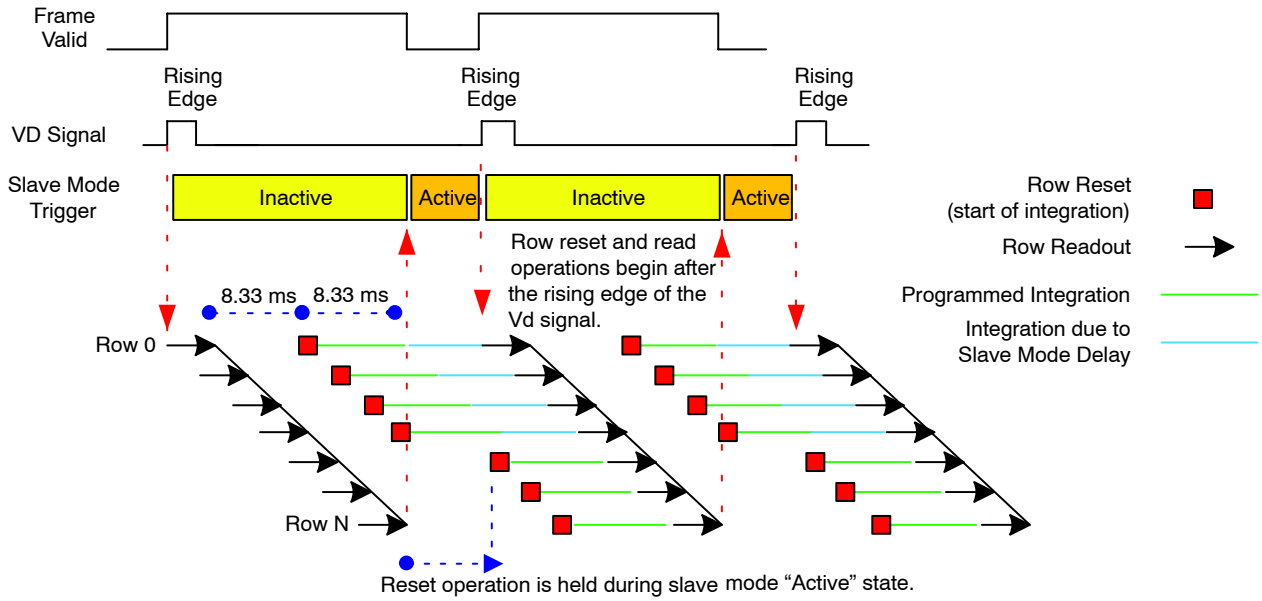


Note: The integration of the last row is started before the end of the programmed integration for the first row.

Figure 30. Slave Mode Example with Equal Integration and Frame Readout Periods

The row shutter and read operations will stop when the slave mode becomes active and is waiting for the VD signal. The following should be considered when configuring the sensor to use the slave mode:

1. The frame period (T_{FRAME}) should be configured to be less than the period of the input VD signal. The sensor will disregard the input VD signal if it appears before the frame readout is finished.
2. If the sensor integration time is configured to be less than the frame period, then the sensor will not have reset all of the sensor rows before it begins waiting for the input VD signal. This error can be minimized by configuring the frame period to be as close as possible to the desired frame rate (period between VD signals).



Note: The sensor read pointer will have paused at row 0 while the shutter pointer pauses at row N/2. The extra integration caused by the slave mode delay will only be seen by rows 0 to N/2. The example below is for a frame readout period of 16.6 ms while the integration time is configured to 8.33 ms.

Figure 31. Slave Mode Example Where the Integration Period is Half of the Frame Readout Period

When the slave mode becomes active, the sensor will pause both row read and row reset operations. (Note: The row integration period is defined as the period from row reset to row read.) The frame-time should therefore be configured so that the slave mode “wait period” is as short as possible. In the case where the sensor integration time is shorter than the frame time, the “wait period” will only increase the integration of the rows that have been reset following the last VD pulse.

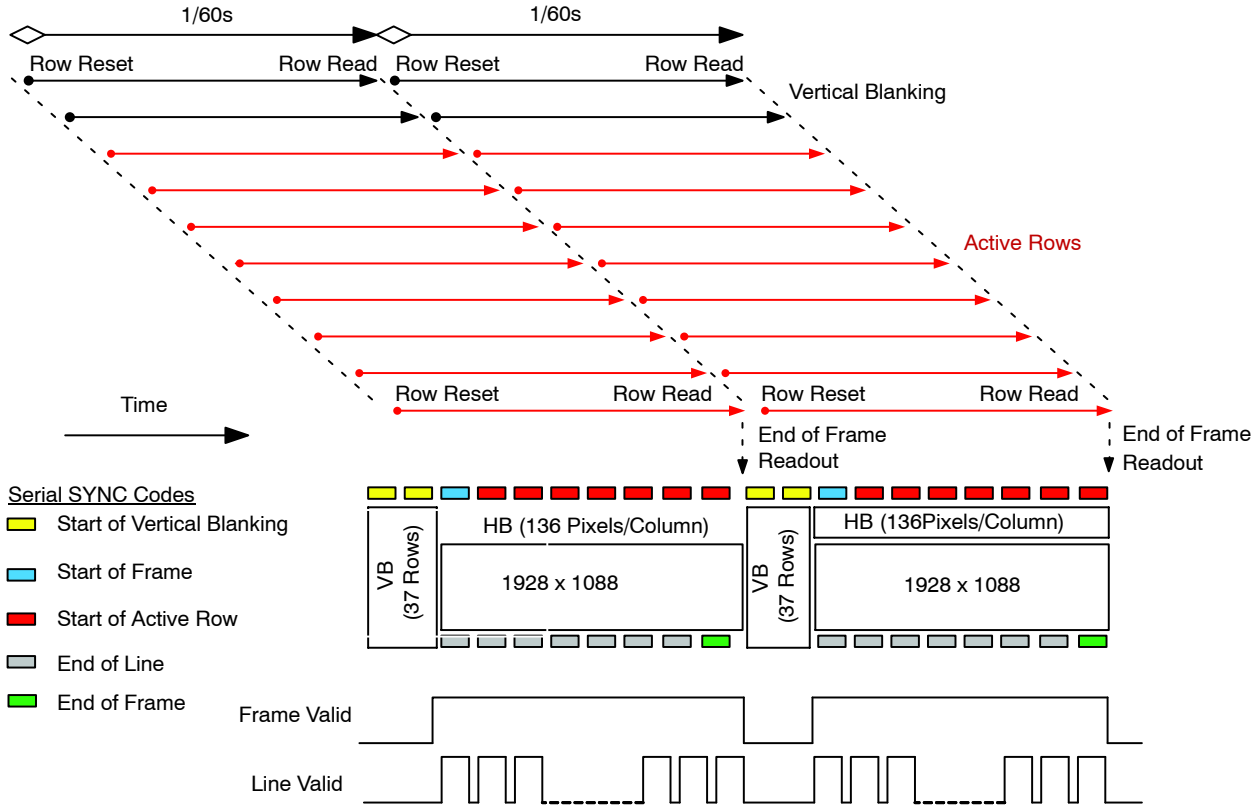
The period between slave mode pulses must also be greater than the frame period. If the rising edge of the VD pulse arrives while the slave mode is inactive, the VD pulse will be ignored and will wait until the next VD pulse has arrived.

To enter slave mode:

1. While in soft-standby, set R0x30CE[4] = 1 to enter slave mode
2. Enable the input pins (TRIGGER) by setting R0x301A[8] = 1
3. Enable streaming by setting R0x301A[2] = 1
4. Apply sync-pulses to the TRIGGER input

FRAME READOUT

The sensor readout begins with vertical blanking rows followed by the active rows. The frame readout period can be defined by the number of row periods within a frame (frame_length_lines) and the row period (*line_length_pck*/*clk_pix*). The sensor will read the first vertical blanking row at the beginning of the frame period and the last active row at the end of the row period.



Note: The frame valid and line valid signals mentioned in this diagram represent internal signals within the sensor. The SYNC codes represented in this diagram represent the HiSPi Streaming−SP protocol.

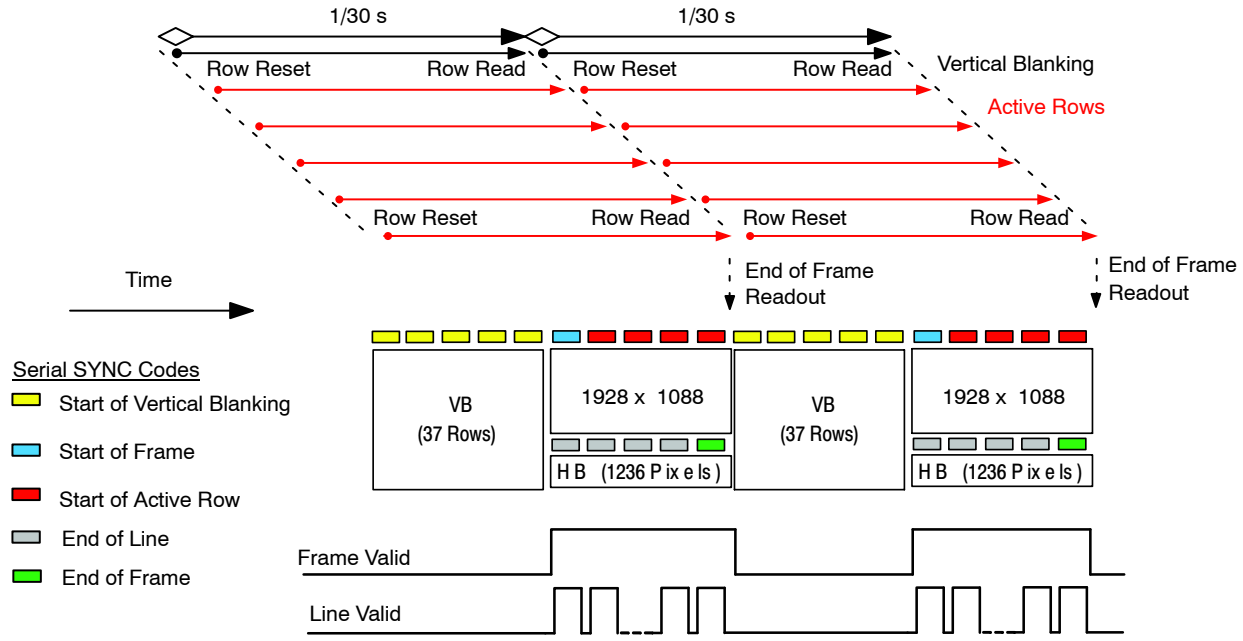
Figure 32. Example of the Sensor Output of a 1928 x 1088 Frame at 60 fps

Figure 32 aligns the frame integration and readout operation to the sensor output. It also shows the sensor output using the HiSPi Streaming-SP protocol. Different sensor protocols will list different SYNC codes.

Table 17. SERIAL SYNC CODES INCLUDED WITH EACH PROTOCOL INCLUDED WITH THE AR0331 SENSOR

Interface/Protocol	Start of Vertical Blanking Row (SOV)	Start of Frame (SOF)	Start of Active Line (SOL)	End of Line (EOL)	End of Frame (EOF)
Parallel	Parallel interface uses FRAME VALID (FV) and LINE VALID (LV) outputs to denote start and end of line and frame.				
HiSPi Streaming-S	Required	Unsupported	Required	Unsupported	Unsupported
HiSPi Streaming-SP	Required	Required	Required	Unsupported	Unsupported
HiSPi Packetized SP	Unsupported	Required	Required	Required	Required

Figure 33 illustrates how the sensor active readout time can be minimized while reducing the frame rate. 1125 VB rows were added to the output frame to reduce the 1928 x1088 frame rate from 60 fps to 30 fps without increasing the delay between the readout of the first and last active row.



Note: The frame valid and line valid signals mentioned in this diagram represent internal signals within the sensor. The SYNC codes represented in this diagram represent the HiSPi Streaming−SP protocol.

Figure 33. Example of the Sensor Output of a 1928 x 1088 Frame at 30 fps

CHANGING SENSOR MODES

Register Changes

All register writes are delayed by one frame. A register that is written to during the readout of frame *n* will not be updated to the new value until the readout of frame *n+2*. This includes writes to the sensor gain and integration registers.

Real-Time Context Switching

In the AR0331, the user may switch between two full register sets A and B by writing to a context switch change bit in R0x30B0[13]. When the context switch is configured to context A the sensor will reference the context A registers. If the context switch is changed from A to B during the readout of frame *n*, the sensor will then reference the context B coarse_integration_time registers in frame *n+1* and all other context B registers at the beginning of reading frame *n+2*. The sensor will show the same behavior when changing from context B to context A.

Table 18. LIST OF CONFIGURABLE REGISTERS FOR CONTEXT A AND CONTEXT B

Context A		Context B	
Register Description	**Address**	**Register Description**	**Address**
coarse_integration_time	0x3012	coarse_integration_time_cb	0x3016
line_length_pck	0x300C	line_length_pck_cb	0x303E
frame_length_lines	0x300A	frame_length_lines_cb	0x30AA
row_bin	0x3040[12]	row_bin_cb	0x3040[10]
col_bin	0x3040[13]	col_bin_cb	0x3040[11]
fine_gain	0x3060[3:0]	fine_gain_cb	0x3060[11:8]
coarse_gain	0x3060[5:4]	coarse_gain_cb	0x3060[13:12]
x_addr_start	0x3004	x_addr_start_cb	0x308A
y_addr_start	0x3002	y_addr_start_cb	0x308C
x_addr_end	0x3008	x_addr_end_cb	0x308E
y_addr_end	0x3006	y_addr_end_cb	0x3090
y_odd_inc	0x30A6	y_odd_inc_cb	0x30A8
x_odd_inc	0x30A2	x_odd_inc_cb	0x30AE
green1_gain	0x3056	green1_gain_cb	0x30BC
blue_gain	0x3058	blue_gain_cb	0x30BE
red_gain	0x305A	red_gain_cb	0x30C0
green2_gain	0x305C	green2_gain_cb	0x30C2
global_gain	0x305E	global_gain_cb	0x30C4
operation_mode_ctrl	0x3082	operation_mode_ctrl_cb	0x3084
bypass_pix_comb	0x318E[13:12]	bypass_pix_comb_cb	0x318E[15:14]

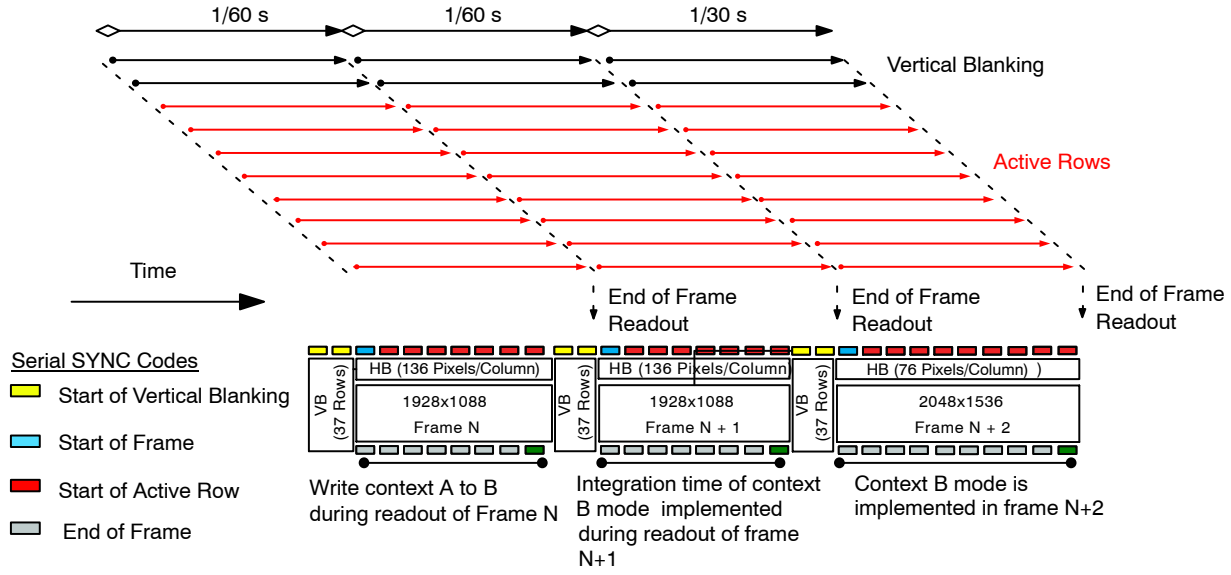


Figure 34. Example of Changing the Sensor from Context A to Context B

Combi Mode

To facilitate faster switching between linear and HDR modes, the AR0331 includes a Combi Mode feature. When enabled, Combi Mode loads a single (HDR) sequencer. When switching from HDR to linear modes, the sequencer remains the same, but only the T1 image is output. While not optimized for linear mode operation, it allows faster mode switching as a new sequencer load is not needed. Combi Mode is enabled by setting bit R0x30BA[8]. See the AR0331 Developer Guide for more information on Combi Mode.

Compression

When the AR0331 is configured for linear mode operation, the sensor can optionally compress 12-bit data to 10-bit using A-law compression. The compression is applied after the data pedestal has been added to the data. See “Pedestals”.

The A-law compression is disabled by default and can be enabled by setting R0x31D0 from “0” to “1”.

Table 19. A−LAW COMPRESSION TABLE FOR 12−10 BITS

	Input Values												Compressed Codeword									
Input Range	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0 to 127	0	0	0	0	0	a	b	c	d	e	f	g	0	0	0	a	b	c	d	e	f	g
128 to 255	0	0	0	0	1	a	b	c	d	e	f	g	0	0	1	a	b	c	d	e	f	g
256 to 511	0	0	0	1	a	b	c	d	e	f	g	X	0	1	0	a	b	c	d	e	f	g
512 to 1023	0	0	1	a	b	c	d	e	f	g	X	X	0	1	1	a	b	c	d	e	f	g
1024 to 2047	0	1	a	b	c	d	e	f	g	h	X	X	1	0	a	b	c	d	e	f	g	h
2048 to 4095	1	a	b	c	d	e	f	g	h	X	X	X	1	1	a	b	c	d	e	f	g	h

Temperature Sensor

The AR0331 sensor has a built-in PTAT-based temperature sensor, accessible through registers, that is capable of measuring die junction temperature.

The temperature sensor can be enabled by writing R0x30B4[0]=1 and R0x30B4[4]=1. After this, the temperature sensor output value can be read from R0x30B2[9:0].

The value read out from the temperature sensor register is an ADC output value that needs to be converted downstream to a final temperature value in degrees Celsius. Since the PTAT device characteristic response is quite linear in the temperature range of operation required, a simple linear function in the format of the equation below can be used to convert the ADC output value to the final temperature in degrees Celsius.

$$\text{Temperature} = \text{slope} \times \text{R0x30B2[9 : 0]} + T_0 \qquad \text{(eq. 9)}$$

For this conversion, a minimum of two known points are needed to construct the line formula by identifying the slope and y-intercept “T_0”. These calibration values can be read from registers R0x30C6 and R0x30C8, which correspond to

value read at 70°C and 55°C respectively. Once read, the slope and y-intercept values can be calculated and used in Equation 9.

For more information on the temperature sensor registers, refer to the AR0331 Register Reference.

Embedded Data and Statistics

The AR0331 has the capability to output image data and statistics embedded within the frame timing. There are two types of information embedded within the frame readout.

- Embedded Data:
  If enabled, these are displayed on the two rows immediately before the first active pixel row is displayed.
- Embedded Statistics:
  If enabled, these are displayed on the two rows immediately after the last active pixel row is displayed.

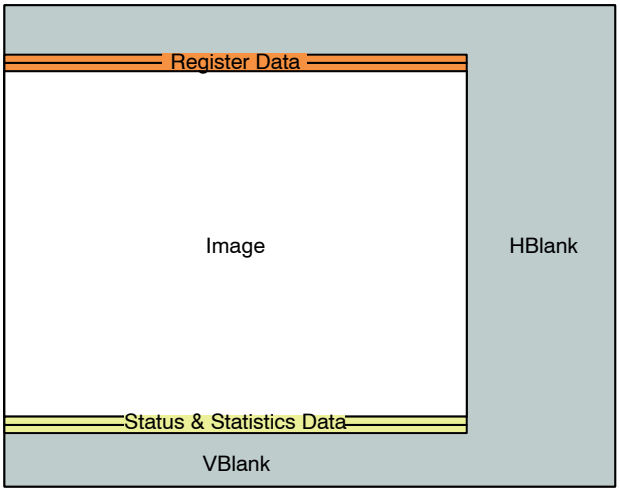


Figure 35. Frame Format with Embedded Data Lines Enabled

Embedded Data

The embedded data contains the configuration of the image being displayed. This includes all register settings used to capture the current frame. The registers embedded in these rows are as follows:

- Line 1: Registers R0x3000 to R0x312F
- Line 2: Registers R0x3136 to R0x31BF, R0x31D0 to R0x31FF

NOTE: All undefined registers will have a value of 0.

The format of the embedded register data transmission is defined per the embedded data section of the SMIA Function Specification.

In parallel mode, since the pixel word depth is 12 bits/pixel, the sensor 16-bit register data will be transferred over 2 pixels where the register data will be broken up into 8 MSB and 8 LSB. The alignment of the 8-bit data will be on the 8 MSB bits of the 12-bit pixel word. For example, if a register value of 0x1234 is to be transmitted, it will be transmitted over two, 12-bit pixels as follows: 0x120, 0x340.

Embedded Statistics

The embedded statistics contain frame identifiers and histogram information of the image in the frame. This can be used by downstream auto-exposure algorithm blocks to make decisions about exposure adjustment.

This histogram is divided into 244 bins with a bin spacing of 64 evenly spaced bins for digital code values 0 to 2^8, 120 evenly spaced bins for values 2^8 to 2^{12}, 60 evenly spaced bins for values 2^{12} to 2^{16}. In HDR with a 16x exposure ratio, this approximately corresponds to the T1 and T2 exposures respectively. The statistics found in line 2 are for backwards compatibility. It is recommended that auto exposure algorithms be developed using the histogram statistics on line 1.

The first pixel of each line in the embedded statistics is a tag value of 0x0B0. This signifies that all subsequent statistics data is 10 bit data aligned to the MSB of the 12-bit pixel.

Figure 36 summarizes how the embedded statistics transmission looks like. It should be noted that data, as shown in Figure 36, is aligned to the MSB of each word:

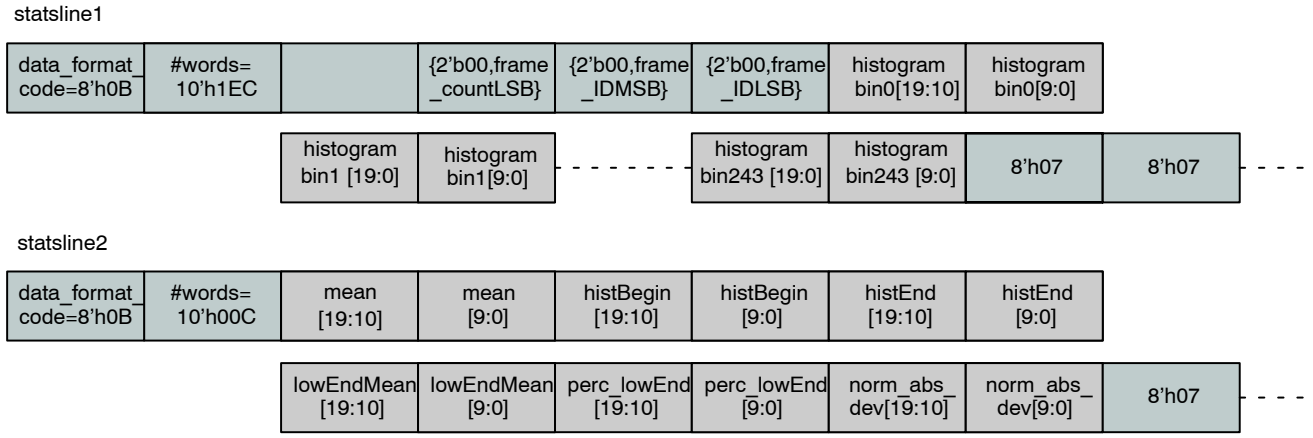


Figure 36. Format of Embedded Statistics Output within a Frame

The statistics embedded in these rows are as follows:

Line 1:

- 0x0B0 – identifier
- Register 0x303A – frame_count
- Register 0x31D2 – frame ID
- Histogram data – histogram bins 0–243

Line 2:

- 0x0B0 (TAG)
- Mean
- Histogram Begin
- Histogram End
- Low End Histogram Mean
- Percentage of Pixels Below Low End Mean
- Normal Absolute Deviation

Test Patterns

The AR0331 has the capability of injecting a number of test patterns into the top of the datapath to debug the digital logic. With one of the test patterns activated, any of the datapath functions can be enabled to exercise it in a deterministic fashion. Test patterns are selected by Test_Pattern_Mode register (R0x3070). Only one of the test patterns can be enabled at a given point in time by setting the Test_Pattern_Mode register according to Table 20. When test patterns are enabled the active area will receive the value specified by the selected test pattern and the dark pixels will receive the value in Test_Pattern_Green (R0x3074 and R0x3078) for green pixels, Test_Pattern_Blue (R0x3076) for blue pixels, and Test_Pattern_Red (R0x3072) for red pixels.

Table 20. TEST PATTERN MODES

Test_Pattern_Mode	Test Pattern Output
0	No Test Pattern (Normal Operation)
1	Solid Color Test Pattern
2	100% Vertical Color Bars Test Pattern
3	Fade-to-Gray Vertical Color Bars Test Pattern
256	Walking 1s Test Pattern (12-bit)

Solid Color

When the color field mode is selected, the value for each pixel is determined by its color. Green pixels will receive the value in Test_Pattern_Green, red pixels will receive the value in Test_Pattern_Red, and blue pixels will receive the value in Test_Pattern_Blue.

Vertical Color Bars

When the vertical color bars mode is selected, a typical color bar pattern will be sent through the digital pipeline.

Walking 1s

When the walking 1 s mode is selected, a walking 1 s pattern will be sent through the digital pipeline. The first value in each row is 1.

TWO-WIRE SERIAL REGISTER INTERFACE

The two-wire serial interface bus enables read/write access to control and status registers within the AR0331.

The interface protocol uses a master/slave model in which a master controls one or more slave devices. The sensor acts as a slave device. The master generates a clock (SCLK) that is an input to the sensor and is used to synchronize transfers. Data is transferred between the master and the slave on a bidirectional signal (SDATA). SDATA is pulled up to VDD_IO off-chip by a 1.5 kΩ resistor. Either the slave or master device can drive SDATA LOW—the interface protocol determines which device is allowed to drive SDATA at any given time.

The protocols described in the two-wire serial interface specification allow the slave device to drive SCLKLOW; the AR0331 uses SCLK as an input only and therefore never drives it LOW.

Protocol

Data transfers on the two-wire serial interface bus are performed by a sequence of low-level protocol elements:

1. a (repeated) start condition
2. a slave address/data direction byte
3. an (a no) acknowledge bit
4. a message byte
5. a stop condition

The bus is idle when both SCLK and SDATA are HIGH. Control of the bus is initiated with a start condition, and the bus is released with a stop condition. Only the master can generate the start and stop conditions.

Start Condition

A start condition is defined as a HIGH-to-LOW transition on SDATA while SCLK is HIGH. At the end of a transfer, the master can generate a start condition without previously generating a stop condition; this is known as a "repeated start" or "restart" condition.

Stop Condition

A stop condition is defined as a LOW-to-HIGH transition on SDATA while SCLK is HIGH.

Data Transfer

Data is transferred serially, 8 bits at a time, with the MSB transmitted first. Each byte of data is followed by an acknowledge bit or a no-acknowledge bit. This data transfer mechanism is used for the slave address/data direction byte and for message bytes.

One data bit is transferred during each SCLK clock period. SDATA can change when SCLK is LOW and must be stable while SCLK is HIGH.

Slave Address/Data Direction Byte

Bits [7:1] of this byte represent the device slave address and bit [0] indicates the data transfer direction. A "0" in bit [0] indicates a WRITE, and a "1" indicates a READ. The default slave addresses used by the AR0331 are 0x20 (write address) and 0x21 (read address) in accordance with the specification. Alternate slave addresses of 0x30 (write address) and 0x31 (read address) can be selected by enabling and asserting the SADDR input.

An alternate slave address can also be programmed through R0x31FC.

Message Byte

Message bytes are used for sending register addresses and register write data to the slave device and for retrieving register read data.

Acknowledge Bit

Each 8-bit data transfer is followed by an acknowledge bit or a no-acknowledge bit in the SCLK clock period following the data transfer. The transmitter (which is the master when writing, or the slave when reading) releases SDATA. The receiver indicates an acknowledge bit by driving SDATA LOW. As for data transfers, SDATA can change when SCLK is LOW and must be stable while SCLK is HIGH.

No-Acknowledge Bit

The no-acknowledge bit is generated when the receiver does not drive SDATA LOW during the SCLK clock period following a data transfer. A no-acknowledge bit is used to terminate a read sequence.

Typical Sequence

A typical READ or WRITE sequence begins by the master generating a start condition on the bus. After the start condition, the master sends the 8-bit slave address/data direction byte. The last bit indicates whether the request is for a read or a write, where a "0" indicates a write and a "1" indicates a read. If the address matches the address of the slave device, the slave device acknowledges receipt of the address by generating an acknowledge bit on the bus.

If the request was a WRITE, the master then transfers the 16-bit register address to which the WRITE should take place. This transfer takes place as two 8-bit sequences and the slave sends an acknowledge bit after each sequence to indicate that the byte has been received. The master then transfers the data as an 8-bit sequence; the slave sends an acknowledge bit at the end of the sequence. The master stops writing by generating a (re)start or stop condition.

If the request was a READ, the master sends the 8-bit write slave address/data direction byte and 16-bit register address, the same way as with a WRITE request. The master then generates a (re)start condition and the 8-bit read slave address/data direction byte, and clocks out the register data, 8 bits at a time. The master generates an acknowledge bit after each 8-bit transfer. The slave's internal register address is automatically incremented after every 8 bits are transferred. The data transfer is stopped when the master sends a no-acknowledge bit.

Single READ from Random Location

This sequence (Figure 37) starts with a dummy WRITE to the 16-bit address that is to be used for the READ. The master terminates the WRITE by generating a restart condition. The master then sends the 8-bit read slave address/data direction byte and clocks out one byte of register data. The master terminates the READ by generating a no-acknowledge bit followed by a stop condition. Figure 37 shows how the internal register address maintained by the AR0331 is loaded and incremented as the sequence proceeds.

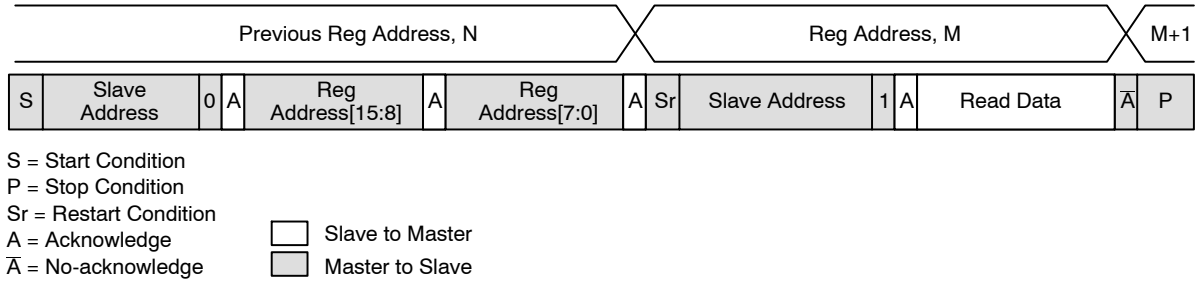


Figure 37. Single READ from Random Location

Single READ From Current Location

This sequence (Figure 38) performs a read using the current value of the AR0331 internal register address. The master terminates the READ by generating a no-acknowledge bit followed by a stop condition. The figure shows two independent READ sequences.

Figure 38. Single READ from Current Location

Sequential READ, Start From Random Location

This sequence (Figure 42) starts in the same way as the single WRITE to random location (Figure 41). Instead of generating a no-acknowledge bit after the first byte of data has been transferred, the master generates an acknowledge bit and continues to perform byte WRITEs until “L” bytes have been written. The WRITE is terminated by the master generating a stop condition.

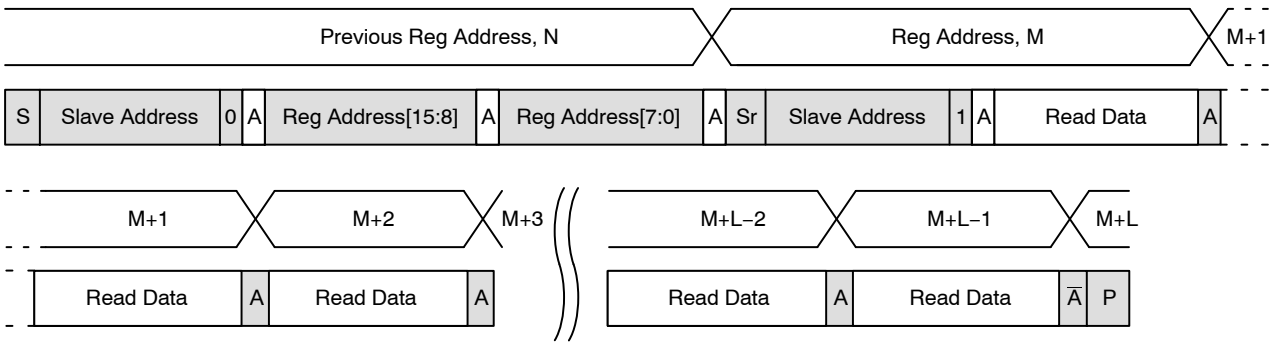


Figure 39. Sequential READ, Start from Random Location

Sequential READ, Start From Current Location

This sequence (Figure 40) starts in the same way as the single READ from current location (Figure 38). Instead of generating a no-acknowledge bit after the first byte of data has been transferred, the master generates an acknowledge bit and continues to perform byte READs until “L” bytes have been read.

Figure 40. Sequential READ, Start from Current Location

Single WRITE to Random Location

This sequence (Figure 41) begins with the master generating a start condition. The slave address/data direction byte signals a WRITE and is followed by the HIGH then LOW bytes of the register address that is to be written. The master follows this with the byte of write data. The WRITE is terminated by the master generating a stop condition.

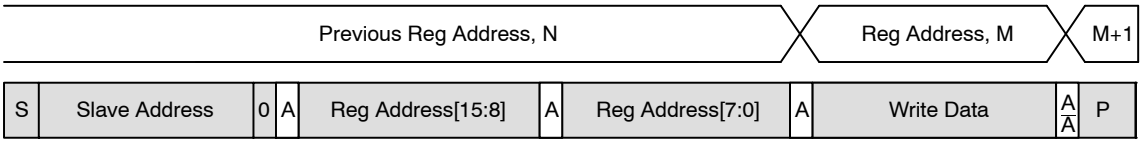


Figure 41. Single WRITE to Random Location

Sequential WRITE, Start at Random Location

This sequence (Figure 42) starts in the same way as the single WRITE to random location (Figure 41). Instead of generating a no−acknowledge bit after the first byte of data has been transferred, the master generates an acknowledge bit and continues to perform byte WRITEs until “L” bytes have been written. The WRITE is terminated by the master generating a stop condition.

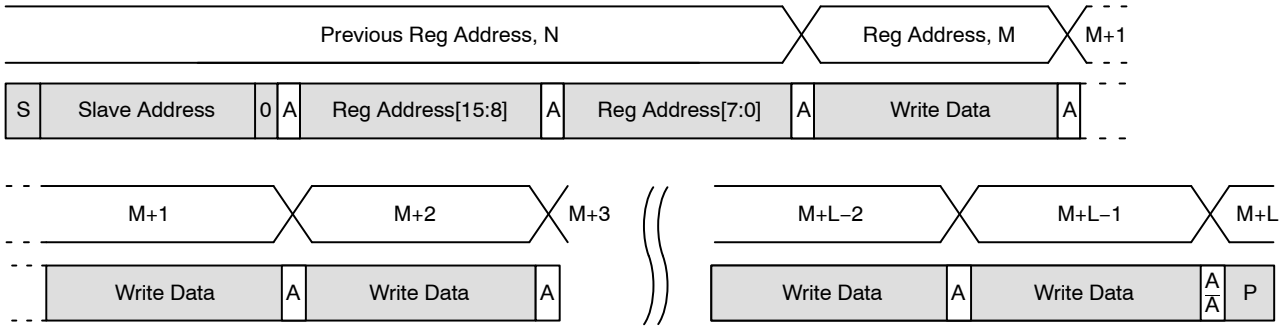


Figure 42. Sequential WRITE, Start at Random Location

SPECTRAL CHARACTERISTICS

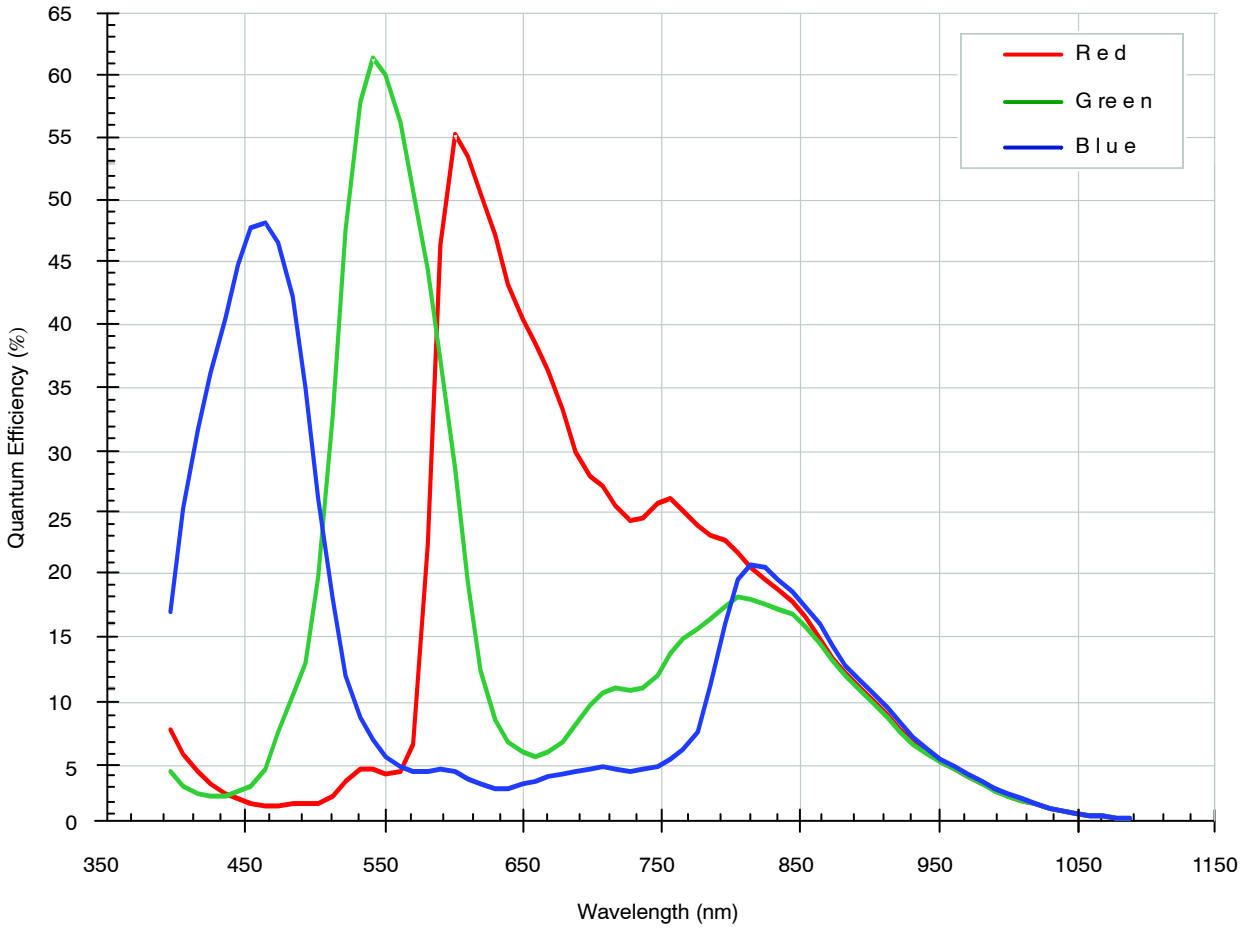


Figure 43. Quantum Efficiency

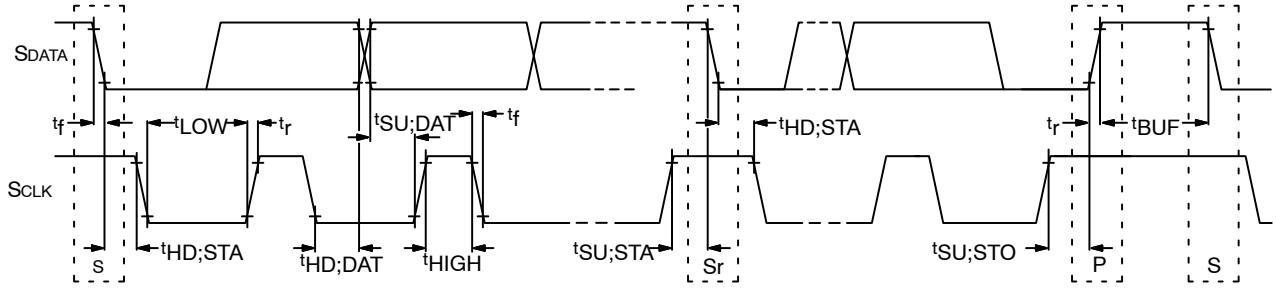
ELECTRICAL SPECIFICATIONS

Unless otherwise stated, the following specifications apply under the following conditions:

- V_{DD} = 1.8 V – 0.10/+0.15; V_{DD}_IO = V_{DD}_PLL = V_{AA} = V_{AA}_PIX = 2.8 V ±0.3 V;
- V_{DD}_SLVS = 0.4 V – 0.1/+0.2; T_A = –30°C to +85°C; output load = 10 pF;
- frequency = 74.25 MHz; HiSPi off.

Two-Wire Serial Register Interface

The electrical characteristics of the two-wire serial register interface (SCLK, SDATA) are shown in Figure 44 and Table 21.



Note: Read sequence: For an 8-bit READ, read waveforms start after WRITE command and register address are issued.

Figure 44. Two-Wire Serial Bus Timing Parameters

Table 21. TWO−WIRE SERIAL BUS CHARACTERISTICS

(^{f}EXTCLK = 27 MHz; V_{DD} = 1.8 V; V_{DD}_IO = 2.8 V; V_{AA} = 2.8 V; V_{AA}_PIX = 2.8 V; V_{DD}_PLL = 2.8 V; V_{DD}_DAC = 2.8 V; T_A = 25°C)

Parameter	Symbol	Standard Mode		Fast Mode		Unit
		Min	Max	Min	Max	
SCLK Clock Frequency	^{f}SCL	0	100	0	400	KHz
Hold Time (Repeated) START Condition						
After this period, the first clock pulse is generated	^{t}HD;STA	4.0	–	0.6	–	µS
LOW Period of the SCLK Clock	^{t}LOW	4.7	–	1.3	–	µS
HIGH Period of the SCLK Clock	^{t}HIGH	4.0	–	0.6	–	µS
Set up Time for a Repeated START Condition	^{t}SU;STA	4.7	–	0.6	–	µS
Data Hold Time	^{t}HD;DAT	0 (Note 4)	3.45 (Note 5)	0 (Note 6)	0.9 (Note 5)	µS
Data Set-up Time	^{t}SU;DAT	250	–	100 (Note 6)	–	nS
Rise Time of Both SDATA and SCLK Signals	^{t}r	–	1000	20 + 0.1Cb (Note 7)	300	nS
Fall Time of Both SDATA and SCLK Signals	^{t}f	–	300	20 + 0.1Cb (Note 7)	300	nS
Set-up Time for STOP Condition	^{t}SU;STO	4.0	–	0.6	–	µS
Bus Free Time between a STOP and START Condition	^{t}BUF	4.7	–	1.3	–	µS
Capacitive Load for Each bus Line	Cb	–	400	–	400	pF
Serial Interface Input pin Capacitance	CIN_SI	–	3.3	–	3.3	pF
SDATA Max Load Capacitance	CLOAD_SD	–	30	–	30	pF
SDATA Pull-up Resistor	RSD	1.5	4.7	1.5	4.7	KΩ

1. This table is based on I^{2}C standard (v2.1 January 2000). Philips Semiconductor.
2. Two-wire control is I^{2}C-compatible.
3. All values referred to V_{IHmin} = 0.9 V_{DD} and V_{ILmax} = 0.1 V_{DD} levels. Sensor EXCLK = 27 MHz.
4. A device must internally provide a hold time of at least 300 ns for the SDATA signal to bridge the undefined region of the falling edge of SCLK.

5. The maximum ^{t}HD;DAT has only to be met if the device does not stretch the LOW period (^{t}LOW) of the SCLK signal.
6. A Fast-mode I^{2}C-bus device can be used in a Standard-mode I^{2}C-bus system, but the requirement ^{t}SU;DAT 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCLK signal. If such a device does stretch the LOW period of the SCLK signal, it must output the next data bit to the SDATA line ^{t}r max + ^{t}SU;DAT = 1000 + 250 = 1250 ns (according to the Standard-mode I^{2}C-bus specification) before the SCLK line is released.
7. Cb = total capacitance of one bus line in pF.

I/O Timing

By default, the AR0331 launches pixel data, FV, and LV with the rising edge of PIXCLK. The expectation is that the user captures DOUT[11:0], FV, and LV using the falling edge of PIXCLK.

See Figure 45 below and Table 22 for I/O timing (AC) characteristics.

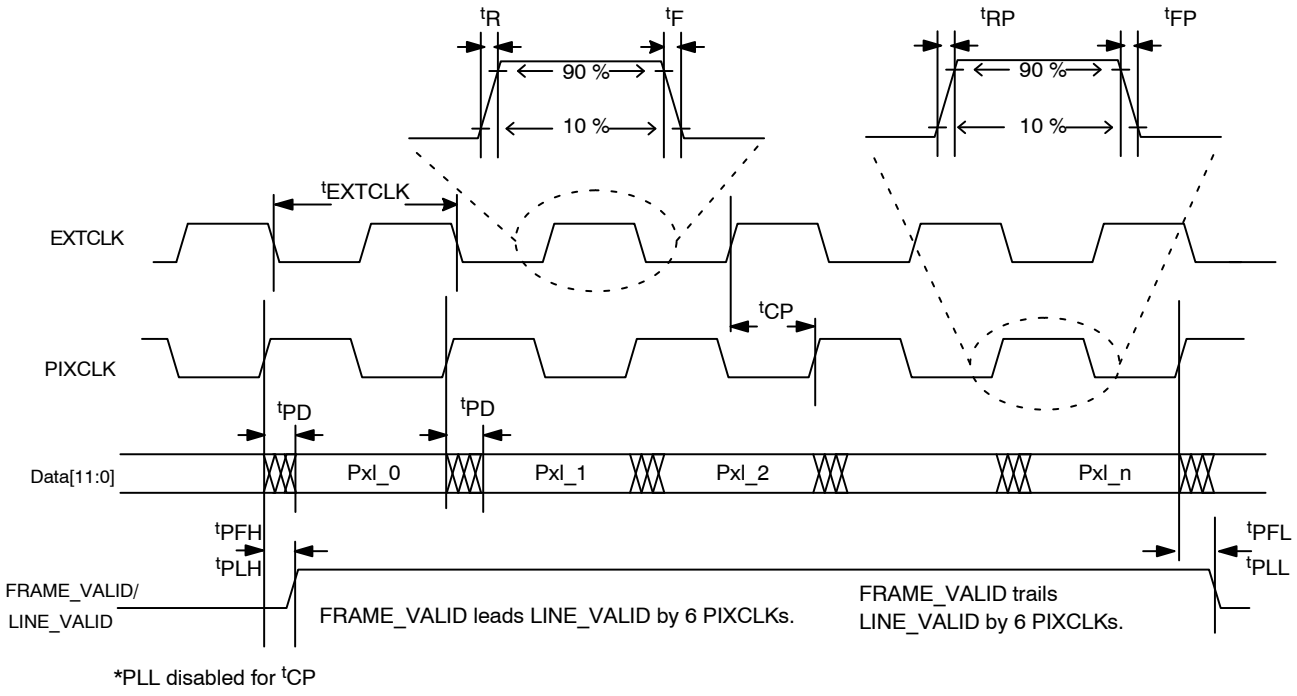


Figure 45. I/O Timing Diagram

Table 22. I/O TIMING CHARACTERISTICS

Symbol	Definition	Condition	Min	Typ	Max	Unit
^{f}EXTCLK1	Input Clock Frequency		6	–	48	MHz
^{t}EXTCLK1	Input Clock Period		20.8	–	166	ns
^{t}R	Input Clock Rise Time		–	3	–	ns
^{t}F	Input Clock Fall Time		–	3	–	ns
^{t}RP	Pixclk Rise Time		–	4	–	ns
^{t}FP	Pixclk Fall Time		–	4	–	ns
	Clock Duty Cycle		40	50	60	%
^{t}(PIX JITTER)	Jitter on PIXCLK		–	1		ns
^{t}CP	EXTCLK to PIXCLK Propagation Delay	Nominal voltages, PLL Disabled	–	11.3	–	ns
^{f}PIXCLK	PIXCLK Frequency	Default, Nominal Voltages	6		74.25	MHz
^{t}PD	PIXCLK to Data Valid	Default, Nominal Voltages	–	2.3	–	ns

Table 22. I/O TIMING CHARACTERISTICS (continued)

Symbol	Definition	Condition	Min	Typ	Max	Unit
^tPFH	PIXCLK to FV HIGH	Default, Nominal Voltages	–	1.5	–	ns
^tPLH	PIXCLK to LV HIGH	Default, Nominal Voltages	–	2.3	–	ns
^tPFL	PIXCLK to FV LOW	Default, Nominal Voltages	–	1.5	–	ns
tPLL	PIXCLK to LV LOW	Default, Nominal Voltages	–	2	–	ns
C_{LOAD}	Output Load Capacitance		–	<10	–	pF
C_{IN}	Input Pin Capacitance		–	2.5	–	pF

1. I/O timing characteristics are measured under the following conditions:
   – Temperature is 25°C ambient
   – 10 pF load

DC Electrical Characteristics

The DC electrical characteristics are shown in the tables below.

Table 23. DC ELECTRICAL CHARACTERISTICS

Symbol	Definition	Condition	Min	Typ	Max	Unit
V_{DD}	Core Digital Voltage		1.7	1.8	1.95	V
V_{DD_IO}	I/O Digital Voltage		1.7/2.5	1.8/2.8	1.9/3.1	V
V_{AA}	Analog Voltage		2.5	2.8	3.1	V
V_{AA_PIX}	Pixel Supply Voltage		2.5	2.8	3.1	V
V_{DD_PLL}	PLL Supply Voltage		2.5	2.8	3.1	V
V_{DD_SLVS}	HiSPi Supply Voltage		0.3	0.4	0.6	V
V_{IH}	Input HIGH Voltage		VDD_IO*0.7	–	–	V
V_{IL}	Input LOW Voltage		–	–	VDD_IO*0.3	V
I_{IN}	Input Leakage Current	No Pull-up Resistor; V_{IN} = V_{DD_IO} or D_{GND}	20	–	–	μA
V_{OH}	Output HIGH Voltage		VDD_IO–0.3	–	–	V
V_{OL}	Output LOW Voltage		–	–	0.4	V
I_{OH}	Output HIGH Current	At Specified V_{OH}	–22	–	–	mA
I_{OL}	Output LOW Current	At Specified V_{OL}	–	–	22	mA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

CAUTION: Stresses greater than those listed in Table 14 may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied

Table 24. ABSOLUTE MAXIMUM RATINGS

Symbol	Definition	Min	Max	Unit
V_{DD}_MAX	Core digital voltage	–0.3	2.4	V
V_{DD}_IO_MAX	I/O digital voltage	–0.3	4	V
V_{AA}_MAX	Analog voltage	–0.3	4	V
V_{AA}_PIX	Pixel supply voltage	–0.3	4	V
V_{DD}_PLL	PLL supply voltage	–0.3	4	V
VDD_SLVS_MAX	HiSPi I/O digital voltage	–0.3	2.4	V
t_{ST}	Storage temperature	–40	85	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Table 25. OPERATING CURRENT CONSUMPTION IN PARALLEL OUTPUT AND LINEAR MODE

Definition	Condition	Symbol	Min	Typ	Max	Unit
Digital Operating Current	Streaming, 2048x1536 20 fps	I_{DD}1	–	122	137	mA
I/O Digital Operating Current	Streaming, 2048x1536 20 fps	I_{DD}_IO	–	25	30	mA
Analog Operating Current	Streaming, 2048x1536 20 fps	I_{AA}	–	32	38	mA
Pixel Supply Current	Streaming, 2048x1536 20 fps	I_{AA}_PIX	–	7	12	mA
PLL Supply Current	Streaming, 2048x1536 20 fps	I_{DD}_PLL	–	8	12	mA
Digital Operating Current	Streaming, 1080p30	I_{DD}1	–	122	137	mA
I/O Digital Operating Current	Streaming, 1080p30	I_{DD}_IO	–	25	30	mA
Analog Operating Current	Streaming, 1080p30	I_{AA}	–	35	40	mA
Pixel Supply Current	Streaming, 1080p30	I_{AA}_PIX	–	7	12	mA
PLL Supply Current	Streaming, 1080p30	I_{DD}_PLL	–	8	12	mA

1. Operating currents are measured at the following conditions:
   V_{AA} = V_{AA}_PIX = V_{DD}_PLL = 2.8 V
   V_{DD} = V_{DD}_IO = 1.8 V
   PLL Enabled and PIXCLK = 74.25 MHz
   T_A = 25°C

Table 26. OPERATING CURRENT CONSUMPTION IN PARALLEL OUTPUT AND HDR MODE

Definition	Condition	Symbol	Min	Typ	Max	Unit
Digital Operating Current	Streaming, 2048x1536 20 fps	I_{DD}	–	156	173	mA
I/O Digital Operating Current	Streaming, 2048x1536 20 fps	I_{DD}_IO	–	30	35	mA
Analog Operating Current	Streaming, 2048x1536 20 fps	I_{AA}	–	50	65	mA
Pixel Supply Current	Streaming, 2048x1536 20 fps	I_{AA}_PIX	–	9	14	mA
PLL Supply Current	Streaming, 2048x1536 20 fps	I_{DD}_PLL	–	8	12	mA
Digital Operating Current	Streaming, 1080p30	I_{DD}	–	161	184	mA
I/O Digital Operating Current	Streaming, 1080p30	I_{DD}_IO	–	30	35	mA
Analog Operating Current	Streaming, 1080p30	I_{AA}	–	54	70	mA
Pixel Supply Current	Streaming, 1080p30	I_{AA}_PIX	–	9	14	mA
PLL Supply Current	Streaming, 1080p30	I_{DD}_PLL	–	8	12	mA

1. Operating currents are measured at the following conditions:
   V_{AA} = V_{AA}_PIX = V_{DD}_PLL = 2.8 V
   V_{DD} = V_{DD}_IO = 1.8 V
   PLL Enabled and PIXCLK = 74.25 MHz
   PLL Enabled and PIXCLK = 74.25 MHz
   T_A = 25°C

Table 27. OPERATING CURRENT IN HiSPi (HIVCM) OUTPUT AND LINEAR MODE

Definition	Condition	Symbol	Min	Typ	Max	Unit
Digital Operating Current	Streaming, 2048x1536 30fps	I_{DD}	–	252	278	mA
Analog Operating Current	Streaming, 2048x1536 30fps	I_{AA}	–	27	35	mA
Pixel Supply Current	Streaming, 2048x1536 30fps	I_{AA_PIX}	–	5	10	mA
PLL Supply Current	Streaming, 2048x1536 30fps	I_{DD_PLL}	–	8	12	mA
SLVS Supply Current	Streaming, 2048x1536 30fps	I_{DD_SLVS}	–	22	26	mA
Digital Operating Current	Streaming, 1080p60	I_{DD}	–	276	302	mA
Analog Operating Current	Streaming, 1080p60	I_{AA}	–	37	45	mA
Pixel Supply Current	Streaming, 1080p60	I_{AA_PIX}	–	7	12	mA
PLL Supply Current	Streaming, 1080p60	I_{DD_PLL}	–	8	12	mA
SLVS Supply Current	Streaming, 1080p60	I_{DD_SLVS}	–	22	26	mA

1. Operating currents are measured at the following conditions:
   V_{AA} = V_{AA_PIX} = V_{DD_PLL}=2.8 V
   V_{DD} = V_{DD_IO}= 1.8 V
   V_{DD_SLVS} = 1.8 V
   PLL Enabled and PIXCLK=74.25 Mhz
   T_A = 25°C

Table 28. OPERATING CURRENT IN HiSPi (HIVCM) OUTPUT AND HDR MODE

Definition	Condition	Symbol	Min	Typ	Max	Unit
Digital Operating Current	Streaming, 2048x1536 30fps	I_{DD}	–	317	358	mA
Analog Operating Current	Streaming, 2048x1536 30fps	I_{AA}	–	45	55	mA
Pixel Supply Current	Streaming, 2048x1536 30fps	I_{AA_PIX}	–	8	13	mA
PLL Supply Current	Streaming, 2048x1536 30fps	I_{DD_PLL}	–	8	12	mA
SLVS Supply Current	Streaming, 2048x1536 30fps	I_{DD_SLVS}	–	22	26	mA
Digital Operating Current	Streaming, 1080p60	I_{DD}	–	323	358	mA
Analog Operating Current	Streaming, 1080p60	I_{AA}	–	55	70	mA
Pixel Supply Current	Streaming, 1080p60	I_{AA_PIX}	–	9	14	mA
PLL Supply Current	Streaming, 1080p60	I_{DD_PLL}	–	8	12	mA
SLVS Supply Current	Streaming, 1080p60	I_{DD_SLVS}	–	24	28	mA

1. Operating currents are measured at the following conditions:
   V_{AA} = V_{AA_PIX} = V_{DD_PLL}=2.8 V
   V_{DD} = V_{DD_IO}= 1.8 V
   V_{DD_SLVS} = 1.8 V
   PLL Enabled and PIXCLK = 74.25 MHz
   T_A = 25°C

Table 29. OPERATING CURRENT IN HiSPi (SLVS) OUTPUT AND LINEAR MODE

Definition	Condition	Symbol	Min	Typ	Max	Unit
Digital Operating Current	Streaming, 2048x1536 30fps	I_{DD}	–	252	278	mA
Analog Operating Current	Streaming, 2048x1536 30fps	I_{AA}	–	27	35	mA
Pixel Supply Current	Streaming, 2048x1536 30fps	I_{AA_PIX}	–	5	10	mA
PLL Supply Current	Streaming, 2048x1536 30fps	I_{DD_PLL}	–	8	12	mA
SLVS Supply Current	Streaming, 2048x1536 30fps	I_{DD_SLVS}	–	9	13	mA
Digital Operating Current	Streaming, 1080p60	I_{DD}	–	276	302	mA
Analog Operating Current	Streaming, 1080p60	I_{AA}	–	37	45	mA
Pixel Supply Current	Streaming, 1080p60	I_{AA_PIX}	–	7	12	mA

Table 29. OPERATING CURRENT IN HiSPi (SLVS) OUTPUT AND LINEAR MODE (continued)

Definition	Condition	Symbol	Min	Typ	Max	Unit
PLL Supply Current	Streaming, 1080p60	I_{DD_PLL}	–	8	12	mA
SLVS Supply Current	Streaming, 1080p60	I_{DD_SLVS}	–	9	13	mA

1. Operating currents are measured at the following conditions:
   V_{AA} = V_{AA_PIX}= V_{DD_PLL}=2.8 V
   V_{DD} =V_{DD_IO}= 1.8 V
   V_{DD_SLVS} = 0.4 V
   PLL Enabled and PIXCLK=74.25 MHz
   T_A = 25°C

Table 30. OPERATING CURRENT IN HiSPi (SLVS) OUTPUT AND HDR MODE

Definition	Condition	Symbol	Min	Typ	Max	Unit
Digital Operating Current	Streaming, 2048x1536 30fps	I_{DD}	–	317	358	mA
Analog Operating Current	Streaming, 2048x1536 30fps	I_{AA}	–	45	55	mA
Pixel Supply Current	Streaming, 2048x1536 30fps	I_{AA_PIX}	–	8	13	mA
PLL Supply Current	Streaming, 2048x1536 30fps	I_{DD_PLL}	–	8	12	mA
SLVS Supply Current	Streaming, 2048x1536 30fps	I_{DD_SLVS}	–	9	13	mA
Digital Operating Current	Streaming, 1080p60	I_{DD}	–	323	358	mA
Analog Operating Current	Streaming, 1080p60	I_{AA}	–	55	70	mA
Pixel Supply Current	Streaming, 1080p60	I_{AA_PIX}	–	9	14	mA
PLL Supply Current	Streaming, 1080p60	I_{DD_PLL}	–	8	12	mA
SLVS Supply Current	Streaming, 1080p60	I_{DD_SLVS}	–	9	13	mA

1. Operating currents are measured at the following conditions:
   VAA=VAA_PIX= VDD_PLL=2.8 V
   VDD = VDD_IO= 1.8 V
   VDD_SLVS = 0.4 V
   PLL Enabled and PIXCLK=74.25 MHz
   T_A = 25°C

HiSPi Electrical Specifications

The ON Semiconductor AR0331 sensor supports both SLVS and HiVCM HiSPi modes. Please refer to the High-Speed Serial Pixel (HiSPi) Interface Physical Layer Specification v2.00.00 for electrical definitions, specifications, and timing information. The V_{DD_SLVS} supply in this datasheet corresponds to V_{DD_TX} in the HiSPi Physical Layer Specification. Similarly, V_{DD} is equivalent to V_{DD_HiSPi} as referenced in the specification. The DLL as implemented on AR0331 is limited in the number of available delay steps and differs from the HiSPi specification as described in this section.

Table 31. CHANNEL SKEW

(Measurement Conditions: VDD_HiSPi = 1.8 V; VDD_HiSPi_TX = 0.8 V; Data Rate = 480 Mbps; DLL set to 0)

Data Lane Skew in Reference to Clock	tCHSKEW1PHY	−150	ps

Table 32. CLOCK DLL STEPS

(Measurement Conditions: VDD_HiSPi = 1.8 V; VDD_HiSPi_TX = 0.8 V; Data DLL set to 0)

Clock DLL Step	1	2	3	4	5	6
Delay at 660 Mbps	0.25	0.375	0.5	0.625	0.75	UI
Eye_opening at 660 Mbps	0.85	0.78	0.71	0.71	0.69	UI

1. The Clock DLL Steps 6 and 7 are not recommended by ON Semiconductor for the AR0331.

Table 33. DATA DLL STEPS

(Measurement Conditions: VDD_HiSPi = 1.8 V;VDD_HiSPi_TX = 0.8 V; Data DLL set to 0)

Clock DLL Step	1	2	4	6	Step
Delay at 660 Mbps	0.25	0.375	0.625	0.875	UI
Eye opening at 660 Mbps	0.79	0.84	0.71	0.61	UI
Eye opening at 360 MHz	0.85	0.83	0.82	0.77	UI

1. The Data DLL Steps 3, 5, and 7 are not recommended by ON Semiconductor for the AR0331.

POWER-ON RESET AND STANDBY TIMING

Power-Up Sequence

The recommended power-up sequence for the AR0331 is shown in Figure 46. The available power supplies (VDD_IO, VDD, VDD_SLVS, VDD_PLL, VAA, VAA_PIX) must have the separation specified below.

1. Turn on VDD_PLL power supply
2. After 100 µs, turn on VAA and VAA_PIX power supply
3. After 100 µs, turn on VDD_IO power supply
4. After 100 µs, turn on VDD power supply
5. After 100 µs, turn on VDD_SLVS power supply
6. After the last power supply is stable, enable EXTCLK
7. Assert RESET_BAR for at least 1 ms. The parallel interface will be tri-stated during this time
8. Wait 150000 EXTCLKs (for internal initialization into software standby
9. Configure PLL, output, and image settings to desired values
10. Wait 1ms for the PLL to lock
11. Set streaming mode (R0x301a[2] = 1)

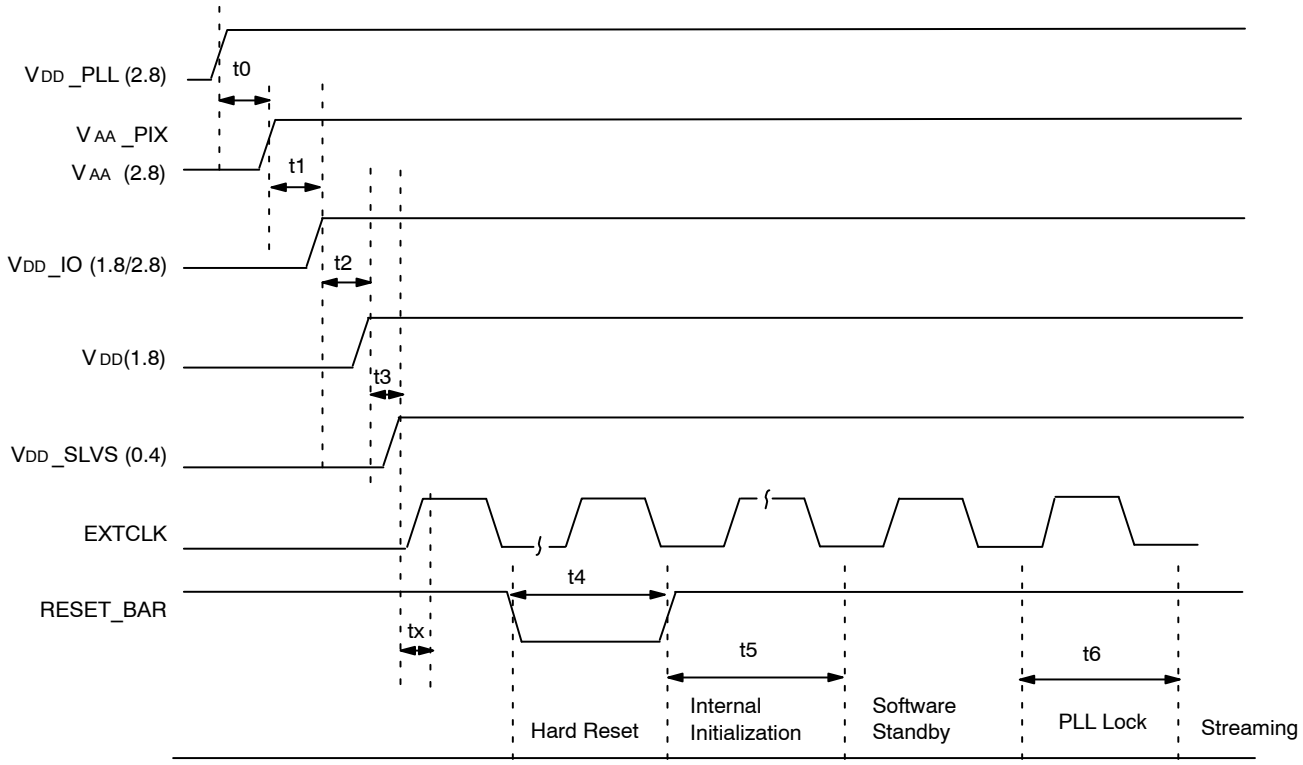


Figure 46. Power Up

Table 34. POWER UP SEQUENCE

Definition	Symbol	Minimum	Typical	Maximum	Unit
VDD_PLL to VAA/VAA_PIX (Note 3)	t0	0	100	–	µS
VAA/VAA_PIX to VDD_IO	t1	0	100	–	µS
VDD_IO to VDD	t2	0	100	–	µS
VDD to VDD_SLVS	t3	0	100	–	µS
Xtal Settle Time	tx	–	30 (Note 1)	–	mS
Hard Reset	t4	1 (Note 2)	–	–	mS
Internal Initialization	t5	150000	–	–	EXTCLKS
PLL Lock Time	t6	1	–	–	mS

1. Xtal settling time is component-dependent, usually taking about 10 – 100 mS.
2. Hard reset time is the minimum time required after power rails are settled. In a circuit where Hard reset is held down by RC circuit, then the RC time must include the all power rail settle time and Xtal settle time.
3. It is critical that VDD_PLL is not powered up after the other power supplies. It must be powered before or at least at the same time as the others. If the case happens that VDD_PLL is powered after other supplies then sensor may have functionality issues and will experience high current draw on this supply.

Power-Down Sequence

The recommended power-down sequence for the AR0331 is shown in Figure 47. The available power supplies (VDD_IO, VDD, VDD_SLVS, VDD_PLL, VAA, VAA_PIX) must have the separation specified below.

1. Disable streaming if output is active by setting standby R0x301a[2] = 0
2. The soft standby state is reached after the current row or frame, depending on configuration, has ended
3. Turn off VDD_SLVS
4. Turn off VDD
5. Turn off VDD_IO
6. Turn off VAA/VAA_PIX
7. Turn off VDD_PLL

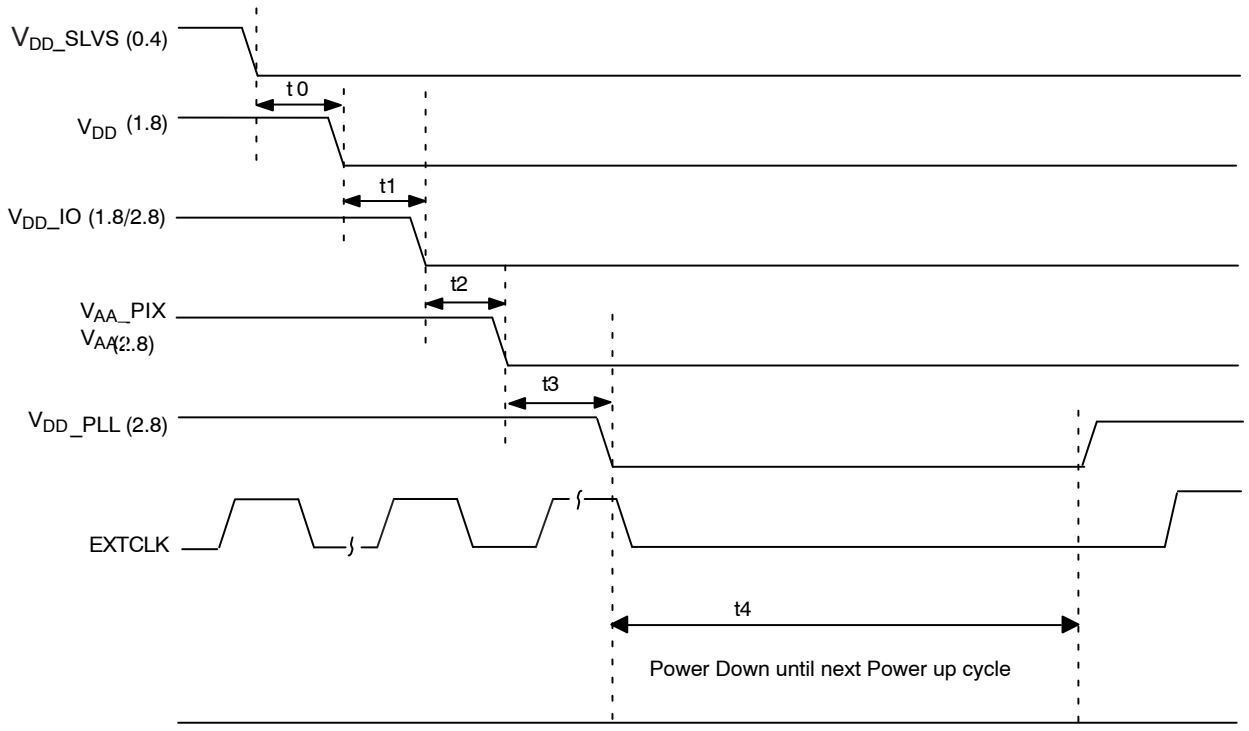


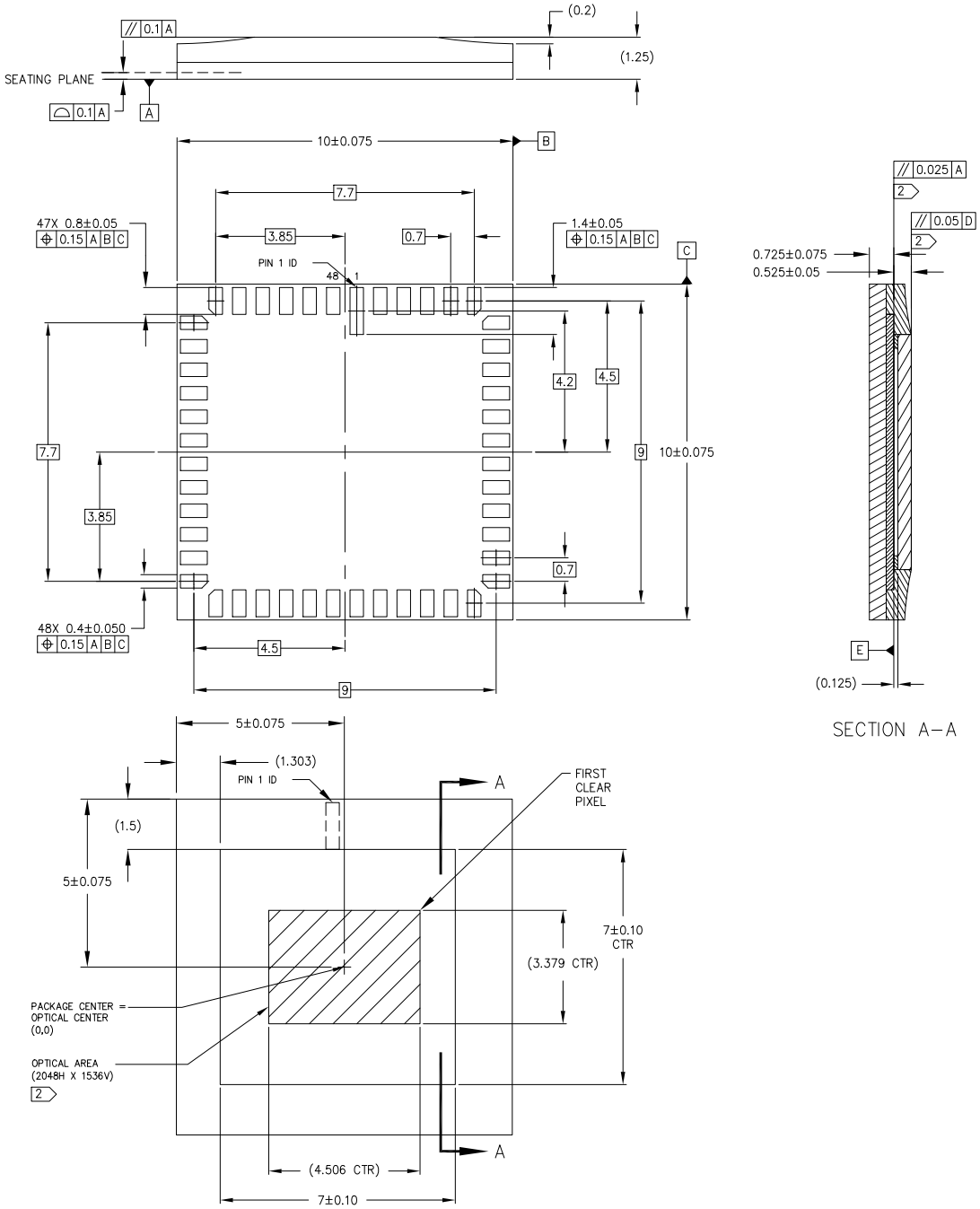
Figure 47. Power Down

Table 35. POWER DOWN SEQUENCE

Definition	Symbol	Minimum	Typical	Maximum	Unit
V_{DD}_SLVS to V_{DD}	t0	0	–	–	µs
V_{DD} to V_{DD}_IO	t1	0	–	–	µs
V_{DD}_IO to V_{AA}/V_{AA}_PIX	t2	0	–	–	µs
V_{AA}/V_{AA}_PIX to V_{DD}_PLL	t3	0	–	–	µs
PwrDn until Next PwrUp Time	t4	100	–	–	ms

1. t4 is required between power down and next power up time; all decoupling caps from regulators must be completely discharged.

ILCC48 10 x 10
CASE 847AG
ISSUE O



NOTES	
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IBGA63 9.5 x 9.5
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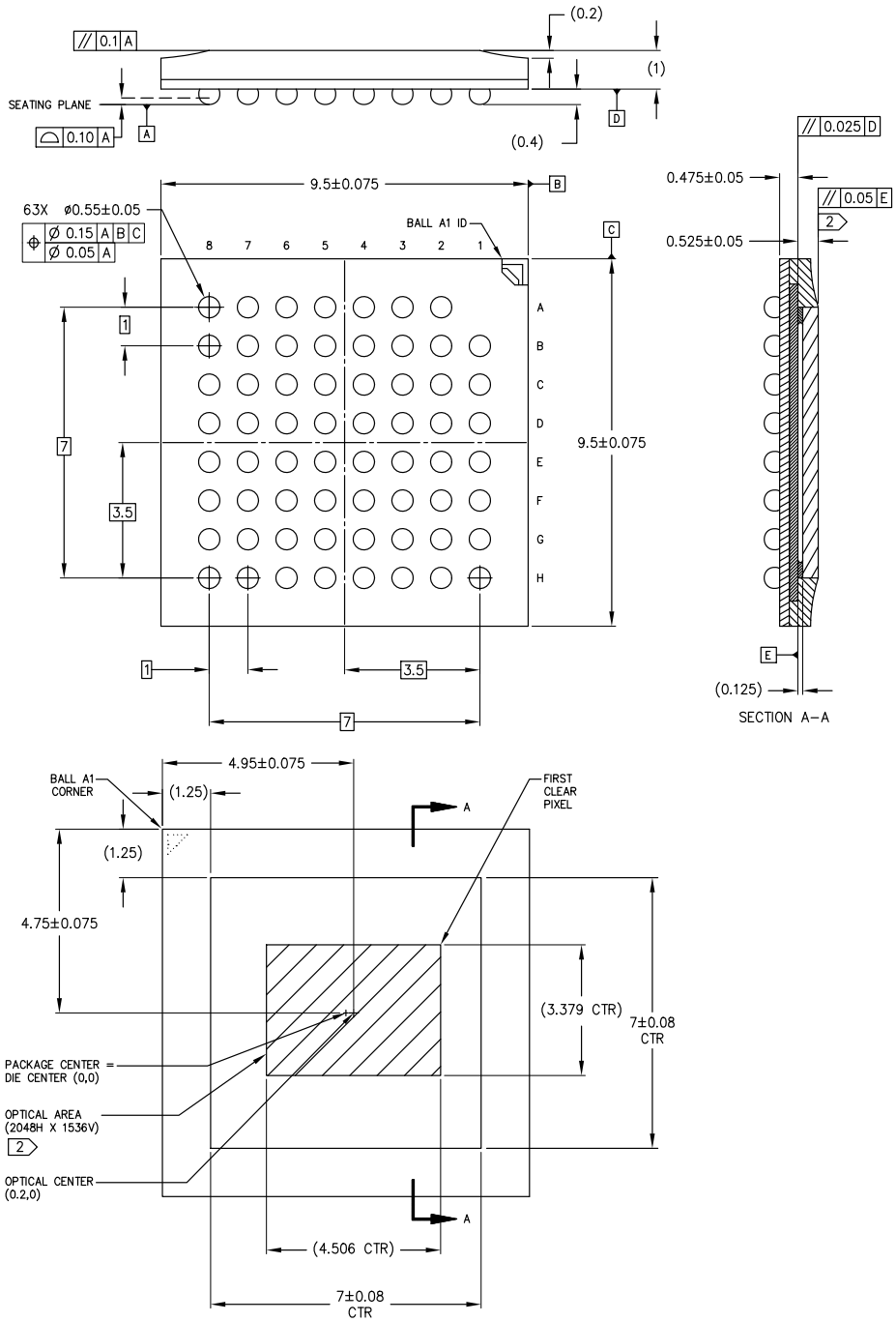
ISSUE O



NOTES	
1	DIMENSIONS IN MM. DIMENSIONS IN ( ) ARE FOR REFERENCE ONLY.
2	MAXIMUM ROTATION OF OPTICAL AREA RELATIVE TO PACKAGE EDGES: 1°. MAXIMUM TILT OF OPTICAL AREA RELATIVE TO SUBSTRATE PLANE D: 25um. MAXIMUM TILT OF COVER GLASS RELATIVE TO OPTICAL AREA PLANE E: 50um.

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