

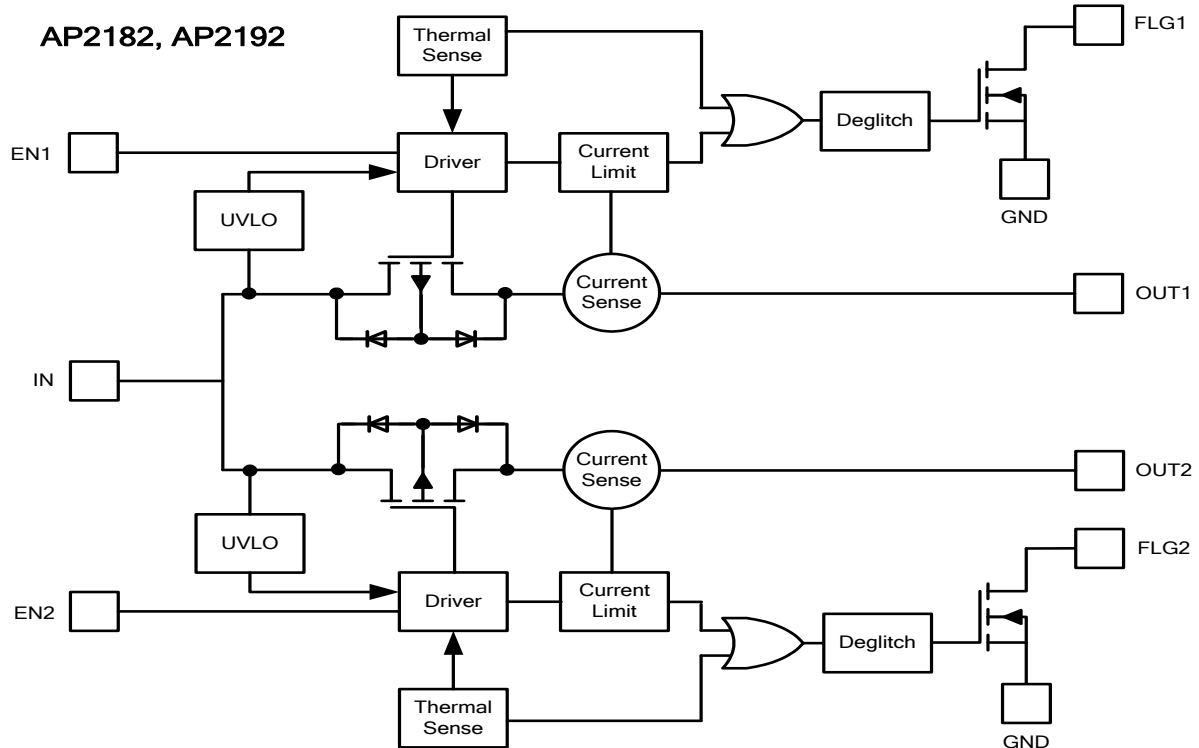
Available Options

Part Number	Channel	Enable Pin (EN)	Current Limit (typ)	Recommended Maximum Continuous Load Current
AP2182	2	Active Low	2.1A	1.5A
AP2192	2	Active High	2.1A	1.5A

Pin Descriptions

Pin Name	Pin Number		Function
	SO-8	MSOP-8EP	
GND	1	1	Ground
IN	2	2	Voltage input pin
EN1	3	3	Switch 1 enable input, active low (AP2182) or active high (AP2192)
EN2	4	4	Switch 2 enable input, active low (AP2182) or active high (AP2192)
FLG2	5	5	Switch 2 over-current and over-temperature fault report; open-drain flag is active low when triggered
OUT2	6	6	Switch 2 voltage output pin
OUT1	7	7	Switch 1 voltage output pin
FLG1	8	8	Switch 1 over-current and over-temperature fault report; open-drain flag is active low when triggered
Exposed Tab	—	Exposed Tab	Exposed pad. It should be connected to GND and thermal mass for enhanced thermal impedance. It should not be used as electrical ground conduction path.

Functional Block Diagram



Absolute Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Symbol	Parameter	Rating	Unit
ESD HBM	Human Body Model ESD Protection	3	kV
ESD MM	Machine Model ESD Protection	300	V
V _{IN}	Input Voltage	6.5	V
V _{OUT}	Output Voltage	V _{IN} +0.3	V
V _{EN} , V _{FLG}	Enable Voltage	6.5	V
I _{LOAD}	Maximum Continuous Load Current	Internal Limited	A
T _{J(MAX)}	Maximum Junction Temperature	+150	°C
T _{ST}	Storage Temperature Range (Note 4)	-65 to +150	°C

Caution: Stresses greater than the 'Absolute Maximum Ratings' specified above, may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions exceeding those indicated in this specification is not implied. Device reliability may be affected by exposure to absolute maximum rating conditions for extended periods of time.
Semiconductor devices are ESD sensitive and may be damaged by exposure to ESD events. Suitable ESD precautions should be taken when handling and transporting these devices.

Note: 4. UL Recognized Rating from -30°C to +70°C (Diodes qualified T_{ST} from -65°C to +150°C).

Recommended Operating Conditions (@T_A = +25°C, unless otherwise specified.)

Symbol	Parameter	Min	Max	Unit
V _{IN}	Input Voltage	2.7	5.5	V
I _{OUT}	Output Current	0	1.5	A
V _{IL}	EN Input Logic Low Voltage	0	0.8	V
V _{IH}	EN Input Logic High Voltage	2	V _{IN}	V
T _A	Operating Ambient Temperature	-40	+85	°C

Electrical Characteristics (@T_A = +25°C, V_{IN} = +5V, unless otherwise specified.)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V _{UVLO}	Input UVLO	R _{LOAD} = 1kΩ	1.6	1.9	2.5	V
I _{SHDN}	Input Shutdown Current	Disabled, I _{OUT} = 0	-	0.5	1	μA
I _Q	Input Quiescent Current, Dual	Enabled, I _{OUT} = 0	-	100	160	μA
I _{LEAK}	Input Leakage Current	Disabled, OUT Grounded	-	-	1	μA
I _{REV}	Reverse Leakage Current	Disabled, V _{IN} = 0V, V _{OUT} = 5V, I _{REV} at V _{IN}	-	1	-	μA
R _{DS(ON)}	Switch On-Resistance	V _{IN} = 5V, MSOP-8EP, -40°C ≤ T _A ≤ +85°C	-	115	150	mΩ
		I _{OUT} = 0.5A, SO-8, -40°C ≤ T _A ≤ +85°C	-	120	160	mΩ
		V _{IN} = 3.3V, I _{OUT} = 0.5A, -40°C ≤ T _A ≤ +85°C	-	140	180	mΩ
I _{SHORT}	Short-Circuit Current Limit	Enabled into short circuit, C _L = 68μF	-	2.0	-	A
I _{LIMIT}	Over-Load Current Limit	V _{IN} = 5V, V _{OUT} = 4.5V, C _L = 68μF, -40°C ≤ T _A ≤ +85°C	1.6	2.1	2.6	A
I _{TRIG}	Current Limiting Trigger Threshold	V _{IN} = V _{EN} , Output Current Slew Rate (<100AWS), C _L = 68μF	-	3.0	-	A
V _{IL}	EN Input Logic Low Voltage	V _{IN} = 2.7V to 5.5V	-	-	0.8	V
V _{IH}	EN Input Logic High Voltage	V _{IN} = 2.7V to 5.5V	2	-	-	V
I _{SINK}	EN Input Leakage	V _{EN} = 5V	-	-	1	μA
T _{D(ON)}	Output Turn-On Delay Time	C _L = 1μF, R _{LOAD} = 10Ω	-	0.05	-	ms
T _R	Output Turn-On Rise Time	C _L = 1μF, R _{LOAD} = 10Ω	-	0.6	1.5	ms
T _{D(OFF)}	Output Turn-Off Delay Time	C _L = 1μF, R _{LOAD} = 10Ω	-	0.01	-	ms
T _F	Output Turn-Off Fall Time	C _L = 1μF, R _{LOAD} = 10Ω	-	0.05	0.1	ms
R _{FLG}	FLG Output FET On-Resistance	I _{FLG} = 10mA	-	30	50	Ω
T _{BLANK}	FLG Blanking Time	C _{IN} = 10μF, C _L = 68μF	4	7	15	ms
T _{SHDN}	Thermal Shutdown Threshold	Enabled, R _{LOAD} = 1kΩ	-	+140	-	°C
T _{HYS}	Thermal Shutdown Hysteresis	-	-	+25	-	°C
θ _{JA}	Thermal Resistance Junction-to-Ambient	SO-8 (Note 5)	-	110	-	°C/W
		MSOP-8EP (Note 6)	-	60	-	°C/W

Notes: 5. Test condition for SO-8: Device mounted on FR-4 2-layer board, 2oz copper, with minimum recommended pad layout.
6. Test condition for MSOP-8EP: Device mounted on FR-4 2-layer board, 2oz copper, with minimum recommended pad on top layer and 3 vias to bottom layer ground plane.

Typical Performance Characteristics

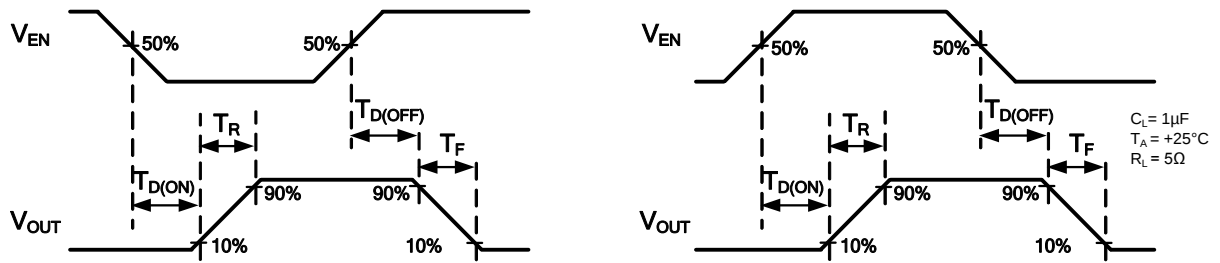
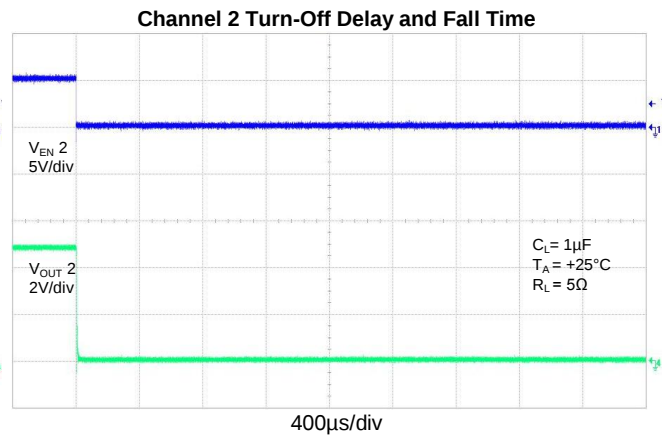
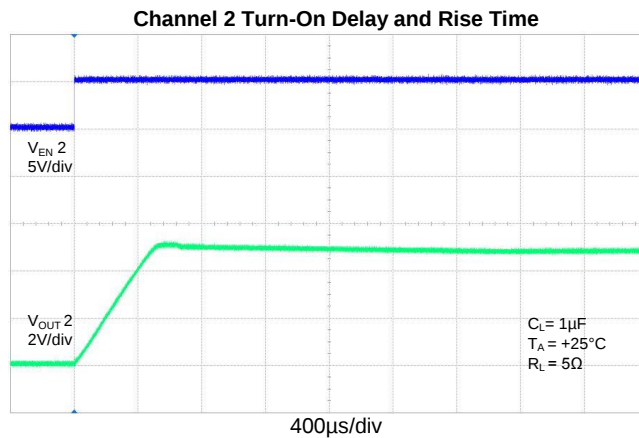
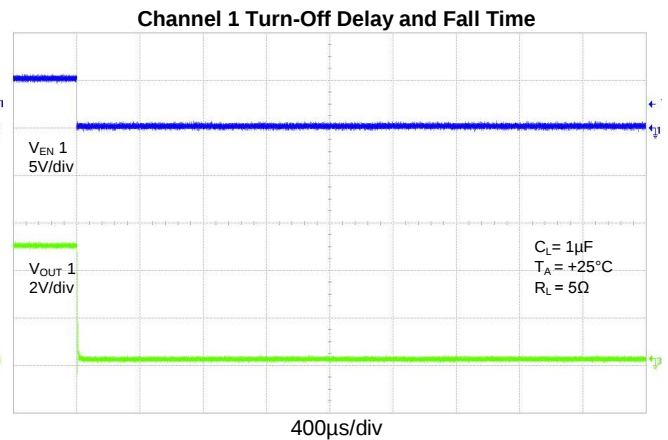
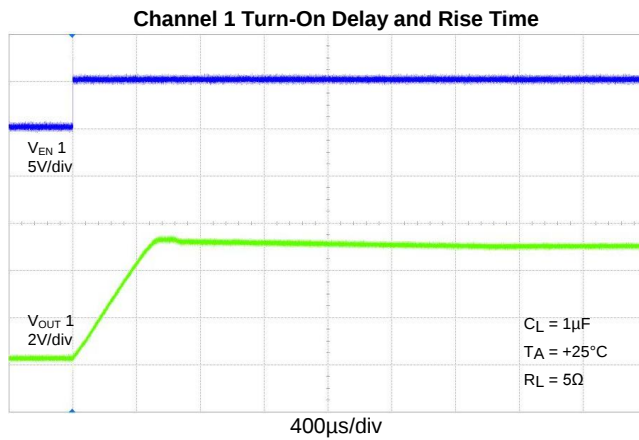


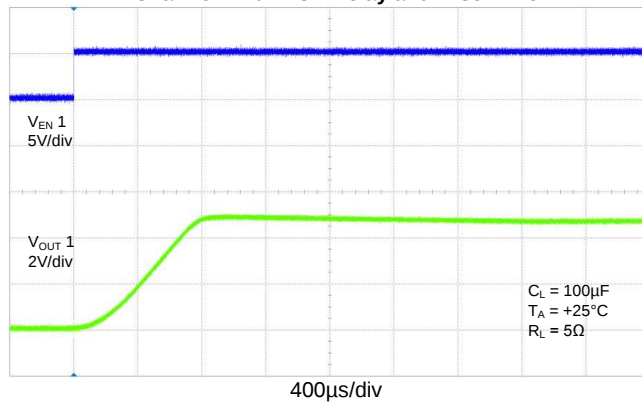
Figure 1 Voltage Waveforms: AP2182 (Left), AP2192 (Right)

All Enable Plots are for AP2192 Active High

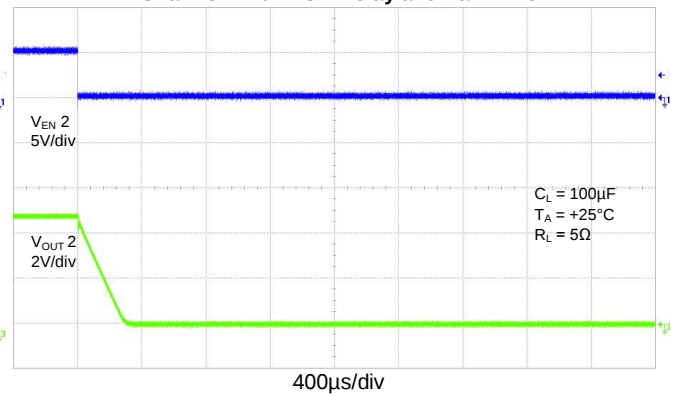


Typical Performance Characteristics (Cont.)

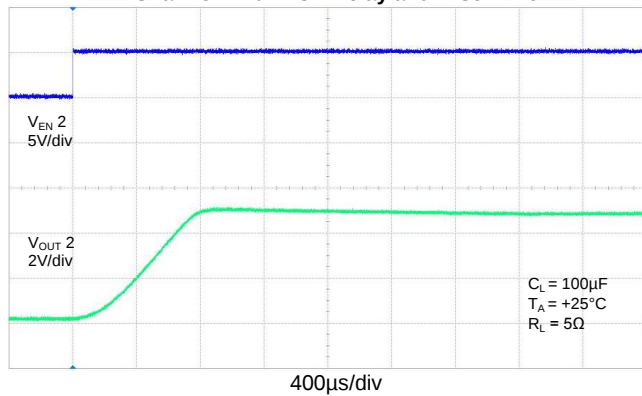
Channel 1 Turn-On Delay and Rise Time



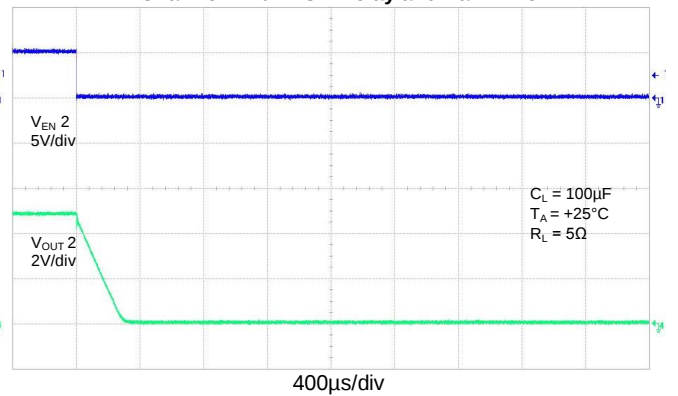
Channel 1 Turn-Off Delay and Fall Time



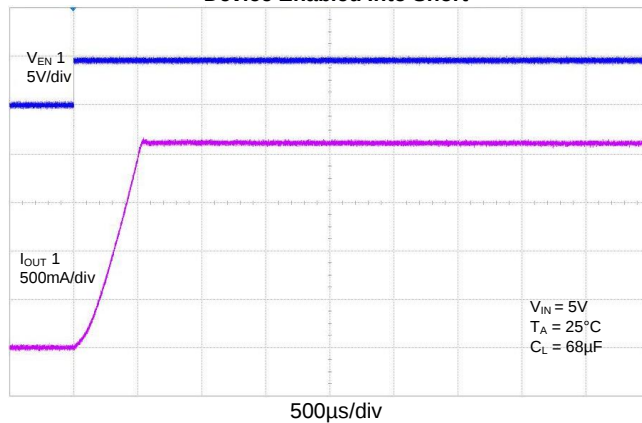
Channel 2 Turn-On Delay and Rise Time



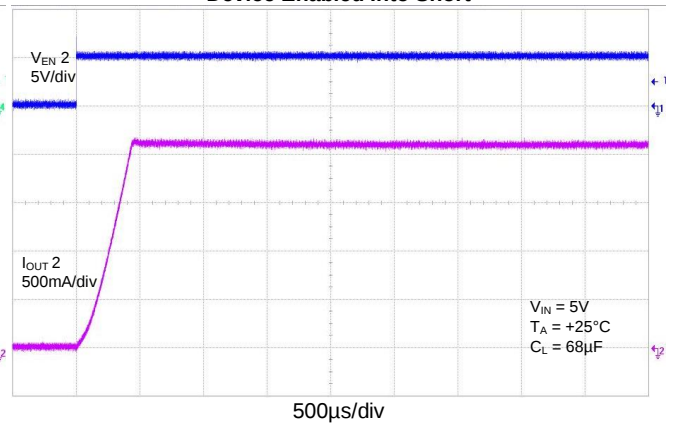
Channel 2 Turn-Off Delay and Fall Time



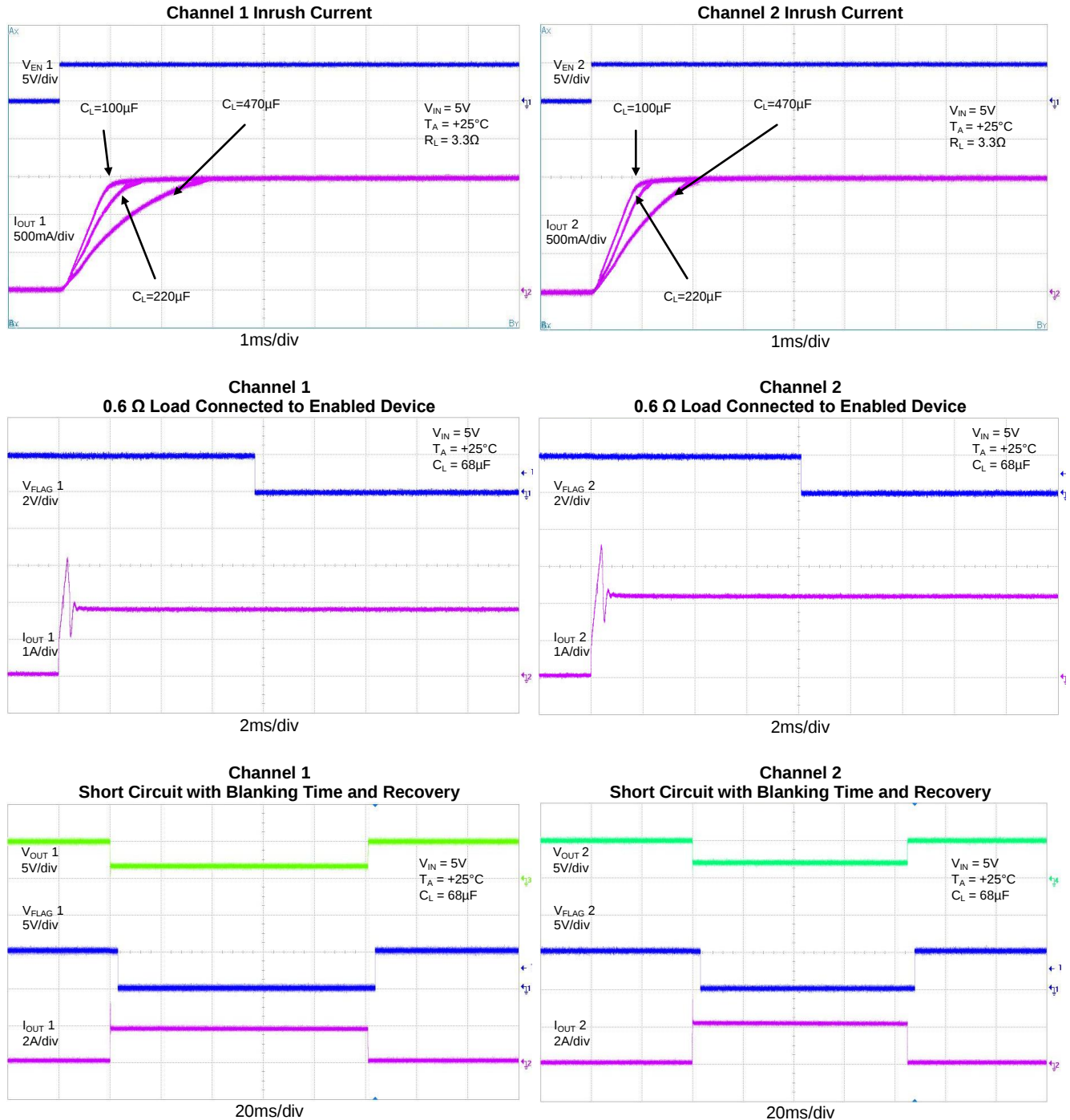
Channel 1 Short Circuit Current,
Device Enabled Into Short



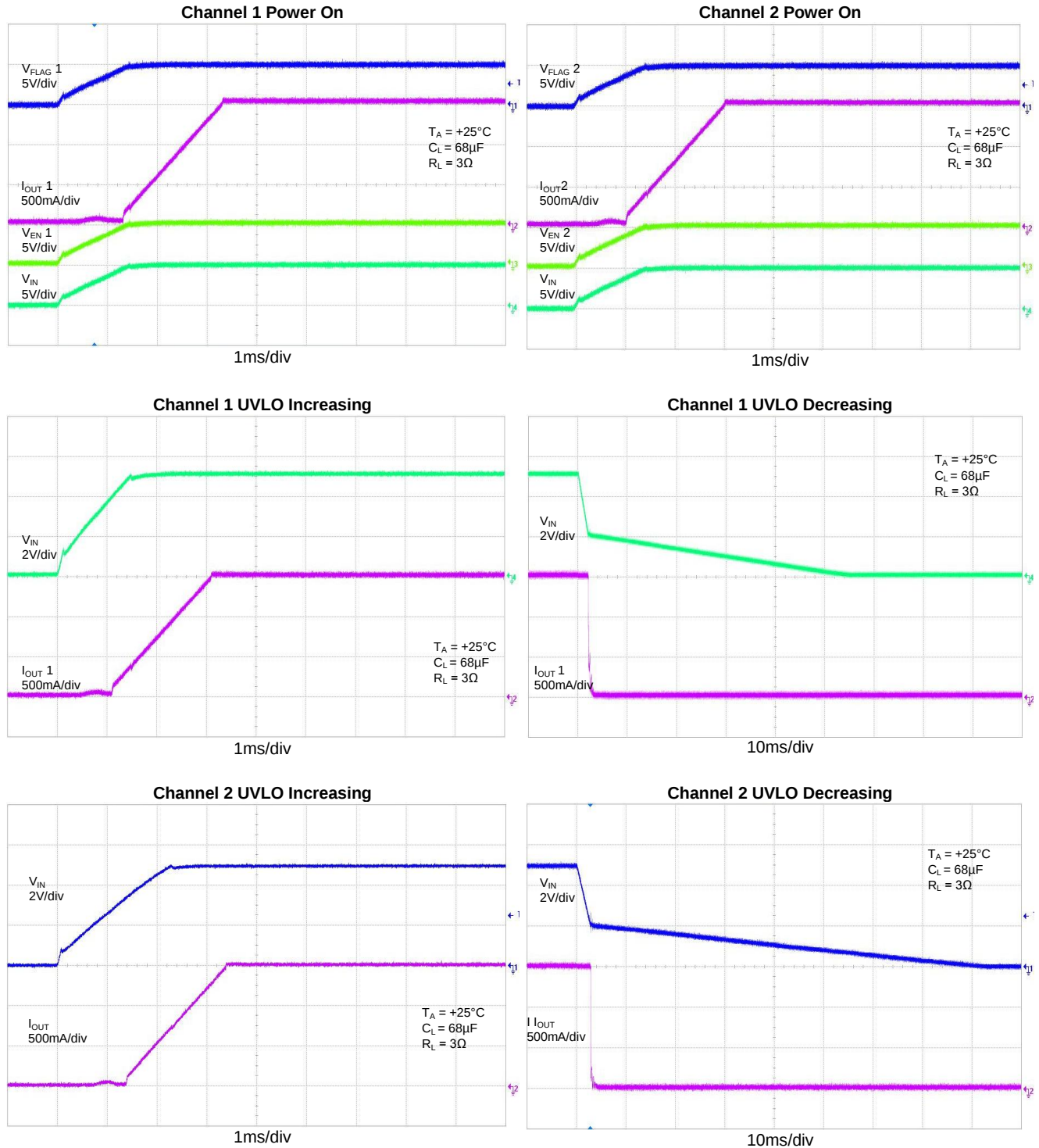
Channel 2 Short Circuit Current,
Device Enabled Into Short



Typical Performance Characteristics (Cont.)

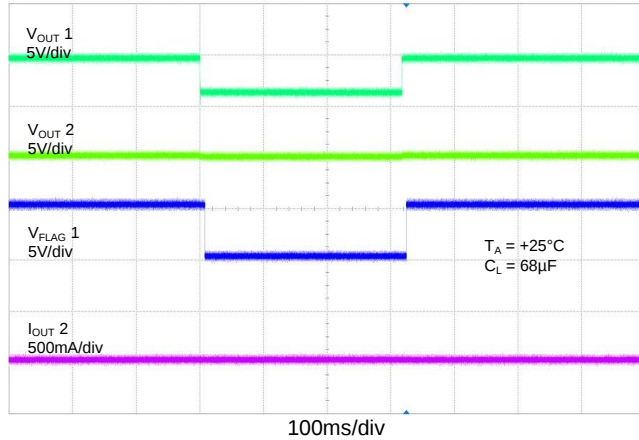


Typical Performance Characteristics (Cont.)

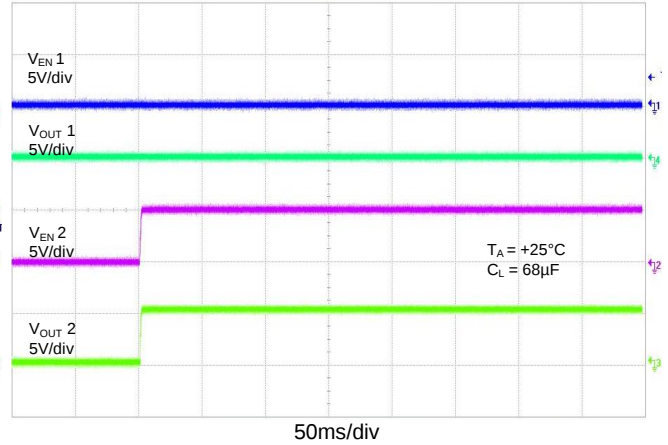


Typical Performance Characteristics (Cont.)

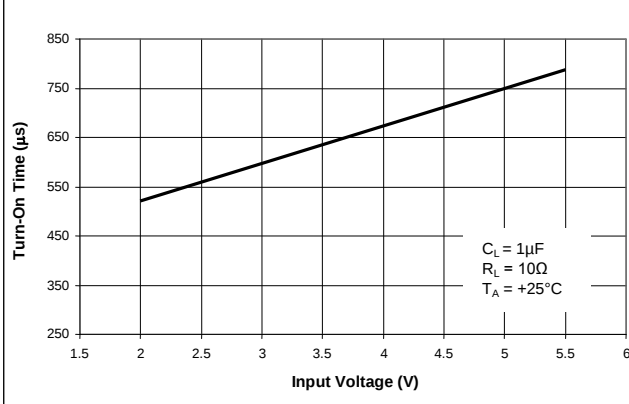
Channel 1 Enabled and Shorted with Channel 2 Disabled



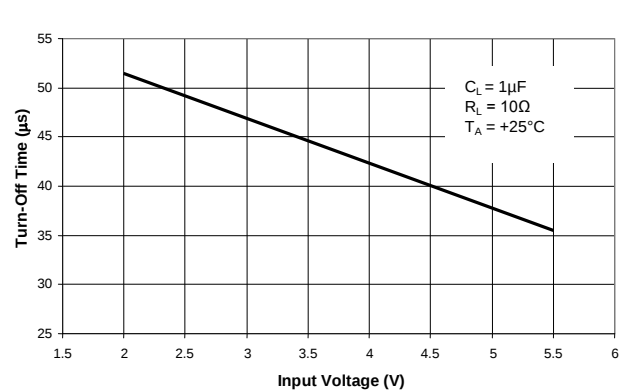
Channel 1 Disabled and Channel 2 Enabled



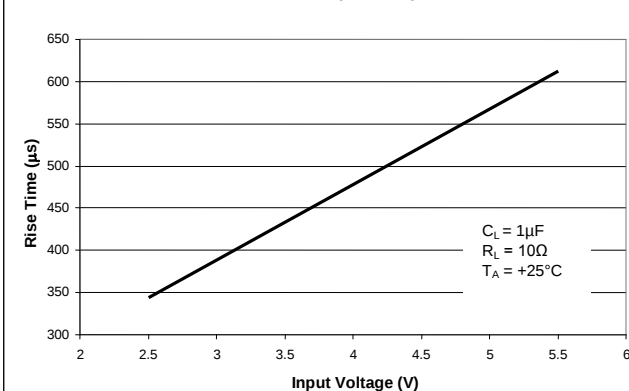
Turn-On Time vs. Input Voltage



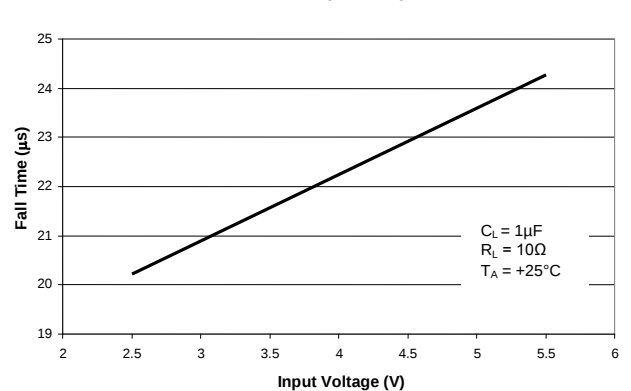
Turn-Off Time vs. Input Voltage



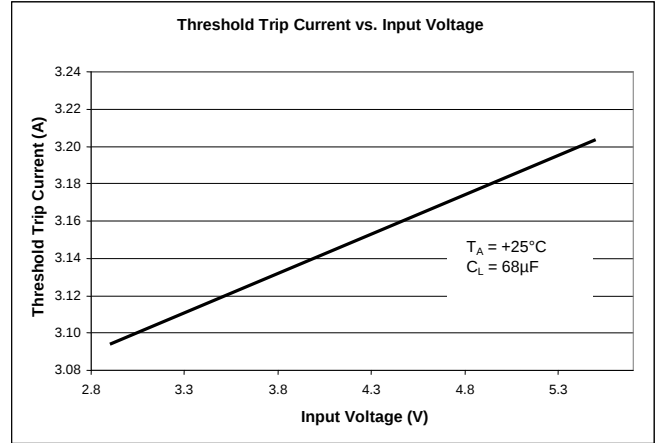
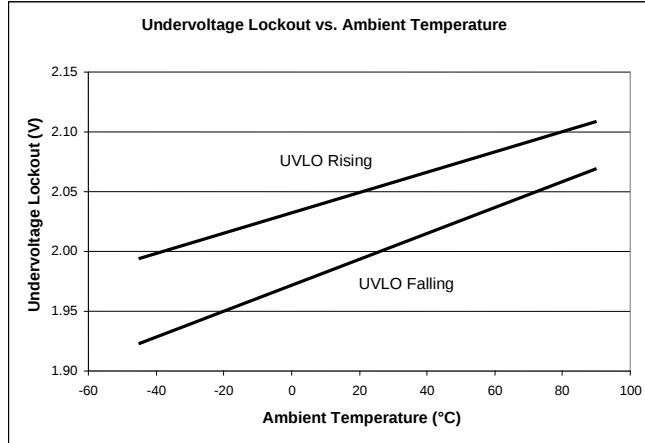
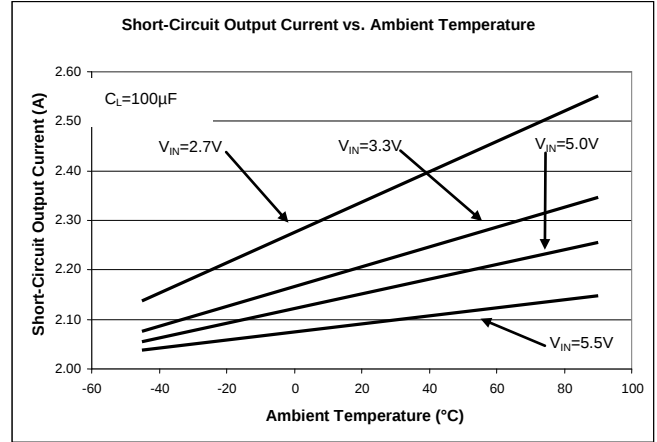
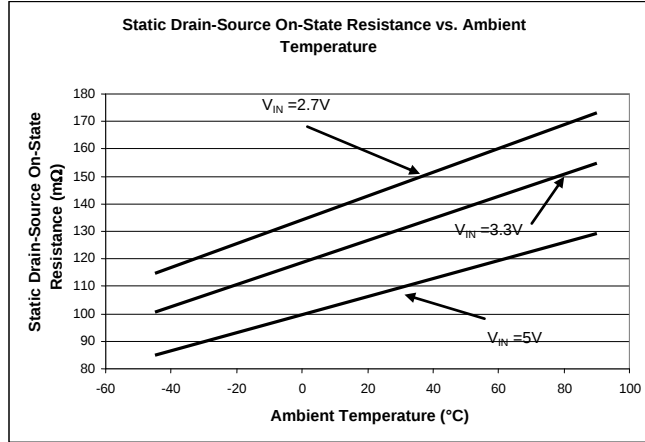
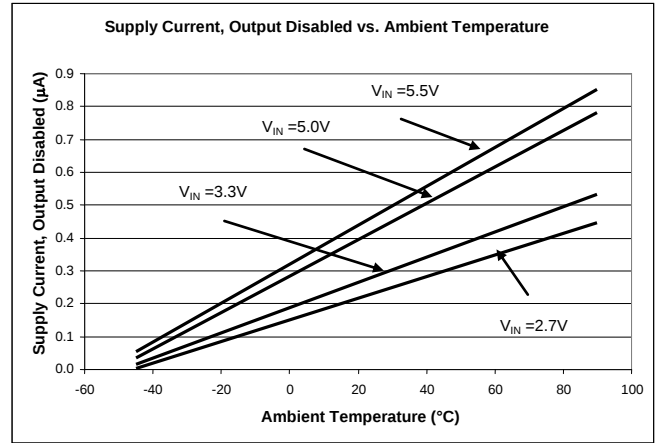
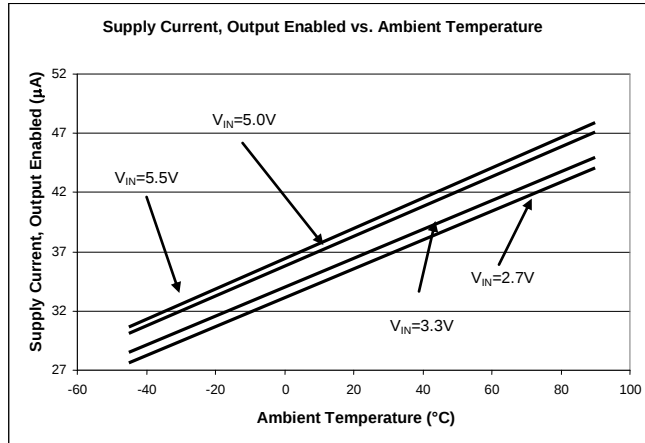
Rise Time vs. Input Voltage



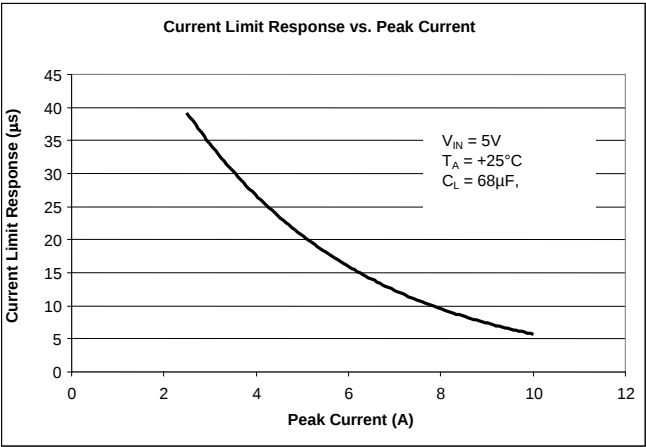
Fall Time vs. Input Voltage



Typical Performance Characteristics (Cont.)



Typical Performance Characteristics (Cont.)



Application Information

Power Supply Considerations

A 0.01-μF to 0.1-μF X7R or X5R ceramic bypass capacitor between IN and GND, close to the device, is recommended. Placing a high-value electrolytic capacitor on the input and output pin(s) is recommended when the output load is heavy. This precaution reduces power-supply transients that may cause ringing on the input. Additionally, bypassing the output with a 0.01-μF to 0.1-μF ceramic capacitor improves the immunity of the device to short-circuit transients.

Over-Current and Short Circuit Protection

An internal sensing FET is employed to check for over-current conditions. Unlike current-sense resistors, sense FETs do not increase the series resistance of the current path. When an overcurrent condition is detected, the device maintains a constant output current and reduces the output voltage accordingly. Complete shutdown occurs only if the fault stays long enough to activate thermal limiting.

Three possible overload conditions can occur. In the first condition, the output has been shorted to GND before the device is enabled or before V_{IN} has been applied. The AP2182/AP2192 senses the short circuit and immediately clamps output current to a certain safe level namely I_{LIMIT} .

In the second condition, an output short or an overload occurs while the device is enabled. At the instance the overload occurs, higher current may flow for a very short period of time before the current limit function can react. After the current limit function has tripped (reached the over-current trip threshold), the device switches into current limiting mode and the current is clamped at I_{LIMIT} .

In the third condition, the load has been gradually increased beyond the recommended operating current. The current is permitted to rise until the current-limit threshold (I_{TRIG}) is reached or until the thermal limit of the device is exceeded. The AP2182/AP2192 is capable of delivering current up to the current-limit threshold without damaging the device. Once the threshold has been reached, the device switches into its current limiting mode and is set at I_{LIMIT} .

FLG Response

When an over-current or over-temperature shutdown condition is encountered, the FLG open-drain output goes active low after a nominal 7-ms deglitch timeout. The FLG output remains low until both over-current and over-temperature conditions are removed. Connecting a heavy capacitive load to the output of the device can cause a momentary over-current condition, which does not trigger the FLG due to the 7-ms deglitch timeout. The AP2182/AP2192 is designed to eliminate false over-current reporting without the need of external components to remove unwanted pulses.

Power Dissipation and Junction Temperature

The low on-resistance of the internal MOSFET allows the small surface-mount packages to pass large current. Using the maximum operating ambient temperature (T_A) and $R_{DS(ON)}$, the power dissipation can be calculated by:

$$P_D = R_{DS(ON)} \times I^2$$

Finally, calculate the junction temperature:

$$T_J = P_D \times R_{\theta JA} + T_A$$

Where:

T_A = Ambient Temperature °C

$R_{\theta JA}$ = Thermal Resistance

P_D = Total Power Dissipation

Thermal Protection

Thermal protection prevents the IC from damage when heavy-overload or short-circuit faults are present for extended periods of time. The AP2182/AP2192 implements a thermal sensing to monitor the operating junction temperature of the power distribution switch. Once the die temperature rises to approximately 140°C due to excessive power dissipation in an over-current or short-circuit condition the internal thermal sense circuitry turns the power switch off, thus preventing the power switch from damage. Hysteresis is built into the thermal sense circuit allowing the device to cool down approximately 25°C before the switch turns back on. The switch continues to cycle in this manner until the load fault or input power is removed. The FLG open-drain output is asserted when an over-temperature shutdown or over-current occurs with 7-ms deglitch.

Application Information (Cont.)

Under-Voltage Lockout (UVLO)

The Under-voltage lockout function (UVLO) keeps the internal power switch from being turned on until the power supply has reached at least 1.9V, even if the switch is enabled. Whenever the input voltage falls below approximately 1.9V, the power switch is quickly turned off. This facilitates the design of hot-insertion systems where it is not possible to turn off the power switch before input power is removed.

Host/Self-Powered HUBs

Hosts and self-powered hubs (SPH) have a local power supply that powers the embedded functions and the downstream ports (see Figure 2). This power supply must provide from 5.25V to 4.75V to the board side of the downstream connection under both full-load and no-load conditions. Hosts and SPHs are required to have current-limit protection and must report over-current conditions to the USB controller. Typical SPHs are desktop PCs, monitors, printers, and stand-alone hubs.

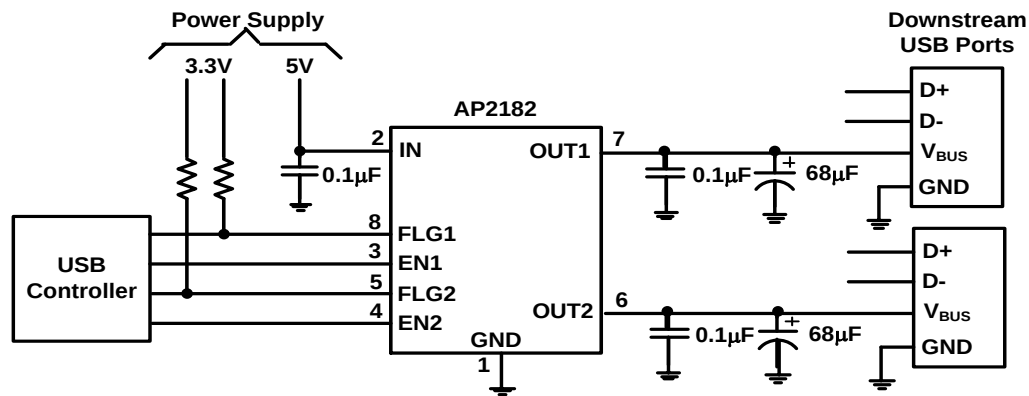


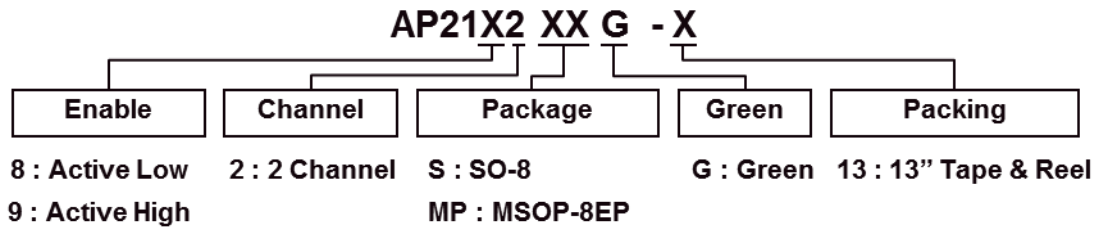
Figure 2 Typical Two-Port USB Host / Self-Powered Hub

Generic Hot-Plug Applications

In many applications it may be necessary to remove modules or pc boards while the main unit is still operating. These are considered hot-plug applications. Such implementations require the control of current surges seen by the main power supply and the card being inserted. The most effective way to control these surges is to limit and slowly ramp the current and voltage being applied to the card, similar to the way in which a power supply normally turns on. Due to the controlled rise times and fall times of the AP2182/AP2192, these devices can be used to provide a softer start-up to devices being hot-plugged into a powered system. The UVLO feature of the AP2182/AP2192 also ensures that the switch is off after the card has been removed, and that the switch is off during the next insertion.

By placing the AP2182/AP2192 between the V_{CC} input and the rest of the circuitry, the input power reaches these devices first after insertion. The typical rise time of the switch is approximately 1ms, providing a slow voltage ramp at the output of the device. This implementation controls system surge current and provides a hot-plugging mechanism for any device.

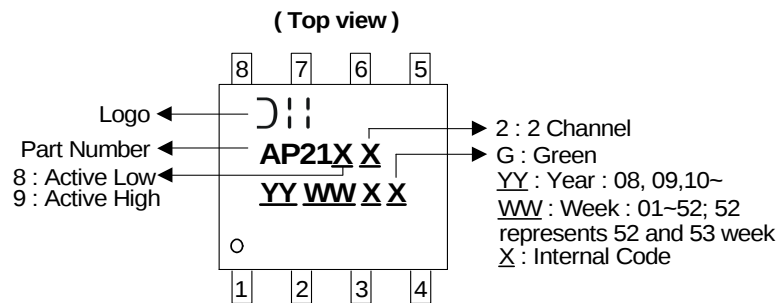
Ordering Information



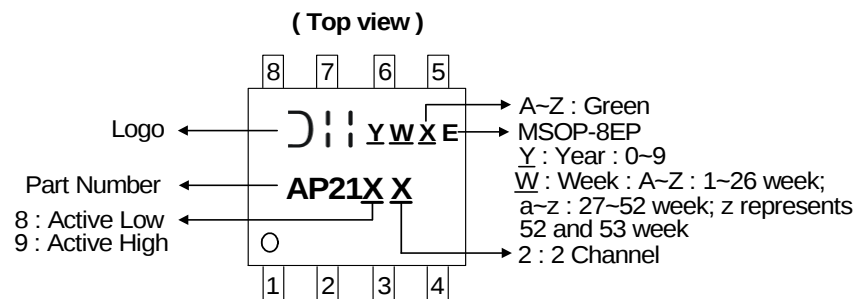
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			Quantity	Part Number Suffix
AP21X2SG-13	S	SO-8	2,500/Tape & Reel	-13
AP21X2MPG-13	MP	MSOP-8EP	2,500/Tape & Reel	-13

Marking Information

(1) SO-8



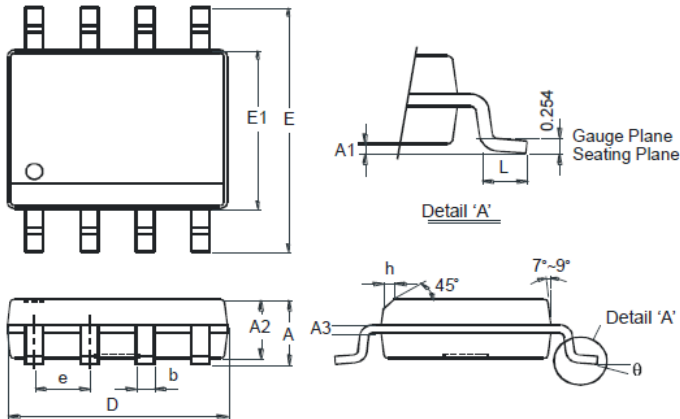
(2) MSOP-8EP



Package Outline Dimensions (All dimensions in mm.)

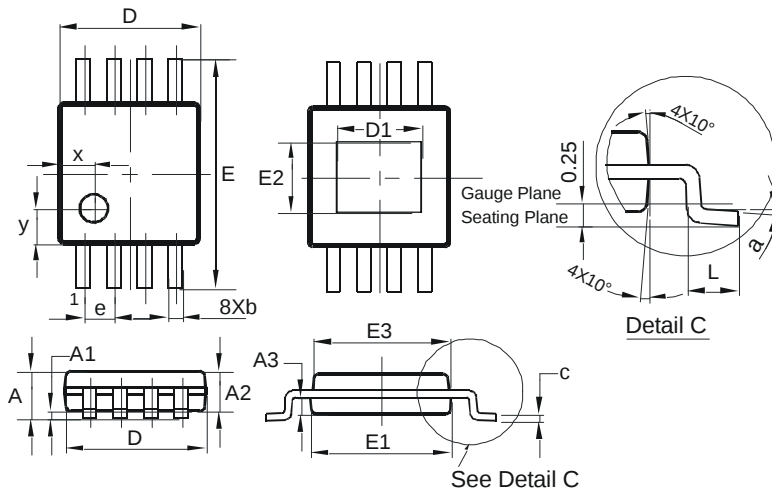
Please see <http://www.diodes.com/package-outlines.html> for the latest version.

(1) Package type: SO-8



SO-8		
Dim	Min	Max
A	-	1.75
A1	0.10	0.20
A2	1.30	1.50
A3	0.15	0.25
b	0.3	0.5
D	4.85	4.95
E	5.90	6.10
E1	3.85	3.95
e	1.27 Typ	
h	-	0.35
L	0.62	0.82
θ	0°	8°
All Dimensions in mm		

(2) Package type: MSOP-8EP

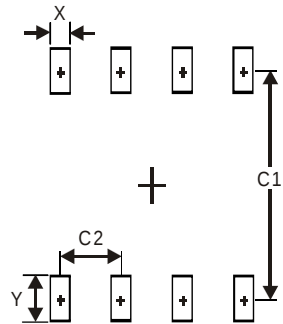


MSOP-8EP			
Dim	Min	Max	Typ
A	-	1.10	-
A1	0.05	0.15	0.10
A2	0.75	0.95	0.86
A3	0.29	0.49	0.39
b	0.22	0.38	0.30
c	0.08	0.23	0.15
D	2.90	3.10	3.00
D1	1.60	2.00	1.80
E	4.70	5.10	4.90
E1	2.90	3.10	3.00
E2	1.30	1.70	1.50
E3	2.85	3.05	2.95
e	-	-	0.65
L	0.40	0.80	0.60
a	0°	8°	4°
x	-	-	0.750
y	-	-	0.750
All Dimensions in mm			

Suggested Pad Layout

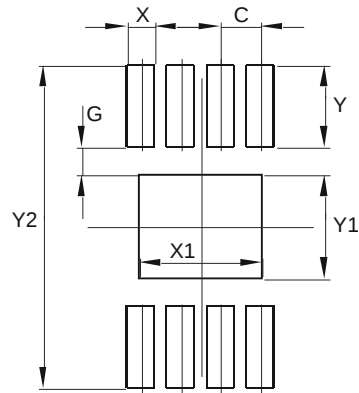
Please see <http://www.diodes.com/package-outlines.html> for the latest version.

(1) Package type: SO-8



Dimensions	Value (in mm)
X	0.60
Y	1.55
C1	5.4
C2	1.27

(2) Package type: MSOP-8EP



Dimensions	Value (in mm)
C	0.650
G	0.450
X	0.450
X1	2.000
Y	1.350
Y1	1.700
Y2	5.300

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