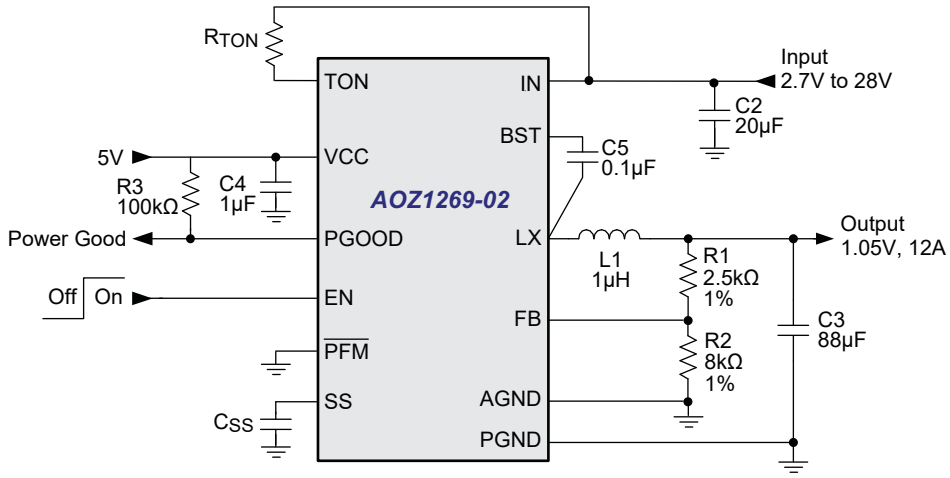
Typical Application

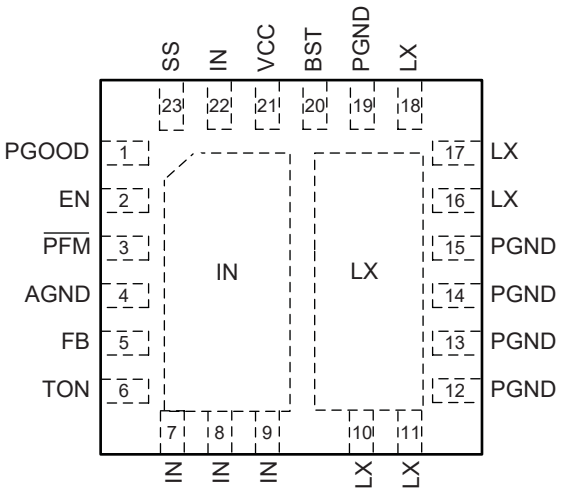


Ordering Information

Part Number	Ambient Temperature Range	Package	Environmental
AOZ1269QI-02	-40°C to +85°C	23-Pin 4mm x 4mm QFN	Green Product

AOS Green Products use reduced levels of Halogens, and are also RoHS compliant.
Please visit www.aosmd.com/media/AOSGreenPolicy.pdf for additional information.

Pin Configuration



23-Pin 4mm x 4mm QFN
(Top View)

Pin Description

Pin Number	Pin Name	Pin Function
1	PGOOD	Power Good Signal Output. PGOOD is an open-drain output used to indicate the status of the output voltage. It is internally pulled low when the output voltage is 18% lower than the nominal regulation voltage for 50µs (typical time) or 20% higher than the nominal regulation voltage. PGOOD is pulled low during soft-start and shut down.
2	EN	Enable Input. The AOZ1269-02 is enabled when EN is pulled high. The device shuts down when EN is pulled low.
3	$\overline{\text{PFM}}$	$\overline{\text{PFM}}$ Selection Input. Connect $\overline{\text{PFM}}$ pin to VCC/VIN for forced PWM operation. Connect $\overline{\text{PFM}}$ pin to ground for $\overline{\text{PFM}}$ operation to improve light load efficiency.
4	AGND	Analog Ground.
5	FB	Feedback Input. Adjust the output voltage with a resistive voltage-divider between the regulator's output and AGND.
6	TON	On-Time Setting Input. Connect a resistor between VIN and TON to set the on time.
7, 8, 9, 22	IN	Supply Input. IN is the regulator input. All IN pins must be connected together.
12, 13, 14, 15, 19	PGND	Power Ground.
10, 11, 16, 17, 18	LX	Switching Node.
20	BST	Bootstrap Capacitor Connection. The AOZ1269-02 includes an internal bootstrap diode. Connect an external capacitor between BST and LX as shown in the Typical Application diagram.
21	VCC	Supply Input for analog functions. Bypass VCC to AGND with a 1µF ceramic capacitor. Place the capacitor close to VCC pin.
23	SS	Soft-Start Time Setting Pin. Connect a capacitor between SS and AGND to set the soft-start time.

Absolute Maximum Ratings

Exceeding the Absolute Maximum Ratings may damage the device.

Parameter	Rating
IN, TON to AGND	-0.3V to 30V
LX to AGND(2)	-2V to 30V
BST to AGND	-0.3V to 36V
SS, PGOOD, FB, EN, VCC, $\overline{PFM}$ to AGND	-0.3V to 6V
PGND to AGND	-0.3V to +0.3V
Junction Temperature (T_J)	+150°C
Storage Temperature (T_S)	-65°C to +150°C
ESD Rating(1)	2kV

Note:

1. Devices are inherently ESD sensitive, handling precautions are required. Human body model rating: 1.5kΩ in series with 100pF.
2. LX to PGND Transient (t<20ns) ------ -7V to V_{IN} + 7V.

Maximum Operating Ratings

The device is not guaranteed to operate beyond the Maximum Operating ratings.

Parameter	Rating
Supply Voltage (V_{IN})	2.7V to 28V
Output Voltage Range	0.8V to 0.85*V_{IN}
Ambient Temperature (T_A)	-40°C to +85°C
Package Thermal Resistance	
(θ_{JA})	40°C/W
(θ_{JC})	4.5°C/W

Electrical Characteristics

T_A = 25°C, V_{IN} = 12V, V_{CC} = 5V, EN = 5V, unless otherwise specified. Specifications in **BOLD** indicate a temperature range of -40°C to +85°C.

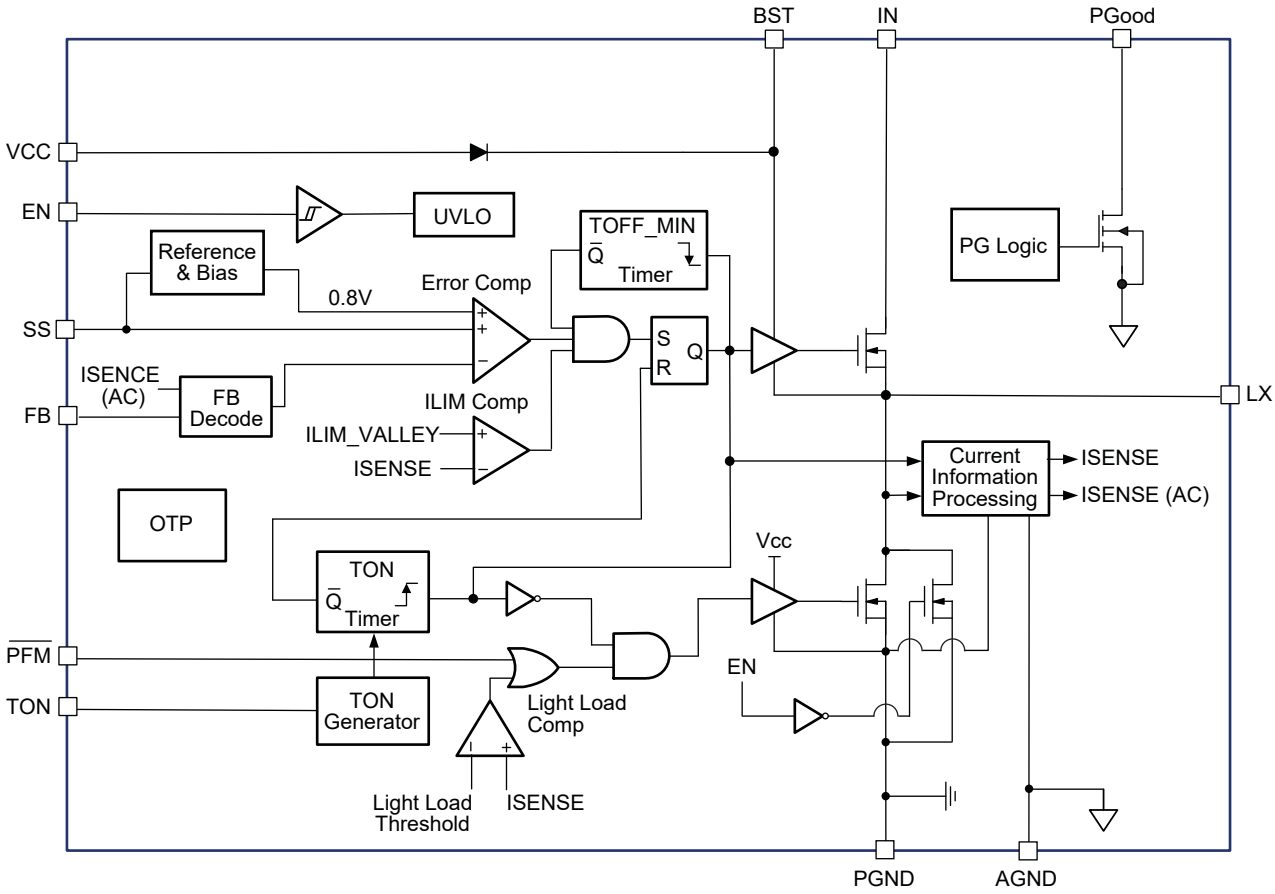
Symbol	Parameter	Conditions	Min.	Typ.	Max	Units
V_{IN}	IN Supply Voltage		**2.7**		**28**	V
V_{UVLO}	Under-Voltage Lockout Threshold of VCC	V_{CC} rising V_{CC} falling	 **3.2**	**4.0** **3.7**	**4.4**	V
I_q	Quiescent Supply Current of VCC	I_{OUT} = 0, V_{FB} = 1V, V_{EN} > 2V		**1**	**1.5**	mA
I_{OFF}	Shutdown Supply Current of VCC	V_{EN} = 0V		**1**	**20**	µA
V_{FB}	Feedback Voltage	T_A = 25°C T_A = 0°C to 85°C	0.792 0.788	0.800 0.800	0.808 0.812	V
	Load Regulation			0.5		%
	Line Regulation			1		%
I_{FB}	FB Input Bias Current				200	nA
Enable						
V_{EN}	EN Input Threshold	Off threshold On threshold	 2.5		0.5	V
V_{EN_HYS}	EN Input Hysteresis			200		mV
$\overline{PFM}$ Control						
$V_{\overline{PFM}}$	$\overline{PFM}$ Input Threshold	PFM Mode threshold Force PWM threshold	 2.5		0.5	V
$V_{\overline{PFM}HYS}$	$\overline{PFM}$ Input Hysteresis			100		mV
Modulator						
T_{ON}	On Time	R_{TON} = 100kΩ, V_{IN} = 12V R_{TON} = 100kΩ, V_{IN} = 24V	200	250 150	300	ns
T_{ON_MIN}	Minimum On Time			100		ns
T_{OFF_MIN}	Minimum Off Time			250		ns

Electrical Characteristics *(Continued)*

T_A = 25°C, V_{IN} = 12V, V_{CC} = 5V, EN = 5V, unless otherwise specified. Specifications in **BOLD** indicate a temperature range of -40°C to +85°C.

Symbol	Parameter	Conditions	Min.	Typ.	Max	Units
Soft-Start						
I_{SS_OUT}	SS Source Current	V_{SS} = 0 C_{SS} = 0.001µF to 0.1µF	7	11	15	µA
Power Good Signal						
V_{PG_LOW}	PGOOD Low Voltage	I_{OL} = 1mA			**0.5**	V
	PGOOD Leakage Current				**±1**	µA
V_{PGH}	PGOOD Threshold (Low Level to High Level)	FB rising	82	85	88	%
V_{PGL}	PGOOD Threshold (High Level to Low Level)	FB rising FB falling	117 79	120 82	123 85	%
	PGOOD Threshold Hysteresis			3		%
T_{PG_L}	PGOOD Fault Delay Time (FB falling)			50		µs
Under Voltage and Over Voltage Protection						
V_{PL}	Under Voltage Threshold	FB falling	79	82	85	%
T_{PL}	Under Voltage Delay Time			128		µs
V_{PH}	Over Voltage Threshold	FB rising	117	120	123	%
T_{UV_LX}	Under Voltage Shutdown Blanking Time	V_{IN} = 12V, V_{EN} = 0V, V_{CC} = 5V		20		ms
Power Stage Output						
$R_{DS(ON)}$	High-Side NFET On-Resistance	V_{IN} = 12V, V_{CC} = 5V		18	20	mΩ
	High-Side NFET Leakage	V_{EN} = 0V, V_{LX} = 0V			10	µA
$R_{DS(ON)}$	Low-Side NFET On-Resistance	V_{LX} = 12V, V_{CC} = 5V		8	10	mΩ
	Low-Side NFET Leakage	V_{EN} = 0V			10	µA
Over-current and Thermal Protection						
I_{LIM}	Valley Current Limit	V_{CC} = 5V	13			A
	Thermal Shutdown Threshold	T_J rising T_J falling		145 100		°C

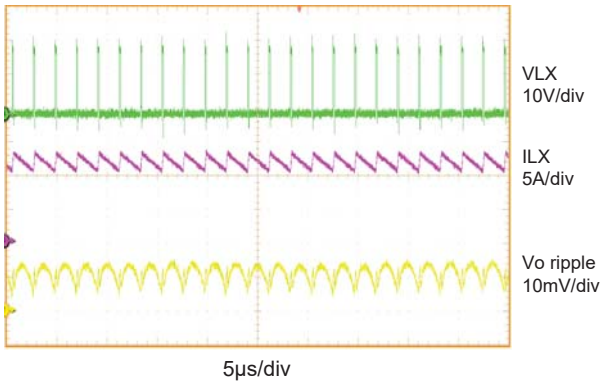
Functional Block Diagram



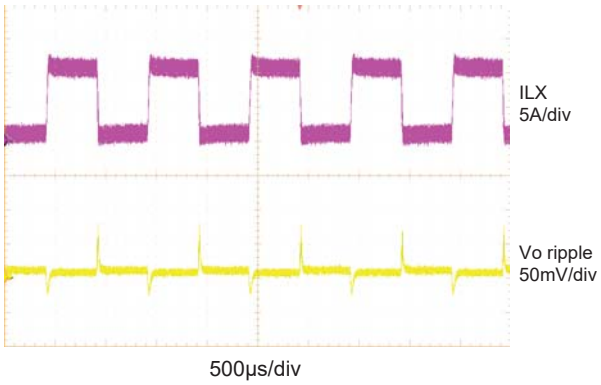
Typical Performance Characteristics

Circuit of Typical Application. T_A = 25°C, V_{IN} = 19V, V_{OUT} = 1.05V, fs = 450kHz unless otherwise specified.

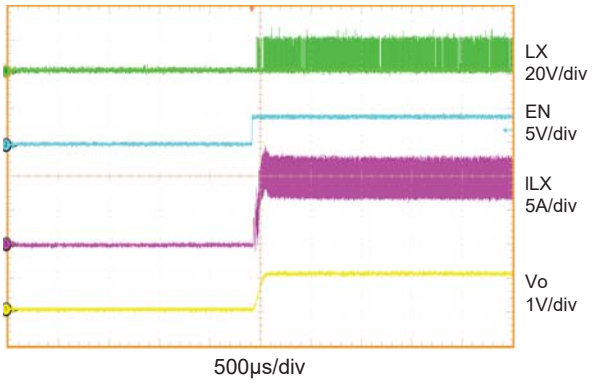
Normal Operation



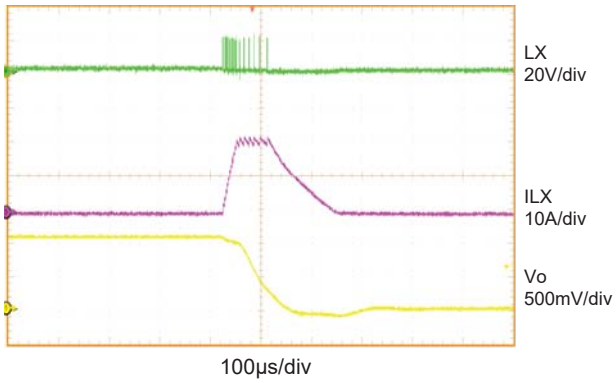
Load Transient 1.2A to 10.8A



Full Load Start-up



Short Circuit Protection



Detailed Description

The AOZ1269-02 is a high-efficiency, easy-to-use, synchronous buck regulator optimized for notebook computers. The regulator is capable of supplying 10A of continuous output current with an output voltage adjustable down to 0.8V. The programmable operating frequency range of 200kHz to 1MHz enables optimizing the configuration for PCB area and efficiency.

The input voltage of AOZ1269-02 can be as low as 2.7V. The highest input voltage of AOZ1269-02 can be 28V. Constant on-time PWM with input feed-forward control scheme results in ultra-fast transient response while maintaining relatively constant switching frequency over the entire input range. True AC current mode control scheme guarantees the regulator can be stable with a ceramic output capacitor. The switching frequency can be externally programmed up to 1MHz. Protection features include V_{CC} under-voltage lockout, valley current limit, output over voltage and under voltage protection, short-circuit protection, and thermal shutdown.

The AOZ1269-02 is available in 23-pin 4mm x 4mm QFN package.

Enable and Soft Start

The AOZ1269-02 has external soft start feature to limit in-rush current and ensure the output voltage ramps up smoothly to regulation voltage. A soft start process begins when V_{CC} rises to 4.1V and voltage on EN pin is HIGH. An internal current source charges the external soft-start capacitor; the FB voltage follows the voltage of soft-start pin (V_{SS}) when it is lower than 0.8V. When V_{SS} is higher than 0.8V, the FB voltage is regulated by internal precise band-gap voltage (0.8V). The soft-start time can be calculated by the following formula:

$$T_{SS}(\mu s) = 330 \times C_{SS}(nF)$$

If C_{SS} is 1nF, the soft-start time will be 330µs; if C_{SS} is 10nF, the soft-start time will be 3.3ms.

Constant-On-Time PWM Control with Input Feed-Forward

The control algorithm of AOZ1269-02 is constant-on-time PWM Control with input feed-forward.

The simplified control schematic is shown in Figure 1.

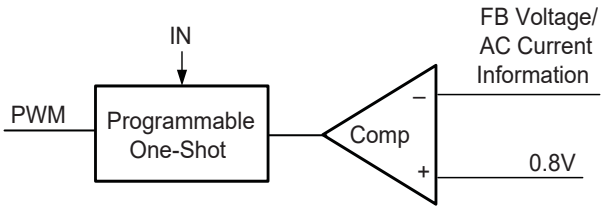


Figure 1. Simplified Control Schematic of AOZ1269-02

The high-side switch on-time is determined solely by a one-shot whose pulse width can be programmed by one external resistor and is inversely proportional to input voltage (IN). The one-shot is triggered when the internal 0.8V is lower than the combined information of FB voltage and the AC current information of inductor, which is processed and obtained through the sensed lower-side MOSFET current once it turns on. The added AC current information can help the stability of constant-on time control even with pure ceramic output capacitors, which have very low ESR. The AC current information has no DC offset, which does not cause offset with output load change, which is fundamentally different from other V^2 constant-on time control schemes.

The constant-on-time PWM control architecture is a pseudo-fixed frequency with input voltage feed-forward. The internal circuit of AOZ1269-02 sets the on-time of high-side switch inversely proportional to the IN.

$$T_{ON} = \frac{26.3 \times 10^{-12} \times R_{TON}(\Omega)}{V_{IN}(V)} \quad (1)$$

To achieve the flux balance of inductor, the buck converter has the equation:

$$F_{SW} = \frac{V_{OUT}}{V_{IN} \times T_{ON}} \quad (2)$$

Once the product of V_{IN} x T_{ON} is constant, the switching frequency keeps constant and is independent with input voltage.

An external resistor between the IN and TON pin sets the switching frequency according to the following equation:

$$F_{SW} = \frac{V_{OUT} \times 10^{12}}{26.3 \times R_{TON}} \quad (3)$$

A further simplified equation will be:

$$F_{SW}(kHz) = \frac{38000 \times V_{OUT}(V)}{R_{TON}(k\Omega)} \quad (4)$$

If V_{OUT} is 1.8V, R_{TON} is 137kΩ, the switching frequency will be 500kHz.

This algorithm results in a nearly constant switching frequency despite the lack of a fixed-frequency clock generator.

True Current Mode Control

The constant-on-time control scheme is intrinsically unstable if output capacitor's ESR is not large enough as an effective current-sense resistor. Ceramic capacitors usually cannot be used as output capacitor.

The AOZ1269-02 senses the low-side MOSFET current and processes it into DC and AC current information using AOS proprietary technique. The AC current information is decoded and added on the FB pin on phase. With AC current information, the stability of constant-on-time control is significantly improved even without the help of output capacitor's ESR, and thus the pure ceramic capacitor solution can be applicable. The pure ceramic capacitor solution can significantly reduce the output ripple (no ESR caused overshoot and undershoot) and less board area design.

Valley Current-Limit Protection

The AOZ1269-02 uses the valley current-limit protection by using R_{DSON} of the lower MOSFET current sensing. To detect real current information, a minimum constant-off (150ns typical) is implemented after a constant-on time. If the current exceeds the valley current-limit threshold, the PWM controller is not allowed to initiate a new cycle. The actual peak current is greater than the valley current-limit threshold by an amount equal to the inductor ripple current. Therefore, the exact current-limit characteristic and maximum load capability are a function of the inductor value as well as input and output voltages. The current limit will keep the low-side MOSFET ON and will not allow another high-side on-time, until the current in the low-side MOSFET reduces below the current limit. Figure 2 shows the inductor current during the current limit.

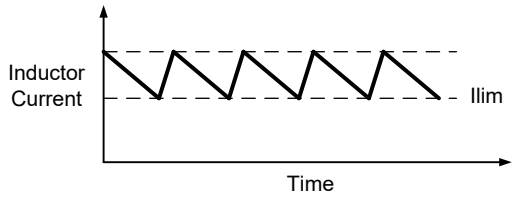


Figure 2. Inductor Current

After 128µs (typical), the AOZ1269-02 considers this is a true failed condition and therefore, turns-off both high-side and low-side MOSFETs and latches off. When triggered, only the enable can restart the AOZ1269-02 again.

Output Voltage Under-Voltage Protection

If the output voltage is lower than 18% by over-current or short circuit, the AOZ1269-02 will wait for 128µs (typical) and turns-off both high-side and low-side MOSFETs and latches off. When triggered, only the enable can restart the AOZ1269-02 again.

Output Voltage Over-Voltage Protection

The threshold of OVP is set 20% higher than 800mV. When the V_{FB} voltage exceeds the OVP threshold, high-side MOSFET is turned-off and low-side MOSFETs is turned-on until V_{FB} voltage is lower than 800mV.

Power Good Output

The power good (PGOOD) output, which is an open drain output, requires the pull-up resistor. When the output voltage is 18% below than the nominal regulation voltage for 50µs (typical), the PGOOD is pulled low. When the output voltage is 20% higher than the nominal regulation voltage, the PGOOD is also pulled low.

When combined with the under-voltage-protection circuit, this current limit method is effective in almost every circumstance.

Application Information

The basic AOZ1269-02 application circuit is shown in page 2. Component selection is explained below.

Input Capacitor

The input capacitor must be connected to the IN pins and PGND pin of the AOZ1269-02 to maintain steady input voltage and filter out the pulsing input current. A small decoupling capacitor, usually 1μF, should be connected to the VCC pin and AGND pin for stable operation of the AOZ1269-02. The voltage rating of input capacitor must be greater than maximum input voltage plus ripple voltage.

The input ripple voltage can be approximated by equation below:

$$\Delta V_{IN} = \frac{I_O}{f \times C_{IN}} \times \left(1 - \frac{V_O}{V_{IN}}\right) \times \frac{V_O}{V_{IN}}$$

Since the input current is discontinuous in a buck converter, the current stress on the input capacitor is another concern when selecting the capacitor. For a buck circuit, the RMS value of input capacitor current can be calculated by:

$$I_{CIN\_RMS} = I_O \times \sqrt{\frac{V_O}{V_{IN}}\left(1 - \frac{V_O}{V_{IN}}\right)}$$

if let *m* equal the conversion ratio:

$$\frac{V_O}{V_{IN}} = m$$

The relation between the input capacitor RMS current and voltage conversion ratio is calculated and shown in Figure 3. It can be seen that when V_O is half of V_{IN}, C_{IN} it is under the worst current stress. The worst current stress on C_{IN} is 0.5 x I_O.

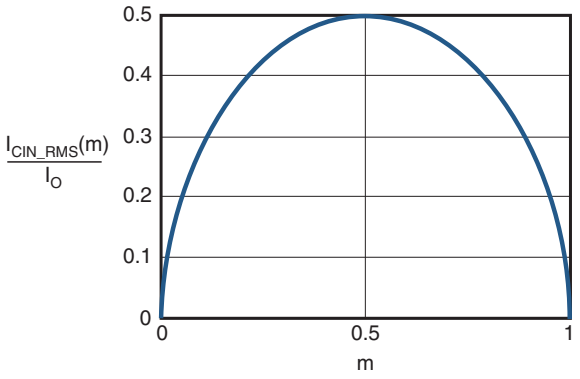


Figure 3. I_{CIN} vs. Voltage Conversion Ratio

For reliable operation and best performance, the input capacitors must have current rating higher than $I_{CIN-RMS}$ at worst operating conditions. Ceramic capacitors are preferred for input capacitors because of their low ESR and high ripple current rating. Depending on the application circuits, other low ESR tantalum capacitor or aluminum electrolytic capacitor may also be used. When selecting ceramic capacitors, X5R or X7R type dielectric ceramic capacitors are preferred for their better temperature and voltage characteristics. Note that the ripple current rating from capacitor manufactures is based on certain amount of life time. Further de-rating may be necessary for practical design requirement.

Inductor

The inductor is used to supply constant current to output when it is driven by a switching voltage. For given input and output voltage, inductance and switching frequency together decide the inductor ripple current, which is:

$$\Delta I_L = \frac{V_O}{f \times L} \times \left(1 - \frac{V_O}{V_{IN}}\right)$$

The peak inductor current is:

$$I_{Lpeak} = I_O + \frac{\Delta I_L}{2}$$

High inductance gives low inductor ripple current but requires a larger size inductor to avoid saturation. Low ripple current reduces inductor core losses. It also reduces RMS current through inductor and switches, which results in less conduction loss. Usually, peak to peak ripple current on inductor is designed to be 30% to 50% of output current.

When selecting the inductor, make sure it is able to handle the peak current without saturation even at the highest operating temperature.

The inductor takes the highest current in a buck circuit. The conduction loss on the inductor needs to be checked for thermal and efficiency requirements.

Surface mount inductors in different shapes and styles are available from Coilcraft, Elytone and Murata. Shielded inductors are small and radiate less EMI noise, but they do cost more than unshielded inductors. The choice depends on EMI requirement, price and size.

Output Capacitor

The output capacitor is selected based on the DC output voltage rating, output ripple voltage specification and ripple current rating.

The selected output capacitor must have a higher rated voltage specification than the maximum desired output voltage including ripple. De-rating needs to be considered for long term reliability.

Output ripple voltage specification is another important factor for selecting the output capacitor. In a buck converter circuit, output ripple voltage is determined by inductor value, switching frequency, output capacitor value and ESR. It can be calculated by the equation below:

$$\Delta V_O = \Delta I_L \times \left(ESR_{CO} + \frac{1}{8 \times f \times C_O} \right)$$

where,

C_O is output capacitor value and

ESR_{CO} is the Equivalent Series Resistor of output capacitor.

When a low ESR ceramic capacitor is used as output capacitor, the impedance of the capacitor at the switching frequency dominates. Output ripple is mainly caused by capacitor value and inductor ripple current. The output ripple voltage calculation can be simplified to:

$$\Delta V_O = \Delta I_L \times \frac{1}{8 \times f \times C_O}$$

If the impedance of ESR at switching frequency dominates, the output ripple voltage is mainly decided by capacitor ESR and inductor ripple current. The output ripple voltage calculation can be further simplified to:

$$\Delta V_O = \Delta I_L \times ESR_{CO}$$

For lower output ripple voltage across the entire operating temperature range, X5R or X7R dielectric type of ceramic, or other low ESR tantalum are recommended to be used as output capacitors.

In a buck converter, output capacitor current is continuous. The RMS current of output capacitor is decided by the peak to peak inductor ripple current. It can be calculated by:

$$I_{CO\_RMS} = \frac{\Delta I_L}{\sqrt{12}}$$

Usually, the ripple current rating of the output capacitor is a smaller issue because of the low current stress. When the buck inductor is selected to be very small and inductor ripple current is high, the output capacitor could be overstressed.

Thermal Management and Layout Consideration

In the AOZ1269-02 buck regulator circuit, high pulsing current flows through two circuit loops. The first loop starts from the input capacitors, to the VIN pin, to the LX pins, to the filter inductor, to the output capacitor and load, and then returns to the input capacitor through ground. Current flows in the first loop when the high side switch is on. The second loop starts from the inductor, to the output capacitors and load, to the low side switch. Current flows in the second loop when the low side switch is on.

In PCB layout, minimizing the two loops area reduces the noise of this circuit and improves efficiency. A ground plane is strongly recommended to connect the input capacitor, output capacitor and PGND pin of the AOZ1269-02.

In the AOZ1269-02 buck regulator circuit, the major power dissipating components are the AOZ1269-02 and output inductor. The total power dissipation of the converter circuit can be measured by input power minus output power.

$$P_{total\_loss} = V_{IN} \times I_{IN} - V_O \times I_O$$

The power dissipation of inductor can be approximately calculated by output current and DCR of inductor and output current.

$$P_{inductor\_loss} = I_O^2 \times R_{inductor} \times 1.1$$

The actual junction temperature can be calculated with power dissipation in the AOZ1269-02 and thermal impedance from junction to ambient.

$$T_{junction} = (P_{total\_loss} - P_{inductor\_loss}) \times \Theta_{JA}$$

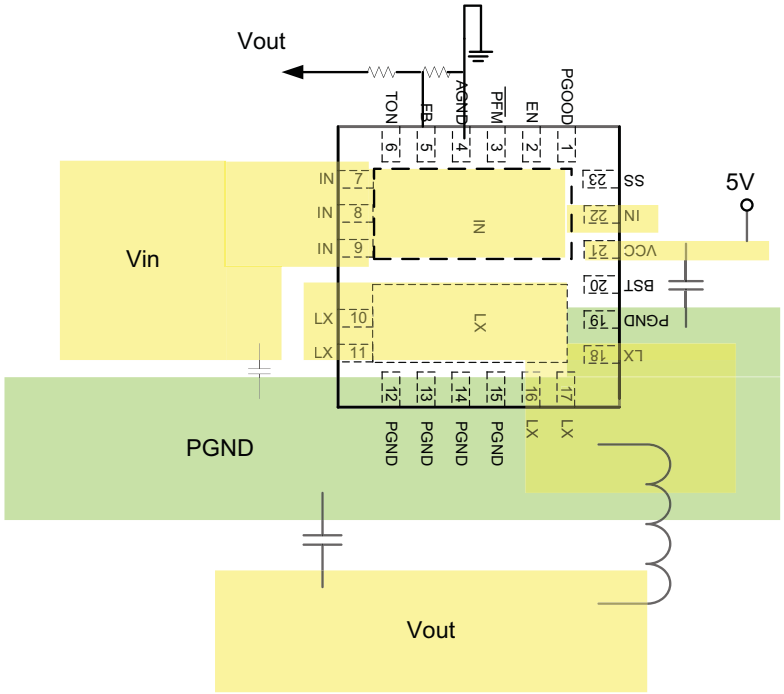
The maximum junction temperature of AOZ1269-02 is 150ºC, which limits the maximum load current capability.

The thermal performance of the AOZ1269-02 is strongly affected by the PCB layout. Extra care should be taken by users during design process to ensure that the IC will operate under the recommended environmental conditions.

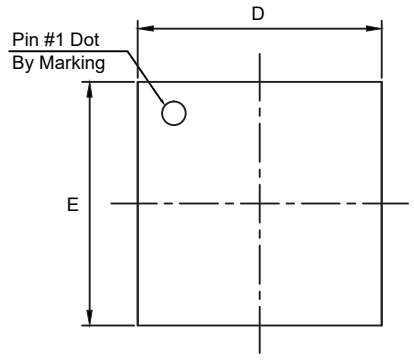
Layout Considerations

Several layout tips are listed below for the best electric and thermal performance.

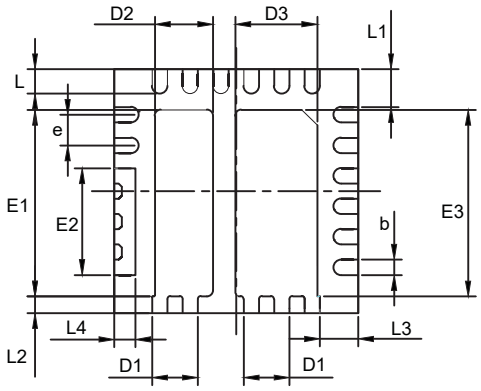
1. The LX pins and pad are connected to internal low side switch drain. They are low resistance thermal conduction path and most noisy switching node. Connect a large copper plane to LX pin to help thermal dissipation.
2. The IN pins and pad are connected to internal high side switch drain. They are also low resistance thermal conduction path. Connect a large copper plane to IN pins to help thermal dissipation.
3. Input capacitors should be connected to the IN pin and the PGND pin as close as possible to reduce the switching spikes.
4. Decoupling capacitor C_{VCC} should be connected to VCC and AGND as close as possible.
5. Voltage divider R1 and R2 should be placed as close as possible to FB and AGND.
6. R_{TON} should be put on PCB reverse side of feedback network or away from FB pin and FB feedback resistors to avoid unwanted touch to short Ton pin and FB together to ground to cause improperly operation.
7. A ground plane is preferred; Pin 19 (PGND) must be connected to the ground plane through via.
8. Keep sensitive signal traces such as feedback trace far away from the LX pins.
9. Pour copper plane on all unused board area and connect it to stable DC nodes, like VIN, GND or VOUT.



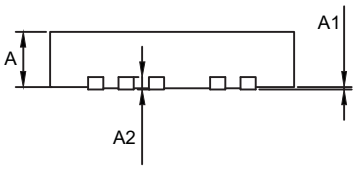
Package Dimensions, QFN 4x4B, 23 Lead EP2_S



TOP VIEW

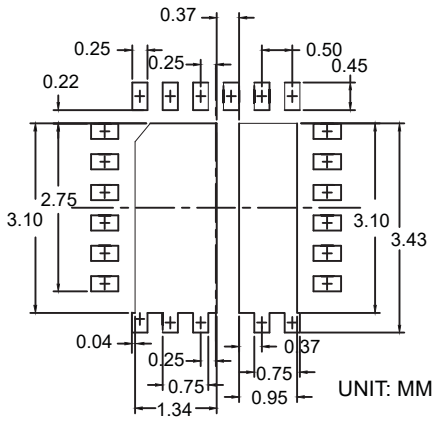


BOTTOM VIEW



SIDE VIEW

RECOMMENDED LAND PATTERN



Dimensions in millimeters

Symbols	Min.	Typ.	Max.
A	0.80	0.90	1.00
A1	0.00	—	0.05
A2		0.2 REF	
E	3.90	4.00	4.10
E1	2.95	3.05	3.15
E2	1.65	1.75	1.85
E3	2.95	3.05	3.15
D	3.90	4.00	4.10
D1	0.65	0.75	0.85
D2	0.85	0.95	1.05
D3	1.24	1.34	1.44
L	0.35	0.40	0.45
L1	0.57	0.62	0.67
L2	0.23	0.28	0.33
L3	0.57	0.62	0.67
L4	0.30	0.35	0.40
b	0.20	0.25	0.30
e		0.50 BSC	

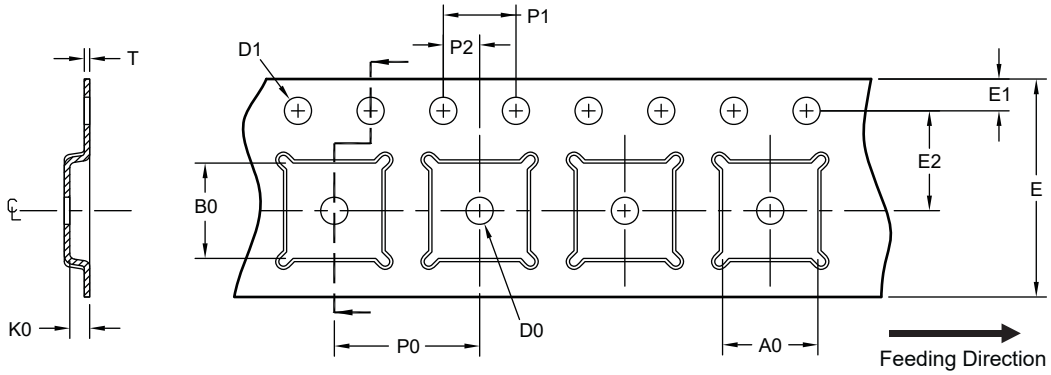
Dimensions in inches

Symbols	Min.	Typ.	Max.
A	0.031	0.035	0.039
A1	0.000	—	0.002
A2		0.008 REF	
E	0.153	0.157	0.161
E1	0.116	0.120	0.124
E2	0.065	0.069	0.073
E3	0.116	0.120	0.124
D	0.153	0.157	0.161
D1	0.026	0.030	0.034
D2	0.033	0.037	0.041
D3	0.049	0.053	0.057
L	0.014	0.016	0.018
L1	0.022	0.024	0.026
L2	0.009	0.011	0.013
L3	0.022	0.024	0.026
L4	0.012	0.014	0.016
b	0.008	0.010	0.012
e		0.020 BSC	

Notes:
1. Controlling dimensions are in millimeters. Converted inch dimensions are not necessarily exact.
2. Tolerance: ± 0.05 unless otherwise specified.
3. Radius on all corners is 0.152 max., unless otherwise specified.
4. Package wrapage: 0.012 max.
5. No plastic flash allowed on the top and bottom lead surface.
6. Pad planarity: ± 0.102
7. Crack between plastic body and lead is not allowed.

Tape and Reel Dimensions, QFN 4x4, 23 Lead EP2_S

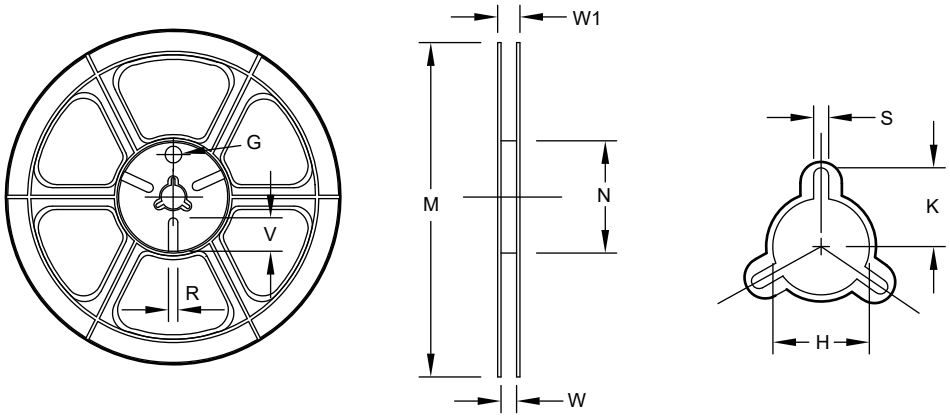
Carrier Tape



UNIT: mm

Package	A0	B0	K0	D0	D1	E	E1	E2	P0	P1	P2	T
QFN 4x4 (12mm)	4.35 ±0.10	4.35 ±0.10	1.10 ±0.10	1.50 Min.	1.50 +0.10/-0	12.00 ±0.30	1.75 ±0.10	5.50 ±0.05	8.00 ±0.10	4.00 ±0.10	2.00 ±0.05	0.30 ±0.05

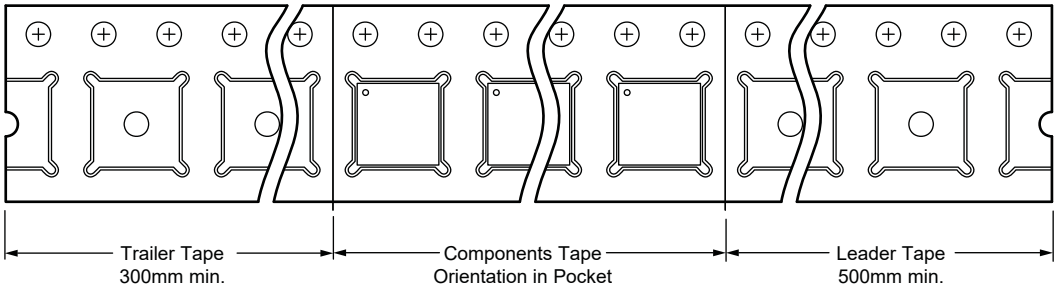
Reel



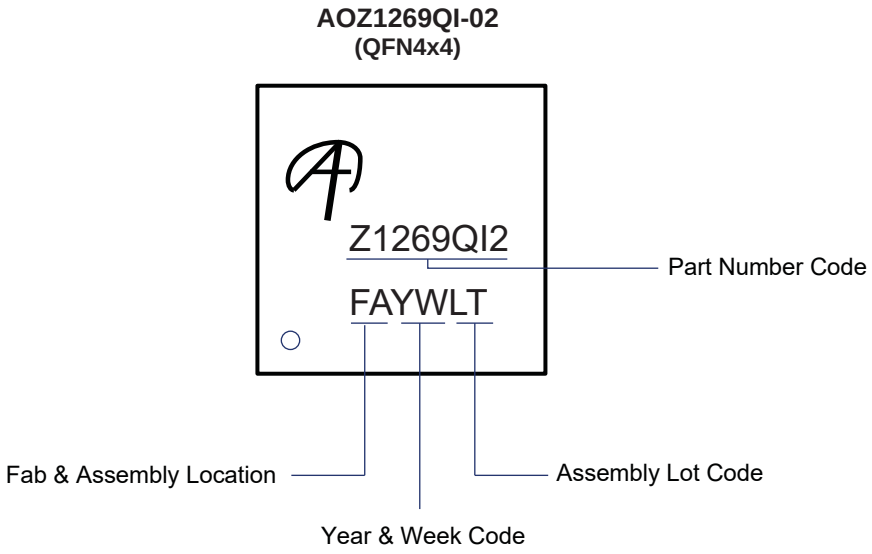
UNIT: mm

Tape Size	Reel Size	M	N	W	W1	H	K	S	G	R	V
12mm	ø330	ø330.0 ±2.0	ø79.0 ±1.0	12.4 +2.0/-0.0	17.0 +2.6/-1.2	ø13.0 ±0.5	10.5 ±0.2	2.0 ±0.5	—	—	—

Leader/Trailer and Orientation



Part Marking



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2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.