

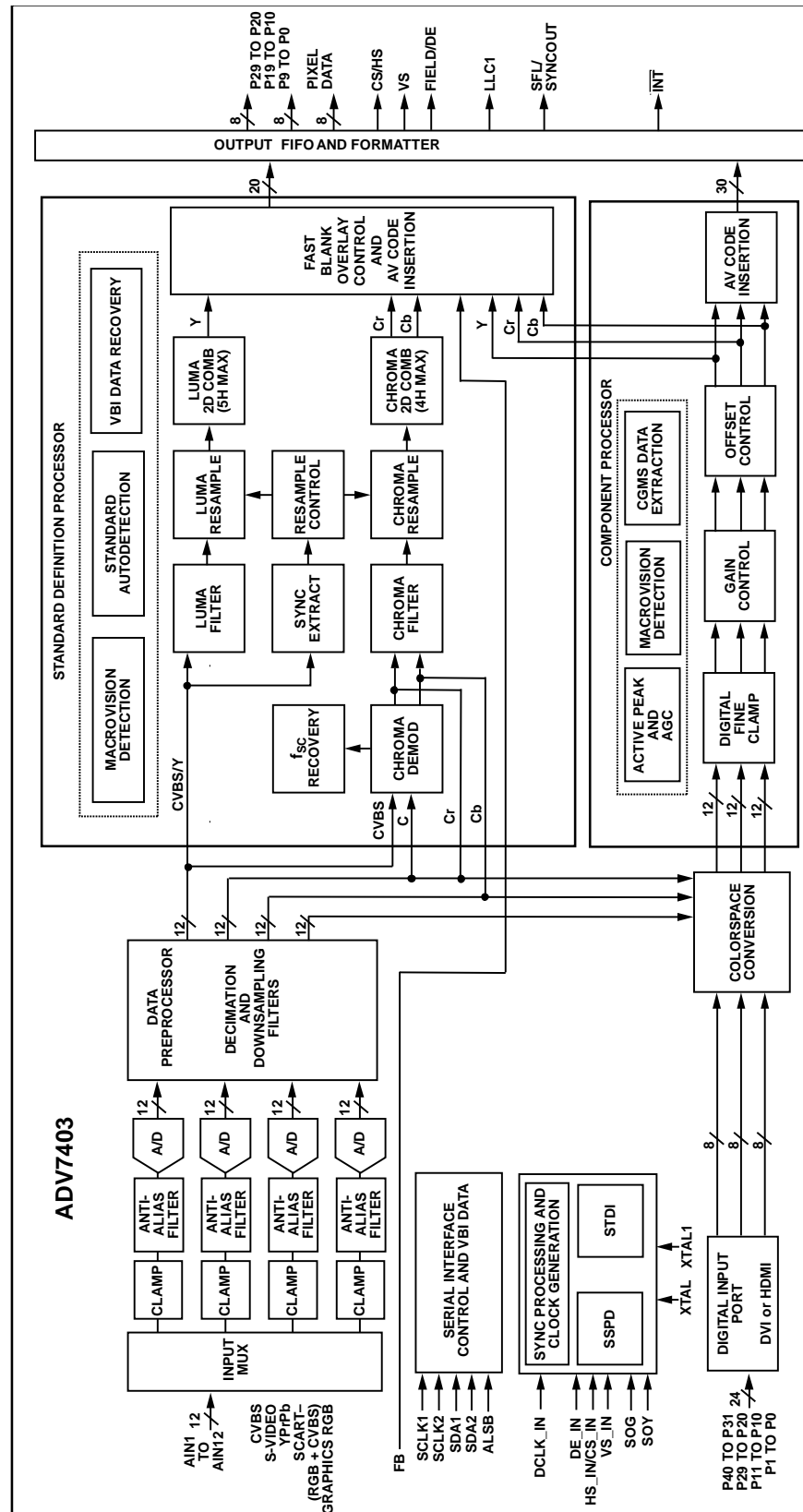
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## REVISION HISTORY

9/13—Revision B: Initial Version

## FUNCTIONAL BLOCK DIAGRAM



05431-001

Figure 1.

## SPECIFICATIONS

### ELECTRICAL CHARACTERISTICS

AVDD = 3.15 V to 3.45 V, DVDD = 1.65 V to 2.0 V, DVDDIO = 3.0 V to 3.6 V, PVDD = 1.71 V to 1.89 V, nominal input range 1.6 V.

Operating temperature range, unless otherwise noted is T<sub>MIN</sub> to T<sub>MAX</sub>: –40°C to +85°C (0°C to 70°C temperature range for ADV7403KSTZ-140).

To obtain all specifications the following write sequence must be included in the programming scripts: Address 0x0E to Data 0x80, Address 0x54 to Data 0x00, and Address 0x0E to Data 0x00.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
STATIC PERFORMANCE <sup>1</sup>						
Resolution (Each ADC)	N				12 <sup>2</sup>	Bits
Integral Nonlinearity	INL	Best straight line (BSL) at 27 MHz at a 12-bit level		±2.0	±8.0 <sup>2</sup>	LSB
		BSL at 54 MHz at a 12-bit level		–2.0/+2.5		LSB
		BSL at 74 MHz at a 10-bit level		±1.0		LSB
		BSL at 110 MHz at a 10-bit level		–3.0/+3.0		LSB
		BSL at 135 MHz at an 8-bit level <sup>3</sup>		±1.3		LSB
Differential Nonlinearity	DNL	At 27 MHz at a 12-bit level		–0.7/+0.85	–0.99/+2.5 <sup>2</sup>	LSB
		At 54 MHz at a 12-bit level		–0.75/+0.9		LSB
		At 74 MHz at a 10-bit level		±0.75		LSB
		At 110 MHz at a 10-bit level		–0.7/+5.0		LSB
		At 135 MHz at an 8-bit level <sup>3</sup>		–0.8/+2.5		LSB
DIGITAL INPUTS						
Input High Voltage <sup>4</sup>	V <sub>IH</sub>		2			V
Input Low Voltage <sup>5</sup>	V <sub>IL</sub>				0.8	V
Input High Voltage	V <sub>IH</sub>	HS_IN, VS_IN low trigger mode	0.7			V
Input Low Voltage	V <sub>IL</sub>	HS_IN, VS_IN low trigger mode			0.3	V
Input Current	I <sub>IN</sub>	P20 to P29, P31 to P40, SCLK2, SDA2, DCLK_IN, DE_IN, RESET	–60		+60	μA
		All other input pins	–10		+10	μA
Input Capacitance <sup>6</sup>	C <sub>IN</sub>				10	pF
DIGITAL OUTPUTS						
Output High Voltage <sup>7</sup>	V <sub>OH</sub>	I <sub>SOURCE</sub> = 0.4 mA	2.4			V
Output Low Voltage <sup>7</sup>	V <sub>OL</sub>	I <sub>SINK</sub> = 3.2 mA			0.4	V
High Impedance Leakage Current	I <sub>LEAK</sub>	INT, P20 to P29, SDA2			60	μA
		All other output pins			10	μA
Output Capacitance <sup>6</sup>	C <sub>OUT</sub>				20	pF
POWER REQUIREMENTS <sup>6</sup>						
Digital Core Power Supply	DVDD		1.65	1.8	2	V
Digital Input/Output Power Supply	DVDDIO		3.0	3.3	3.6	V
PLL Power Supply	PVDD		1.71	1.8	1.89	V
Analog Power Supply	AVDD		3.15	3.3	3.45	V
Digital Core Supply Current	I <sub>DVDD</sub>	CVBS input sampling at 54 MHz		105		mA
		Graphics RGB sampling at 135 MHz		137		mA
		SCART RGB FB sampling at 54 MHz		106		mA
Digital Input/Output Supply Current	I <sub>DVDDIO</sub>	CVBS input sampling at 54 MHz		4		mA
		Graphics RGB sampling at 135 MHz		19		mA
PLL Supply Current	I <sub>PVDD</sub>	CVBS input sampling at 54 MHz		11		mA
		Graphics RGB sampling at 135 MHz		12		mA

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
Analog Supply Current <sup>8</sup>	I <sub>AVDD</sub>	CVBS input sampling at 54 MHz		99		mA
		Graphics RGB sampling at 135 MHz		242		mA
		SCART RGB FB sampling at 54 MHz		269		mA
Power-Down Current	I <sub>PWRDN</sub>			2.25		mA
Green Mode Power-Down	I <sub>PWRDNG</sub>	Sync bypass function		16		mA
Power-Up Time	T <sub>PWRUP</sub>			20		ms

<sup>1</sup> All ADC linearity tests performed at input range of full scale – 12.5% and at zero scale + 12.5%.

<sup>2</sup> Maximum INL and DNL specifications obtained with device configured for component video input.

<sup>3</sup> This specification is for the ADV7403KSTZ-140 only.

<sup>4</sup> To obtain specified V<sub>IH</sub> level on the XTAL pin (Pin 38), program Subaddress 0x13 (write only) with 0x04 value. When Subaddress 0x13 is set to 0x00 value, V<sub>IH</sub> level on the XTAL pin = 1.2 V.

<sup>5</sup> To obtain specified V<sub>IL</sub> level on the XTAL pin (Pin 38), program Subaddress 0x13 (write only) with 0x04 value. When Subaddress 0x13 is set to 0x00 value, V<sub>IL</sub> level on the XTAL pin (Pin 38) = 0.4 V.

<sup>6</sup> Guaranteed by characterization.

<sup>7</sup> V<sub>OH</sub> and V<sub>OL</sub> levels obtained using default drive strength value (0xD5) in Subaddress 0xF4.

<sup>8</sup> Analog current measurements for CVBS made with only ADC0 are powered up; for RGB, only ADC0, ADC1, and ADC2 are powered up; and for SCART FB, all ADCs powered up.

## VIDEO SPECIFICATIONS

AVDD = 3.15 V to 3.45 V, DVDD = 1.65 V to 2.0 V, DVDDIO = 3.0 V to 3.6 V, PVDD = 1.71 V to 1.89 V. Operating temperature range, unless otherwise noted is T<sub>MIN</sub> to T<sub>MAX</sub>: –40°C to +85°C (0°C to 70°C temperature range for [ADV7403KSTZ-140](#)). Guaranteed by characterization.

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
NONLINEAR SPECIFICATIONS						
Differential Phase	DP	CVBS input, modulated 5 step		0.4		Degrees
Differential Gain	DG	CVBS input, modulated 5 step		0.4		%
Luma Nonlinearity	LNL	CVBS input, 5 step		0.4		%
NOISE SPECIFICATIONS						
SNR Unweighted		Luma ramp	61	64		dB
		Luma flat field	64	65		dB
Analog Front End Crosstalk				60		dB
LOCK TIME SPECIFICATIONS						
Horizontal Lock Range			–5		+5	%
Vertical Lock Range			40		70	Hz
f <sub>SC</sub> Subcarrier Lock Range				±1.3		kHz
Color Lock in Time				60		Lines
Sync Depth Range <sup>1</sup>			20		200	%
Color Burst Range			5		200	%
Vertical Lock Time				2		Fields
Horizontal Lock Time				100		Lines
CHROMA SPECIFICATIONS						
Hue Accuracy	HUE			1		Degrees
Color Saturation Accuracy	CL_AC			1		%
Color AGC Range			5		400	%
Chroma Amplitude Error				0.4		%
Chroma Phase Error				0.3		Degrees
Chroma Luma Intermodulation				0.1		%
LUMA SPECIFICATIONS						
Luma Accuracy						
Brightness		CVBS, 1 V input		1		%
Contrast		CVBS, 1 V input		1		%

<sup>1</sup> Nominal sync depth is 300 mV at 100% sync depth range.

**TIMING CHARACTERISTICS**

AVDD = 3.15 V to 3.45 V, DVDD = 1.65 V to 2.0 V, DVDDIO = 3.0 V to 3.6 V, PVDD = 1.71 V to 1.89 V. Operating temperature range, unless otherwise noted is T<sub>MIN</sub> to T<sub>MAX</sub>: -40°C to +85°C (0°C to 70°C temperature range for ADV7403KSTZ-140). Guaranteed by characterization.

**Table 3.**

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
<b>SYSTEM CLOCK AND CRYSTAL</b>						
Crystal Nominal Frequency				28.63636		MHz
Crystal Frequency Stability					±50	ppm
Horizontal Sync Input Frequency			14.8		110	kHz
LLC1 Frequency Range <sup>1</sup>			12.825		140	MHz
<b>I<sup>2</sup>C PORT<sup>2</sup></b>						
SCLK Frequency					400	kHz
SCLK Minimum Pulse Width High	t <sub>1</sub>		0.6			μs
SCLK Minimum Pulse Width Low	t <sub>2</sub>		1.3			μs
Hold Time (Start Condition)	t <sub>3</sub>		0.6			μs
Setup Time (Start Condition)	t <sub>4</sub>		0.6			μs
SDA Setup Time	t <sub>5</sub>		100			ns
SCLK and SDA Rise Time	t <sub>6</sub>				300	ns
SCLK and SDA Fall Time	t <sub>7</sub>				300	ns
Setup Time for Stop Condition	t <sub>8</sub>			0.6		μs
<b>RESET FEATURE</b>						
Reset Pulse Width			5			ms
<b>CLOCK OUTPUTS</b>						
LLC1 Mark Space Ratio	t <sub>9</sub> :t <sub>10</sub>		45:55		55:45	% duty cycle
<b>DATA AND CONTROL OUTPUTS</b>						
Data Output Transition Time SDR (SDP) <sup>3</sup>	t <sub>11</sub>	Negative clock edge to start of valid data			3.6	ns
	t <sub>12</sub>	End of valid data to negative clock edge			2.4	ns
Data Output Transition Time SDR (CP) <sup>4</sup>	t <sub>13</sub>	End of valid data to negative clock edge			2.8	ns
	t <sub>14</sub>	Negative clock edge to start of valid data			0.1	ns
Data Output Transition Time DDR (CP) <sup>4, 5</sup>	t <sub>15</sub>	Positive clock edge to end of valid data	-4 + TLLC1/4			ns
	t <sub>16</sub>	Positive clock edge to start of valid data	0.25 + TLLC1/4			ns
	t <sub>17</sub>	Negative clock edge to end of valid data	-2.95 + TLLC1/4			ns
	t <sub>18</sub>	Negative clock edge to start of valid data	-0.5 + TLLC1/4			ns
<b>DATA and CONTROL INPUTS<sup>2</sup></b>						
Input Setup Time (Digital Input Port)	t <sub>19</sub>	HS_IN, VS_IN	9			ns
		DE_IN, data inputs	2.2			ns
Input Hold Time (Digital Input Port)	t <sub>20</sub>	HS_IN, VS_IN	7			ns
		DE_IN, data inputs	2			ns

<sup>1</sup> Maximum LLC1 frequency is 110 MHz for ADV7403BSTZ-110.

<sup>2</sup> TTL input values are 0 V to 3 V with rise/fall times ≥ 3 ns measured between the 10% and 90% points.

<sup>3</sup> SDP timing figures obtained using default drive strength value (0xD5) in Subaddress 0xF4.

<sup>4</sup> CP timing figures obtained using maximum drive strength value (0xFF) in Subaddress 0xF4.

<sup>5</sup> DDR timing specifications dependent on LLC1 output pixel clock; TLCC1/4 = 9.25 ns at LLC1 = 27 MHz.

## Timing Diagram

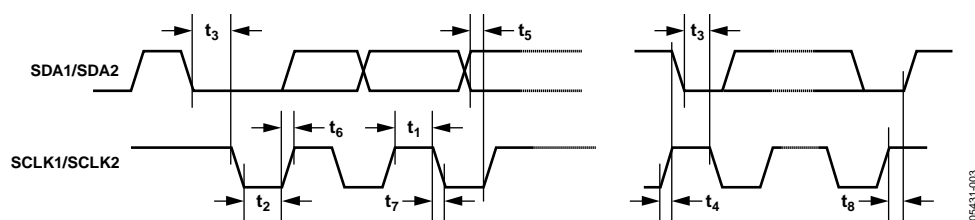


Figure 2. I²C Timing

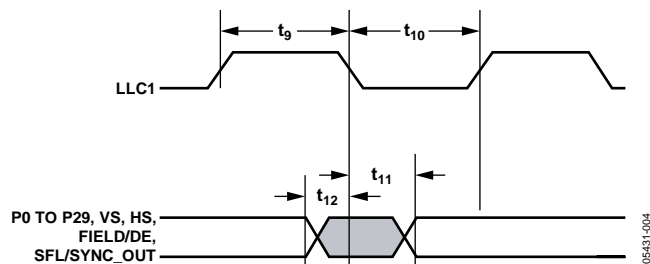


Figure 3. Pixel Port and Control SDR Output Timing (SD Core)

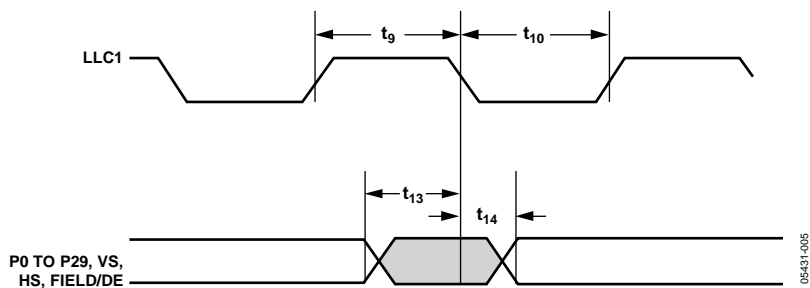


Figure 4. Pixel Port and Control SDR Output Timing (CP Core)

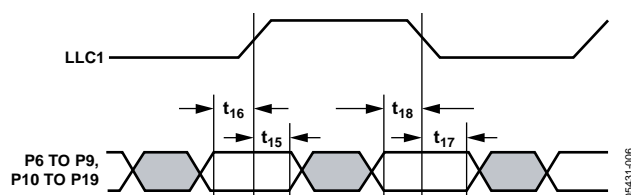


Figure 5. Pixel Port and Control DDR Output Timing (CP Core)

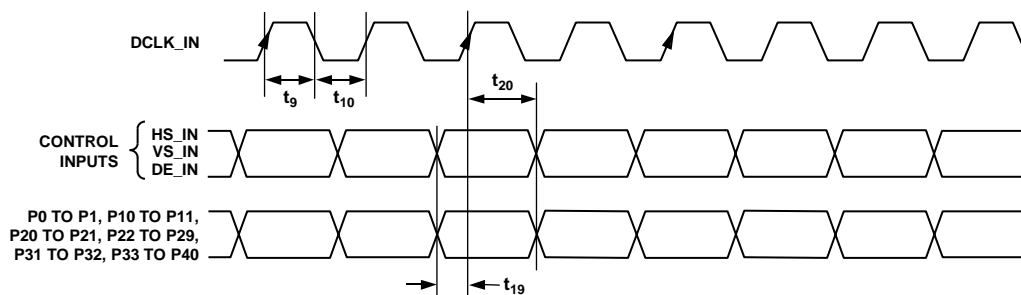


Figure 6. Digital Input Port and Control Input Timing

**ANALOG SPECIFICATIONS**

AVDD = 3.15 V to 3.45 V, DVDD = 1.65 V to 2.0 V, DVDDIO = 3.0 V to 3.6 V, PVDD = 1.71 V to 1.89 V. Operating temperature range, unless otherwise noted is T<sub>MIN</sub> to T<sub>MAX</sub>: -40°C to +85°C (0°C to 70°C temperature range for ADV7403KSTZ-140). Recommended analog input video signal range: 0.5 V to 1.6 V, typically 1 V p-p. Guaranteed by characterization.

**Table 4.**

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
<b>CLAMP CIRCUITRY</b>					
External Clamp Capacitor	Clamps switched off		0.1		μF
Input Impedance (Except the FB Pin, Pin 51)			10		MΩ
Input Impedance of Pin 51 (FB)			20		kΩ
CML			1.86		V
ADC Full-Scale Level			CML + 0.8		V
ADC Zero-Scale Level			CML - 0.8		V
ADC Dynamic Range			1.6		V
Clamp Level (When Locked)	CVBS input		CML - 0.292		V
	SCART RGB input (R, G, B signals)		CML - 0.4		V
	S-Video input (Y signal)		CML - 0.292		V
	S-Video input (C signal)		CML - 0		V
	Component input (Y, Pr, Pb signals)		CML - 0.3		V
	PC RGB input (R, G, B signals)		CML - 0.3		V
Large Clamp	SDP only				
Source Current	SDP only		0.75		mA
Sink Current			0.9		mA
Fine Clamp					
Source Current			17		μA
Sink Current			17		μA

## ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	Rating
AVDD to AGND	4 V
DVDD to DGND	2.2 V
PVDD to AGND	2.2 V
DVDDIO to DGND	4 V
DVDDIO to AVDD	–0.3 V to +0.3 V
PVDD to DVDD	–0.3 V to +0.3 V
DVDDIO to PVDD	–0.3 V to +2 V
DVDDIO to DVDD	–0.3 V to +2 V
AVDD to PVDD	–0.3 V to +2 V
AVDD to DVDD	–0.3 V to +2 V
Digital Inputs Voltage to DGND	DGND – 0.3 V to DVDDIO + 0.3 V
Digital Outputs Voltage to DGND	DGND – 0.3 V to DVDDIO + 0.3 V
Analog Inputs to AGND	AGND – 0.3 V to AVDD + 0.3 V
Maximum Junction Temperature ( $T_{J\text{ MAX}}$ )	125°C
Storage Temperature Range	–65°C to +150°C
Infrared Reflow Soldering (20 sec)	260°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## PACKAGE THERMAL PERFORMANCE

To reduce power consumption when using the device, the user is advised to turn off any unused ADCs.

Keep the junction temperature less than the maximum junction temperature ( $T_{J\text{ MAX}}$ ) of 125°C. The junction temperature is calculated by

$$T_J = T_{A\text{ MAX}} + (\theta_{JA} \times W_{\text{MAX}})$$

where:

$$T_{A\text{ MAX}} = 85^\circ\text{C}.$$

$$\theta_{JA} = 30^\circ\text{C/W}.$$

$$W_{\text{MAX}} = ((AVDD \times I_{AVDD}) + (DVDD \times I_{DVDD}) + (DVDDIO \times I_{DVDDIO}) + (PVDD \times I_{PVDD})).$$

## THERMAL RESISTANCE

$\theta_{JA}$  is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 6.

Package Type	$\theta_{JA}$ <sup>1</sup>	$\theta_{JC}$ <sup>2</sup>	Unit
100-Lead LQFP	30	7	°C/W

<sup>1</sup> It is a 4-layer printed circuit board (PCB) with a solid ground plane (still air).

<sup>2</sup> It is a 4-layer PCB with a solid ground plane.

## ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.



## PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

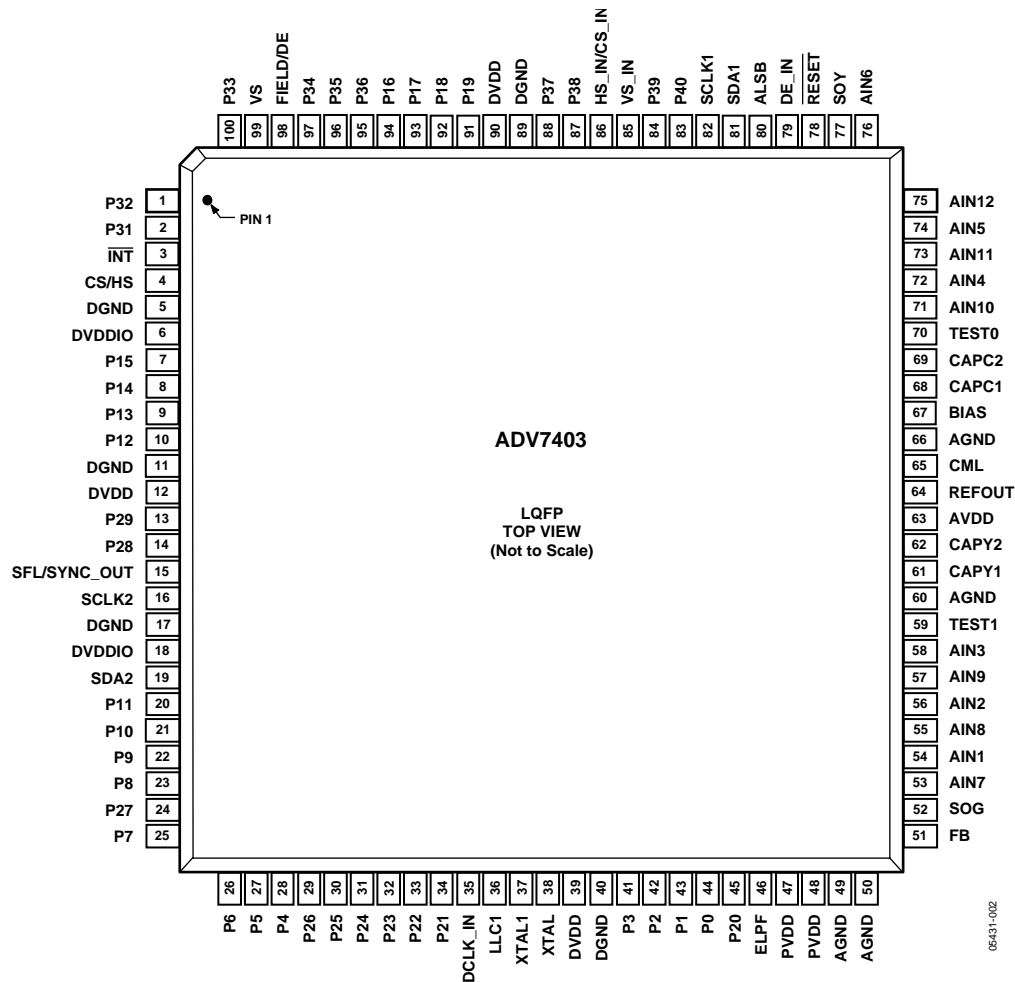


Figure 7. Pin Configuration

Table 7. Pin Function Descriptions

Pin No.	Mnemonic	Type <sup>1</sup>	Description
1, 2, 83, 84, 87, 88, 95 to 97, 100	P31 to P40	I	Video Pixel Input Port.
3	$\overline{\text{INT}}$	O	Interrupt. This pin can be active low or active high. When SDP/CP status bits change, this pin triggers. The set of events that triggers an interrupt is under user control.
4	CS/HS	O	Digital Composite Synchronization Signal (CS). The CS pin can be selected while in CP mode. Horizontal Synchronization Output Signal (HS). The HS pin can be selected while in SDP or CP modes.
5, 11, 17, 40, 89	DGND	G	Digital Ground.
6, 18	DVDDIO	P	Digital Input/Output Supply Voltage (3.3 V).
7 to 10, 22, 23, 25 to 28, 41, 42, 91 to 94	P2 to P9, P12 to P19	O	Video Pixel Output Port.
12, 39, 90	DVDD	P	Digital Core Supply Voltage (1.8 V).
13, 14, 20, 21, 24, 29 to 34, 43 to 45	P0 to P1, P10 to P11, P20 to P29	I/O	Video Pixel Input/Output Port.

Pin No.	Mnemonic	Type <sup>1</sup>	Description
15	SFL/SYNC_OUT	O	Subcarrier Frequency Lock (SFL). This pin contains a serial output stream that can be used to lock the subcarrier frequency when the decoder is connected to any Analog Devices, Inc., digital video encoder.
16, 82	SCLK1, SCLK2	I	Sliced Sync Output Signal (SYNC_OUT). This pin is only available in CP mode. I <sup>2</sup> C Port Serial Clock Input (Maximum Clock Rate of 400 kHz) Pins. SCLK1 is the clock line for the control port, and SCLK2 is the clock line for the VBI data readback port.
19, 81	SDA1, SDA2	I/O	I <sup>2</sup> C Port Serial Data Input/Output Pins. SDA1 is the data line for the control port, and SDA2 is the data line for the VBI readback port.
35	DCLK_IN	I	Clock Input Signal. This pin is used in 24-bit digital input mode (for example, processing 24-bit RGB data from a DVI receiver IC) and also in digital CVBS input mode.
36	LLC1	O	Line-Locked Output Clock for Pixel Data. This pin range is 12.825 MHz to 140 MHz for the <a href="#">ADV7403KSTZ-140</a> , and 12.825 MHz to 110 MHz for the <a href="#">ADV7403BSTZ-110</a> .
37	XTAL1	O	Connect this pin to the 28.63636 MHz crystal, or if an external 3.3 V, 28.63636 MHz clock oscillator source is used to clock the <a href="#">ADV7403</a> , leave this pin as no connect. In crystal mode, the crystal must be a fundamental crystal.
38	XTAL	I	Input Pin for 28.63636 MHz crystal. To clock the <a href="#">ADV7403</a> , this pin can also be overdriven by an external 3.3 V, 28.63636 MHz clock oscillator source.
46	ELPF	O	External Loop PLL Filter. Connect the recommend external loop filter to the ELPF pin.
47, 48	PVDD	P	PLL Supply Voltage (1.8 V).
49, 50, 60, 66	AGND	G	Analog Ground.
51	FB	I	Fast Switch Overlay Input. This pin switches between CVBS and RGB analog signals.
52	SOG	I	Sync on Green Input. This pin is used in embedded sync mode.
53 to 58, 71 to 76	AIN1 to AIN12	I	Analog Video Input Channels.
59	TEST1	O	Leave this pin unconnected.
61, 62	CAPY1, CAPY2	I	ADC Capacitor Network.
63	AVDD	P	Analog Supply Voltage (3.3 V).
64	REFOUT	O	Internal Voltage Reference Output.
65	CML	O	Common-Mode Level (CML) Pin for the Internal ADCs.
67	BIAS	O	External Bias Setting Pin. Connect the recommended resistor (1.35 k $\Omega$ ) between the BIAS pin and ground.
68, 69	CAPC1, CAPC2	I	ADC Capacitor Network.
70	TEST0	NC	Leave this pin unconnected, or alternately, tie this pin to AGND.
77	SOY	I	Sync on Luma Input. This pin is used in embedded sync mode.
78	RESET	I	System Reset Input (Active Low). A minimum low reset pulse width of 5 ms is required to reset the circuitry of the <a href="#">ADV7403</a> .
79	DE_IN	I	Data Enable Input Signal. This pin is used in 24-bit digital input port mode (for example, processing 24-bit RGB data from a DVI receiver IC).
80	ALSB	I	This pin selects the I <sup>2</sup> C device address for the control and VBI readback ports of the <a href="#">ADV7403</a> . When ALSB is set to Logic 0, it sets the address for a write to the control port to Address 0x40 and the readback address for the VBI port to Address 0x21. When ALSB is set to Logic 1, it sets the address for a write to the control port to Address 0x42 and the readback address for the VBI port to Address 0x23.
85	VS_IN	I	VS Input Signal. This pin is used in CP mode for 5-wire timing mode.
86	HS_IN/CS_IN	I	Can be configured in CP mode to be either a digital HS input signal or a digital CS input signal used to extract timing in a 5-wire or 4-wire RGB mode.
98	FIELD/DE	O	Field Synchronization Output Signal for All Interlaced Video Modes (FIELD). This is a multifunction pin. It can also be enabled as a data enable signal (DE) in CP mode to allow direct connection to a HDMI/DVI transmitter IC.
99	VS	O	Vertical Synchronization Output Signal (SDP and CP Modes).

<sup>1</sup> G = ground, P = power, I = input, O = output, I/O = input/output, and NC = no connect.

## FUNCTIONAL OVERVIEW

The following overview provides a brief description of the functionality of the [ADV7403](#). More details are available in the Theory of Operation section.

### ANALOG FRONT END

The analog front end of the [ADV7403](#) provides four 140 MHz ([ADV7403](#)KSTZ-140), NSV, 12-bit ADCs to enable 10-bit video decoding, a multiplexer with 12 analog input channels to enable multisource connection without the requirement of an external multiplexer, and four current and voltage clamp control loops to ensure that dc offsets are removed from the video signal. SCART functionality and standard definition RGB overlay with CVBS are controlled by the fast blank input. This front end also features four antialias filters to remove out-of-band noise on standard definition input video signals.

### STANDARD DEFINITION PROCESSOR (SDP) PIXEL DATA OUTPUT MODES

The [ADV7403](#) features the following SDP output modes:

- 8-/10-bit ITU-R BT.656 4:2:2 YCrCb with embedded time codes and/or HS, VS, and FIELD
- 16-/20-bit YCrCb with embedded time codes and/or HS, VS, and FIELD
- 24-/30-bit YCrCb with embedded time codes and/or HS, VS, and FIELD

### COMPONENT PROCESSOR (CP) PIXEL DATA OUTPUT MODES

The [ADV7403](#) features two single data rate (SDR) outputs: 16-/20-bit 4:2:2 YCrCb for all standards, and 24-/30-bit 4:4:4 YCrCb/RGB for all standards. The [ADV7403](#) also features two double data rate (DDR) outputs: 8-/10-bit 4:2:2 YCrCb for all standards, and 12-bit 4:4:4 YCrCb/RGB for all standards.

### COMPOSITE AND S-VIDEO PROCESSING

The [ADV7403](#) supports NTSC (J, M, 4.43), PAL (B, D, I, G, H, M, N, Nc, 60), and SECAM (B, D, G, K, L) standards for CVBS and S-Video formats. Superadaptive 2D, 5-line comb filters for NTSC and PAL provide superior chrominance and luminance separation for composite video.

The composite and S-Video processing functionalities also include fully automatic detection of switching among worldwide standards (PAL/NTSC/SECAM); automatic gain control (AGC) with white peak mode to ensure that the video is processed without compromising the video processing range; adaptive digital line length tracking (ADLLT™); and proprietary architecture for locking to weak, noisy, and unstable sources from VCRs and tuners. The IF filter block compensates for high frequency luma attenuation due to the tuner SAW filter.

The [ADV7403](#) also features chroma transient improvement (CTI) and luminance digital noise reduction (DNR), as well as teletext, closed captioning (CC), extended data service (EDS), and wide-screen signaling (WSS). It offers certified Macrovision® copy protection detection on composite and S-Video for all worldwide formats (PAL/NTSC/SECAM), and a copy generation management system (CGMS). Other features include 4× oversampling (54 MHz) for CVBS, S-Video, and YUV modes; line-locked clock output (LLC); vertical interval time codes (VITC); support for letterbox detection; a free-run output mode for stable timing when no video input is present; clocking from a single 28.63636 MHz crystal; Gemstar™ 1×/2× electronic program guide compatible; and subcarrier frequency lock (SFL) output for downstream video encoders.

In addition, the device has color controls for hue, brightness, saturation, and contrast and controls for Cr and Cb offsets. The [ADV7403](#) also incorporates a vertical blanking interval data processor and a video programming system (VPS) on the device.

The differential gain of the [ADV7403](#) is 0.4% typical, and the differential phase is 0.4° typical.

### COMPONENT VIDEO PROCESSING

The [ADV7403](#) supports 525i, 625i, 525p, 625p, 720p, 1080i, 1080p, and many other HDTV formats. It provides automatic adjustments for gain (contrast) and offset (brightness), as well as manual adjustment controls. Furthermore, the [ADV7403](#) not only supports analog component YPrPb/RGB video formats with embedded synchronization or with separate HS, VS, and CS, but also supports YCrCb-to-RGB and RGB-to-YCrCb conversions by any-to-any, 3 × 3 color-space conversion matrices.

Standard identification (STDI) enables detection of the component format at the system level, and a synchronization source polarity detector (SSPD) determines the source and polarity of the synchronization signals that accompany the input video.

Certified Macrovision copy protection detection is available on component formats (525i, 625i, 525p, and 625p).

When no video input is present, free-run output mode provides stable timing.

The [ADV7403](#) also supports arbitrary pixel sampling for nonstandard video sources.

## RGB GRAPHICS PROCESSING

The [ADV7403](#) provides 140 MSPS conversion rate support of RGB input resolutions up to  $1280 \times 1024$  at 75 Hz (SXGA) and 110 MSPS conversion rate for the [ADV7403BSTZ-110](#). It also provides automatic or manual clamp and gain controls for graphics modes.

The RGB graphics processing functionality features contrast and brightness controls, automatic detection of synchronization source and polarity by the SSPD block, standard identification enabled by the STDI block, and arbitrary pixel sampling support for nonstandard video sources.

Additional RGB graphics processing features of the [ADV7403](#) include the following:

- 32-phase DLL support of optimum pixel clock sampling.
- Color-space conversion of RGB to YCrCb and decimation to a 4:2:2 format for videocentric back-end IC interfacing.
- Data enable (DE) output signal supplied for direct connection to the HDMI/DVI transmitter IC.

## DIGITAL VIDEO INPUT PORT

The [ADV7403](#) supports raw 8-/10-bit CVBS data from a digital tuner and 24-bit RGB input data from a DVI receiver chip, output converted to YCrCb 4:2:2. It also supports 24-bit 4:4:4, 16-/20-bit 4:2:2 525i, 625i, 525p, 625p, 1080i, 720p, VGA to SXGA at 60 Hz input data from HDMI receiver chip, output converted to 16-bit 4:2:2 YCrCb.

## GENERAL FEATURES

The [ADV7403](#) features HS, VS, and FIELD output signals with programmable position, polarity, and width. It also includes a programmable interrupt request output pin ( $\overline{\text{INT}}$ ), signals SDP/CP status changes, and supports two I<sup>2</sup>C host port interfaces (control and VBI).

The [ADV7403](#) offers low power consumption: 1.8 V digital core, 3.3 V analog and digital input/output, low power power-down mode, and green PC mode.

The [ADV7403BSTZ-110](#) operates over the industrial temperature range ( $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ) and is available in a 100-lead, 14 mm  $\times$  14 mm, RoHS-compliant LQFP.

It is also available in a 140 MHz speed grade ([ADV7403KST-140](#)).

## THEORY OF OPERATION

### ANALOG FRONT END

The [ADV7403](#) analog front end comprises four noise shaped video (NSV®), 12-bit ADCs that digitize the analog video signal before applying it to the standard definition processor (SDP) or component processor (CP). See Table 8 for the maximum sampling rates. The analog front end uses differential channels to each ADC to ensure high performance in a mixed signal application.

The front end also includes a 12-channel input mux that enables multiple video signals to be applied to the [ADV7403](#). Current and voltage clamps are positioned in front of each ADC to ensure that the video signal remains within the range of the converter. Fine clamping of the video signals is performed downstream by digital fine clamping either in the CP or SDP.

Optional antialiasing filters are positioned in front of each ADC. These filters can be used to band-limit standard definition video signals, removing spurious, out-of-band noise.

The ADCs are configured to run in 4× oversampling mode when decoding composite and S-Video inputs; 2× oversampling is performed for component 525i, 625i, 525p, and 625p sources. All other video standards are 1× oversampled. Oversampling the video signals reduces the cost and complexity of external antialiasing filters with the benefit of an increased signal-to-noise ratio (SNR).

The [ADV7403](#) can support simultaneous processing of CVBS and RGB standard definition signals to enable SCART compatibility and overlay functionality. A combination of CVBS and RGB inputs can be mixed and output under control of I²C registers and the fast blank pin.

**Table 8. Maximum ADC Sampling Rates**

Model	Maximum ADC Sampling Rate (MHz)
<a href="#">ADV7403BSTZ-110</a>	110
<a href="#">ADV7403KSTZ-140</a>	140

### STANDARD DEFINITION PROCESSOR (SDP)

The SDP section is capable of decoding a large selection of baseband video signals in composite S-Video and YUV formats. The video standards supported by the SDP include PAL (B, D, I, G, H, M, N, Nc, 60), NTSC (J, M, 4.43), and SECAM (B, D, G, K, L). The [ADV7403](#) can automatically detect the video standard and process it accordingly.

The SDP has a super adaptive 2-D, 5-line comb filter that gives superior chrominance and luminance separation when decoding a composite video signal. This highly adaptive filter automatically adjusts its processing mode according to video standard and signal quality with no user intervention required. The SDP has an IF filter block that compensates for attenuation in the high frequency luma spectrum due to the tuner SAW filter.

The SDP has specific luminance and chrominance parameter control for brightness, contrast, saturation, and hue.

The [ADV7403](#) implements a patented adaptive digital line length tracking (ADLLT™) algorithm to track varying video line lengths from sources such as a VCR. ADLLT enables the [ADV7403](#) to track and decode poor quality video sources such as VCRs, noisy sources from tuner outputs, VCD players, and camcorders. The SDP also contains a chroma transient improvement (CTI) processor. This processor increases the edge rate on chroma transitions, resulting in a sharper video image.

The SDP can process a variety of VBI data services, such as TeleText, closed captioning (CC), wide screen signaling (WSS), video programming system (VPS), vertical interval time codes (VITC), copy generation management system (CGMS), Gemstar 1×/2×, and extended data service (XDS). The [ADV7403](#) SDP section has a Macrovision 7.1 detection circuit that allows it to detect Types I, II, and III protection levels. The decoder is also fully robust to all Macrovision signal inputs.

### COMPONENT PROCESSOR (CP)

The CP section is capable of decoding/digitizing a wide range of component video formats in any color space. Component video standards supported by the CP are 525i, 625i, 525p, 625p, 720p, 1080i, 1250i, VGA up to SXGA at 75 Hz ([ADV7403KSTZ-140](#) only), and many other standards not listed here.

The CP section of the [ADV7403](#) contains an AGC block. When no embedded sync is present, the video gain can be set manually. The AGC section is followed by a digital clamp circuit that ensures that the video signal is clamped to the correct blanking level. Automatic adjustments within the CP include gain (contrast) and offset (brightness); manual adjustment controls are also supported.

A fully programmable any-to-any, 3 × 3 color space conversion matrix is placed between the analog front end and the CP section. This enables YPrPb-to-RGB and RGB-to-YCrCb conversions. Many other standards of color space can be implemented using the color space converter.

The output section of the CP is highly flexible. It can be configured in SDR with one data packet per clock cycle or in a DDR mode where data is presented on the rising and falling edges of the clock. In SDR mode, a 16-/20-bit 4:2:2 or 24-/30-bit 4:4:4 output is possible. In these modes, HS, VS, and FIELD/DE (where applicable) timing reference signals are provided. In DDR mode, the [ADV7403](#) can be configured in an 8-/10-bit 4:2:2 YcrCb or 12-bit 4:4:4 YcrCb/RGB pixel output interface with corresponding timing signals.

The [ADV7403](#) is capable of supporting an external DVI/HDMI receiver. The digital interface expects 24-bit 4:4:4 or 16-/20-bit 4:2:2 bit data (either graphics RGB or component video YcrCb), accompanied by HS, VS, DE, and a fully synchronous clock signal. The data is processed in the CP and output as 16-bit 4:2:2 YcrCb data.

The CP section contains circuitry to enable the detection of Macrovision encoded YPrPb signals for 525i, 625i, 525p, and 625p. It is designed to be fully robust when decoding these types of signals.

VBI extraction of CGMS data is performed by the CP section of the [ADV7403](#) for interlaced, progressive, and high definition scanning rates. The data extracted can be read back over the I<sup>2</sup>C interface. For more detailed product information, see the [ADV7403](#) product page.

## PIXEL INPUT/OUTPUT FORMATTING

Table 9. SDP, CP Pixel Input/Output Pin Map (P19 to P0)

Processor Mode	Format	Pixel Port Pins P[19:0]																			
		19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SDP	Video out, 8-bit, 4:2:2	YcrCb[7:0] <sub>OUT</sub>																			
SDP	Video out, 10-bit, 4:2:2	YcrCb[9:0] <sub>OUT</sub>																			
SDP	Video out, 16-bit, 4:2:2	Y[7:0] <sub>OUT</sub>										CrCb[7:0] <sub>OUT</sub>									
SDP	Video out, 20-bit, 4:2:2	Y[9:0] <sub>OUT</sub>										CrCb[9:0] <sub>OUT</sub>									
SDP	Video out, 24-bit, 4:4:4	Y[7:0] <sub>OUT</sub>										Cb[7:0] <sub>OUT</sub>									
SDP	Video out, 30-bit, 4:4:4	Y[9:0] <sub>OUT</sub>										Cb[9:0] <sub>OUT</sub>									
SM-SDP	Digital tuner input[1]	Output choices are the same as video out 16-/20-bit or pseudo 8-/10-bit DDR																			
CP	8-bit, 4:2:2, DDR	D7	D6	D5	D4	D3	D2	D1	D0												
CP	10-bit, 4:2:2, DDR	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0										
CP	12-bit, 4:4:4, RGB DDR	D7	D6	D5	D4	D3	D2	D1	D0			D11	D10	D9	D8						
CP	Video out, 16-bit, 4:2:2	CHA[7:0] <sub>OUT</sub> (for example, Y[7:0])										CHB/C[7:0] <sub>OUT</sub> (for example, Cr/Cb[7:0])									
CP	Video out, 20-bit, 4:2:2	CHA[9:0] <sub>OUT</sub> (for example, Y[9:0])										CHB/C[9:0] <sub>OUT</sub> (for example, Cr/Cb[9:0])									
CP	Video out, 24-bit, 4:4:4	CHA[7:0] <sub>OUT</sub> (for example, G[7:0])										CHB[7:0] <sub>OUT</sub> (for example, B[7:0])									
CP	Video out, 30-bit, 4:4:4	CHA[9:0] <sub>OUT</sub> (for example, G[9:0])										CHB[9:0] <sub>OUT</sub> (for example, B[9:0])									
SM-CP	HDMI receiver support, 24-bit, 4:4:4 input	CHA[7:0] <sub>OUT</sub> (for example, Y[7:0])									R[5:4] <sub>IN</sub>	CHB/C[7:0] <sub>OUT</sub> (for example, Cr/Cb[7:0])									R[1:0] <sub>IN</sub>
SM-CP	HDMI receiver support 16-bit pass through	CHA[7:0] <sub>OUT</sub> (for example, Y[7:0])										CHB/C[7:0] <sub>OUT</sub> (for example, Cr/Cb[7:0])									
SM-CP	HDMI receiver support, 20-bit, pass through	CHA[9:0] <sub>OUT</sub> (for example, Y[9:0])										CHB/C[9:0] <sub>OUT</sub> (for example, Cr/Cb[9:0])									

Table 10. SDP, CP Pixel Input/Output Pin Map (P40 to P20)

Processor Mode	Format	Pixel Port Pins P[40:31], P[29:20]																			
		40	39	38	37	36	35	34	33	32	31	29	28	27	26	25	24	23	22	21	20
SDP	Video out, 8-bit, 4:2:2																				
SDP	Video out, 10-bit, 4:2:2																				
SDP	Video out, 16-bit, 4:2:2																				
SDP	Video out, 20-bit, 4:2:2																				
SDP	Video out, 24-bit, 4:4:4																				
SDP	Video out, 30-bit, 4:4:4																				
SM-SDP	Digital tuner input[1]	DCVBS[9:0] <sub>IN</sub>																			
CP	8-bit, 4:2:2, DDR																				
CP	10-bit, 4:2:2, DDR																				
CP	12-bit, 4:4:4, RGB DDR																				
CP	Video out, 16-bit, 4:2:2																				
CP	Video out, 20-bit, 4:2:2																				
CP	Video out, 24-bit, 4:4:4 input																				
CP	Video out, 30-bit, 4:4:4 input																				
SM-CP	HDMI receiver support, 24-bit, 4:4:4 input	G[7:0] <sub>IN</sub>								R[7:6] <sub>IN</sub>		B[7:0] <sub>IN</sub>						R[3:2] <sub>IN</sub>			
SM-CP	HDMI receiver support, 16-bit, pass through	CHA[7:0] <sub>IN</sub> (for example, Y[7:0])										CHB/C[7:0] <sub>IN</sub> (for example, Cr/Cb[7:0])									
SM-CP	HDMI receiver support, 20-bit, pass through	CHA[9:0] <sub>IN</sub> (for example, Y[9:0])										CHB/C[9:0] <sub>IN</sub> (for example, Cr/Cb[9:0])									



## RECOMMENDED EXTERNAL LOOP FILTER COMPONENTS

Place the external loop filter components for the ELPF pin as close as possible to the respective pins. Figure 8 shows the recommended component values.

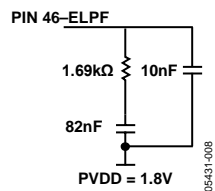
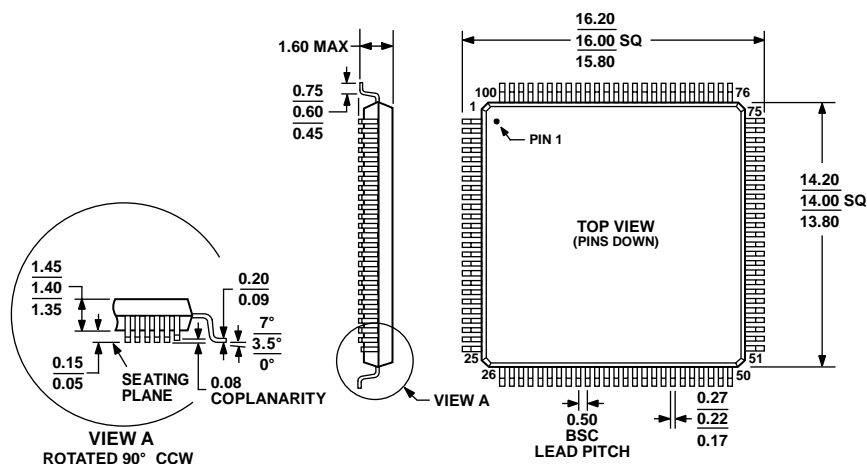


Figure 8. ELPF Components

[illegible]

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## OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-026-BED

Figure 10. 100-Lead Low Profile Quad Flat Package [LQFP]  
(ST-100)

Dimensions shown in millimeters

051706-A

## ORDERING GUIDE

Model <sup>1, 2</sup>	Temperature Range	Package Description	Package Option
ADV7403BSTZ-110	−40°C to +85°C	100-Lead Low Profile Quad Flat Package [LQFP]	ST-100
ADV7403KSTZ-140	0°C to 70°C	100-Lead Low Profile Quad Flat Package [LQFP]	ST-100
EVAL-ADV7403EBZ		Evaluation Board	

<sup>1</sup> The **ADV7403** is a Pb-free, environmentally friendly product. It is manufactured using the most up-to-date materials and processes. The coating on the leads of each device is 100% pure Sn electroplate. The device is suitable for Pb-free applications and is able to withstand surface-mount soldering at up to 255°C (±5°C). In addition, it is backward-compatible with conventional SnPb soldering processes. This means that the electroplated Sn coating can be soldered with SnPb solder pastes at conventional reflow temperatures of 220°C to 235°C.

<sup>2</sup> Z = RoHS Compliant Part.