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5/12—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS—5 V OPERATION

All typical specifications are at T_A = 25°C, V_{DD1} = V_{DD2} = 5 V. Minimum/maximum specifications apply over the entire recommended operation range of 4.5 V ≤ V_{DD1} ≤ 5.5 V, 4.5 V ≤ V_{DD2} ≤ 5.5 V, and −40°C ≤ T_A ≤ +105°C, unless otherwise noted. Switching specifications are tested with C_L = 15 pF and CMOS signal levels, unless otherwise noted.

Table 1.

		A Grade			C Grade				
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions/Comments**
SWITCHING SPECIFICATIONS									
Pulse Width	PW	250			40			ns	Within PWD limit
Data Rate				1			25	Mbps	Within PWD limit
Propagation Delay	t_{PHL}, t_{PLH}		50	75	32	41	50	ns	50% input to 50% output
Pulse Width Distortion	PWD		10	25		2	5	ns	$\|t_{PLH} - t_{PHL}\|$
Change vs. Temperature			5			3		ps/°C	
Propagation Delay Skew[1]	t_{PSK}			20			10	ns	
Channel Matching									
Codirectional	t_{PSKCD}			25		2	4	ns	
Opposing Direction	t_{PSKOD}			30		2	6	ns	
Jitter			2			2		ns	

[1] t_{PSK} is the magnitude of the worst-case difference in t_{PHL} or t_{PLH} that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions.

Table 2.

		1 Mbps—A, C Grades			25 Mbps—C Grade				
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions/Comments**
SUPPLY CURRENT									
ADuM7240	I_{DD1}		2.2	2.8		16	21	mA	
	I_{DD2}		1.7	2.2		3.9	5.7	mA	
ADuM7241	I_{DD1}		1.9	2.4		9.3	13	mA	
	I_{DD2}		1.9	2.4		8.2	12	mA	

Table 3. For All Models

Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions/Comments**
DC SPECIFICATIONS						
Logic High Input Threshold	V_{IH}	0.7 V_{DDx}			V	
Logic Low Input Threshold	V_{IL}			0.3 V_{DDx}	V	
Logic High Output Voltages	V_{OH}	V_{DDx} − 0.1	V_{DDx}		V	I_{Ox} = −20 µA, V_{Ix} = V_{IxH}
		V_{DDx} − 0.4	V_{DDx} − 0.3		V	I_{Ox} = −4 mA, V_{Ix} = V_{IxH}
Logic Low Output Voltages	V_{OL}		0.0	0.1	V	I_{Ox} = 20 µA, V_{Ix} = V_{IxL}
			0.2	0.4	V	I_{Ox} = 4 mA, V_{Ix} = V_{IxL}
Input Current per Channel	I_I	−10	+0.01	+10	µA	0 V ≤ V_{Ix} ≤ V_{DDx}
Supply Current per Channel						
Quiescent Input Supply Current	$I_{DDI(Q)}$		1	1.4	mA	
Quiescent Output Supply Current	$I_{DDO(Q)}$		0.8	1.1	mA	
Dynamic Input Supply Current	$I_{DDI(D)}$		0.29		mA/Mbps	
Dynamic Output Supply Current	$I_{DDO(D)}$		0.03		mA/Mbps	
AC SPECIFICATIONS						
Output Rise/Fall Time	t_R/t_F		2.0		ns	10% to 90%
Common-Mode Transient Immunity[1]	|CM|	15	25		kV/µs	V_{Ix} = V_{DDx}, V_{CM} = 1000 V, transient magnitude = 800 V
Refresh Rate	f_r		600		kHz	DC data inputs

[1] |CM| is the maximum common-mode voltage slew rate that can be sustained while maintaining V_O > 0.8 V_{DDx}. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

ELECTRICAL CHARACTERISTICS—3.3 V OPERATION

All typical specifications are at T_A = 25°C, V_{DD1} = V_{DD2} = 3.3 V. Minimum/maximum specifications apply over the entire recommended operation range of 3.0 V ≤ V_{DD1} ≤ 3.6 V, 3.0 V ≤ V_{DD2} ≤ 3.6 V, and −40°C ≤ T_A ≤ +105°C, unless otherwise noted. Switching specifications are tested with C_L = 15 pF and CMOS signal levels, unless otherwise noted.

Table 4.

Parameter	Symbol	A Grade Min	A Grade Typ	A Grade Max	C Grade Min	C Grade Typ	C Grade Max	Unit	Test Conditions/Comments
SWITCHING SPECIFICATIONS									
Pulse Width	PW	250			40			ns	Within PWD limit
Data Rate				1			25	Mbps	Within PWD limit
Propagation Delay	t_{PHL}, t_{PLH}		60	85	37	50	64	ns	50% input to 50% output
Pulse Width Distortion	PWD		10	25		2	5	ns	$\|t_{PLH} - t_{PHL}\|$
Change vs. Temperature			5			3		ps/°C	
Propagation Delay Skew[1]	t_{PSK}			20			10	ns	
Channel Matching									
Codirectional	t_{PSKCD}			25		2	4	ns	
Opposing Direction	t_{PSKOD}			30		2	7	ns	
Jitter			2			2		ns	

[1] t_{PSK} is the magnitude of the worst-case difference in t_{PHL} or t_{PLH} that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions.

Table 5.

Parameter	Symbol	1 Mbps—A, C Grades Min	1 Mbps—A, C Grades Typ	1 Mbps—A, C Grades Max	25 Mbps—C Grade Min	25 Mbps—C Grade Typ	25 Mbps—C Grade Max	Unit	Test Conditions/Comments
SUPPLY CURRENT									
ADuM7240	I_{DD1}		1.6	2.0		12	15	mA	
	I_{DD2}		1.3	1.6		2.6	4.4	mA	
ADuM7241	I_{DD1}		1.4	1.8		6.7	9.2	mA	
	I_{DD2}		1.4	1.8		5.9	8.2	mA	

Table 6. For All Models

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DC SPECIFICATIONS						
Logic High Input Threshold	V_{IH}	0.7 V_{DDx}			V	
Logic Low Input Threshold	V_{IL}			0.3 V_{DDx}	V	
Logic High Output Voltages	V_{OH}	V_{DDx} − 0.2	V_{DDx}		V	I_{Ox} = −20 µA, V_{Ix} = V_{IxH}
		V_{DDx} − 0.4	V_{DDx} − 0.3		V	I_{Ox} = −4 mA, V_{Ix} = V_{IxH}
Logic Low Output Voltages	V_{OL}		0.0	0.1	V	I_{Ox} = 20 µA, V_{Ix} = V_{IxL}
			0.2	0.4	V	I_{Ox} = 4 mA, V_{Ix} = V_{IxL}
Input Current per Channel	I_I	−10	+0.01	+10	µA	0 V ≤ V_{Ix} ≤ V_{DDx}
Supply Current per Channel						
Quiescent Input Supply Current	$I_{DDI(Q)}$		0.71	1.0	mA	
Quiescent Output Supply Current	$I_{DDO(Q)}$		0.59	0.8	mA	
Dynamic Input Supply Current	$I_{DDI(D)}$		0.20		mA/Mbps	
Dynamic Output Supply Current	$I_{DDO(D)}$		0.02		mA/Mbps	
AC SPECIFICATIONS						
Output Rise/Fall Time	t_R/t_F		2.8		ns	10% to 90%
Common-Mode Transient Immunity[1]	|CM|	15	25		kV/µs	V_{Ix} = V_{DDx}, V_{CM} = 1000 V, transient magnitude = 800 V
Refresh Rate	f_r		550		kHz	DC data inputs

[1] |CM| is the maximum common-mode voltage slew rate that can be sustained while maintaining V_O > 0.8 V_{DDx}. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

ELECTRICAL CHARACTERISTICS—MIXED 5 V/3.3 V OPERATION

All typical specifications are at T_A = 25°C, V_{DD1} = 5 V, V_{DD2} = 3.3 V. Minimum/maximum specifications apply over the entire recommended operation range of 4.5 V ≤ V_{DD1} ≤ 5.5 V, 3.0 V ≤ V_{DD2} ≤ 3.6 V, and −40°C ≤ T_A ≤ +105°C, unless otherwise noted. Switching specifications are tested with C_L = 15 pF and CMOS signal levels, unless otherwise noted.

Table 7.

Parameter	Symbol	A Grade			C Grade			Unit	Test Conditions/Comments
		Min	Typ	Max	Min	Typ	Max		
SWITCHING SPECIFICATIONS									
Pulse Width	PW	250			40			ns	Within PWD limit
Data Rate				1			25	Mbps	Within PWD limit
Propagation Delay	t_{PHL}, t_{PLH}		55	80	34	44	54	ns	50% input to 50% output
Pulse Width Distortion	PWD		10	25		2	5	ns	$\|t_{PLH} - t_{PHL}\|$
Change vs. Temperature			5			3		ps/°C	
Propagation Delay Skew[1]	t_{PSK}			20			10	ns	
Channel Matching									
Codirectional	t_{PSKCD}			25		2	5	ns	
Opposing Direction	t_{PSKOD}			30		3	9	ns	
Jitter			2			2		ns	

[1] t_{PSK} is the magnitude of the worst-case difference in t_{PHL} or t_{PLH} that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions.

Table 8.

Parameter	Symbol	1 Mbps—A, C Grades			25 Mbps—C Grade			Unit	Test Conditions/Comments
		Min	Typ	Max	Min	Typ	Max		
SUPPLY CURRENT									
ADuM7240	I_{DD1}		2.2	2.9		16	21	mA	
	I_{DD2}		1.3	1.6		2.8	3.6	mA	
ADuM7241	I_{DD1}		1.9	2.3		9.2	12	mA	
	I_{DD2}		1.4	1.6		5.9	7.2	mA	

Table 9. For All Models

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DC SPECIFICATIONS						
Logic High Input Threshold	V_{IH}	0.7 V_{DDx}			V	
Logic Low Input Threshold	V_{IL}			0.3 V_{DDx}	V	
Logic High Output Voltages	V_{OH}	V_{DDx} − 0.1	V_{DDx}		V	I_{Ox} = −20 µA, $V_{Ix} = V_{IxH}$
		V_{DDx} − 0.4	V_{DDx} − 0.3		V	I_{Ox} = −4 mA, $V_{Ix} = V_{IxH}$
Logic Low Output Voltages	V_{OL}		0.0	0.1	V	I_{Ox} = 20 µA, $V_{Ix} = V_{IxL}$
			0.2	0.4	V	I_{Ox} = 4 mA, $V_{Ix} = V_{IxL}$
Input Current per Channel	I_I	−10	+0.01	+10	µA	0 V ≤ V_{Ix} ≤ V_{DDx}
Supply Current per Channel						
Quiescent Input Supply Current	$I_{DDI(Q)}$		1.0	1.45	mA	
Quiescent Output Supply Current	$I_{DDO(Q)}$		0.59	0.80	mA	
Dynamic Input Supply Current	$I_{DDI(D)}$		0.25		mA/Mbps	
Dynamic Output Supply Current	$I_{DDO(D)}$		0.02		mA/Mbps	
AC SPECIFICATIONS						
Output Rise/Fall Time	t_R/t_F		2.5		ns	10% to 90%
Common-Mode Transient Immunity[1]	|CM|	15	25		kV/µs	$V_{Ix} = V_{DDx}$, V_{CM} = 1000 V, transient magnitude = 800 V
Refresh Rate	f_r		600		kHz	DC data inputs

[1] \|CM\| is the maximum common-mode voltage slew rate that can be sustained while maintaining V_O > 0.8 V_{DDx}. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

ELECTRICAL CHARACTERISTICS—MIXED 3.3 V/5 V OPERATION

All typical specifications are at T_A = 25°C, V_{DD1} = 3.3 V, V_{DD2} = 5 V. Minimum/maximum specifications apply over the entire recommended operation range of 3.0 V ≤ V_{DD1} ≤ 3.6 V, 4.5 V ≤ V_{DD2} ≤ 5.5 V, and −40°C ≤ T_A ≤ +105°C, unless otherwise noted. Switching specifications are tested with C_L = 15 pF and CMOS signal levels, unless otherwise noted.

Table 10.

Parameter	Symbol	A Grade			C Grade			Unit	Test Conditions/Comments
		Min	Typ	Max	Min	Typ	Max		
SWITCHING SPECIFICATIONS									
Pulse Width	PW	250			40			ns	Within PWD limit
Data Rate				1			25	Mbps	Within PWD limit
Propagation Delay	t_{PHL}, t_{PLH}		55	80	35	47	59	ns	50% input to 50% output
Pulse Width Distortion	PWD		10	25		2	5	ns	$\|t_{PLH} − t_{PHL}\|$
Change vs. Temperature			5			3		ps/°C	
Propagation Delay Skew[1]	t_{PSK}			20			10	ns	
Channel Matching									
Codirectional	t_{PSKCD}			25		2	5	ns	
Opposing Direction	t_{PSKOD}			30		5	10	ns	
Jitter			2			2		ns	

[1] t_{PSK} is the magnitude of the worst-case difference in t_{PHL} or t_{PLH} that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions.

Table 11.

Parameter	Symbol	1 Mbps—A, C Grades			25 Mbps—C Grade			Unit	Test Conditions/Comments
		Min	Typ	Max	Min	Typ	Max		
SUPPLY CURRENT									
ADuM7240	I_{DD1}		1.6	2.0		12	15	mA	
	I_{DD2}		1.7	2.1		3.8	4.8	mA	
ADuM7241	I_{DD1}		1.4	1.6		6.8	8.2	mA	
	I_{DD2}		1.9	2.3		8.2	10.2	mA	

Table 12. For All Models

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DC SPECIFICATIONS						
Logic High Input Threshold	V_{IH}	0.7 V_{DDx}			V	
Logic Low Input Threshold	V_{IL}			0.3 V_{DDx}	V	
Logic High Output Voltages	V_{OH}	V_{DDx} − 0.1	V_{DDx}		V	I_{Ox} = −20 µA, V_{Ix} = V_{IxH}
		V_{DDx} − 0.4	V_{DDx} − 0.3		V	I_{Ox} = −4 mA, V_{Ix} = V_{IxH}
Logic Low Output Voltages	V_{OL}		0.0	0.1	V	I_{Ox} = 20 µA, V_{Ix} = V_{IxL}
			0.2	0.4	V	I_{Ox} = 4 mA, V_{Ix} = V_{IxL}
Input Current per Channel	I_I	−10	+0.01	+10	µA	0 V ≤ V_{Ix} ≤ V_{DDx}
Supply Current per Channel						
Quiescent Input Supply Current	$I_{DDI(Q)}$		0.71	1.0	mA	
Quiescent Output Supply Current	$I_{DDO(Q)}$		0.80	1.1	mA	
Dynamic Input Supply Current	$I_{DDI(D)}$		0.20		mA/Mbps	
Dynamic Output Supply Current	$I_{DDO(D)}$		0.03		mA/Mbps	
AC SPECIFICATIONS						
Output Rise/Fall Time	t_R/t_F		2.5		ns	10% to 90%
Common-Mode Transient Immunity[1]	|CM|	15	25		kV/µs	V_{Ix} = V_{DDx}, V_{CM} = 1000 V, transient magnitude = 800 V
Refresh Rate	f_r		550		kHz	DC data inputs

[1] |CM| is the maximum common-mode voltage slew rate that can be sustained while maintaining V_O > 0.8 V_{DDx}. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

PACKAGE CHARACTERISTICS

Table 13.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Resistance (Input-to-Output)[1]	R_{I-O}		10^{13}		Ω	
Capacitance (Input-to-Output)[1]	C_{I-O}		2		pF	f = 1 MHz
Input Capacitance[2]	C_I		4		pF	
IC Junction-to-Ambient Thermal Resistance	θ_{JA}		85		°C/W	Thermocouple located at center of package underside

[1] The device is considered a 2-terminal device: Pin 1 through Pin 4 are shorted together, and Pin 5 through Pin 8 are shorted together.
[2] Input capacitance is from any input data pin to ground.

REGULATORY INFORMATION

The ADuM7240/ADuM7241 are pending approval by the organizations listed in Table 14. See Table 18 and the Insulation Lifetime section for recommended maximum working voltages for specific cross-isolation waveforms and insulation levels.

Table 14.

UL
Recognized Under UL 1577 Component Recognition Program[1]
Single Protection, 1000 V rms Isolation Voltage
File E214100

[1] In accordance with UL 1577, each ADuM7240/ADuM7241 is proof tested by applying an insulation test voltage ≥1200 V rms for 1 sec (current leakage detection limit = 5 µA).

INSULATION AND SAFETY-RELATED SPECIFICATIONS

Table 15.

Parameter	Symbol	Value	Unit	Test Conditions/Comments
Rated Dielectric Insulation Voltage		1000	V rms	1-minute duration
Minimum External Air Gap (Clearance)	L(I01)	4.0	mm min	Measured from input terminals to output terminals, shortest distance through air
Minimum External Tracking (Creepage)	L(I02)	4.0	mm min	Measured from input terminals to output terminals, shortest distance path along body
Minimum Internal Gap (Internal Clearance)		2.6	µm min	Distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>175	V	DIN IEC 112/VDE 0303 Part 1
Isolation Group		IIIa		Material Group (DIN VDE 0110, 1/89, Table 1)

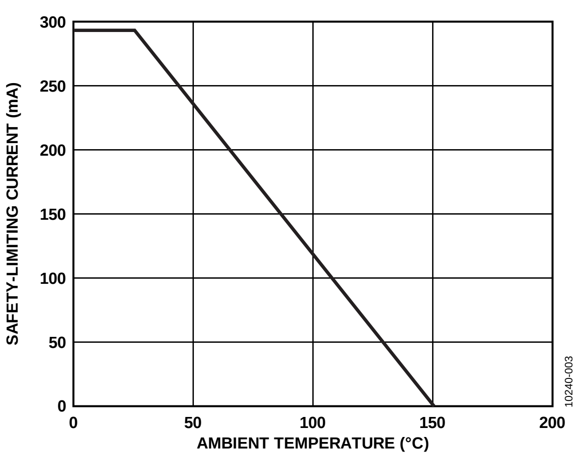


Figure 3. Thermal Derating Curve, Dependence of Safety-Limiting Values with Ambient Temperature per DIN V VDE V 0884-10

RECOMMENDED OPERATING CONDITIONS

Table 16.

Parameter	Symbol	Min	Max	Unit
Operating Temperature	T_A	−40	+105	°C
Supply Voltages[1]	V_{DD1}, V_{DD2}	3.0	5.5	V
Input Signal Rise and Fall Times			1.0	ms

[1] All voltages are relative to their respective ground. See the DC Correctness section for information about immunity to external magnetic fields.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

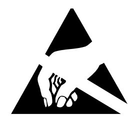
Table 17.

Parameter	Rating
Storage Temperature (T_{ST}) Range	−65°C to +150°C
Ambient Operating Temperature (T_A) Range	−40°C to +105°C
Supply Voltages (V_{DD1}, V_{DD2})	−0.5 V to +7.0 V
Input Voltages (V_{IA}, V_{IB})[1]	−0.5 V to V_{DDI} + 0.5 V
Output Voltages (V_{OA}, V_{OB})[1]	−0.5 V to V_{DDO} + 0.5 V
Average Output Current per Pin[2]	
Side 1 (I_{O1})	−10 mA to +10 mA
Side 2 (I_{O2})	−10 mA to +10 mA
Common-Mode Transients[3]	−100 kV/µs to +100 kV/µs

[1] V_{DDI} and V_{DDO} refer to the supply voltages on the input and output sides of a given channel, respectively. See the Printed Circuit Board Layout section.
[2] See Figure 3 for maximum rated current values for various temperatures.
[3] Refers to common-mode transients across the insulation barrier. Common-mode transients exceeding the absolute maximum ratings may cause latch-up or permanent damage.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

Table 18. Maximum Continuous Working Voltage[1]

Parameter	Max	Unit	Constraint
AC Voltage, Bipolar Waveform	300	V rms	50-year minimum lifetime
DC Voltage	300	V dc	50-year minimum lifetime

[1] Refers to continuous voltage magnitude imposed across the isolation barrier. See the Insulation Lifetime section for more details.

Table 19. ADuM7240 Truth Table (Positive Logic)[1]

V_{IA} Input	V_{IB} Input	V_{DD1} State	V_{DD2} State	V_{OA} Output	V_{OB} Output	Notes
H	H	Powered	Powered	H	H	
L	L	Powered	Powered	L	L	
H	L	Powered	Powered	H	L	
L	H	Powered	Powered	L	H	
X	X	Unpowered	Powered	H	H	Outputs return to the input state within 1 µs of V_{DDI} power restoration.
X	X	Powered	Unpowered	Indeterminate	Indeterminate	Outputs return to the input state within 1 µs of V_{DDO} power restoration.

[1] H = high, L = low, X = don't care.

Table 20. ADuM7241 Truth Table (Positive Logic)[1]

V_{IA} Input	V_{IB} Input	V_{DD1} State	V_{DD2} State	V_{OA} Output	V_{OB} Output	Notes
H	H	Powered	Powered	H	H	
L	L	Powered	Powered	L	L	
H	L	Powered	Powered	H	L	
L	H	Powered	Powered	L	H	
X	X	Unpowered	Powered	Indeterminate	H	Outputs return to the input state within 1 µs of V_{DDI} power restoration.
X	X	Powered	Unpowered	H	Indeterminate	Outputs return to the input state within 1 µs of V_{DDO} power restoration.

[1] H = high, L = low, X = don't care.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

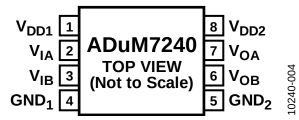


Figure 4. ADuM7240 Pin Configuration

Table 21. ADuM7240 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{DD1}	3.0 V to 5.5 V Supply Voltage for Isolator Side 1.
2	V_{IA}	Logic Input A.
3	V_{IB}	Logic Input B.
4	GND_1	Ground 1. Ground reference for Isolator Side 1.
5	GND_2	Ground 2. Ground reference for Isolator Side 2.
6	V_{OB}	Logic Output B.
7	V_{OA}	Logic Output A.
8	V_{DD2}	3.0 V to 5.5 V Supply Voltage for Isolator Side 2.

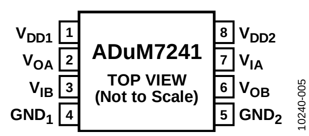


Figure 5. ADuM7241 Pin Configuration

Table 22. ADuM7241 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{DD1}	3.0 V to 5.5 V Supply Voltage for Isolator Side 1.
2	V_{OA}	Logic Output A.
3	V_{IB}	Logic Input B.
4	GND_1	Ground 1. Ground reference for Isolator Side 1.
5	GND_2	Ground 2. Ground reference for Isolator Side 2.
6	V_{OB}	Logic Output B.
7	V_{IA}	Logic Input A.
8	V_{DD2}	3.0 V to 5.5 V Supply Voltage for Isolator Side 2.

TYPICAL PERFORMANCE CHARACTERISTICS

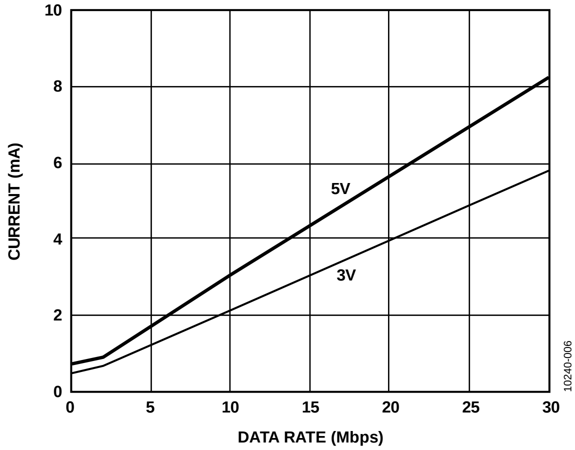


Figure 6. Typical Supply Current per Input Channel vs. Data Rate for 5 V and 3 V Operation

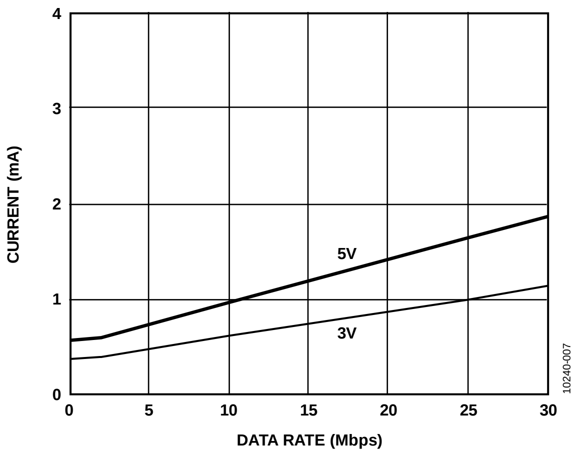


Figure 7. Typical Supply Current per Output Channel vs. Data Rate for 5 V and 3 V Operation (No Output Load)

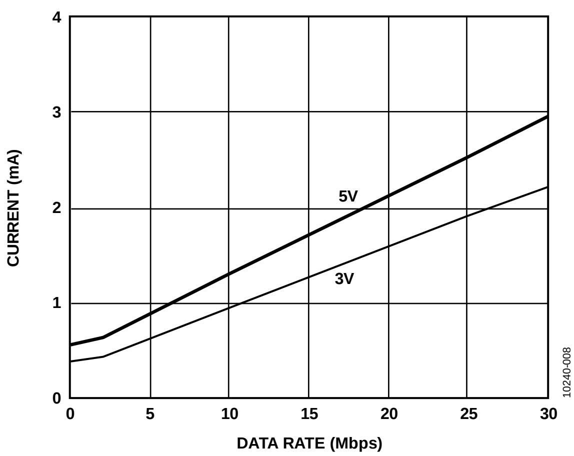


Figure 8. Typical Supply Current per Output Channel vs. Data Rate for 5 V and 3 V Operation (15 pF Output Load)

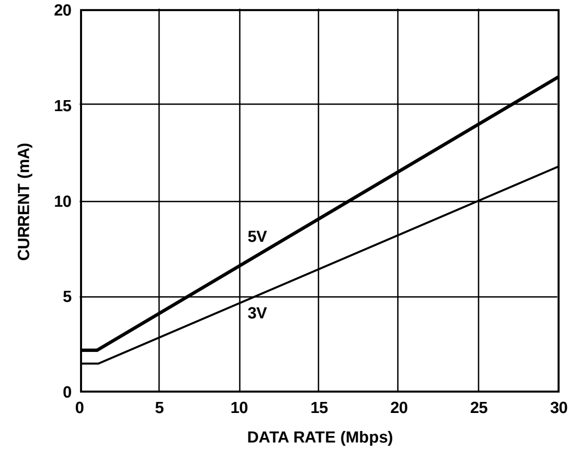


Figure 9. Typical ADuM7240 V_{DD1} Supply Current vs. Data Rate for 5 V and 3 V Operation

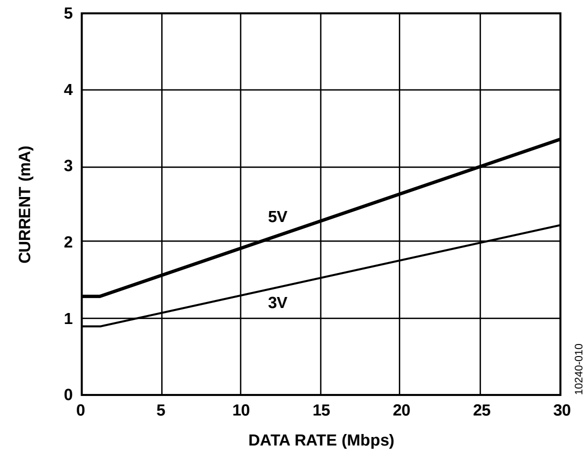


Figure 10. Typical ADuM7240 V_{DD2} Supply Current vs. Data Rate for 5 V and 3 V Operation

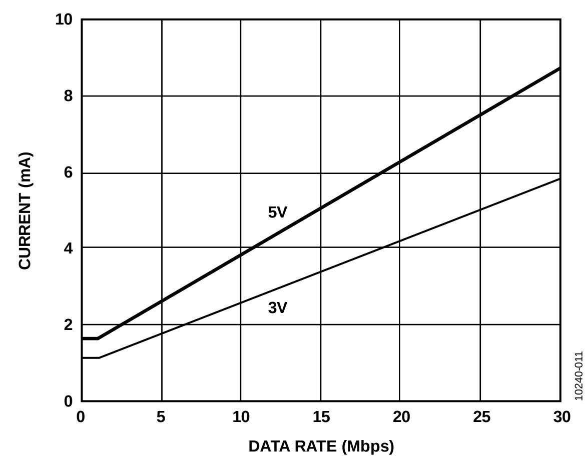


Figure 11. Typical ADuM7241 V_{DD1} Supply Current vs. Data Rate for 5 V and 3 V Operation

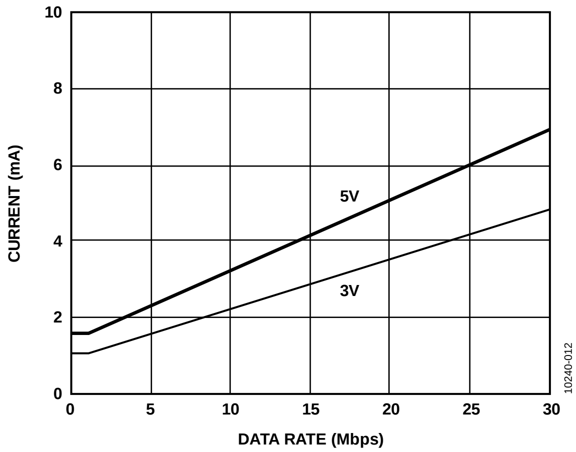


Figure 12. Typical ADuM7241 V_{DD2} Supply Current vs. Data Rate for 5 V and 3 V Operation

APPLICATIONS INFORMATION

PRINTED CIRCUIT BOARD LAYOUT

The ADuM7240/ADuM7241 digital isolators require no external interface circuitry for the logic interfaces. Power supply bypassing is strongly recommended at both input and output supply pins: V_{DD1} and V_{DD2}. The capacitor value should be between 0.01 µF and 0.1 µF. The total lead length between both ends of the capacitor and the input power supply pin should not exceed 20 mm.

In applications involving high common-mode transients, it is important to minimize board coupling across the isolation barrier. Furthermore, users should design the board layout so that any coupling that does occur affects all pins on a given component side equally. Failure to ensure this can cause voltage differentials between pins exceeding the absolute maximum ratings of the device, thereby leading to latch-up or permanent damage.

With proper PCB design choices, the ADuM7240/ADuM7241 can readily meet CISPR 22 Class A (and FCC Class A) emissions standards, as well as the more stringent CISPR 22 Class B (and FCC Class B) standards in an unshielded environment. Refer to the AN-1109 Application Note for PCB-related EMI mitigation techniques, including board layout and stack-up issues.

PROPAGATION DELAY-RELATED PARAMETERS

Propagation delay is a parameter that describes the time it takes a logic signal to propagate through a component. The input-to-output propagation delay time for a high-to-low transition may differ from the propagation delay time for a low-to-high transition.

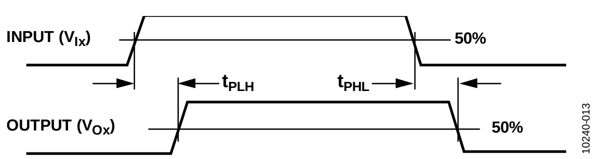


Figure 13. Propagation Delay Parameters

Pulse width distortion is the maximum difference between these two propagation delay values and is an indication of how accurately the timing of the input signal is preserved.

Channel-to-channel matching refers to the maximum amount that the propagation delay differs between channels within a single ADuM7240/ADuM7241 component.

Propagation delay skew refers to the maximum amount the propagation delay differs between multiple ADuM7240/ADuM7241 components operating under the same conditions.

DC CORRECTNESS

Positive and negative logic transitions at the isolator input cause narrow (~1 ns) pulses to be sent to the decoder via the transformer. The decoder is bistable and is, therefore, either set or reset by the pulses, indicating input logic transitions. In the absence of logic transitions at the input for more than ~1 µs, a periodic set of refresh pulses indicative of the correct input state is sent to ensure dc correctness at the output. If the decoder receives no internal pulses for more than approximately 5 µs, the input side is assumed to be unpowered or nonfunctional, and the isolator output is forced to a default high state by the watchdog timer circuit.

MAGNETIC FIELD IMMUNITY

The magnetic field immunity of the ADuM7240/ADuM7241 is determined by the changing magnetic field, which induces a voltage in the transformer's receiving coil large enough to either falsely set or reset the decoder. The following analysis defines the conditions under which this can occur. The 3 V operating condition of the ADuM7240/ADuM7241 is examined because it represents the most susceptible mode of operation.

The pulses at the transformer output have an amplitude greater than 1.0 V. The decoder has a sensing threshold at about 0.5 V, thus establishing a 0.5 V margin in which induced voltages can be tolerated. The voltage induced across the receiving coil is given by

$$V = (-d\beta/dt) \sum \pi r_n^2; n = 1, 2, \dots, N$$

where:
β is the magnetic flux density (gauss).
r_n is the radius of the n^{th} turn in the receiving coil (cm).
N is the number of turns in the receiving coil.

Given the geometry of the receiving coil in the ADuM7240/ADuM7241 and an imposed requirement that the induced voltage be, at most, 50% of the 0.5 V margin at the decoder, a maximum allowable magnetic field at a given frequency can be calculated. The result is shown in Figure 14.

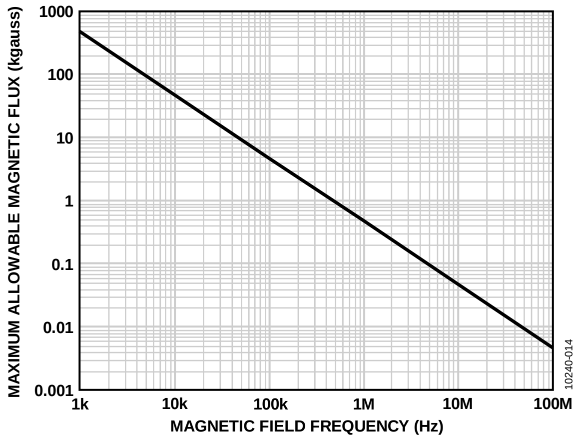


Figure 14. Maximum Allowable External Magnetic Flux Density

For example, at a magnetic field frequency of 1 MHz, the maximum allowable magnetic field of 0.5 kgauss induces a voltage of 0.25 V at the receiving coil. This voltage is about 50% of the sensing threshold and does not cause a faulty output transition. Similarly, if such an event occurs during a transmitted pulse (and is of the worst-case polarity), it reduces the received pulse from >1.0 V to 0.75 V, still well above the 0.5 V sensing threshold of the decoder.

The preceding magnetic flux density values correspond to specific current magnitudes at given distances from the ADuM7240/ADuM7241 transformers. Figure 15 shows these allowable current magnitudes as a function of frequency for selected distances. As shown in Figure 15, the ADuM7240/ ADuM7241 is extremely immune and can be affected only by extremely large currents operated at high frequency very close to the component. For the 1 MHz example, a 1.2 kA current placed 5 mm away from the ADuM7240/ADuM7241 is required to affect the operation of the component.

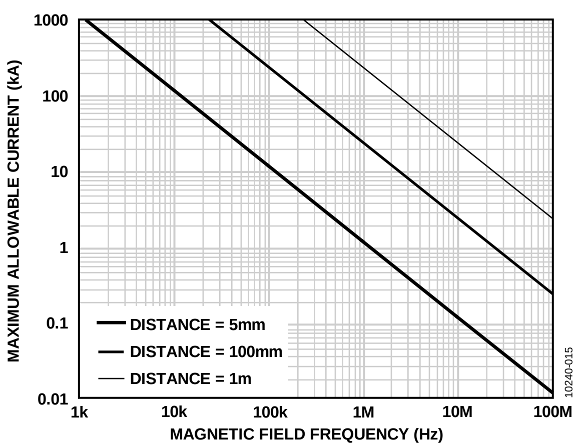


Figure 15. Maximum Allowable Current for Various Current-to-ADuM7240/ADuM7241 Spacings

Note that with extreme combinations of strong magnetic field and high frequency current, loops formed by printed circuit board traces can induce error voltages large enough to trigger the thresholds of receiver circuitry. Take care in the layout of such traces to avoid this possibility.

POWER CONSUMPTION

The supply current at a given channel of the ADuM7240/ ADuM7241 isolator is a function of the supply voltage, the data rate of the channel, and the output load of the channel.

For each input channel, the supply current is given by

$$I_{DDI} = I_{DDI(Q)} \qquad f \le 0.5\, f_r$$

$$I_{DDI} = I_{DDI(D)} \times (2f - f_r) + I_{DDI(Q)} \qquad f > 0.5\, f_r$$

For each output channel, the supply current is given by

$$I_{DDO} = I_{DDO(Q)} \qquad f \le 0.5\, f_r$$

$$I_{DDO} = (I_{DDO(D)} + (0.5 \times 10^{-3}) \times C_L \times V_{DDO}) \times (2f - f_r) + I_{DDO(Q)} \qquad f > 0.5\, f_r$$

where:

$I_{DDI(D)}$, $I_{DDO(D)}$ are the input and output dynamic supply currents per channel (mA/Mbps).
C_L is the output load capacitance (pF).
V_{DDO} is the output supply voltage (V).
f is the input logic signal frequency (MHz); it is half the input data rate, expressed in units of Mbps.
f_r is the input stage refresh rate (Mbps).
$I_{DDI(Q)}$, $I_{DDO(Q)}$ are the specified input and output quiescent supply currents (mA).

To calculate the total V_{DD1} and V_{DD2} supply current, the supply currents for each input and output channel corresponding to V_{DD1} and V_{DD2} are calculated and totaled. Figure 6 and Figure 7 show per-channel supply currents as a function of data rate for an unloaded output condition. Figure 8 shows the per-channel supply current as a function of data rate for a 15 pF output condition. Figure 9 through Figure 12 show the total V_{DD1} and V_{DD2} supply current as a function of data rate for ADuM7240 and ADuM7241 channel configurations.

INSULATION LIFETIME

All insulation structures eventually break down when subjected to voltage stress over a sufficiently long period. The rate of insulation degradation is dependent on the characteristics of the voltage waveform applied across the insulation. In addition to the testing performed by the regulatory agencies, Analog Devices carries out an extensive set of evaluations to determine the lifetime of the insulation structure within the ADuM7240/ ADuM7241.

Analog Devices performs accelerated life testing using voltage levels higher than the rated continuous working voltage. Acceleration factors for several operating conditions are determined. These factors allow calculation of the time to failure at the actual working voltage. The values shown in Table 18 summarize the working voltage for 50 years of service life.

OUTLINE DIMENSIONS

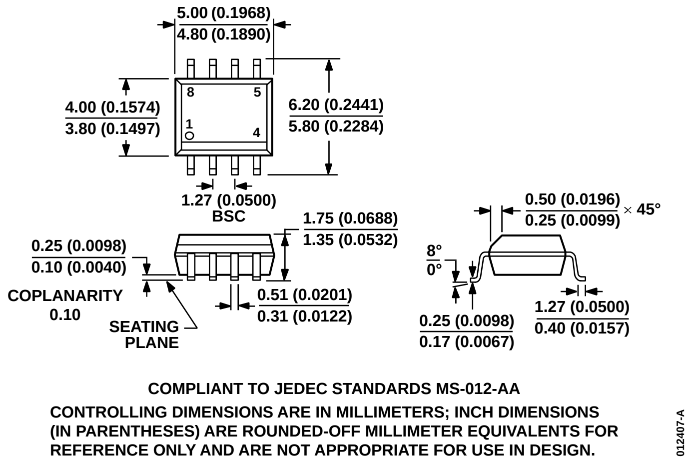


Figure 16. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body (R-8)
Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model[1]	No. of Inputs, V_{DD1} Side	No. of Inputs, V_{DD2} Side	Maximum Data Rate (Mbps)	Maximum Propagation Delay, 5 V (ns)	Temperature Range	Package Description	Package Option
ADuM7240ARZ	2	0	1	75	−40°C to +105°C	8-Lead SOIC_N	R-8
ADuM7240ARZ-RL7	2	0	1	75	−40°C to +105°C	8-Lead SOIC_N, 7" Tape and Reel	R-8
ADuM7240CRZ	2	0	25	50	−40°C to +105°C	8-Lead SOIC_N	R-8
ADuM7240CRZ-RL7	2	0	25	50	−40°C to +105°C	8-Lead SOIC_N, 7" Tape and Reel	R-8
ADuM7241ARZ	1	1	1	75	−40°C to +105°C	8-Lead SOIC_N	R-8
ADuM7241ARZ-RL7	1	1	1	75	−40°C to +105°C	8-Lead SOIC_N, 7" Tape and Reel	R-8
ADuM7241CRZ	1	1	25	50	−40°C to +105°C	8-Lead SOIC_N	R-8
ADuM7241CRZ-RL7	1	1	25	50	−40°C to +105°C	8-Lead SOIC_N, 7" Tape and Reel	R-8

[1] Z = RoHS Compliant Part.

NOTES

NOTES

D10240-0-10/15(B)