

## TABLE OF CONTENTS

Features .....	1
Applications .....	1
General Description .....	1
Functional Block Diagram .....	1
Revision History .....	2
Specifications.....	3
Timing Specifications .....	4
Switching Characteristics .....	4
Regulatory Information.....	5
Insulation and Safety-Related Specifications.....	5
VDE 0884 Insulation Characteristics .....	6
Absolute Maximum Ratings.....	7
ESD Caution.....	7
Pin Configuration and Function Descriptions.....	8
Typical Performance Characteristics .....	9
Test Circuits.....	12

## REVISION HISTORY

### 12/2017—Rev. D to Rev. E

Changes to Logic Side <i>iso</i> Power Current, Dominant State Parameter and TxD/RxD Data Rate 1 Mbps Parameter, Table 1 .....	3
Moved Figure 3 .....	4
Change to T <sub>j</sub> Junction Temperature, Table 6 .....	7
Changes to Figure 28.....	15

### 7/2017—Rev. C to Rev. D

Moved Figure 1 .....	3
Changes to Figure 1.....	3
Change to Tracking Resistance (Comparative Tracking Index) Parameter, Table 4.....	6
Changes to Table 8.....	9
Changes to Power Isolation Section.....	14
Changes to PCB Layout Section and Figure 28 .....	16
Added R <sub>s</sub> Pin Section.....	17
Changes to Figure 32.....	18

Circuit Description.....	13
CAN Transceiver Operation .....	13
Signal Isolation .....	13
Power Isolation .....	13
Truth Tables.....	13
Thermal Shutdown .....	13
DC Correctness and Magnetic Field Immunity.....	14
Applications Information .....	15
PCB Layout .....	15
EMI Considerations .....	15
R <sub>s</sub> Pin.....	16
Insulation Lifetime .....	16
Typical Applications.....	17
Outline Dimensions .....	18
Ordering Guide .....	18

### 11/2016—Rev. B to Rev. C

Change to Table 4 .....	5
Changes to Figure 11 Caption .....	10
Changes to Ordering Guide .....	18

### 2/2013—Rev. A to Rev. B

Changes to Features Section .....	1
Changes to Table 3.....	5
Changes to Table 7.....	7

### 3/2012—Rev. 0 to Rev. A

Changes to Features Section .....	1
Changes to Table 3.....	5
Changes to VDE 0884 Insulation Characteristics Section.....	6
Changes to Figure 6.....	9
Changes to Figure 11.....	10
Changes to Applications Information Section .....	15

### 5/2011—Revision 0: Initial Version

## SPECIFICATIONS

All voltages are relative to their respective grounds;  $4.5\text{ V} \leq V_{CC} \leq 5.5\text{ V}$ ;  $3.0\text{ V} \leq V_{IO} \leq 5.5\text{ V}$ . All minimum/maximum specifications apply over the entire recommended operation range, unless otherwise noted. All typical specifications are at  $T_A = 25^\circ\text{C}$ ,  $V_{CC} = 5\text{ V}$ , and  $V_{IO} = 5\text{ V}$  unless otherwise noted.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
<b>SUPPLY CURRENT</b>						
Logic Side <i>iso</i> Power Current						
Recessive State	$I_{CC}$		29	36	mA	$R_L = 60\ \Omega$ , $R_S = \text{low}$ , see Figure 25
Dominant State	$I_{CC}$		195	260	mA	$R_L = 60\ \Omega$ , $R_S = \text{low}$ , see Figure 25
TxD/RxD Data Rate 1 Mbps	$I_{CC}$		139	200	mA	$R_L = 60\ \Omega$ , $R_S = \text{low}$ , see Figure 25
Logic Side <i>i</i> Coupler Current						
TxD/RxD Data Rate 1 Mbps	$I_{IO}$		1.6	2.5	mA	
<b>DRIVER</b>						
Logic Inputs						
Input Voltage High	$V_{IH}$	$0.7 V_{IO}$			V	Output recessive
Input Voltage Low	$V_{IL}$			$0.25 V_{IO}$	V	Output dominant
CMOS Logic Input Currents	$I_{IH}$ , $I_{IL}$			500	$\mu\text{A}$	TxD
Differential Outputs						
Recessive Bus Voltage	$V_{CANL}$ , $V_{CANH}$	2.0		3.0	V	TxD = high, $R_L = \infty$ , see Figure 22
CANH Output Voltage	$V_{CANH}$	2.75		4.5	V	TxD = low, see Figure 22
CANL Output Voltage	$V_{CANL}$	0.5		2.0	V	TxD = low, see Figure 22
Differential Output Voltage	$V_{OD}$	1.5		3.0	V	TxD = low, $R_L = 45\ \Omega$ , see Figure 22
	$V_{OD}$	-500		+50	mV	TxD = high, $R_L = \infty$ , see Figure 22
Short-Circuit Current, CANH	$I_{SCCANH}$			-200	mA	$V_{CANH} = -5\text{ V}$
			-100		mA	$V_{CANH} = -36\text{ V}$
Short-Circuit Current, CANL	$I_{SCCANL}$			200	mA	$V_{CANL} = 36\text{ V}$
<b>RECEIVER</b>						
Differential Inputs						
Differential Input Voltage Recessive	$V_{IDR}$	-1.0		+0.5	V	$-7\text{ V} < V_{CANL}$ , $V_{CANH} < +12\text{ V}$ , see Figure 23, $C_L = 15\text{ pF}$
Differential Input Voltage Dominant	$V_{IDD}$	0.9		5.0	V	$-7\text{ V} < V_{CANL}$ , $V_{CANH} < +12\text{ V}$ , see Figure 23, $C_L = 15\text{ pF}$
Input Voltage Hysteresis	$V_{HYS}$		150		mV	See Figure 3
CANH, CANL Input Resistance	$R_{IN}$	5		25	k $\Omega$	
Differential Input Resistance	$R_{DIFF}$	20		100	k $\Omega$	
Logic Outputs						
Output Low Voltage	$V_{OL}$		0.2	0.4	V	$I_{OUT} = 1.5\text{ mA}$
Output High Voltage	$V_{OH}$	$V_{IO} - 0.3$	$V_{IO} - 0.2$		V	$I_{OUT} = -1.5\text{ mA}$
Short Circuit Current	$I_{OS}$	7		85	mA	$V_{OUT} = \text{GND1 or } V_{IO}$
<b>VOLTAGE REFERENCE</b>						
Reference Output Voltage	$V_{REF}$	2.025		3.025	V	$ I_{REF}  = 50\ \mu\text{A}$
<b>COMMON-MODE TRANSIENT IMMUNITY<sup>1</sup></b>						
		25			kV/ $\mu\text{s}$	$V_{CM} = 1\text{ kV}$ , transient magnitude = 800 V
<b>SLOPE CONTROL</b>						
Current for Slope Control Mode	$I_{SLOPE}$	-10		-200	$\mu\text{A}$	
Slope Control Mode Voltage	$V_{SLOPE}$	1.8		3.3	V	

<sup>1</sup> CM is the maximum common-mode voltage slew rate that can be sustained while maintaining specification compliant operation. VCM is the common-mode potential difference between the logic and bus sides. The transient magnitude is the range over which the common mode is slewed. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

## TIMING SPECIFICATIONS

All voltages are relative to their respective ground;  $3.0\text{ V} \leq V_{IO} \leq 5.5\text{ V}$ ;  $4.5\text{ V} \leq V_{CC} \leq 5.5\text{ V}$ .  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ , unless otherwise noted.

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DRIVER						
Maximum Data Rate		1			Mbps	
Propagation Delay from TxD On to Bus Active	$t_{\text{onTxD}}$			90	ns	$R_S = 0\ \Omega$ ; see Figure 2 and Figure 24 $R_L = 60\ \Omega$ , $C_L = 100\text{ pF}$
Propagation Delay from TxD Off to Bus Inactive	$t_{\text{offTxD}}$			120	ns	$R_S = 0\ \Omega$ ; see Figure 2 and Figure 24 $R_L = 60\ \Omega$ , $C_L = 100\text{ pF}$
RECEIVER						
Propagation Delay from TxD On to Receiver Active	$t_{\text{onRxD}}$			200	ns	$R_S = 0\ \Omega$ ; see Figure 2
				630	ns	$R_S = 47\text{ k}\Omega$ ; see Figure 2
Propagation Delay from TxD Off to Receiver Inactive <sup>1</sup>	$t_{\text{offRxD}}$			250	ns	$R_S = 0\ \Omega$ ; see Figure 2
				480	ns	$R_S = 47\text{ k}\Omega$ ; see Figure 2
CANH, CANL SLEW RATE	SR		7		V/ $\mu\text{s}$	$R_S = 47\text{ k}\Omega$

<sup>1</sup> Guaranteed by design and characterization.

## SWITCHING CHARACTERISTICS

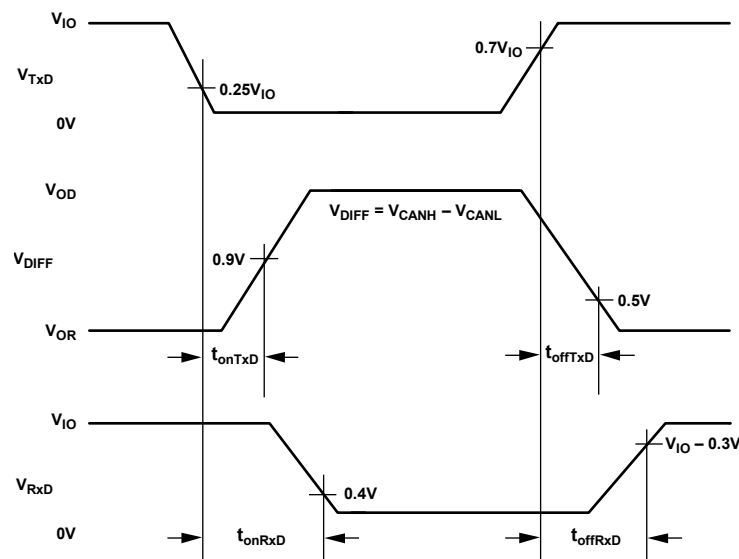


Figure 2. Driver Propagation Delay, Rise/Fall Timing

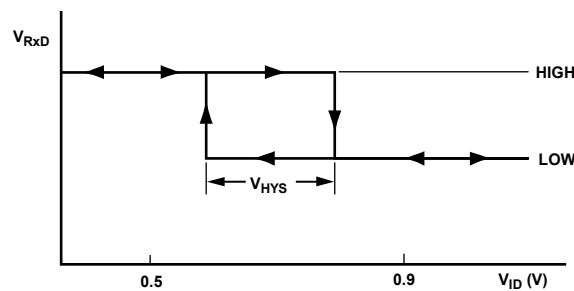


Figure 3. Receiver Input Hysteresis

## REGULATORY INFORMATION

Table 3. ADM3053 Approvals

Organization	Approval Type	Notes
UL	Recognized under the Component Recognition Program of Underwriters Laboratories, Inc.	In accordance with UL 1577, each ADM3053 is proof tested by applying an insulation test voltage $\geq 2500$ V rms for 1 second. File E214100.
VDE	Certified according to DIN EN 60747-5-2 (VDE 0884 Part 2): 2003-01.	In accordance with VDE 0884-2. File 2471900-4880-0001.
CSA	Approved under CSA Component Acceptance Notice 5A. Testing was conducted per CSA 60950-1-07 and IEC 60950-1, 2nd Edition at 2.5 kV rated voltage. Testing was conducted per CSA 61010-1-04 and IEC 61010-1 2nd Edition at 2.5 kV rated voltage.	Basic insulation at 760 V rms (1074 V peak) working voltage. Reinforced insulation at 380 V rms (537 V peak) working voltage. Basic insulation at 424 V rms (600 V peak) working voltage. Reinforced insulation at 300 V rms (424 V peak) working voltage. File 205078.

## INSULATION AND SAFETY-RELATED SPECIFICATIONS

Table 4.

Parameter	Symbol	Value	Unit	Test Conditions/Comments
Rated Dielectric Insulation Voltage		2500	V rms	1-minute duration
Minimum External Air Gap (Clearance)	L(I01)	7.7	mm	Measured from input terminals to output terminals, shortest distance through air
Minimum External Tracking (Creepage)	L(I02)	7.6	mm	Measured from input terminals to output terminals, shortest distance along body
Minimum Internal Gap (Internal Clearance)		0.017 min	mm	Insulation distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>400	V	DIN IEC 112/VDE 0303-1
Isolation Group		II		Material group (DIN VDE 0110: 1989-01, Table 1)

**VDE 0884 INSULATION CHARACTERISTICS**

This isolator is suitable for basic electrical isolation only within the safety limit data. Maintenance of the safety data must be ensured by means of protective circuits.

**Table 5.**

Description	Test Conditions/Comments	Symbol	Characteristic	Unit
<b>CLASSIFICATIONS</b> Installation Classification per DIN VDE 0110 for Rated Mains Voltage $\leq 150$ V rms $\leq 300$ V rms $\leq 400$ V rms Climatic Classification Pollution Degree	DIN VDE 0110, see Table 3		I to IV I to III I to II 40/85/21 2	
<b>VOLTAGE</b> Maximum Working Insulation Voltage Input-to-Output Test Voltage Method b1 Highest Allowable Overvoltage	$V_{IORM} \times 1.875 = V_{PR}$ , 100% production tested, $t_m = 1$ sec, partial discharge < 5 pC (Transient overvoltage, $t_{TR} = 10$ sec)	$V_{IORM}$ $V_{PR}$ $V_{TR}$	560 1050 4000	$V_{PEAK}$ $V_{PEAK}$ $V_{PEAK}$
<b>SAFETY-LIMITING VALUES</b> Case Temperature Input Current Output Current Insulation Resistance at $T_s$	Maximum value allowed in the event of a failure  $V_{IO} = 500$ V	$T_s$ $I_{S, INPUT}$ $I_{S, OUTPUT}$ $R_s$	150 265 335 $>10^9$	$^{\circ}\text{C}$ mA mA $\Omega$

## ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$ , unless otherwise noted. All voltages are relative to their respective ground.

Table 6.

Parameter	Rating
$V_{CC}$	–0.5 V to +6 V
$V_{IO}$	–0.5 V to +6 V
Digital Input Voltage, TxD	–0.5 V to $V_{IO} + 0.5$ V
Digital Output Voltage, RxD	–0.5 V to $V_{IO} + 0.5$ V
CANH, CANL	–36 V to +36 V
$V_{REF}$	–0.5 V to +6 V
$R_S$	–0.5 V to +6 V
Operating Temperature Range	–40°C to +85°C
Storage Temperature Range	–55°C to +150°C
ESD (Human Body Model)	3 kV
Lead Temperature	
Soldering (10 sec)	300°C
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C
$\theta_{JA}$ Thermal Impedance	53°C/W
$T_J$ Junction Temperature	150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Table 7. Maximum Continuous Working Voltage<sup>1</sup>

Parameter	Max	Unit	Reference Standard
AC Voltage			
Bipolar Waveform	424	V peak	50 year minimum lifetime
Unipolar Waveform			
Basic Insulation	1074	V peak	Maximum approved working voltage per IEC60950-1
Reinforced Insulation	537	V peak	Maximum approved working voltage per IEC60950-1
DC Voltage			
Basic Insulation	1074	V peak	Maximum approved working voltage per IEC60950-1
Reinforced Insulation	537	V peak	Maximum approved working voltage per IEC60950-1

<sup>1</sup> Refers to continuous voltage magnitude imposed across the isolation barrier. See the Insulation Lifetime section for more details.

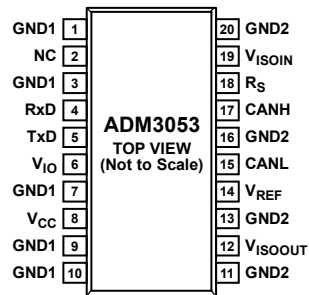
## ESD CAUTION



### ESD (electrostatic discharge) sensitive device.

Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

## PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



## NOTES

1. NC = NO CONNECT. DO NOT CONNECT TO THIS PIN.
2. PIN 12 AND PIN 19 MUST BE CONNECTED EXTERNALLY.

00293-005

Figure 4. Pin Configuration

Table 8. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 3, 7, 9, 10	GND1	Ground, Logic Side.
2	NC	No Connect. Do not connect to this pin.
4	RxD	Receiver Output Data.
5	TxD	Driver Input Data.
6	V <sub>IO</sub>	<i>i</i> Coupler Power Supply. It is recommended that a 0.1 $\mu$ F and a 0.01 $\mu$ F decoupling capacitor be fitted between Pin 6 and GND1. See Figure 28 for layout recommendations.
8	V <sub>CC</sub>	<i>iso</i> Power Power Supply. It is recommended that a 0.1 $\mu$ F and a 10 $\mu$ F decoupling capacitor be fitted between Pin 8 and Pin 9.
11, 13	GND2	Ground for Isolated DC-to-DC Converter. It is recommended to connect Pin 11 and Pin 13 together through one ferrite bead to the PCB ground.
12	V <sub>ISOOUT</sub>	Isolated Power Supply Output. This pin must be connected externally to V <sub>ISOIN</sub> . It is recommended that a ferrite bead reservoir capacitor of 10 $\mu$ F and a decoupling capacitor of 0.1 $\mu$ F be fitted between Pin 12 and Pin 11.
14	V <sub>REF</sub>	Reference Voltage Output. It is recommended not to connect to this pin.
15	CANL	Low-Level CAN Voltage Input/Output.
16, 20	GND2	Ground, Bus Side.
17	CANH	High-Level CAN Voltage Input/Output.
18	R <sub>S</sub>	Slope Control Pin. Short this pin to GND2 (Pin 16 or Pin 20) for full speed operation. Use a weak pull-down for slope control. An input high places the transceiver in standby. This pin must not be left floating.
19	V <sub>ISOIN</sub>	Isolated Power Supply Input. This pin must be connected externally to V <sub>ISOOUT</sub> . It is recommended this pin have a 0.1 $\mu$ F capacitor to GND2 (Pin 13 or Pin 11). Connect this pin through a ferrite bead and short trace length to V <sub>ISOIN</sub> for operation.

## TYPICAL PERFORMANCE CHARACTERISTICS

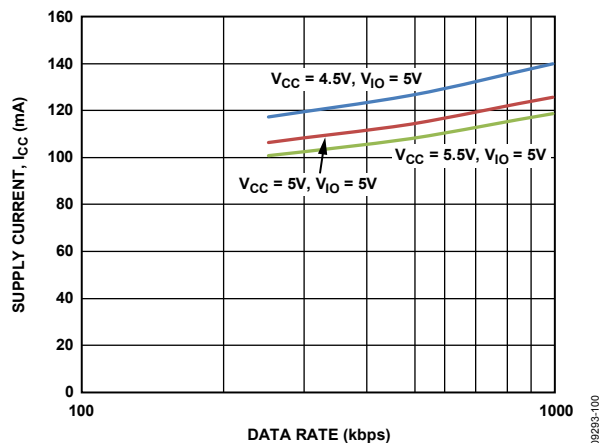
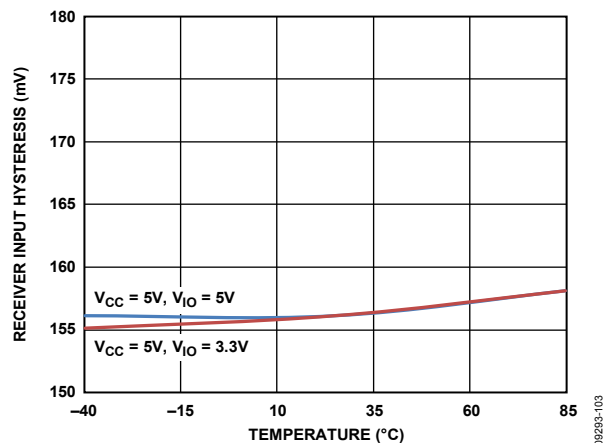
Figure 5. Supply Current,  $I_{CC}$  vs. Data Rate

Figure 8. Receiver Input Hysteresis vs. Temperature

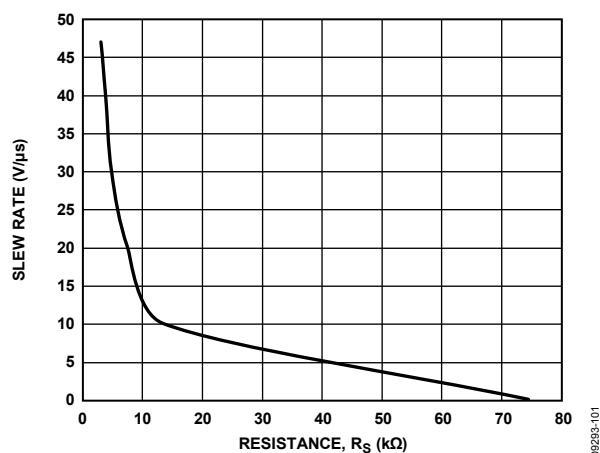
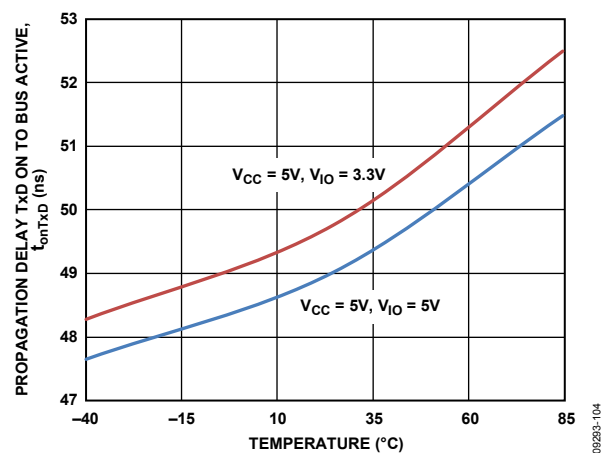
Figure 6. Driver Slew Rate vs. Resistance,  $R_S$ 

Figure 9. Propagation Delay from TxD On to Bus Active vs. Temperature

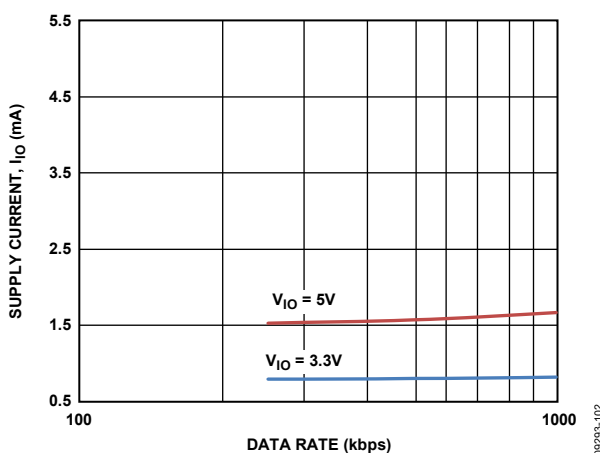
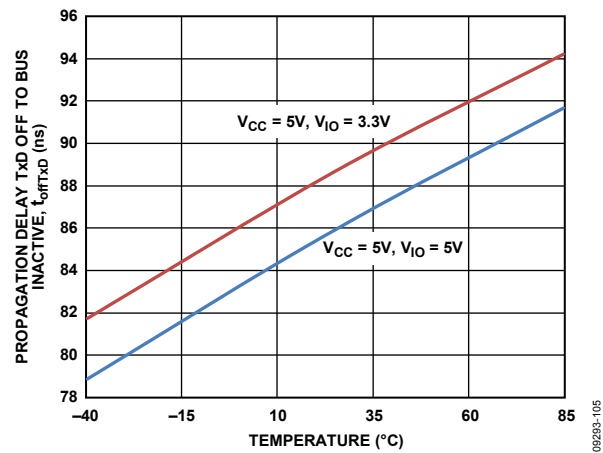
Figure 7. Supply Current,  $I_{IO}$  vs. Data Rate

Figure 10. Propagation Delay from TxD Off to Bus Inactive vs. Temperature



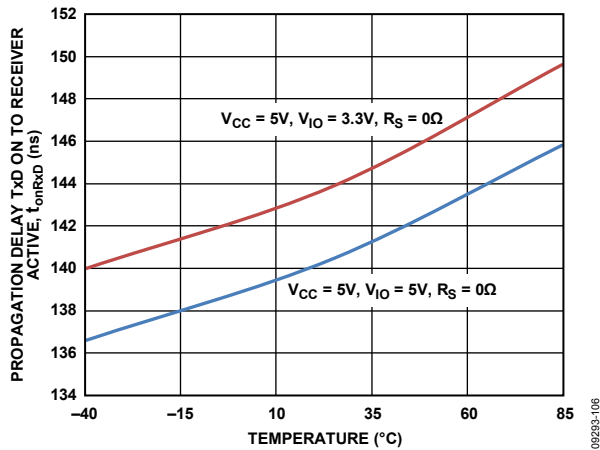


Figure 11. Propagation Delay from TxD On to Receiver Active vs. Temperature

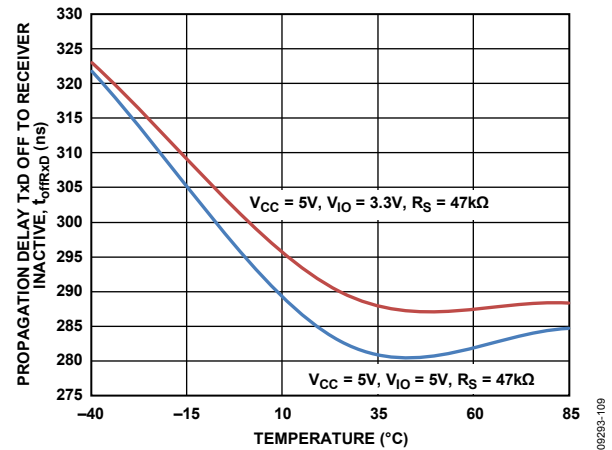


Figure 14. Propagation Delay from TxD Off to Receiver Inactive vs. Temperature

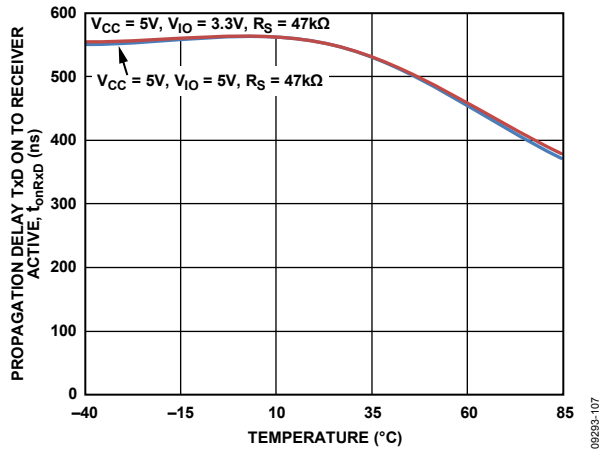


Figure 12. Propagation Delay from TxD On to Receiver Active vs. Temperature

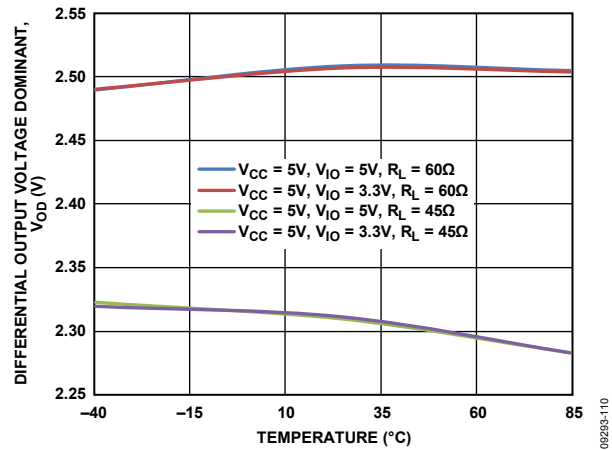


Figure 15. Differential Output Voltage Dominant vs. Temperature

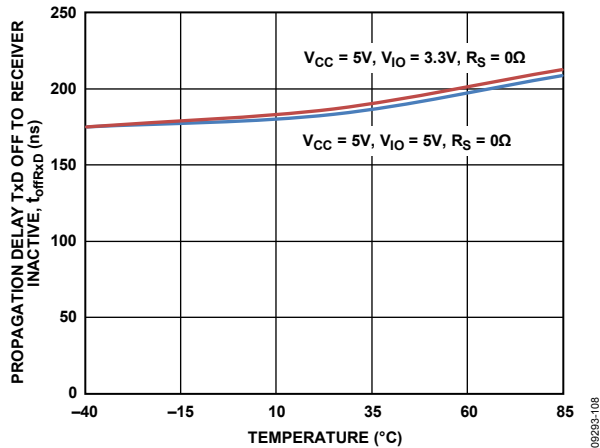


Figure 13. Propagation Delay from TxD Off to Receiver Inactive vs. Temperature

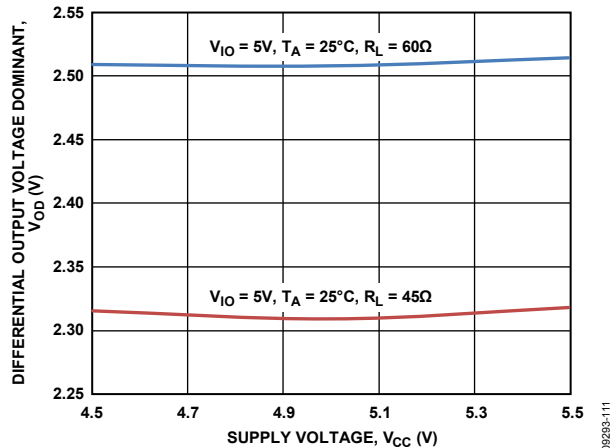


Figure 16. Differential Output Voltage Dominant vs. Supply Voltage,  $V_{CC}$

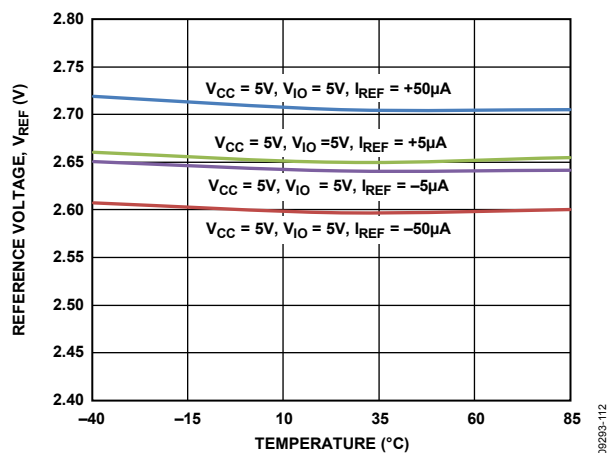


Figure 17. Reference Voltage vs. Temperature

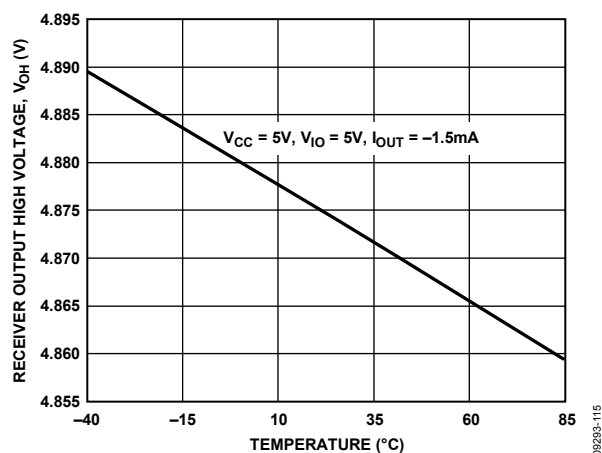


Figure 20. Receiver Output High Voltage vs. Temperature

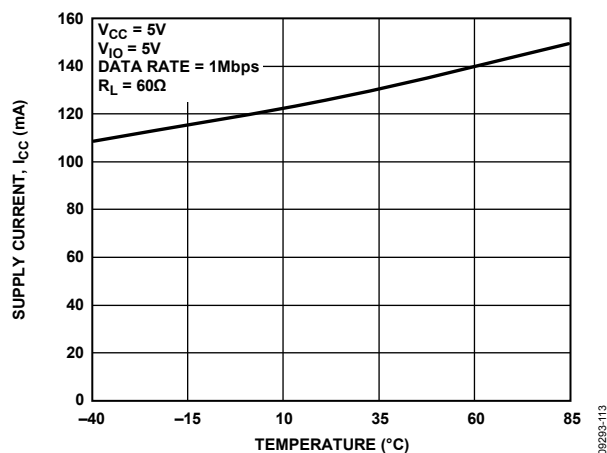
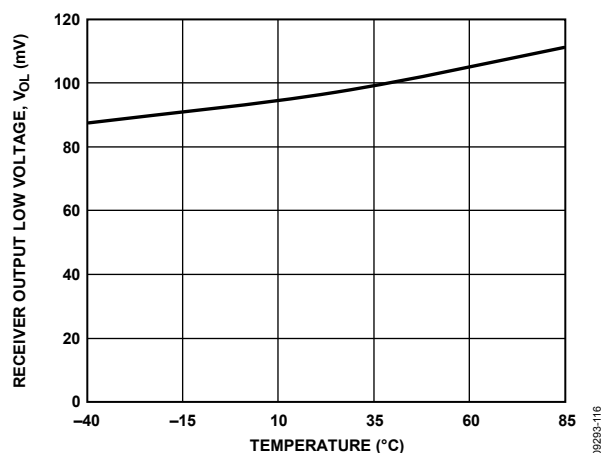
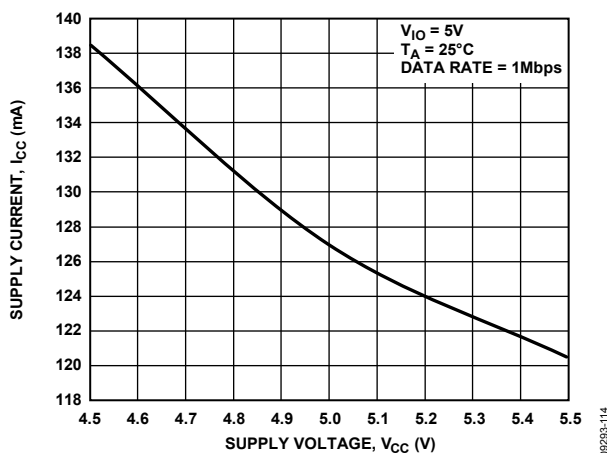
Figure 18. Supply Current  $I_{CC}$  vs. Temperature

Figure 21. Receiver Output Low Voltage vs. Temperature

Figure 19. Supply Current,  $I_{CC}$  vs. Supply Voltage  $V_{CC}$

## TEST CIRCUITS

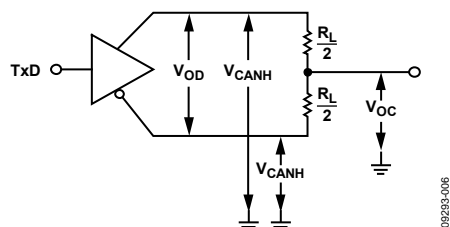


Figure 22. Driver Voltage Measurement

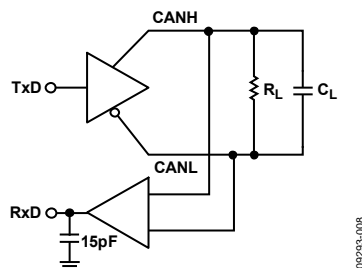


Figure 24. Switching Characteristics Measurements

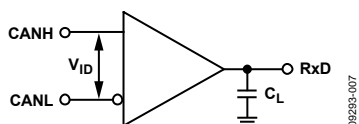


Figure 23. Receiver Voltage Measurements

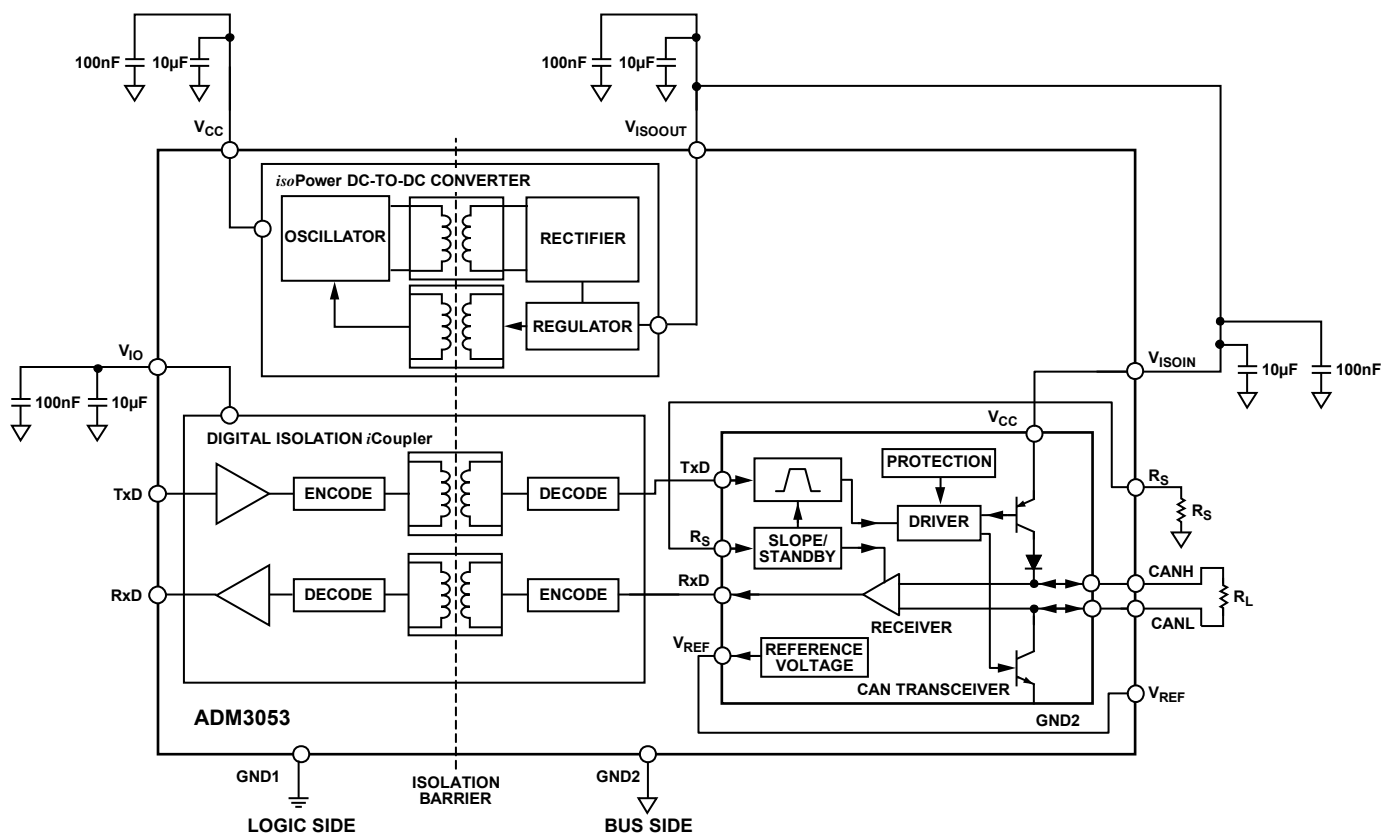


Figure 25. Supply Current Measurement Test Circuit

## CIRCUIT DESCRIPTION

### CAN TRANSCEIVER OPERATION

A CAN bus has two states called dominant and recessive. A dominant state is present on the bus when the differential voltage between CANH and CANL is greater than 0.9 V. A recessive state is present on the bus when the differential voltage between CANH and CANL is less than 0.5 V. During a dominant bus state, the CANH pin is high, and the CANL pin is low. During a recessive bus state, both the CANH and CANL pins are in the high impedance state.

Pin 18 (R<sub>S</sub>) allows two different modes of operation to be selected: high-speed and slope control. For high-speed operation, the transmitter output transistors are simply switched on and off as fast as possible. In this mode, no measures are taken to limit the rise and fall slopes. A shielded cable is recommended to avoid electromagnetic interference (EMI) problems. High-speed mode is selected by connecting Pin 18 to ground.

Slope control mode allows the use of an unshielded twisted pair or a parallel pair of wires as bus lines. To reduce EMI, the rise and fall slopes must be limited. The rise and fall slopes can be programmed with a resistor connected from Pin 18 to ground. The slope is proportional to the current output at Pin 18.

### SIGNAL ISOLATION

The ADM3053 signal isolation is implemented on the logic side of the interface. The part achieves signal isolation by having a digital isolation section and a transceiver section (see Figure 1). Data applied to the TxD pin referenced to logic ground (GND1) are coupled across an isolation barrier to appear at the transceiver section referenced to isolated ground (GND2). Similarly, the single-ended receiver output signal, referenced to isolated ground in the transceiver section, is coupled across the isolation barrier to appear at the RxD pin referenced to logic ground (GND1). The signal isolation is powered by the V<sub>IO</sub> pin and allows the digital interface to 3.3 V or 5 V logic.

### POWER ISOLATION

The ADM3053 power isolation is implemented using an *isoPower* integrated isolated dc-to-dc converter. The dc-to-dc converter section of the ADM3053 works on principles that are common to most modern power supplies. It is a secondary side controller architecture with isolated pulse-width modulation (PWM) feedback. V<sub>CC</sub> power is supplied to an oscillating circuit that switches current into a chip-scale air core transformer. Power transferred to the secondary side is rectified and regulated to 5 V. The secondary (V<sub>ISO</sub>) side controller regulates the output by creating a PWM control signal that is sent to the primary (V<sub>CC</sub>) side by a dedicated *iCoupler* data channel. The PWM modulates the oscillator circuit to control the power being sent to the secondary side. Feedback allows for significantly higher power and efficiency.

The ADM3053 integrated dc-to-dc converter is designed as a self contained solution and must not drive an external load. To meet additional isolated power needs, *isoPower* isolated dc-to-dc converters are available in a variety of power or power plus standard data channel options.

### TRUTH TABLES

The truth tables in this section use the abbreviations found in Table 9.

**Table 9. Truth Table Abbreviations**

Letter	Description
H	High level
L	Low level
X	Don't care
Z	High impedance (off)
I	Indeterminate
NC	Not connected

**Table 10. Transmitting**

Supply Status		Input	Outputs		
V <sub>IO</sub>	V <sub>CC</sub>	TxD	Bus State	CANH	CANL
On	On	L	Dominant	H	L
On	On	H	Recessive	Z	Z
On	On	Floating	Recessive	Z	Z
Off	On	X	Recessive	Z	Z
On	Off	L	Indeterminate	I	I

**Table 11. Receiving**

Supply Status		Inputs		Output
V <sub>IO</sub>	V <sub>CC</sub>	V <sub>ID</sub> = CANH – CANL	Bus State	RxD
On	On	≥ 0.9 V	Dominant	L
On	On	≤ 0.5 V	Recessive	H
On	On	0.5 V < V <sub>ID</sub> < 0.9 V	X <sup>1</sup>	I
On	On	Inputs open	Recessive	H
Off	On	X <sup>1</sup>	X <sup>1</sup>	I
On	Off	X <sup>1</sup>	X <sup>1</sup>	H

<sup>1</sup> X means don't care.

### THERMAL SHUTDOWN

The ADM3053 contains thermal shutdown circuitry that protects the part from excessive power dissipation during fault conditions. Shorting the driver outputs to a low impedance source can result in high driver currents. The thermal sensing circuitry detects the increase in die temperature under this condition and disables the driver outputs. This circuitry is designed to disable the driver outputs when a die temperature of 150°C is reached. As the device cools, the drivers are reenabled at a temperature of 140°C.

## DC CORRECTNESS AND MAGNETIC FIELD IMMUNITY

The digital signals transmit across the isolation barrier using *i*Coupler technology. This technique uses chip-scale transformer windings to couple the digital signals magnetically from one side of the barrier to the other.

Digital inputs are encoded into waveforms that are capable of exciting the primary transformer winding. At the secondary winding, the induced waveforms are decoded into the binary value that was originally transmitted.

Positive and negative logic transitions at the isolator input cause narrow (~1 ns) pulses to be sent to the decoder via the transformer. The decoder is bistable and is, therefore, either set or reset by the pulses, indicating input logic transitions. In the absence of logic transitions at the input for more than 1  $\mu$ s, periodic sets of refresh pulses indicative of the correct input state are sent to ensure dc correctness at the output. If the decoder receives no internal pulses of more than approximately 5  $\mu$ s, the input side is assumed to be unpowered or nonfunctional, in which case, the isolator output is forced to a default state by the watchdog timer circuit.

This situation must occur in the ADM3053 devices only during power-up and power-down operations. The limitation on the ADM3053 magnetic field immunity is set by the condition in which induced voltage in the transformer receiving coil is sufficiently large to either falsely set or reset the decoder. The following analysis defines the conditions under which this can occur.

The 3.3 V operating condition of the ADM3053 is examined because it represents the most susceptible mode of operation. The pulses at the transformer output have an amplitude of >1.0 V. The decoder has a sensing threshold of about 0.5 V, thus establishing a 0.5 V margin in which induced voltages can be tolerated. The voltage induced across the receiving coil is given by

$$V = (-d\beta/dt)\Sigma\pi r_n^2; n = 1, 2, \dots, N$$

where:

$\beta$  is magnetic flux density (gauss).

$N$  is the number of turns in the receiving coil.

$r_n$  is the radius of the  $n^{\text{th}}$  turn in the receiving coil (cm).

Given the geometry of the receiving coil in the ADM3053 and an imposed requirement that the induced voltage be, at most, 50% of the 0.5 V margin at the decoder, a maximum allowable magnetic field is calculated as shown in Figure 26.

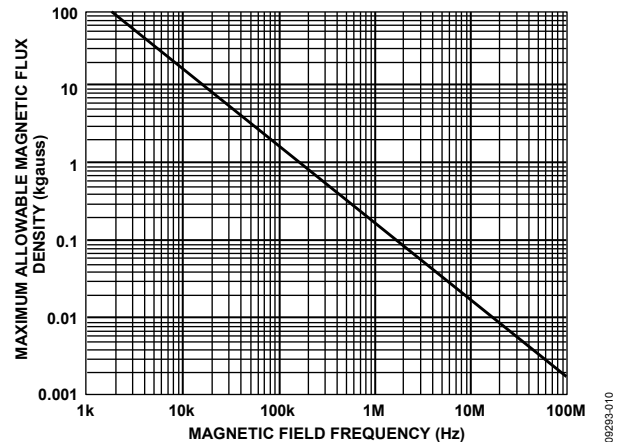


Figure 26. Maximum Allowable External Magnetic Flux Density

For example, at a magnetic field frequency of 1 MHz, the maximum allowable magnetic field of 0.2 kgauss induces a voltage of 0.25 V at the receiving coil. This is about 50% of the sensing threshold and does not cause a faulty output transition. Similarly, if such an event occurs during a transmitted pulse (and is of the worst-case polarity), it reduces the received pulse from >1.0 V to 0.75 V, which is still well above the 0.5 V sensing threshold of the decoder.

The preceding magnetic flux density values correspond to specific current magnitudes at given distances from the ADM3053 transformers. Figure 27 expresses these allowable current magnitudes as a function of frequency for selected distances. As shown in Figure 27, the ADM3053 is extremely immune and can be affected only by extremely large currents operated at high frequency very close to the component. For the 1 MHz example, a 0.5 kA current must be placed 5 mm away from the ADM3053 to affect component operation.

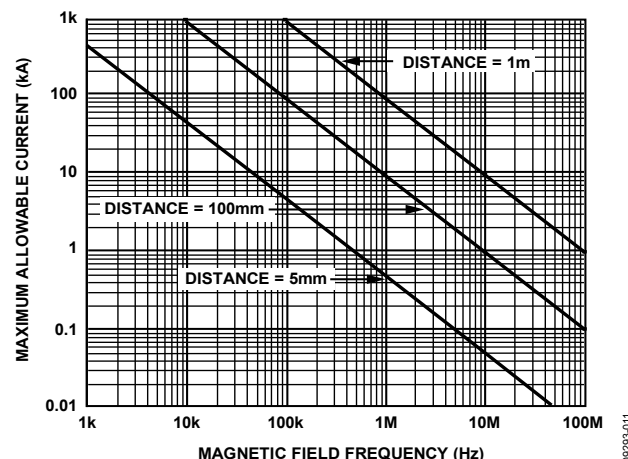


Figure 27. Maximum Allowable Current for Various Current-to-ADM3053 Spacings

Note that in combinations of strong magnetic field and high frequency, any loops formed by the printed circuit board (PCB) traces can induce error voltages sufficiently large to trigger the thresholds of succeeding circuitry. Proceed with caution in the layout of such traces to prevent this from occurring.

## APPLICATIONS INFORMATION

### PCB LAYOUT

The ADM3053 signal and power isolated CAN transceiver contains an *isoPower* integrated dc-to-dc converter, requiring no external interface circuitry for the logic interfaces. Power supply bypassing is required at the input and output supply pins (see Figure 28). The power supply section of the ADM3053 uses a 180 MHz oscillator frequency to pass power efficiently through its chip-scale transformers. In addition, the normal operation of the data section of the *iCoupler* introduces switching transients on the power supply pins.

Bypass capacitors are required for several operating frequencies. Noise suppression requires a low inductance, high frequency capacitor, whereas ripple suppression and proper regulation require a large value capacitor. These capacitors are connected between GND1 and Pin 6 ( $V_{IO}$ ) for  $V_{IO}$ . It is recommended that a combination of 100 nF and 10 nF be placed as shown in Figure 28 (C6 and C4). It is recommended that a combination of two capacitors, with values of 100 nF and 10  $\mu$ F, are placed between Pin 8 ( $V_{CC}$ ) and Pin 9 (GND1) for  $V_{CC}$  as shown in Figure 28 (C2 and C1). The  $V_{ISOIN}$  and  $V_{ISOOUT}$  capacitors are connected between Pin 11 (GND2) and Pin 12 ( $V_{ISOOUT}$ ) with recommended values of 100 nF and 10  $\mu$ F as shown in Figure 28 (C5 and C8). Two capacitors are recommended to be fitted Pin 19 ( $V_{ISOIN}$ ) and Pin 20 (GND2) with values of 100nF and 10nF as shown in Figure 28 (C9 and C7). The best practice recommended is to use a very low inductance ceramic capacitor, or its equivalent, for the smaller value. The total lead length between both ends of the capacitor and the input power supply pin must not exceed 10 mm.

The ADM3053 features an internal split paddle, lead frame on the bus side. For the best noise suppression, filter both the GND2 pins (Pin 11 and Pin13) and  $V_{ISOOUT}$  signals of the integrated dc-to-dc converter for high frequency currents. Use surface-mount ferrite beads in series with the signals before routing back to the device. See Figure 28 for the recommended PCB layout.

The impedance of the ferrite bead is chosen to be about 2 k $\Omega$  between the 100 MHz and 1 GHz frequency range, to reduce the emissions at the 180 MHz primary switching frequency and the 360 MHz secondary side rectifying frequency and harmonics.

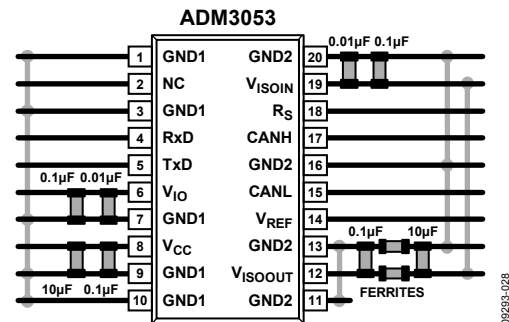


Figure 28. Recommended PCB Layout

In applications involving high common-mode transients, ensure that board coupling across the isolation barrier is minimized. Furthermore, design the board layout such that any coupling that does occur equally affects all pins on a given component side.

Failure to ensure this can cause voltage differentials between pins exceeding the absolute maximum ratings for the device, thereby leading to latch-up and/or permanent damage.

The ADM3053 dissipates approximately 650 mW of power when fully loaded. Because it is not possible to apply a heat sink to an isolation device, the devices primarily depend on heat dissipation into the PCB through the GND pins. If the devices are used at high ambient temperatures, provide a thermal path from the GND pins to the PCB ground plane. The board layout in Figure 28 shows enlarged pads for Pin 1, Pin 3, Pin 9, Pin 10, Pin 11, Pin 14, Pin 16, and Pin 20. Implement multiple vias from the pad to the ground plane to reduce the temperature inside the chip significantly. The dimensions of the expanded pads are at the discretion of the designer and dependent on the available board space.

### EMI CONSIDERATIONS

The dc-to-dc converter section of the ADM3053 must, of necessity, operate at very high frequency to allow efficient power transfer through the small transformers. This creates high frequency currents that can propagate in circuit board ground and power planes, causing edge and dipole radiation. Grounded enclosures are recommended for applications that use these devices. If grounded enclosures are not possible, good RF design practices must be followed in the layout of the PCB. See the [AN-0971 Application Note, Recommendations for Control of Radiated Emissions with \*isoPower\* Devices](#), for more information.

## R<sub>S</sub> PIN

For high speed mode, the R<sub>S</sub> pin is connected directly to GND2 (Pin 16 or Pin 20). The transition time of the CAN bus signals are short as possible, allowing higher speed signaling. A shielded cable is recommended to avoid EMI problems in high speed mode.

Slope control mode allows the use of unshielded twisted pair wires or parallel pair wires as bus lines. The signal rise and fall transition times are slowed to reduce EMI and ringing. The rise and fall slopes are adjusted with the resistor (R<sub>SLOPE</sub>) connected from R<sub>S</sub> to GND2. See Figure 6 for details.

The R<sub>S</sub> pin cannot be left floating.

## INSULATION LIFETIME

All insulation structures eventually break down when subjected to voltage stress over a sufficiently long period. The rate of insulation degradation is dependent on the characteristics of the voltage waveform applied across the insulation. Analog Devices conducts an extensive set of evaluations to determine the lifetime of the insulation structure within the ADM3053.

Accelerated life testing is performed using voltage levels higher than the rated continuous working voltage. Acceleration factors for several operating conditions are determined, allowing calculation of the time to failure at the working voltage of interest. The values shown in Table 5 summarize the peak voltages for 50 years of service life in several operating conditions. In many cases, the working voltage approved by agency testing is higher than the 50 year service life voltage. Operation at working voltages higher than the service life voltage listed leads to premature insulation failure.

The insulation lifetime of the ADM3053 depends on the voltage waveform type imposed across the isolation barrier. The iCoupler insulation structure degrades at different rates, depending on whether the waveform is bipolar ac, unipolar ac, or dc. Figure 29, Figure 30, and Figure 31 illustrate these different isolation voltage waveforms.

Bipolar ac voltage is the most stringent environment. A 50 year operating lifetime under the bipolar ac condition determines the Analog Devices recommended maximum working voltage.

In the case of unipolar ac or dc voltage, the stress on the insulation is significantly lower. This allows operation at higher working voltages while still achieving a 50 year service life. The working voltages listed in Table 5 can be applied while maintaining the 50 year minimum lifetime, provided the voltage conforms to either the unipolar ac or dc voltage cases. Any cross insulation voltage waveform that does not conform to Figure 30 or Figure 31 must be treated as a bipolar ac waveform, and its peak voltage must be limited to the 50-year lifetime voltage value listed in Table 5.

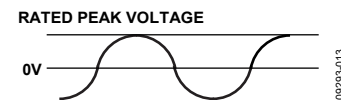


Figure 29. Bipolar AC Waveform

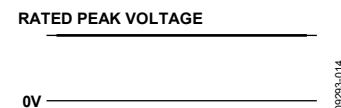
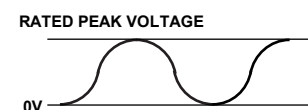


Figure 30. DC Waveform



**NOTES**  
1. THE VOLTAGE IS SHOWN AS SINUSOIDAL FOR ILLUSTRATION PURPOSES ONLY. IT IS MEANT TO REPRESENT ANY VOLTAGE WAVEFORM VARYING BETWEEN 0 AND SOME LIMITING VALUE. THE LIMITING VALUE CAN BE POSITIVE OR NEGATIVE, BUT THE VOLTAGE CANNOT CROSS 0V.

Figure 31. Unipolar AC Waveform

## TYPICAL APPLICATIONS

Figure 32 is an example circuit diagram using the ADM3053.

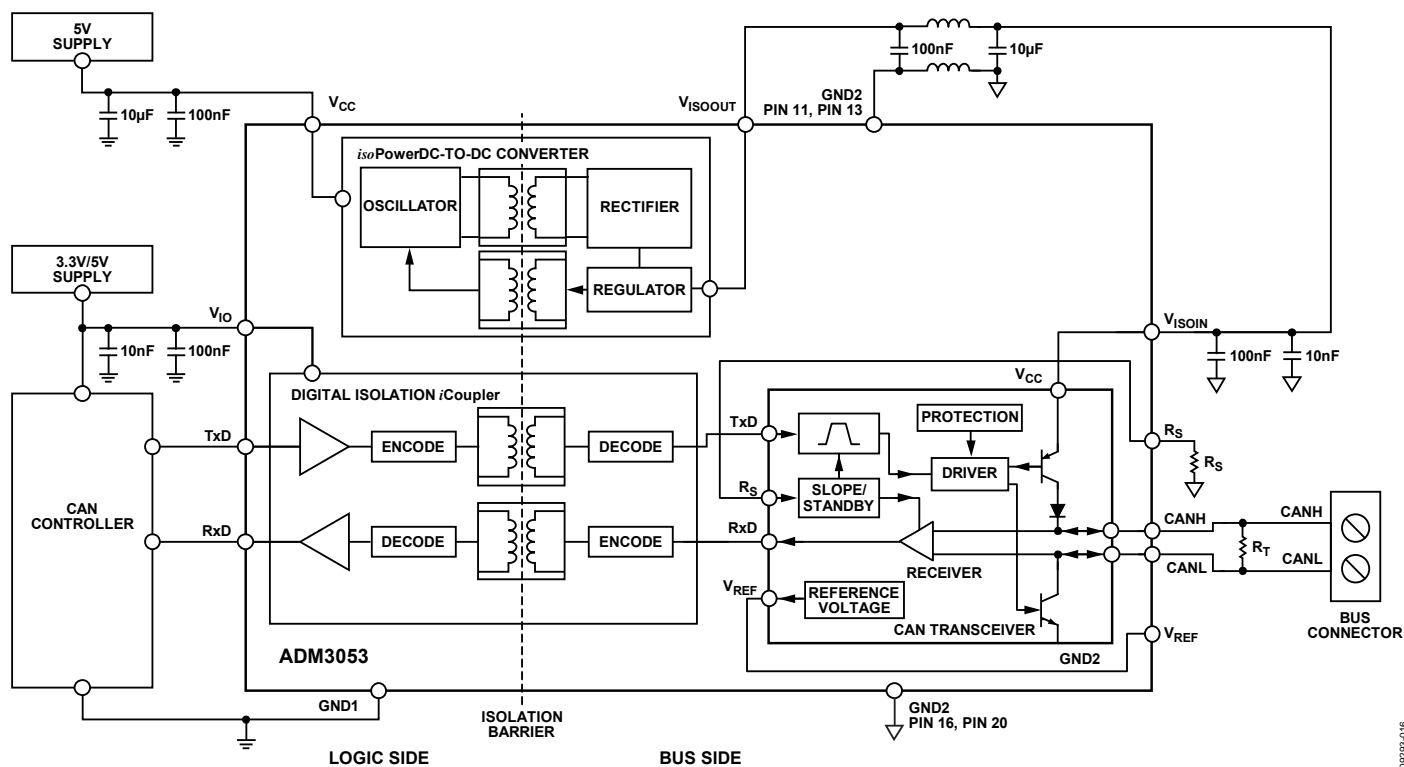
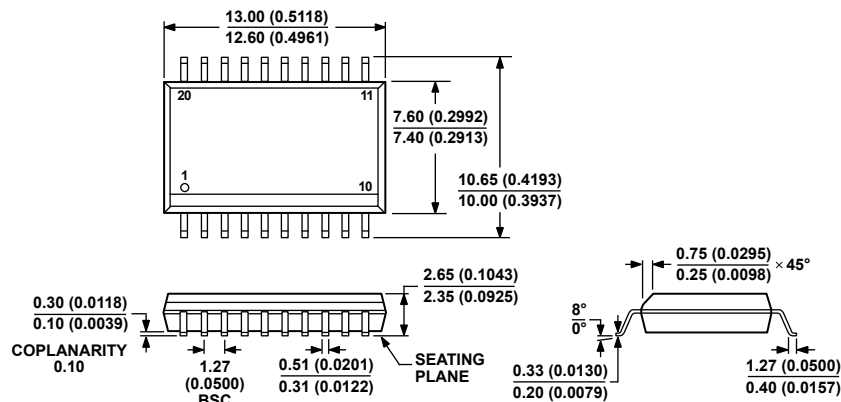


Figure 32. Example Circuit Diagram Using the ADM3053

002035-016



OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-013-AC  
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS  
(IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR  
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 33. 20-Lead Standard Small Outline Package [SOIC\_W]  
Wide Body  
(RW-20)  
Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model <sup>1</sup>	Temperature Range	Package Description	Package Option
ADM3053BRWZ	−40°C to +85°C	20-Lead Standard Small Outline Package [SOIC_W]	RW-20
ADM3053BRWZ-REEL7	−40°C to +85°C	20-Lead Standard Small Outline Package [SOIC_W]	RW-20
EVAL-ADM3053EBZ		Evaluation Board	
EZLINX-IIIDE-EBZ		iCoupler Isolated Interface Development Environment Evaluation Board	

<sup>1</sup> Z = RoHS Compliant Part.