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REVISION HISTORY

11/2020—Rev. D to Rev. E

Changed CP-32-2 to CP-32-7 ... Throughout
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Updated Outline Dimensions ... 32
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3/2019—Rev. C to Rev. D

Change to DAC Control Register (0x02), Table 9 ... 26
Updated Outline Dimensions ... 32

11/2017—Rev. B to Rev. C

Changed CP-32-7 to CP-32-2 ... Throughout
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8/2016—Rev. A to Rev. B

Changes to Table 7 ... 20
Updated Outline Dimensions ... 32
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6/2010—Rev. 0 to Rev. A

Added Digital Input Voltage to Table 2 ... 5
Added Exposed Pad Notation to Figure 3 and Table 3 ... 5
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Added Endnote 1 to Table 9 ... 26
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Changes to Table 15 and Table 16 ... 31
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10/2007—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL SPECIFICATIONS

AVDD (1.8 V), DVDD (1.8 V), and DVDD_I/O = 1.8 V ± 5%, T = 25°C, R_{SET} = 4.64 kΩ, DAC full-scale current = 2 mA, external reference clock frequency = 250 MHz with REF_CLK multiplier disabled, unless otherwise noted.

Table 1.

Parameter	Conditions/Comments	Min	Typ	Max	Unit
REF_CLK INPUT CHARACTERISTICS					
Frequency Range					
REF_CLK Multiplier	Disabled			250	MHz
	Enabled			250	MHz
REF_CLK Input Divider Frequency	Full temperature range			83	MHz
VCO Oscillation Frequency	VCO1	16		250	MHz
	VCO2	100		250	MHz
PLL Lock Time	25 MHz reference clock, 10× PLL		60		µs
External Crystal Mode			25		MHz
CMOS Mode	VIH	0.9			V
	VIL			0.65	V
Input Capacitance			3		pF
Input Impedance (Differential)			2.7		kΩ
Input Impedance (Single-Ended)			1.35		kΩ
Duty Cycle		45		55	%
REF_CLK Input Level		355		1000	mV p-p
DAC OUTPUT CHARACTERISTICS					
Full-Scale Output Current				4.6	mA
Gain Error		−14		−6	%FS
Output Offset				+0.1	µA
Differential Nonlinearity		−0.4		+0.4	LSB
Integral Nonlinearity		−0.5		+0.5	LSB
AC Voltage Compliance Range			±400		mV
SPURIOUS-FREE DYNAMIC RANGE	Refer to Figure 6				
SERIAL PORT TIMING CHARACTERISTICS					
SCLK Frequency				32	MHz
SCLK Pulse Width	Low	17.5			ns
	High	3.5			ns
SCLK Rise/Fall Time				2	ns
Data Setup Time to SCLK		5.5			ns
Data Hold Time to SCLK		0			ns
Data Valid Time in Read Mode				22	ns
PARALLEL PORT TIMING CHARACTERISTICS					
PCLK Frequency				33	MHz
PCLK Pulse Width	Low	10			ns
	High	20			ns
PCLK Rise/Fall Time				2	ns
Address/Data Setup Time to PCLK		3.0			ns
Address/Data Hold Time to PCLK		0.3			ns
Data Valid Time in Read Mode				8	ns
IO_UPDATE/PROFILE(2:0) TIMING					
Setup Time to SYNC_CLK		0.5			ns
Hold Time to SYNC_CLK		1			SYNC_CLK cycles

Parameter	Conditions/Comments	Min	Typ	Max	Unit
MISCELLANEOUS TIMING CHARACTERISTICS					
Wake-Up Time[1]					
Fast Recovery Mode				1	SYSCLK cycles[2]
Full Sleep Mode				60	µs
Reset Pulse Width High		5			SYSCLK cycles
DATA LATENCY (PIPELINE DELAY)					
Frequency, Phase-to-DAC Output	Matched latency enabled		11		SYSCLK cycles
Frequency-to-DAC Output	Matched latency disabled		11		SYSCLK cycles
Phase-to-DAC Output	Matched latency disabled		10		SYSCLK cycles
Delta Tuning Word-to-DAC Output (Linear Sweep)			14		SYSCLK cycles
CMOS LOGIC INPUTS					
Logic 1 Voltage		1.2			V
Logic 0 Voltage				0.4	V
Logic 1 Current		−700		+700	nA
Logic 0 Current		−700		+700	nA
Input Capacitance			3		pF
CMOS LOGIC OUTPUTS	1 mA load				
Logic 1 Voltage		1.5			V
Logic 0 Voltage				0.125	V
POWER SUPPLY CURRENT					
DVDD (1.8 V) Pin Current Consumption				46.5	mA
DAC_CLK_AVDD (1.8 V)				4.7	mA
DAC_AVDD (1.8 V) Pin Current Consumption				6.2	mA
PLL_AVDD (1.8 V)				1.8	mA
CLK_AVDD (1.8 V) Pin Current Consumption				4.3	mA
POWER CONSUMPTION					
Single Tone Mode	PLL enabled, CMOS input		50	66.5	mW
	PLL disabled, differential input		57	70.5	mW
	PLL enabled, XTAL input		52	68.5	mW
Modulus Mode	PLL disabled			94.6	mW
Linear Sweep Mode	PLL disabled			98.4	mW
Power-Down					
Full				15	mW
Safe	PLL enabled			44.8	mW
PLL Modes					
VCO 1					
Differential Input Mode				11	mW
CMOS Input Mode				7.5	mW
Crystal Mode				5.4	mW
VCO 2					
Differential Input Mode				15	mW
CMOS Input Mode				11.5	mW
Crystal Mode				9.4	mW

[1] Refer to the Power-Down Features section.
[2] SYSCLK cycle refers to the actual clock frequency used on-chip by the DDS. If the reference clock multiplier is used to multiply the external reference clock frequency, the SYSCLK frequency is the external frequency multiplied by the reference clock multiplication factor. If the reference clock multiplier and divider are not used, the SYSCLK frequency is the same as the external reference clock frequency.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Maximum Junction Temperature	150°C
AVDD, DVDD	2 V
Digital Input Voltage	−0.7 V to +2.2 V
Digital Output Current	5 mA
Storage Temperature	−65°C to +150°C
Operating Temperature	−40°C to +105°C
Lead Temperature (Soldering, 10 sec)	300°C
θ_{JA}	36.1°C/W
θ_{JC}	4.2°C/W

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

EQUIVALENT CIRCUITS

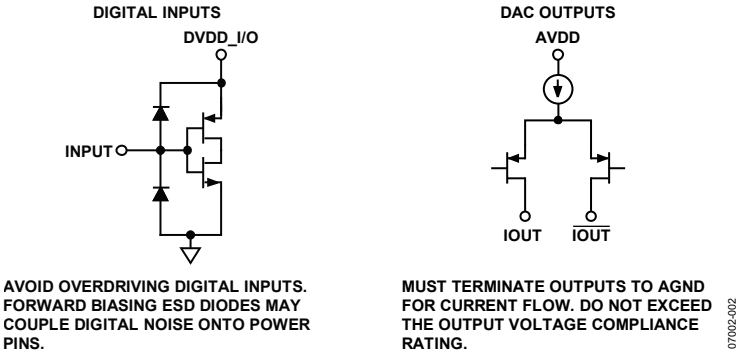


Figure 2. Equivalent Input and Output Circuits

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

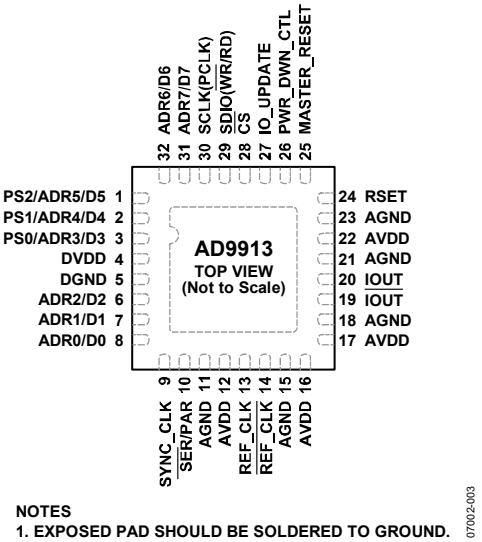


Figure 3. Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	I/O	Description
1	PS2/ADR5/D5	I/O	Multipurpose pin: Profile Select Pin (PS2) in Direct Switch Mode, Parallel Port Address Line (ADR5), and Data Line (D5) to program registers.
2	PS1/ADR4/D4	I/O	Multipurpose pin: Profile Select Pin (PS1) in Direct Switch Mode or Linear Sweeping Mode, Parallel Port Address Line (ADR4), and Data Line (D4) to program registers.
3	PS0/ADR3/D3	I/O	Multipurpose pin: Profile Select Pin (PS0) in Direct Switch Mode or Linear Sweeping Mode, Parallel Port Address Line (ADR3), and Data Line (D3) to program registers.
4	DVDD	I	Digital Power Supply (1.8 V).
5	DGND	I	Digital Ground.
6	ADR2/D2	I/O	Parallel Port Address Line 2 and Data Line 2.
7	ADR1/D1	I/O	Parallel Port Address Line 1and Data Line 1.
8	ADR0/D0	I/O	Parallel Port Address Line 0 and Data Line 0.
9	SYNC_CLK	O	Clock Out. The profile pins [PS0:PS2] and the IO_UPDATE pin (Pin 27) should be set up to the rising edge of this signal to maintain constant pipe line delay through the device.
10	$\overline{\text{SER}}$/PAR	I	Serial Port and Parallel Port Selection. Logic low = serial mode; logic high = parallel mode.
11, 15, 18, 21, 23	AGND	I	Analog Ground.
12, 16, 17, 22	AVDD	I	Analog Power Supply (1.8 V).
13	REF_CLK	I	Reference Clock Input. See the REF_CLK Overview section for more details.
14	$\overline{\text{REF\_CLK}}$	I	Complementary Reference Clock Input. See the REF_CLK Overview section for more details.
19	$\overline{\text{IOUT}}$	O	Open Source DAC Complementary Output Source. Current mode. Connect through 50 Ω to AGND.
20	IOUT	O	Open Source DAC Output Source. Current mode. Connect through 50 Ω to AGND.
24	RSET	I	Analog Reference. This pin programs the DAC output full-scale reference current. Attach a 4.64 kΩ resistor to AGND.
25	MASTER_RESET	I	Master Reset, Digital Input (Active High). This pin clears all memory elements and reprograms registers to default values.

Pin No.	Mnemonic	I/O	Description
26	PWR_DWN_CTL	I	External Power-Down, Digital Input (Active High). A high level on this pin initiates the currently programmed power-down mode. See the Power-Down Features section for further details. If unused, tie to ground.
27	IO_UPDATE	I	I/O Update; Digital Input. A high on this pin indicates a transfer of the contents of the I/O buffers to the corresponding internal registers.
28	$\overline{CS}$	I	Chip Select for Serial and Parallel Port. Digital input (active low). Bringing this pin low enables the AD9913 to detect serial (SCLK) or parallel (PCLK) clock rising/falling edges. Bringing this pin high causes the AD9913 to ignore input on the data pins.
29	SDIO($\overline{WR}$/RD)	I/O	Bidirectional Data Line for Serial Port Operation and Write/Read Enable for Parallel Port Operation.
30	SCLK/PCLK	I	Input Clock for Serial and Parallel Port.
31	ADR7/D7	I/O	Parallel Port Address Line 7 and Data Line 7.
32	ADR6/D6	I/O	Parallel Port Address Line 6 and Data Line 6.
33	Exposed Paddle		The EPAD should be soldered to ground.

TYPICAL PERFORMANCE CHARACTERISTICS

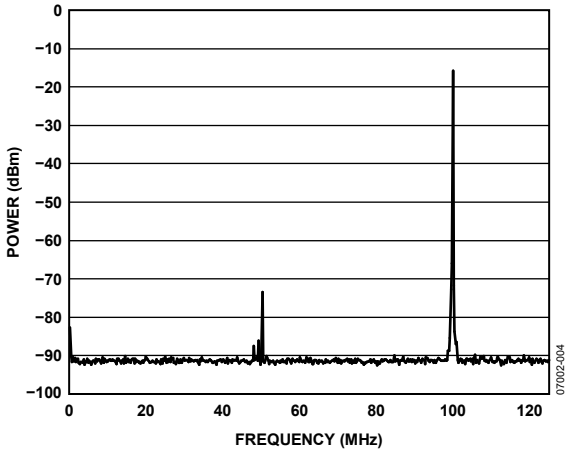


Figure 4. Wideband SFDR @ 99.76 MHz f_{OUT}
(250 MHz Clock, 4 mA DAC Full-Scale Current, PLL Bypassed)

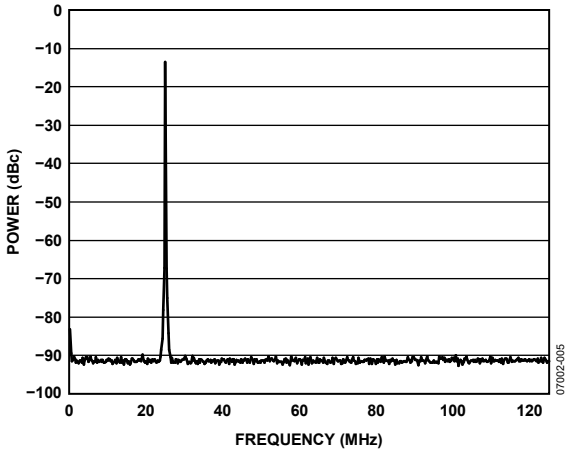


Figure 5. Wideband SFDR @ 25.14 MHz fOUT
(250 MHz Clock, 4 mA DAC Full-Scale Current, PLL Bypassed)

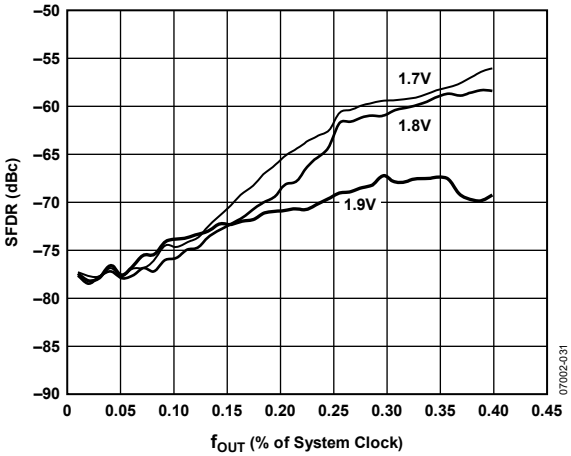


Figure 6. SFDR vs. Supply Variation
(250 MHz Clock, 4 mA DAC Full-Scale Current, PLL Bypassed)

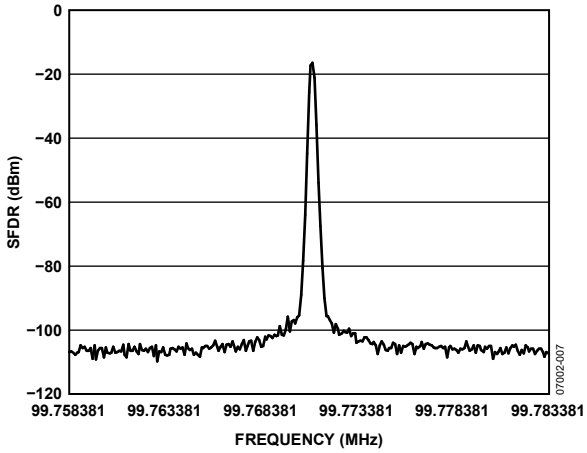


Figure 7. Narrow-Band SFDR @ 99.76 MHz f_{OUT}
(250 MHz Clock, 4 mA DAC Full-Scale Current, PLL Bypassed)

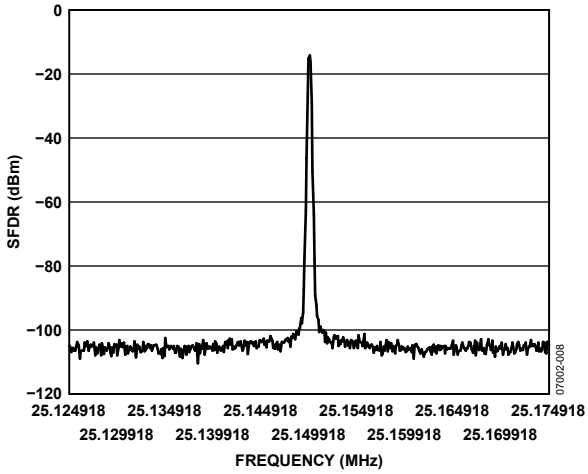


Figure 8. Narrow-Band SFDR @ 25.14 MHz f_{OUT}
(250 MHz Clock, 4 mA DAC Full-Scale Current, PLL Bypassed)

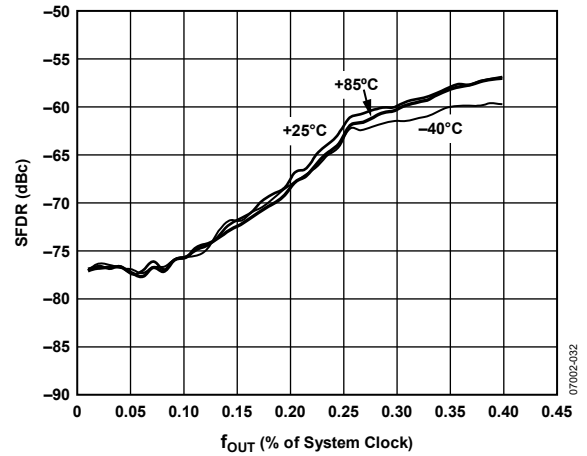


Figure 9. SFDR vs. Temperature
(250 MHz Clock, 4 mA DAC Full-Scale Current, PLL Bypassed)

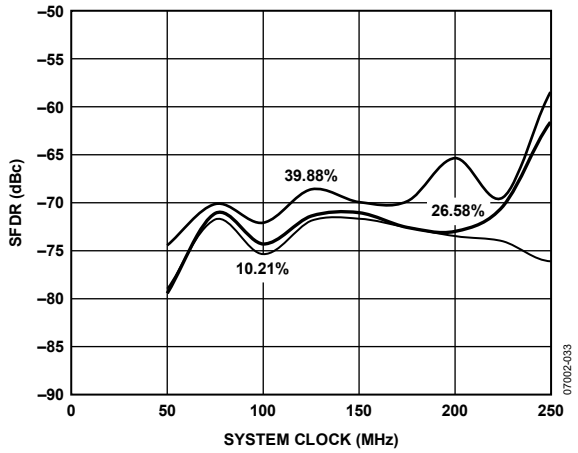


Figure 10. SFDR vs. System Clock Frequency (PLL Bypassed)

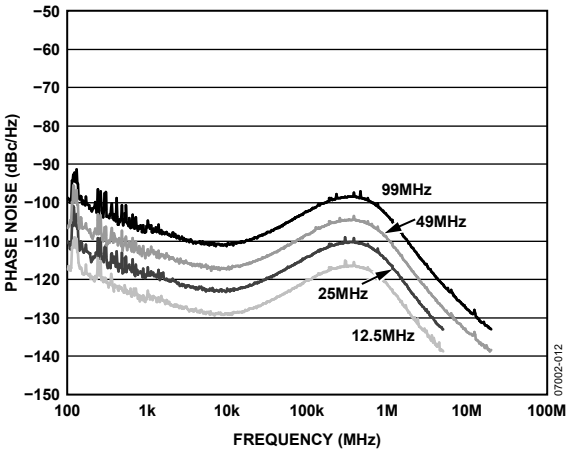


Figure 12. Absolute Phase Noise vs. fOUT Using the Internal PLL (REF_CLK 25 MHz × 10 = 250 MHz Using PLL)

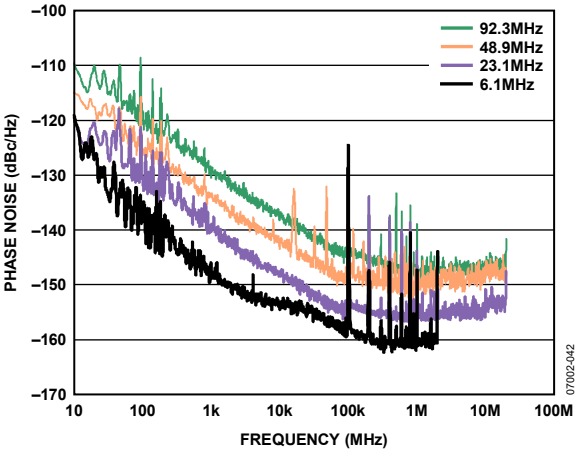


Figure 11. Residual Phase Noise vs. f_{OUT} (PLL Bypassed)

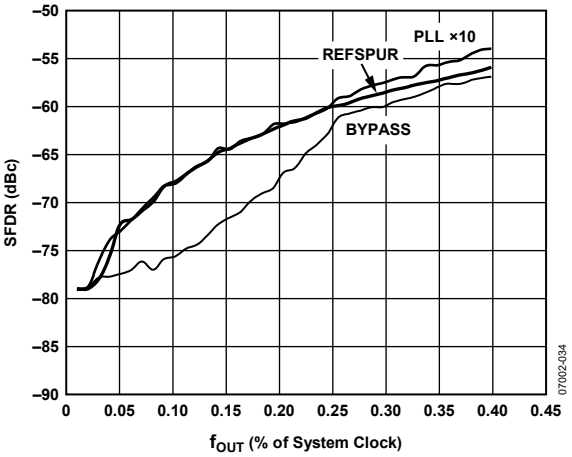


Figure 13. SFDR Without the Internal PLL (REF_CLK = 25 MHz × 10 = 250 MHz Using PLL, 4 mA DAC Full-Scale Current)

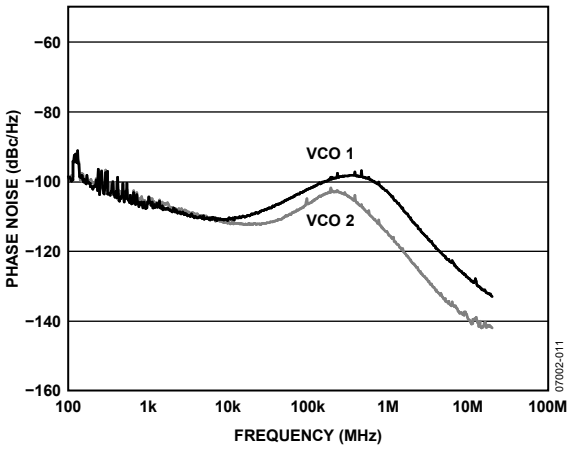


Figure 14. Absolute Phase Noise, VCO1 vs. VCO2

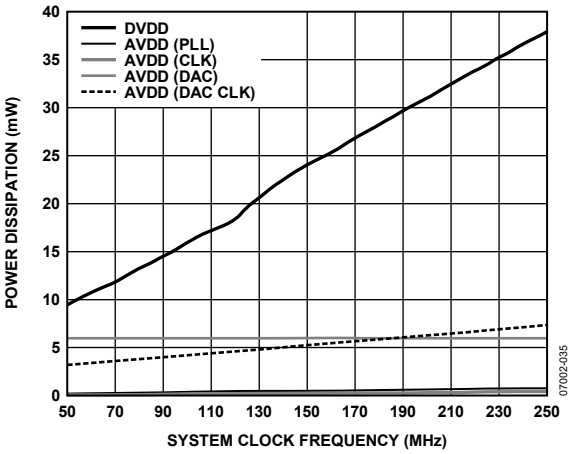


Figure 15. Power Supply Current Domains
(CMOS Input Mode, 4 mA DAC Full-Scale Current, Single Tone)

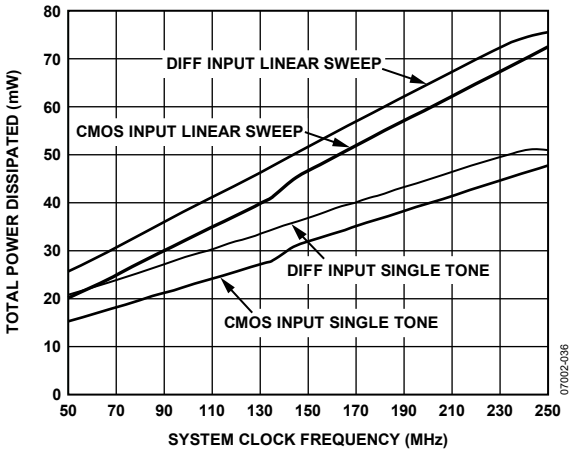


Figure 16. Power Dissipation vs. System Clock Frequency
vs. Clock Input Mode

APPLICATIONS CIRCUITS

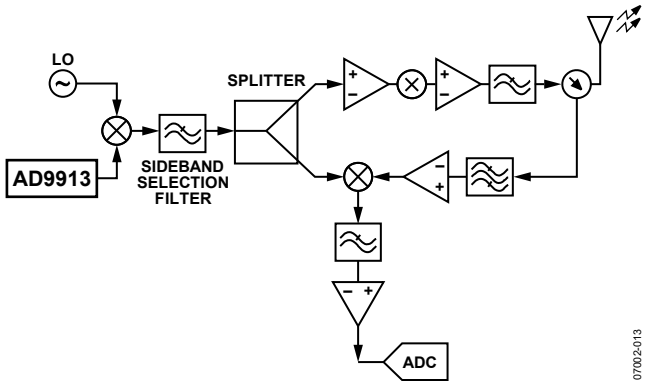


Figure 17. RFID Block Diagram (Only I-Channel of Receiver Shown)

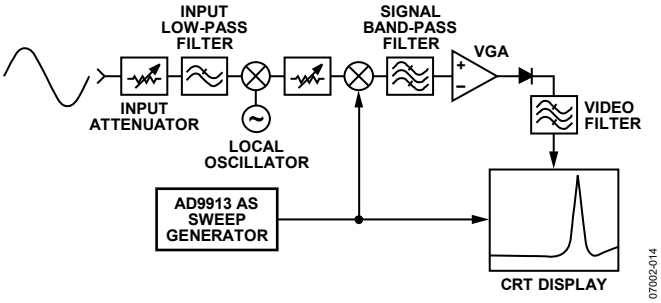


Figure 18. Handheld Spectrum Analyzer

THEORY OF OPERATION

DDS CORE

The DDS block generates a reference signal (sine or cosine based on the selected DDS sine output bit). The parameters of the reference signal (frequency and phase), are applied to the DDS at its frequency and phase offset control inputs, as shown in Figure 19.

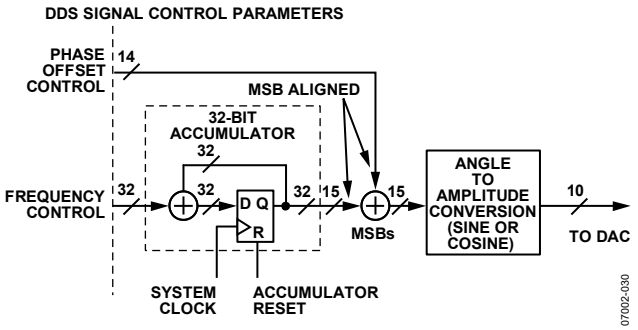


Figure 19. DDS Block Diagram

The output frequency (f_{OUT}) of the AD9913 is controlled by the frequency tuning word (FTW) at the frequency control input to the DDS. In all modes except for programmable modulus, the relationship between f_{OUT}, FTW, and f_{SYSCLK} is:

$$f_{OUT} = \left(\frac{FTW}{2^{32}}\right) f_{SYSCLK} \quad (1)$$

where *FTW* is a 32-bit integer ranging in value from 0 to 2,147,483,647 ($2^{31} - 1$), which represents the lower half of the full 32-bit range. This range constitutes frequencies from dc to Nyquist (that is, ½ f_{SYSCLK}).

The FTW required to generate a desired value of f_{OUT} is found by solving Equation 1 for FTW as given in Equation 2

$$FTW = \text{round}\left(2^{32}\left(\frac{f_{OUT}}{f_{SYSCLK}}\right)\right) \quad (2)$$

where the round*(x)* function rounds the argument (the value of x) to the nearest integer. This is required because the FTW is constrained to be an integer value.

For applications where rounding to the nearest available frequency is not acceptable, programmable modulus mode enables additional options.

The relative phase of the DDS signal can be digitally controlled by means of a 14-bit phase offset word (POW). The phase offset is applied prior to the angle-to-amplitude conversion block internal to the DDS core. The relative phase offset (Δθ) is given by

$$\Delta\theta = \begin{vmatrix} 2\pi\left(\frac{POW}{2^{14}}\right) \\ 360\left(\frac{POW}{2^{14}}\right) \end{vmatrix}$$

where the upper quantity is for the phase offset expressed as radian units and the lower quantity as degrees. To find the POW value necessary to develop an arbitrary Δθ, solve the above equation for POW and round the result (in a manner similar to that described for finding an arbitrary FTW in Equation 1 and Equation 2).

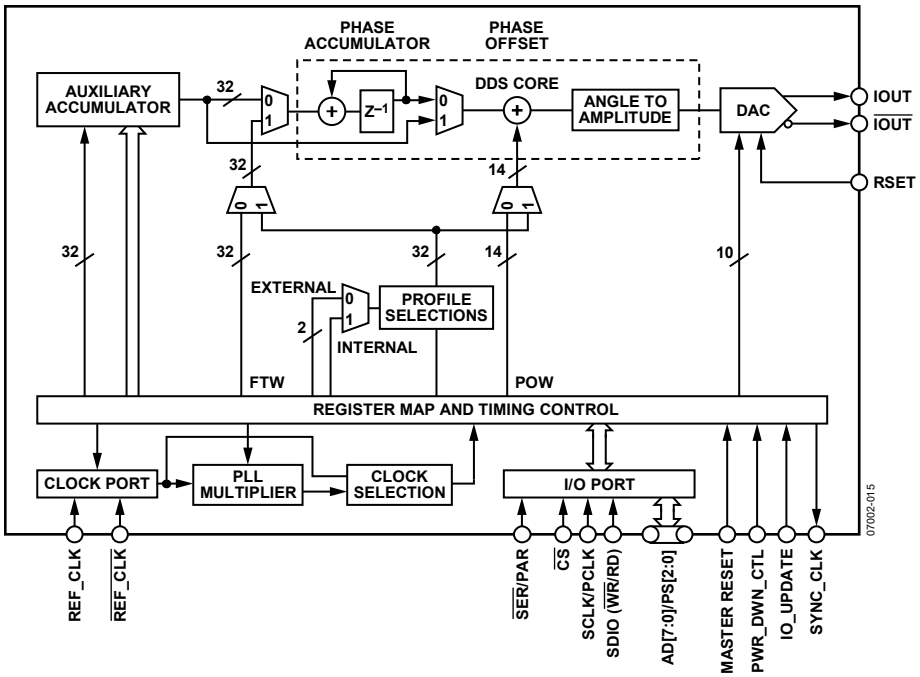


Figure 20. Detailed Block Diagram

AUXILIARY ACCUMULATOR

In addition to the phase accumulator of the DDS, the AD9913 has an auxiliary accumulator. This accumulator can be configured to support either an automatic sweep of one of the programmable characteristics of the DDS output (frequency or phase), or it can be configured to implement a change in the denominator of the frequency equation given in the DDS Core section. For further details, refer to the Programmable Modulus Mode section.

10-BIT DAC

The AD9913 incorporates an integrated 10-bit, current output DAC. The output current is delivered as a balanced signal using two outputs. The use of balanced outputs reduces the potential amount of common-mode noise present at the DAC output, offering the advantage of an increased signal-to-noise ratio. An external resistor (R_{SET}) connected between the RSET pin and AGND establishes the reference current. The full-scale output current of the DAC (I_{OUT}) is produced as a scaled version of the reference current. The recommended value of R_{SET} is 4.62 kΩ.

The following equation computes the typical full-scale current with respect to the R_{set} resistor value and the gain control setting:

$$I_{OUT}(x, R_{SET}) = \frac{0.0206}{R_{SET}} \times (1 + x)$$

The DAC is designed to operate with full-scale current values up to 4.58 mA. Based on the equation and assuming a 4.62 kΩ resistor value for R_{SET}, and x = 0x1FF, the nominal output current for the DAC is 2.28 mA.

Figure 21 shows the range of DAC output current vs. the DAC FS value assuming an R_{SET} value of 4.62 kΩ.

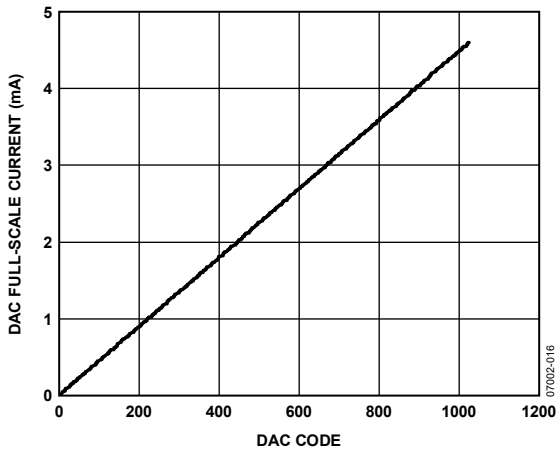


Figure 21. DAC Output Current vs. DAC FS Bits

Pay careful attention to the load termination to ensure that the output voltage remains within the specified compliance range; voltages developed beyond this range cause excessive distortion and can damage the DAC output circuitry.

I/O PORT

The AD9913 I/O port can be configured as a synchronous serial communications port that allows easy interface to many industry-standard microcontrollers and microprocessors. The serial I/O port is compatible with most synchronous transfer formats, including both the Motorola 6905/11 SPI and Intel 8051 SSR protocols. For faster programming requirements, a parallel mode is also provided.

PROFILE SELECTIONS

The AD9913 supports the use of profiles, which consist of a group of eight registers containing pertinent operating parameters for a particular operating mode. Profiles enable rapid switching between parameter sets. Profile parameters are programmed via the I/O port. Once programmed, a specific profile is activated by means of Register CFR1 Bits [22:20], or three external profile select pins. The external profile pins option is only available in serial mode.

MODES OF OPERATION

The AD9913 operates in four modes:

- Single tone
- Direct switch
- Programmable modulus
- Linear sweep

The modes relate to the data source used to supply the DDS with its signal control parameters: frequency, phase, or amplitude. The partitioning of the data into different combinations of frequency, phase, and amplitude is handled automatically based on the mode and/or specific control bits.

SINGLE TONE MODE

Single tone mode is the default operational mode and is active when both the direct switch mode bit and the auxiliary accumulator enable bit are not set. This mode outputs a single frequency as programmed by the user in the frequency tuning word (FTW) register. A phase offset value is also available in single tone mode via the POW register.

DIRECT SWITCH MODE

Direct switch mode enables FSK or PSK modulation. This mode simply selects the frequency or phase value programmed into the profile registers. Frequency or phase is determined by the destination bits in CFR1 [13:12]. Direct switch mode is enabled using the direct switch mode active bit in register CFR1 [16].

Two approaches are designed for switching between profile registers. The first is programming the internal profile control bits, CFR1 [22:20], to the desired value and issuing an IO_UPDATE. The second approach, with higher data throughput, is achieved by changing the profile control pins [2:0]. Control bit CFR1 [27] is for selection between the two approaches. The default state uses the profile pins.

To perform 8-tone FSK or PSK, program the FTW word or phase offset word in each profile. The internal profile control bits or the profile pins are used for the FSK or PSK data.

Table 4 shows the relationship between the profile selection pin or bit approach.

Table 4. Profile Selection

Profile Pins PS [2:0] or CFR1 Bits [22:20]	Profile Selection
000	Profile 0
001	Profile 1
010	Profile 2
011	Profile 3
100	Profile 4
101	Profile 5
110	Profile 6
111	Profile 7

PROGRAMMABLE MODULUS MODE

In programmable modulus mode, the auxiliary accumulator is used to alter the frequency equation of the DDS core, making it possible to implement fractions which are not restricted to a power of 2 in the denominator.

A standard DDS is restricted to powers of 2 as a denominator because the phase accumulator is a set of bits as wide as the frequency tuning word. When in programmable modulus mode, the frequency equation becomes

$$f_0 = (FTW)(f_S)/x \text{ with } 0 \le FTW \le 2^{31}$$

$$f_0 = f_S \times (1 - (FTW/x)) \text{ with } 2^{31} < FTW < 2^{32} - 1$$

where $0 \le x \le 2^{32}$.

When in programmable modulus mode, the auxiliary accumulator is set up to roll over before it reaches full capacity. Every time it rolls over, an extra LSB value is added to the phase accumulator. In order to determine the values that must be programmed in the registers, the user must define the desired output to sampling clock frequency as a ratio of integers (M/N, where N must not exceed 2^{32}).

Refer to the AN-953 Application Note for detailed steps of how to implement a programmable modulus. The AN-953 defines how to calculate the three required values (A, B, and X) used for programmable modulus. The following assigns the required values to the appropriate register.

- Register 0x06 [63:32] holds the B value.
- Register 0x06 [31:0] holds the X value.
- Register 0x07 [31:0] holds the A value.

LINEAR SWEEP MODE

One purpose of linear sweep mode is to provide better bandwidth containment compared to direct switch mode by enabling more gradual, user-defined changes between a starting point (S0) to an endpoint (E0). The auxiliary accumulator enable bit is located in Register CFR1 [11]. Linear sweep uses the auxiliary accumulator to sweep frequency or phase from S0 to E0. A frequency or phase sweep is determined by the destination bits in CFR1 [13:12]. The trigger to initiate the sweep can be edge or level triggered. This is determined by Register CFR1 [9]. Note that, in level triggered mode, the sweep automatically repeats as long as the appropriate profile pin is held high.

In linear sweep mode, S0 and E0 (upper and lower limits) are loaded into the linear sweep parameter register (Register 0x06). If configured for frequency sweep, the resolution is 32-bits. For phase sweep, the resolution is 14 bits. When sweeping the phase, the word value must be MSB-aligned; unused bits are ignored. The profile pins or the internal profile bits trigger and control the direction (up/down) of the linear sweep for frequency or phase. Table 5 depicts the direction of the sweep.

Table 5. Determining the Direction of the Linear Sweep

Profile Pins [2:0] or CFR1 Bits [22:20]	Linear Sweep Mode
x00[1]	Sweep off
x01[1]	Ramp up
x10[1]	Ramp down
x11[1]	Bidirectional ramp

[1] x = don't care.

Note that if the part is used in parallel port programming mode, the sweep mode is only determined by the internal profile control bits, CFR1 [22:20]. If the part is used in serial port programming mode, either the internal profile control bits or the external profile select pins can work as the sweep control. CFR1 [27] selects between these two approaches.

Setting the Slope of the Linear Sweep

The slope of the linear sweep is set by the intermediate step size (delta tuning word) between S0 and E0 (see Figure 22) and the time spent (sweep ramp rate word) at each step. The resolution of the delta tuning word is 32 bits for frequency and 14 bits for phase. The resolution for the delta ramp rate word is 16 bits.

In linear sweep mode, the user programs a rising delta word (RDW, Register 0x07) and a rising sweep ramp rate (RSRR, Register 0x08). These settings apply when sweeping from S0 to E0. The falling delta word (FDW, Register 0x07) and falling sweep ramp rate (FSRR, Register 0x08) apply when sweeping from E0 to S0.

Note that if the auxiliary accumulator is allowed to overflow, an uncontrolled, continuous sweep operation occurs. To avoid this, the magnitude of the rising or falling delta word should be smaller than the difference between full-scale and the E0 value (full-scale − E0). For a frequency sweep, full-scale is $2^{32} - 1$. For a phase sweep, full-scale is $2^{14} - 1$.

Figure 22 displays a linear sweep up and then down. This depicts the dwell mode (see CRF1 [8]). If the no-dwell bit, CFR1 [8], is set, the sweep accumulator returns to 0 upon reaching E0.

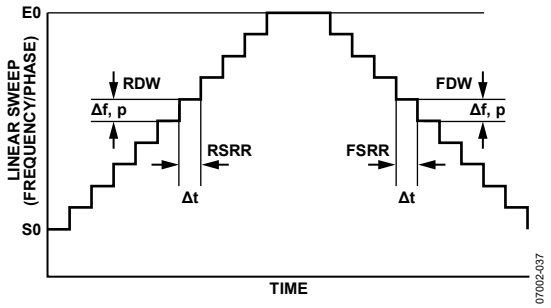


Figure 22. Linear Sweep Mode

For a piecemeal or a nonlinear transition between S0 and E0, the delta tuning words and ramp rate words can be reprogrammed during the transition.

The formulas for calculating the step size of RDW or FDW are

$$Frequency\ Step = \left(\frac{RDW}{2^{32}}\right) f_{SYSCLK} \quad \text{(MHz)}$$

$$Phase\ Step = \left(\frac{\pi RDW}{2^{13}}\right) \quad \text{(radians)}$$

$$Phase\ Step = \left(\frac{45RDW}{2^{11}}\right) \quad \text{(degrees)}$$

The formula for calculating delta time from RSRR or FSRR is

$$\Delta t = (RSRR) / f_{SYSCLK}\,(\text{Hz})$$

At 250 MSPS operation, (f_{SYSCLK} =250 MHz). The minimum time interval between steps is 1/250 MHz × 1 = 4 ns. The maximum time interval is (1/250 MHz) × 65,535= 262 µs.

Frequency Linear Sweep Example

In linear sweep mode, when sweeping from low to high, the RDW is applied to the input of the auxiliary accumulator and the RSRR register is loaded into the sweep rate timer.

The RDW accumulates at the rate given by the ramp rate (RSRR) until the output equals the upper limit in the linear sweep parameter register (Register 0x06). The sweep is then complete.

When sweeping from high to low, the FDW is applied to the input of the auxiliary accumulator and the FSRR register is loaded into the sweep rate timer.

The FDW accumulates at the rate given by the ramp rate (FSRR) until the output equals the lower limit in the linear sweep parameter register value (Register 0x06). The sweep is then complete. A phase sweep works in the same manner with fewer bits.

To view sweep capabilities using the profile pins and the no-dwell bit, refer to Figure 23, Figure 24, and Figure 25.

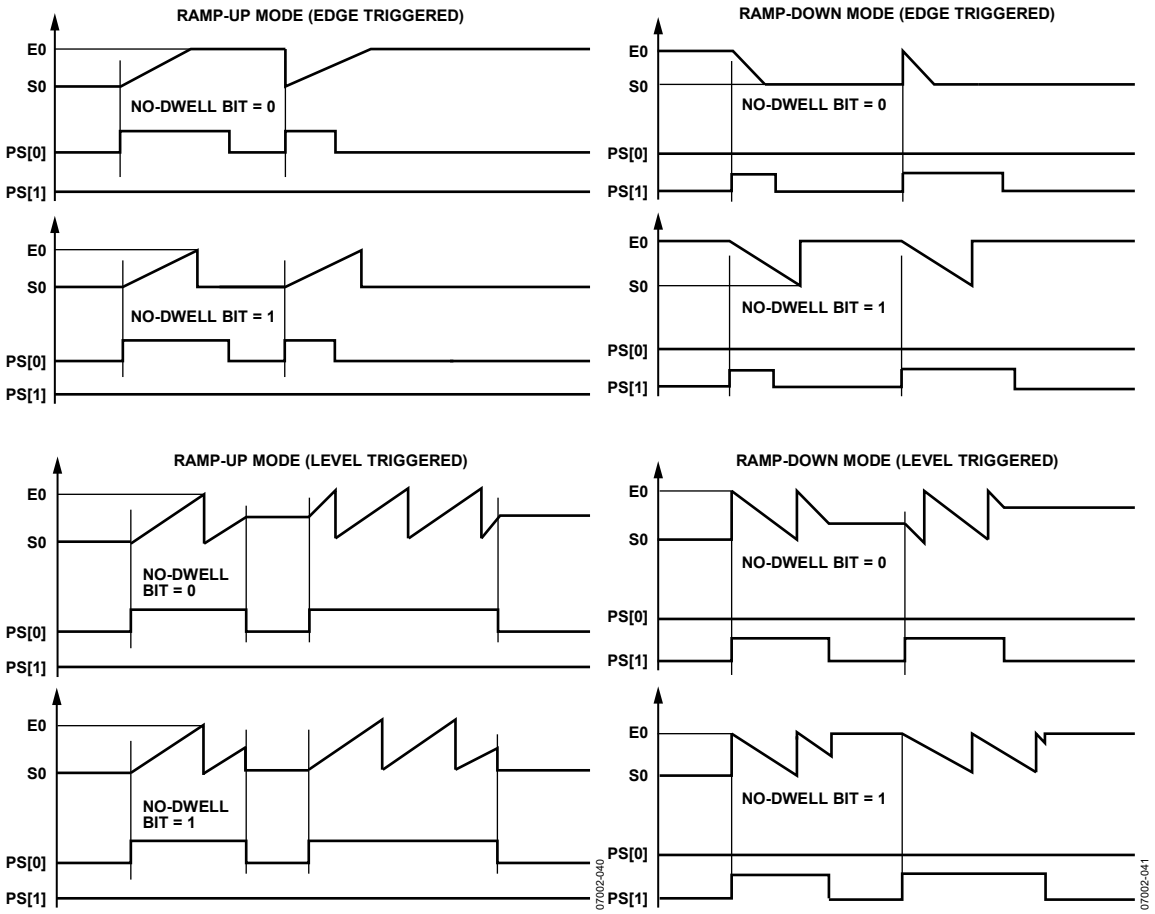


Figure 23. Display of Ramp-Up and Ramp-Down Capability Using the External Profile Pins

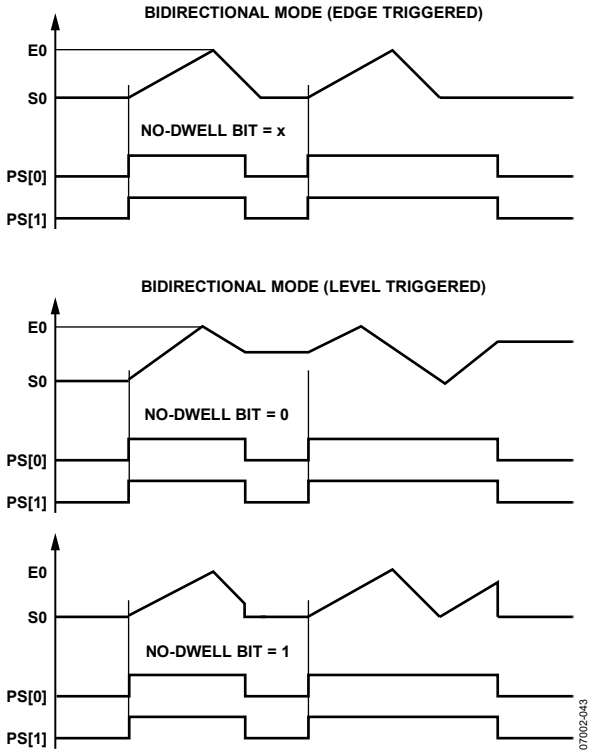


Figure 24. Display of Bidirectional Ramp Capability Using the External Profile Pins

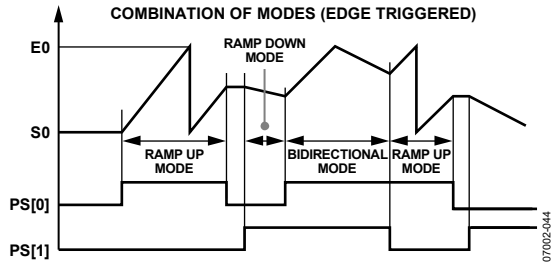


Figure 25. Combination of Sweep Modes Using the External Profile Pins

Clear Functions

The AD9913 allows for a programmable continuous zeroing of the sweep logic and the phase accumulator as well as clear-and-release, or automatic zeroing function. Each feature is individually controlled via bits in the control registers.

Continuous Clear Bits

The continuous clear bits are simply static control signals that hold the respective accumulator (and associated logic) at zero for the entire time the bit is active.

Clear-and-Release Function

The auto clear auxiliary accumulator bit, when active, clears and releases the auxiliary accumulator upon receiving an I/O_UPDATE or change in profile bits.

The auto clear phase accumulator, when active, clears and releases the phase accumulator upon receiving a I/O_UPDATE or a change in profile bits.

The automatic clearing function is repeated for every subsequent I/O_UPDATE or change in profile bits until the control bit is cleared.

These bits are programmed independently and do not have to be active at the same time. For example, one accumulator may be using the clear and release function while the other is continuously cleared.

CLOCK INPUT (REF_CLK)

REF_CLK OVERVIEW

The AD9913 supports a number of options for producing the internal SYSCLK signal (that is, the DAC sample clock) via the REF_CLK input pins. The REF_CLK input can be driven directly from a differential or single-ended source, or it can accept a crystal connected across the two input pins. There is also an internal phase-locked loop (PLL) multiplier that can be independently enabled. The various input configurations are controlled by means of the control bits in the CFR2 [7:5] register.

Table 6. Clock Input Mode Configuration

CFR2 [7:5]	Mode Configuration
000	Differential Input, PLL Enabled
001	Differential Input, PLL Disabled (Default)
x10[1]	XTAL Input, PLL Enabled
x11[1]	XTAL Input, PLL Disabled
100	CMOS Input, PLL Enabled
101	CMOS Input PLL Disabled

[1] x = don't care.

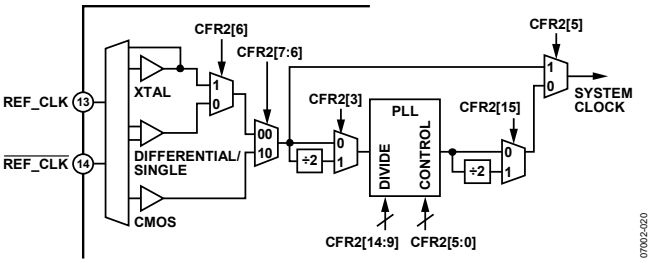


Figure 26. Internal Clock Path Functional Block Diagram

CRYSTAL-DRIVEN REF_CLK

When using a crystal at the REF_CLK input, the resonant frequency should be approximately 25 MHz. Figure 27 shows the recommended circuit configuration.

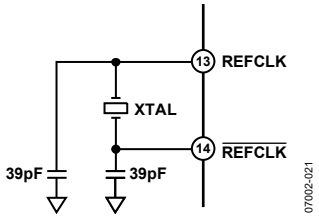


Figure 27. Crystal Connection Diagram

DIRECT-DRIVEN REF_CLK

When driving the REF_CLK inputs directly from a signal source, either single-ended or differential signals can be used. With a differential signal source, the REF_CLK pins are driven with complementary signals and ac-coupled with 0.1 µF capacitors. With a single-ended signal source, either a single-ended-to-differential conversion can be employed or the REF_CLK input can be driven single-ended directly. In either case, 0.1 µF capacitors are used to ac couple both REF_CLK pins to avoid disturbing the internal dc bias voltage of ~1.35 V. See Figure 28 for more details.

The REF_CLK input resistance is ~2.7 kΩ differential (~1.35 kΩ single-ended). Most signal sources have relatively low output impedances. The REF_CLK input resistance is relatively high, therefore, its effect on the termination impedance is negligible and can usually be chosen to be the same as the output impedance of the signal source. The bottom two examples in Figure 28 assume a signal source with a 50 Ω output impedance.

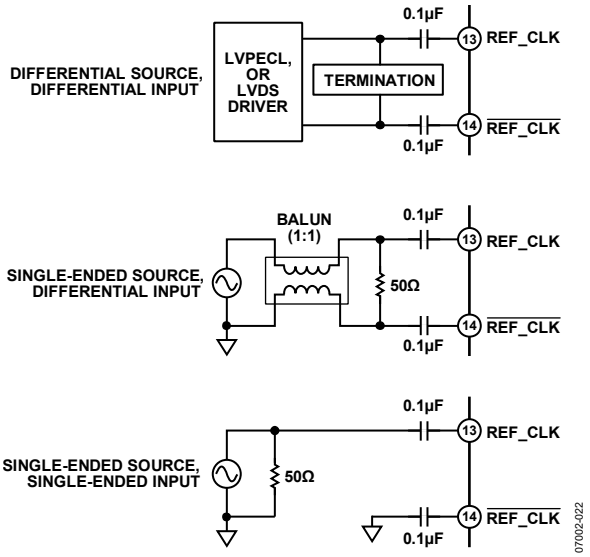


Figure 28. Direct Connection Diagram

CMOS-DRIVEN REF_CLK

This mode is enabled by writing CFR2 [7] to be true. In this state, the AD9913 must be driven at Pin 13 with the reference clock source. Additionally, it is recommended that Pin 14 in CMOS mode be tied to ground through a 10 kΩ resistor.

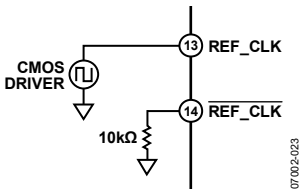


Figure 29. CMOS-Driven Diagram

PHASE-LOCKED LOOP (PLL) MULTIPLIER

An internal phase-locked loop (PLL) provides users of the AD9913 the option to use a reference clock frequency that is lower than the system clock frequency. The PLL supports a wide range of programmable frequency multiplication factors (1× to 64×). See Table 7 for details on configuring the PLL multiplication factor. The PLL is also equipped with a PLL_LOCK bit.

CFR2 [15:8] and CFR2 [5:1] control the PLL operation. Upon power-up, the PLL is off. To initialize the PLL, CFR2 [5] must be cleared and CFR2 [1] must be set. The function of CFR2 [1]

is to reset digital logic in the PLL circuit with an active low signal. The function of CFR2 [5] is to power up or power down the PLL.

CFR2 [4] is the PLL LO range bit. When operating the AD9913 with the PLL enabled, CFR2 [4] adjusts PLL loop filter components to allow low frequency reference clock inputs.

CFR2 [3] enables a divide-by-two circuit at the input of the PLL phase detector. If this bit is enabled the reference clock signal is divided by 2 prior to multiplication in the PLL. Refer to the electrical specifications for the maximum reference clock input frequency when utilizing the PLL with the divide by 2 circuit enabled. If the divide by 2 circuit is disabled and the PLL is enabled, then the maximum reference clock input frequency is one-half the maximum rate indicated in the electrical specifications table for the maximum input divider frequency.

The AD9913 PLL uses one of two VCOs for producing the system clock signal. CFR2 Bit 2 is a select bit that enables an alternative VCO in the PLL. The basic operation of the PLL is not affected by the state of this bit. The purpose of offering two VCOs is to provide performance options. The two VCOs have approximately the same gain characteristics, but differ in other aspects. The overall spurious performance, phase noise, and power consumption may change based on the setting of CFR2 Bit 2. It is important to consider that for either VCO, the minimum oscillation frequency must be satisfied, and that minimum oscillation frequency is significantly different between the two oscillators.

CFR2 [15:9], along with CFR2 [3], determine the multiplication of the PLL. CFR2 [15] enables a divider at the output of the PLL. The bits CFR [14:9] control the feedback divider. The feedback divider is composed of two stages: ÷ N (1:31) selected by CFR2 [13:9]; ÷1 or ÷2 selected by CFR2 [14].

Note that the same system clock frequency can be obtained with different combinations of CFR2 [15:9] and CFR2 [3]. One combination may work better in a given application either to run at lower power or to satisfy the VCOs minimum oscillation frequency.

Note that the AD9913 maximum system clock frequency is 250 MHz. If the user intends to use high values for the PLL feedback divider ratio, then care should be taken that the system clock frequency does not exceed 250 MHz.

PLL LOCK INDICATION

CFR2 [0] is a read-only bit that displays the status of the PLL lock signal.

When the AD9913 is programmed to use the PLL, there is some amount of time required for the loop to lock. While the loop is not locked, the chip system clock operates at the reference clock frequency presented to the part at the pins. Once the PLL lock signal goes high, the system clock frequency switches asynchronously to operate at the PLL output frequency. To maintain a system clock frequency with or without a locked loop if the PLL lock signal transistions low, the chip reverts to the reference clock signal while the loop attempts to acquire lock once again.

Table 7 describes how to configure the PLL multiplication factor using the appropriated register bits.

Table 7. PLL Multiplication Factor Configuration

	CFR2 [15:14], CFR2 [3]							
CFR2 [13:9]	**= 000**	**= 001**	**= 100**	**= 101**	**= 010**	**= 011**	**= 110**	**= 111**
00000	32	16	16	8	64	32	32	16
00001	1	0.5	0.5	0.25	2	1	1	0.5
00010	2	1	1	0.5	4	2	2	1
00011	3	1.5	1.5	0.75	6	3	3	1.5
00100	4	2	2	1	8	4	4	2
00101	5	2.5	2.5	1.25	10	5	5	2.5
00110	6	3	3	1.5	12	6	6	3
00111	7	3.5	3.5	1.75	14	7	7	3.5
01000	8	4	4	2	16	8	8	4
01001	9	4.5	4.5	2.25	18	9	9	4.5
01010	10	5	5	2.5	20	10	10	5
01011	11	5.5	5.5	2.75	22	11	11	5.5
01100	12	6	6	3	24	12	12	6
01101	13	6.5	6.5	3.25	26	13	13	6.5
01110	14	7	7	3.5	28	14	14	7
01111	15	7.5	7.5	3.75	30	15	15	7.5
10000	16	8	8	4	32	16	16	8
10001	17	8.5	8.5	4.25	34	17	17	8.5
10010	18	9	9	4.5	36	18	18	9
10011	19	9.5	9.5	4.75	38	19	19	9.5
10100	20	10	10	5	40	20	20	10
10101	21	10.5	10.5	5.25	42	21	21	10.5
10110	22	11	11	5.5	44	22	22	11
10111	23	11.5	11.5	5.75	46	23	23	11.5
11000	24	12	12	6	48	24	24	12
11001	25	12.5	12.5	6.25	50	25	25	12.5
11010	26	13	13	6.5	52	26	26	13
11011	27	13.5	13.5	6.75	54	27	27	13.5
11100	28	14	14	7	56	28	28	14
11101	29	14.5	14.5	7.25	58	29	29	14.5
11110	30	15	15	7.5	60	30	30	15
11111	31	15.5	15.5	7.75	62	31	31	15.5

POWER-DOWN FEATURES

The AD9913 supports an externally controlled power-down feature as well as software programmable power-down bits consistent with other Analog Devices, Inc. DDS products.

The external PWR_DWN_CTL pin determines the power-down scheme. A low on this pin allows the user to power down DAC, PLL, input clock circuitry, and the digital section of the chip individually via the unique control bits, CFR1 [6:4]. In this mode, CFR1 [7] is inactive.

When the PWR_DWN_CTL is set, CFR1 [6:4] lose their meaning. At the same time, the AD9913 provides two different power-down modes based on the value of CFR1 [7]: a fast recovery power-down mode in which only the digital logic and the DAC digital logic are powered down, and a full power-down mode in which all functions are powered down. A significant amount of time is required to recover from power-down mode.

Table 8 indicates the logic level for each power-down bit that drives out of the AD9913 core logic to the analog section and the digital clock generation section of the chip for the external power-down operation.

Table 8. Power-Down Controls

Control	Mode Active	Description
PWR_DWN_CTL = 0 CFR1 [7] = don't care	Software Control	Digital power-down = CFR1 [6] DAC power-down = CFR1 [5] Input clock power-down = CFR1 [4]
PWRDWNCTL = 1 CFR1 [7] = 0	External Control, Fast recovery power-down mode	N/A
PWRDWNCTL = 1 CFR1 [7] = 1	External Control, Full power-down mode	N/A

I/O PROGRAMMING

SERIAL PROGRAMMING

The AD9913 serial port is a flexible, synchronous serial communications port allowing an easy interface to many industry standard microcontrollers and microprocessors.

The interface allows read/write access to all registers that configure the AD9913. MSB first or LSB first transfer formats are supported. The AD9913 serial interface port is configured as a single pin I/O (SDIO), which allows a two-wire interface. The AD9913 does not have a SDO pin for 3-wire operation.

With the AD9913, the instruction byte specifies read/write operation and the register address. Serial operations on the AD9913 occur only at the register level, not the byte level.

For the AD9913, the serial port controller recognizes the instruction byte register address and automatically generates the proper register byte address. In addition, the controller expects that all bytes of that register are accessed. It is a requirement that all bytes of a register be accessed during serial I/O operations.

There are two phases to a communication cycle with the AD9913. Phase 1 is the instruction cycle, which is the writing of an instruction byte into the AD9913, coincident with the first eight SCLK rising edges. The instruction byte provides the AD9913 serial port controller with information regarding the data transfer cycle, which is Phase 2 of the communication cycle. The Phase 1 instruction byte defines whether the upcoming data transfer is read or write and the serial address of the register being accessed.

The first eight SCLK rising edges of each communication cycle are used to write the instruction byte into the AD9913. The remaining SCLK edges are for Phase 2 of the communication cycle. Phase 2 is the actual data transfer between the AD9913 and the system controller. The number of bytes transferred during Phase 2 of the communication cycle is a function of the register accessed. For example, when accessing the Control Function Register 2, which is two bytes wide, Phase 2 requires that two bytes be transferred. If accessing one of the profile registers, which are six bytes wide, Phase 2 requires that six bytes be transferred. After transferring all data bytes per the instruction, the communication cycle is completed.

At the completion of any communication cycle, the AD9913 serial port controller expects the next eight rising SCLK edges to be the instruction byte of the next communication cycle.

All data input to the AD9913 is registered on the rising edge of SCLK. All data is driven out of the AD9913 on the falling edge of SCLK. Figure 30 through Figure 32 illustrate the general operation of serial ports.

Note that IO_UPDATE is not shown in Figure 30 and Figure 31. The IO_UPDATE transfers the contents of the write sequence to the active register. See the Register Update (I/O Update) section.

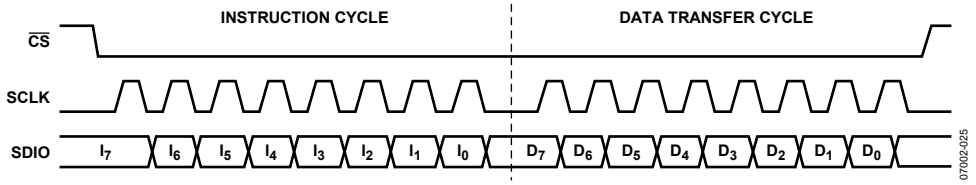


Figure 30. Serial Port Writing Timing—Clock Stall Low

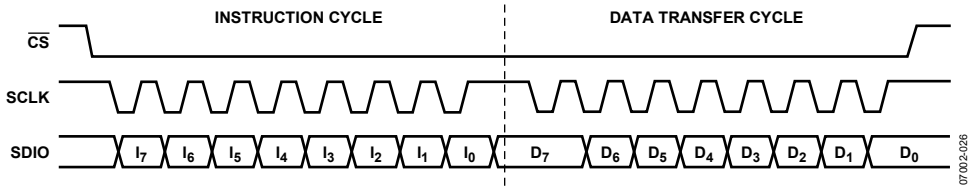


Figure 31. Serial Port Write Timing—Clock Stall High

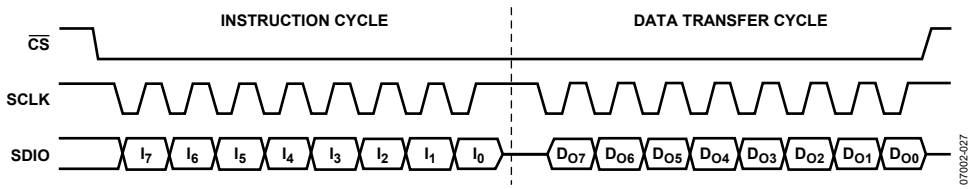


Figure 32. Two-Wire Serial Port Read Timing—Clock Stall High

Instruction Byte

The instruction byte contains the following information as shown in the instruction byte bit map.

Instruction Byte Information Bit Map

MSB **LSB**

D7	D6	D5	D4	D3	D2	D1	D0
R/$\overline{W}$	X	X	A4	A3	A2	A1	A0

R/$\overline{W}$—Bit 7 of the instruction byte determines whether a read or write data transfer occurs after the instruction byte write. Logic high indicates read operation. Logic 0 indicates a write operation.

X, X—Bit 6 and Bit 5 of the instruction byte are don't care.

A4, A3, A2, A1, A0—Bit 4, Bit 3, Bit 2, Bit 1, and Bit 0 of the instruction byte determine which register is accessed during the data transfer portion of the communications cycle.

Serial Interface Port Pin Description

SCLK—Serial Port Clock

The serial clock pin is used to synchronize data to and from the AD9913 and to run the internal state machines.

$\overline{CS}$—Chip Select

Active low input that allows more than one device on the same serial communications line. The SDIO pin goes to a high impedance state when this input is high. If driven high during any communications cycle, that cycle is suspended until chip select is reactivated low. Chip select can be tied low in systems that maintain control of SCLK.

SDIO—Serial Data I/O.

Data is always written into and read from the AD9913 on this pin.

MSB/LSB Transfers

The AD9913 serial port can support both most significant bit (MSB) first or least significant bit (LSB) first data formats. This functionality is controlled by the CFR1 [23]. The default value is MSB first. The instruction byte must be written in the format indicated by Control Register 0x00 Bit 8. That is, if the AD9913 is in LSB first mode, the instruction byte must be written from least significant bit to most significant bit.

For MSB first operation, the serial port controller generates the most significant byte (of the specified register) address first followed by the next less significant byte addresses until the I/O operation is complete. All data written to (read from) the AD9913 must be in MSB first order.

If the LSB mode is active, the serial port controller generates the least significant byte address first followed by the next greater significant byte addresses until the I/O operation is complete. All data written to (read from) the AD9913 must be in LSB first order.

Notes on Serial Port Operation

The LSB first bit resides in CFR1 [23]. Note that the configuration changes immediately upon writing to the byte containing the LSB first bit. Therefore, care must be taken to compensate for this new configuration for the remainder of the current communication cycle.

Reading profile registers requires that the external profile select pins (PS[2:0]) be configured to select the corresponding register.

PARALLEL I/O PROGRAMMING

Parallel Port Interface Pin Description

$\overline{CS}$—Chip Select

An active low on this pin indicates that a read/write operation is about to be performed. If this pin goes high during an access, the parallel port is reset to its initial condition.

R/$\overline{W}$—Read/Write

A high on Pin 29 combined with $\overline{CS}$ active low indicates a read operation. A low on this pin indicates a write operation.

PCLK—Parallel Port Clock

The parallel clock pin is used to synchronize data to and from the AD9913 and to run the internal state machines.

ADDR/DATA [7:0]

The 8-bit address/data bus. It works in a bidirectional fashion to support both read and write operations.

Notes on Parallel Port Operation

Each operation works in a 3-PCLK cycle with the first clock cycle for addressing, the second for reading or writing, and the third for re-initialization. In parallel port operation, each byte is programmed individually.

Data Read Operation

A typical read operation follows the steps shown in Figure 33.

1. The user supplies PCLK, $\overline{CS}$, R/$\overline{W}$, and the parallel address of the register using the address pins (ADR0 through ADR7) for the read operation.
2. $\overline{CS}$, R/$\overline{W}$, and the address lines must meet the setup and hold times relative to the 1st PCLK rising edge.
3. The user releases the bus to read.
4. The AD9913 drives data onto the bus after the second PCLK rising edge.
5. $\overline{CS}$ must meet the set up and hold times to the 3rd PCLK rising edge.

Data Write Operation

Write operations work in a similar fashion as read operations except that the user drives the bus for both PCLK cycles. A typical write access follows the steps shown in Figure 34.

1. The user supplies the PCLK, $\overline{CS}$, R/$\overline{W}$, and the parallel address of the register and using the address pins (ADR0/D0 through ADR7/D7).
2. $\overline{CS}$, R/$\overline{W}$, and the address lines must meet the set up and hold times relative to the 1st PCLK rising edge.
3. Data lines must meet the set up and hold times relative to the 2nd PCLK rising edge.
4. $\overline{CS}$ must meet the set up and hold times relative to the 3rd PCK rising edge.
5. The IO_UPDATE is not shown in Figure 34. The IO_UPDATE transfers the contents from a write sequence to the active register. See the Register Update (I/O Update) section.

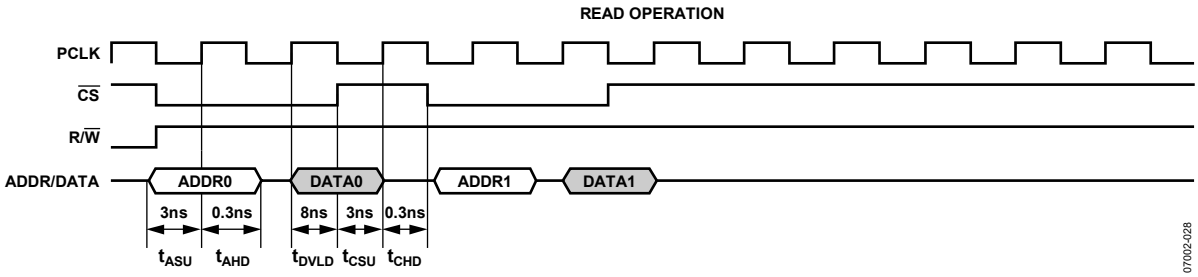


Figure 33. Parallel Port Read Timing

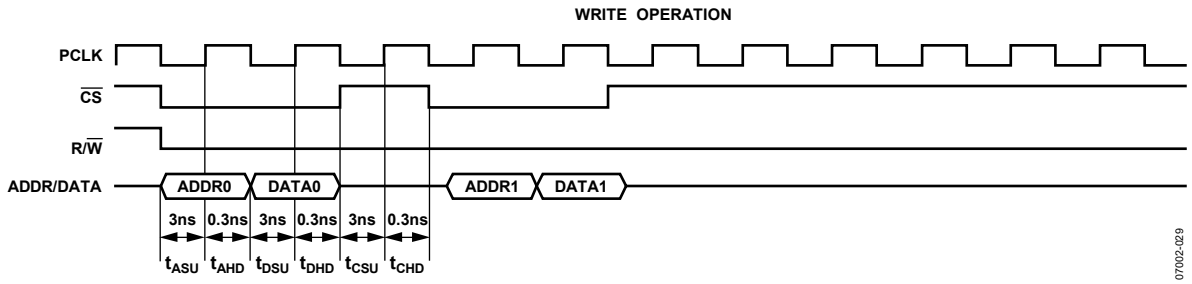


Figure 34. Parallel Port Write Timing

REGISTER UPDATE (I/O UPDATE)

Functionality of the I/O UPDATE and SYNC_CLK

Data from a write sequence is stored in a buffer register (data inactive). An active register exists for every buffer register. The I/O update signal and SYNC_CLK are used to transfer the contents from the buffer register into the active register.

I/O_UPDATE initiates the start of a buffer transfer. It can be sent synchronously or asynchronously relative to the SYNC_CLK. If the setup time between the two signals is met, then constant latency (pipeline) to the DAC output exists. For example, if constant propagation delay of phase offset changes via the SPI or parallel port is desired, the setup time must be met, otherwise, a time uncertainty of one SYNC_CLK period is present.

The I/O_UPDATE is sampled by the SYNC_CLK. Therefore, I/O_UPDATE must have a minimum pulse width greater than one SYNC_CLK period.

The timing diagram shown in Figure 35 depicts how data in the buffer is transferred to the active registers. An I/O_UPDATE is not required for every register write, it can be sent after multiple register writes.

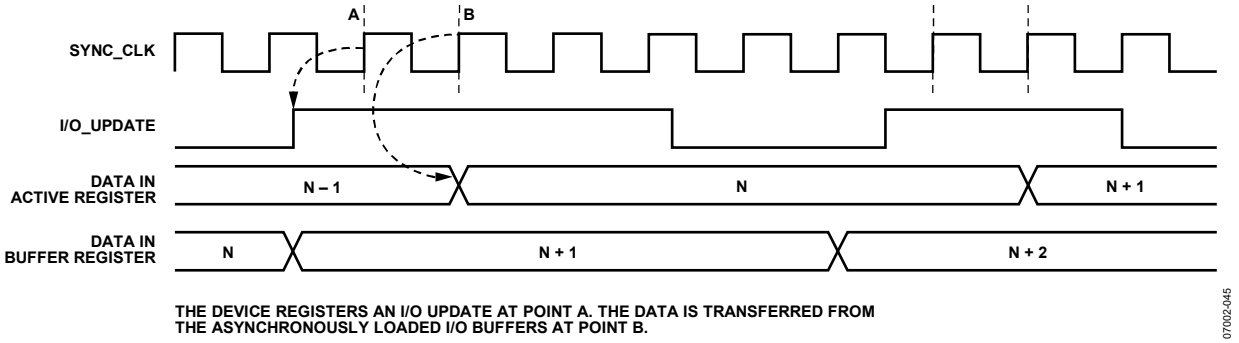


Figure 35. I/O Synchronization Timing Diagram

REGISTER MAP AND BIT DESCRIPTIONS

REGISTER MAP

Note that the highest number found in the Serial Bit Range column for each register in the following tables is the MSB and the lowest number is the LSB for that register.

Table 9. Control Registers

Register Name (Serial Address)	[Serial Bit Range]/Parallel Address	MSB Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	LSB Bit 0	Default Value
CFR1—Control Function Register 1 (0x00)	[7:0]/0x00	External Power-Down Mode	Digital Power-Down	DAC Power-Down	Clock Input Power-Down	Load SRR @ IO_UPDATE	Autoclear Auxiliary Accum.	Autoclear Phase Accum.	Enable Sine Output	0x00
	[15:8]/0x01	Clear Auxiliary Accum.	Clear Phase Accum.	Destination [1:0] 00: Frequency Word 01: Phase Word		Auxiliary Accumulator Enable	DC Output Active	Linear Sweep State Trigger Active	Linear Sweep No-Dwell Active	0x00
	[23:16]/0x02	LSB First	Internal Profile Control [2:0]			Sync Clock Disable	Open	Open	Direct Switch Mode Active	0x00
	[31:24]/0x03	Open	Open	Open	Modulus Enable	Use Internal Profile	Match Pipe Delays Active	Open	Open	0x00
CFR2—Control Function Register 2 (0x01)	[7:0]/0x04	CMOS Clock Mode[1]	Crystal Clock Mode[1]	PLL Power-Down[1]	PLL LO Range	PLL Input Div by 2	VCO2 Sel	PLL Reset	PLL Lock	0x32
	[15:8]/0x05	PLL Output Div by 2	PLL Multiplication Factor [5:0]						Open	0x14
DAC Control Register (0x02)	[7:0]/0x06	FS C [7:0]								0xFF
	[15:8]/0x07	Open	Open	Reserved			Open	FSC [9:8]		0x11
	[23:16]/0x08	Reserved								0x7F
	[31:24]/0x09	Reserved								0x00
FTW (0x03)	[7:0]/0x0A	Frequency Tuning Word [7:0]								0x00
	[15:8]/0x0B	Frequency Tuning Word [15:8]								0x00
	[23:16]/0x0C	Frequency Tuning Word [23:16]								0x00
	[31:24]/0x0D	Frequency Tuning Word [31:24]								0x00
POW (0x04)	[7:0]/0x0E	Phase Offset Word [7:0]								0x00
	[15:8]/0x0F	Open [1:0]	Phase Offset Word [13:8]							0x00
Linear Sweep Parameter Register (0x06)	[7:0]/0x12	Sweep Parameter Word 0 [7:0]								0x00
	[15:8]/0x13	Sweep Parameter Word 0 [15:8]								0x00
	[23:16]/0x14	Sweep Parameter Word 0 [23:16]								0x00
	[31:24]/0x15	Sweep Parameter Word 0 [31:24]								0x00
	[39:32]/0x16	Sweep Parameter Word 1 [7:0]								0x00
	[47:40]/0x17	Sweep Parameter Word 1 [15:8]								0x00
	[55:48]/0x18	Sweep Parameter Word 1 [23:16]								0x00
	[63:56]/0x19	Sweep Parameter Word 1 [31:24]								0x00
Linear Sweep Delta Parameter Register (0x07)	[7:0]/0x1A	Rising Delta Word [7:0]								0x00
	[15:8]/0x1B	Rising Delta Word [15:8]								0x00
	[23:16]/0x1C	Rising Delta Word [23:16]								0x00
	[31:24]/0x1D	Rising Delta Word [31:24]								0x00
	[39:32]/0x1E	Falling Delta Word [7:0]								0x00
	[47:40]/0x1F	Falling Delta Word [15:8]								0x00
	[55:48]/0x20	Falling Delta Word [23:16]								0x00
	[63:56]/0x21	Falling Delta Word [31:24]								0x00

Register Name (Serial Address)	[Serial Bit Range]/Parallel Address	MSB Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	LSB Bit 0	Default Value
Linear Sweep Ramp Rate Register (0x08)	[7:0]/0x22	Rising Sweep Ramp Rate Word [7:0]								0x00
	[15:8]/0x23	Rising Sweep Ramp Rate Word [15:8]								0x00
	[23:16]/0x24	Falling Sweep Ramp Rate Word [7:0]								0x00
	[31:24]/0x25	Falling Sweep Ramp Rate Word [15:8]								0x00
Profile 0 (0x09)	[7:0]/0x26	Frequency Tuning Word [7:0]								0x00
	[15:8]/0x27	Frequency Tuning Word [15:8]								0x00
	[23:16]/0x28	Frequency Tuning Word [23:16]								0x00
	[31:24]/0x29	Frequency Tuning Word [31:24]								0x00
	[39:32]/0x2A	Phase Offset Word [7:0]								0x00
	[47:40]/0x2B	Open [1:0]		Phase Offset Word [13:8]						0x00
Profile 1 (0x0A)	[7:0]/0x2C	Frequency Tuning Word [7:0]								0x00
	[15:8]/0x2D	Frequency Tuning Word [15:8]								0x00
	[23:16]/0x2E	Frequency Tuning Word [23:16]								0x00
	[31:24]/0x2F	Frequency Tuning Word [31:24]								0x00
	[39:32]/0x30	Phase Offset Word [7:0]								0x00
	[47:40]/0x31	Open [1:0]		Phase Offset Word [13:8]						0x00
Profile 2 (0x0B)	[7:0]/0x32	Frequency Tuning Word [7:0]								0x00
	[15:8]/0x33	Frequency Tuning Word [15:8]								0x00
	[23:16]/0x34	Frequency Tuning Word [23:16]								0x00
	[31:24]/0x35	Frequency Tuning Word [31:24]								0x00
	[39:32]/0x36	Phase Offset Word [7:0]								0x00
	[47:40]/0x37	Open [1:0]		Phase Offset Word [13:8]						0x00
Profile 3 (0x0C)	[7:0]/0x38	Frequency Tuning Word [7:0]								0x00
	[15:8]/0x39	Frequency Tuning Word [15:8]								0x00
	[23:16]/0x3A	Frequency Tuning Word [23:16]								0x00
	[31:24]/0x3B	Frequency Tuning Word [31:24]								0x00
	[39:32]/0x3C	Phase Offset Word [7:0]								0x00
	[47:40]/0x3D	Open [1:0]		Phase Offset Word [13:8]						0x00
Profile 4 (0x0D)	[7:0]/0x3E	Frequency Tuning Word [7:0]								0x00
	[15:8]/0x3F	Frequency Tuning Word [15:8]								0x00
	[23:16]/0x40	Frequency Tuning Word [23:16]								0x00
	[31:24]/0x41	Frequency Tuning Word [31:24]								0x00
	[39:32]/0x42	Phase Offset Word [7:0]								0x00
	[47:40]/0x43	Open [1:0]		Phase Offset Word [13:8]						0x00
Profile 5 (0x0E)	[7:0]/0x44	Frequency Tuning Word [7:0]								0x00
	[15:8]/0x45	Frequency Tuning Word [15:8]								0x00
	[23:16]/0x46	Frequency Tuning Word [23:16]								0x00
	[31:24]/0x47	Frequency Tuning Word [31:24]								0x00
	[39:32]/0x48	Phase Offset Word [7:0]								0x00
	[47:40]/0x49	Open [1:0]		Phase Offset Word [13:8]						0x00
Profile 6 (0x0F)	[7:0]/0x4A	Frequency Tuning Word [7:0]								0x00
	[15:8]/0x4B	Frequency Tuning Word [15:8]								0x00
	[23:16]/0x4C	Frequency Tuning Word [23:16]								0x00
	[31:24]/0x4D	Frequency Tuning Word [31:24]								0x00
	[39:32]/0x4E	Phase Offset Word [7:0]								0x00
	[47:40]/0x4F	Open	Open	Phase Offset Word [13:8]						0x00
Profile 7 (0x10)	[7:0]/0x50	Frequency Tuning Word [7:0]								0x00
	[15:8]/0x51	Frequency Tuning Word [15:8]								0x00
	[23:16]/0x52	Frequency Tuning Word [23:16]								0x00
	[31:24]/0x53	Frequency Tuning Word [31:24]								0x00
	[39:32]/0x54	Phase Offset Word [7:0]								0x00
	[47:40]/0x55	Open	Open	Phase Offset Word [13:8]						0x00

[1] These bits are active immediately following the write sequence of the byte in which they reside in. As a result, they do not require an I/O_UPDATE to enable/disable.

REGISTER BIT DESCRIPTIONS

The serial I/O port registers span an address range of 0 to 16 (0x00 to 0x10 in hexadecimal notation). This represents a total of 17 registers. However, one of these registers (0x05) is unused, yielding a total of 16 available registers.

The registers are not of uniform depth; each contains the number of bytes necessary for its particular function. Additionally, the registers are assigned names according to their functionality. In some cases, a register is given a mnemonic descriptor. For example, the register at Serial Address 0x00 is named Control Function Register 1 and is assigned the mnemonic CFR1.

The following section provides a detailed description of each bit in the AD9913 register map. For cases in which a group of bits serve a specific function, the entire group is considered as a binary word and described in aggregate.

This section is organized in sequential order of the serial addresses of the registers. Each subheading includes the register name and optional register mnemonic (in parentheses). Also given is the serial address in hexadecimal format and the number of bytes assigned to the register.

Following each subheading is a table containing the individual bit descriptions for that particular register. The location of the bit(s) in the register are indicated by a single number or a pair of numbers separated by a colon. A pair of numbers (A:B) indicates a range of bits from the most significant (A) to the least significant (B). For example, 5:2 implies Bit Position 5 down to Bit Position 2, inclusive, with Bit 0 identifying the LSB of the register.

Unless otherwise stated, programmed bits are not transferred to their internal destinations until the assertion of the I/O_UPDATE pin.

Control Function Register 1 (CFR1)

Address 0x00; 4 bytes are assigned to this register.

Table 10. Bit Description for CFR1

Bit(s)	Bit Name	Description
31:29	Open	Leave these bits at their default values.
28	Modulus Enable	This bit is ignored if linear sweep is disabled. 0 = the auxiliary accumulator is used for linear sweep generation. 1 = the auxiliary accumulator is used for programmable modulus.
27	Use Internal Profile	0 = profiles are controlled by profile pins; only valid in serial mode. 1 = profiles are controlled by CFR1 [22:20].
26	Match Pipeline Delays Active	0 = the latency across the auxiliary accumulator, the phase offset word, and phase accumulator are matched. 1 = the latency across the auxiliary accumulator, the phase offset word, and phase accumulator are not matched.
25:24	Open	Leave these bits at the default values.
23	LSB First	0 = MSB first format is used. 1 = LSB first format is used.
22:20	Internal Profile Control	Ineffective unless Bit 27 = 1. Default is 000_2. Refer to the Linear Sweep Mode section for details on how to program these registers during linear sweep, and refer to the Direct Switch Mode section for details on how to program these registers in direct switch mode.
19	Sync Clock Disable	0 = the SYNC_CLK pin is active. 1 = the SYNC_CLK pin assumes a static Logic 0 state (disabled). In this state, the pin drive logic is shut down, minimizing the noise generated by the digital circuitry.
18:17	Open	Leave these bits in their default values.
16	Direct Switch Mode Active	0 = direct switch mode is disabled. 1 = direct switch mode is enabled.
15	Clear Auxiliary Accumulator	0 = normal operation of the auxiliary accumulator (default). 1 = asynchronous, static reset of the auxiliary accumulator. The ramp accumulator remains reset as long as this bit remains set. This bit is synchronized with either an I/O update or a profile change and the next rising edge of SYNC_CLK.
14	Clear Phase Accumulator	0 = normal operation of the DDS phase accumulator (default). 1 = asynchronous, static reset of the DDS phase accumulator.

Bit(s)	Bit Name	Description
13:12	Destination	00 = In direct switch mode, use this setting for FSK. In linear sweep mode, the auxiliary accumulator is used for frequency sweeping. In programmable modulus mode, these bits must be 00. 01 = In direct switch mode, use this setting for PSK. In linear sweep mode, the auxiliary accumulator is used for phase sweeping.
11	Auxiliary Accumulator Enable	0 = auxiliary accumulator is inactive. 1 = auxiliary accumulator is active.
10	DC Output Active	This bit is ignored if linear sweep is disabled (see CFR1 [11]). 0 = normal operating state. 1 = the output of the DAC is driven to full-scale and the DDS output is disabled.
9	Linear Sweep State Trigger Active	0 = edge triggered mode active. 1 = state triggered mode active.
8	Linear Sweep No-Dwell Active	This bit is ignored if linear sweep is disabled (see CFR1[11]). 0 = when a sweep is completed, the device holds at the final state. 1 = when a sweep is completed, the device reverts to the initial state.
7	External Power-Down Mode	0 = the external power-down mode selected is the fast recovery power-down mode. In this mode, when the PWR_DWN_CTL input pin is high, the digital logic and the DAC digital logic are powered down. The DAC bias circuitry, PLL, oscillator, and clock input circuitry are not powered down. 1 = the external power-down mode selected is the full power-down mode. In this mode, when the PWR_DWN_CTL pin is high, all functions are powered down. This includes the DAC and PLL, which take a significant amount of time to power up.
6	Digital Power-Down	0 = the digital core is enabled for operation. 1 = the digital core is disabled and is in a low power dissipation state.
5	DAC Power-Down	0 = the DAC is enabled for operation. 1 = the DAC is disabled and is in its lowest power dissipation state.
4	Clock Input Power-Down	0 = normal operation. 1 = shut down all clock generation including the system clock signal going into the digital section.
3	LOAD SRR @ IO_UPDATE	0 = every time the linear sweep rate register is updated, the ramp rate timer keeps its operation until it times out and then loads the update value into the timer. 1 = the timer is interrupted immediately upon the assertion of IO_UPDATE and the value is loaded.
2	Autoclear Auxiliary Accumulator	0 = normal operation. 1 = the auxiliary accumulator is synchronously cleared (zero is loaded) for one cycle upon receipt of the IO_UPDATE sequence indicator.
1	Autoclear Phase Accumulator	0 = normal operation. 1 = the phase accumulator is synchronously cleared for one cycle upon receipt of the IO_UPDATE sequence indicator.
0	Enable Sine Output	0 = the angle-to-amplitude conversion logic employs a cosine function. 1 = the angle-to-amplitude conversion logic employs a sine function.

Control Function Register 2 (CFR2)

Address 0x01; 2 bytes are assigned to this register.

Table 11. Bit Descriptions for CFR2

Bit(s)	Bit Name	Description
15	PLL Output Div by 2	See Table 7 for details on multiplication factor configuration.
14:9	PLL Multiplication Factor	
8	Open	Leave this bit at the default state.
7	CMOS Clock Mode	See Table 6 for directions on programming this bit.
6	Crystal Clock Mode	See Table 6 for directions on programming this bit.
5	PLL Power-Down	0 = PLL is active 1 = PLL is inactive and in its lowest power state
4	PLL LO Range	0 = use this setting for PLL if the PLL reference frequency is >5 MHz. 1 = use this setting for PLL if the PLL reference frequency is <5 MHz.
3	PLL Input Div by 2	0 = the PLL reference frequency = the REF_CLK input frequency. 1 = the PLL reference frequency = ½ the REF_CLK input frequency.
2	VCO2 Sel	0 = use this setting for VCO frequencies below 100 MHz and/or to optimize for power rather than performance. 1 = use this setting to optimize for performance; this setting results in slightly higher power consumption. Note: When setting this bit, an IO_UPDATE must occur within 40 μs of the PLL power-down bit (CFR2 [5]) going low.
1	PLL Reset	0 = the PLL logic is reset and non-operational until this bit is set. 1 = the PLL logic operates normally.
0	PLL Lock	This read-only bit is set when the REF_CLK PLL is locked.

DAC Control Register

Address 0x02; 4 bytes are assigned to this register.

Table 12. Bit Descriptions for DAC Control Register

Bit(s)	Bit Name	Description
15:14, 10	Open	Leave these bits at their default state.
9:0	FSC	This 10-bit number controls the full-scale output current of the DAC.
31:16,13:11	Reserved	Leave these bits at their default state.

Frequency Tuning Word Register (FTW)

Address 0x03, 4 bytes are assigned to this register.

Table 13. Bit Descriptions for FTW Register

Bit(s)	Bit Name	Description
31:0	Frequency Tuning Word	32-bit frequency tuning word.

Phase Offset Word Register (POW)

Address 0x04, 2 bytes are assigned to this register.

Table 14. Bit Descriptions for POW Register

Bit(s)	Bit Name	Description
15:14	Open	Leave these bits at their default state.
13:0	Phase Offset Word	14-bit phase offset word.

Linear Sweep Parameter Register

Address 0x06, 8 bytes are assigned to this register. This register is only effective if CFR1 [11] or CFR1 [28] are set. See the Auxiliary Accumulator section.

Table 15. Bit Descriptions for Linear Sweep Limit Register

Bit(s)	Bit Name	Description
63:32	Sweep Parameter Word 1	32-bit linear sweep upper limit value. In programmable modulus mode, these bits are used to set the B value found in the AN-953 Application Note.
31:0	Sweep Parameter Word 0	32-bit linear sweep lower limit value. In programmable modulus mode, these bits are used to set the X value found in the AN-953 Application Note.

Linear Sweep Delta Parameter Register

Address 0x07, 8 bytes are assigned to this register. This register is only effective if CFR1 [11] or CFR1 [28] are set. See the Auxiliary Accumulator section.

Table 16. Bit Descriptions for Linear Sweep Step Size Register

Bit(s)	Bit Name	Description
63:32	Falling Delta Word	32-bit linear sweep decrement step size value.
31:0	Rising Delta Word	32-bit linear sweep increment step size value. In programmable modulus mode, these bits are used to set the A value found in the AN-953 Application Note.

Linear Sweep Ramp Rate Register

Address 0x08, 4 bytes are assigned to this register. This register is only effective if CFR1 [11] or CFR1 [28] are set. See the Auxiliary Accumulator section.

Table 17. Bit Descriptions for Linear Sweep Rate Register

Bit(s)	Bit Name	Description
31:16	Falling Sweep Ramp Rate	16-bit linear sweep negative slope value that defines the time interval between decrement values.
15:0	Rising Sweep Ramp Rate	16-bit linear sweep positive slope value that defines the time interval between increment values.

Profile Registers

There are eight consecutive serial I/O addresses dedicated to device profiles. In normal operation, the active profile register is selected using the external profile select pins.

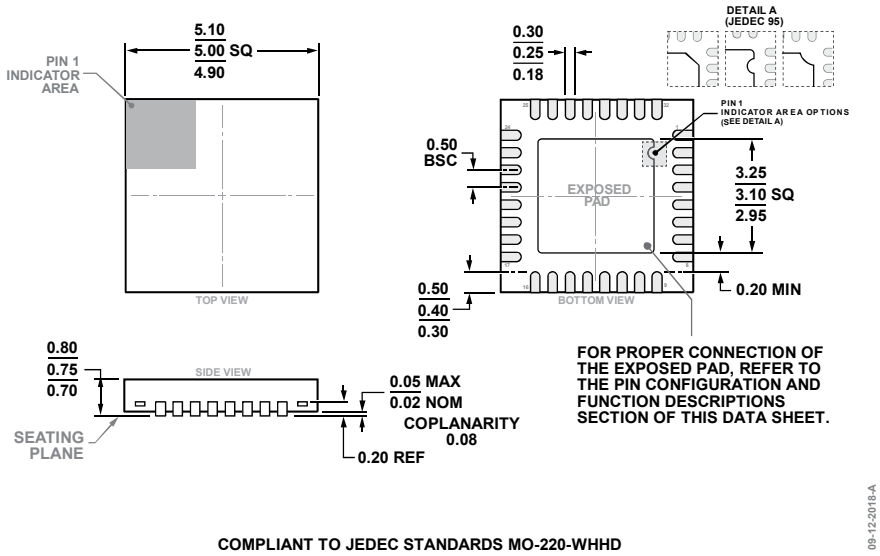
Profile 0 to Profile 7—Single Tone Register

Address 0x09 to Address 0x10, 6 bytes are assigned to these registers.

Table 18. Bit Descriptions for Profile 0 to Profile 7 Single Tone Register

Bit(s)	Bit Name	Description
47:46	Open	Leave these bits at their default state.
45:32	Phase Offset Word	This 14-bit number controls the DDS phase offset.
31:0	Frequency Tuning Word	This 32-bit number controls the DDS frequency.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-WHHD

Figure 36. 32-Lead Lead Frame Chip Scale Package [LFCSP]
5 mm × 5 mm Body and 0.75 mm Package Height
(CP-32-7)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD9913BCPZ	–40°C to +85°C	32-Lead Lead Frame Chip Scale Package [LFCSP]	CP-32-7
AD9913BCPZ-REEL7	–40°C to +85°C	32-Lead Lead Frame Chip Scale Package [LFCSP]	CP-32-7
AD9913/PCBZ		Evaluation Board	

[1] Z = RoHS Compliant Part.