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SPECIFICATIONS

T_A = 25°C, V_S = 5 V, R_L = 2 kΩ to 2.5 V, unless otherwise noted.

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Small Signal Bandwidth	G = +1, V_O = 0.2 V p-p	70	110		MHz
	G = −1, +2, V_O = 0.2 V p-p		50		MHz
Bandwidth for 0.1 dB Flatness	G = +2, V_O = 0.2 V p-p, R_L = 150 Ω to 2.5 V, R_F = 806 Ω		20		MHz
Slew Rate	G = −1, V_O = 2 V step	100	145		V/µs
Full Power Response	G = +1, V_O = 2 V p-p		35		MHz
Settling Time to 0.1%	G = −1, V_O = 2 V step		50		ns
NOISE/DISTORTION PERFORMANCE					
Total Harmonic Distortion (See Figure 11)	f_C = 5 MHz, V_O = 2 V p-p, G = +2		−67		dB
Input Voltage Noise	f = 10 kHz		16		nV/√Hz
Input Current Noise	f = 10 kHz		850		fA/√Hz
Differential Gain Error (NTSC)	G = +2, R_L = 150 Ω to 2.5 V		0.09		%
	R_L = 1 kΩ to 2.5 V		0.03		%
Differential Phase Error (NTSC)	G = +2, R_L = 150 Ω to 2.5 V		0.19		Degrees
	R_L = 1 kΩ to 2.5 V		0.03		Degrees
Crosstalk	f = 5 MHz, G = +2		−60		dB
DC PERFORMANCE					
Input Offset Voltage			1.7	10	mV
	T_{MIN} to T_{MAX}			25	mV
Offset Drift			10		µV/°C
Input Bias Current			1.4	2.5	µA
	T_{MIN} to T_{MAX}			3.25	µA
Input Offset Current			0.1	0.75	µA
Open-Loop Gain	R_L = 2 kΩ to 2.5 V	86	98		dB
	T_{MIN} to T_{MAX}		96		dB
	R_L = 150 Ω to 2.5 V	76	82		dB
	T_{MIN} to T_{MAX}		78		dB
INPUT CHARACTERISTICS					
Input Resistance			290		kΩ
Input Capacitance			1.4		pF
Input Common-Mode Voltage Range			−0.2 to +4		V
Common-Mode Rejection Ratio	V_{CM} = 0 V to 3.5 V	72	88		dB
OUTPUT CHARACTERISTICS					
Output Voltage Swing	R_L = 10 kΩ to 2.5 V		0.015 to 4.985		V
	R_L = 2 kΩ to 2.5 V	0.100 to 4.900	0.025 to 4.975		V
	R_L = 150 Ω to 2.5 V	0.300 to 4.625	0.200 to 4.800		V
Output Current	V_{OUT} = 0.5 V to 4.5 V		45		mA
	T_{MIN} to T_{MAX}		45		mA
Short-Circuit Current	Sourcing		80		mA
	Sinking		130		mA
Capacitive Load Drive	G = +1		50		pF
POWER SUPPLY					
Operating Range		3		12	V
Quiescent Current/Amplifier			4.4	5	mA
Power Supply Rejection Ratio	ΔV_S = ±1 V	70	80		dB
OPERATING TEMPERATURE RANGE		−40		+85	°C

T_A = 25°C, V_S = +3 V, R_L = 2 kΩ to +1.5 V, unless otherwise noted.

Table 2.

Parameter	Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Small Signal Bandwidth	G = +1, V_O = 0.2 V p-p	70	110		MHz
	G = −1, +2, V_O = 0.2 V p-p		50		MHz
Bandwidth for 0.1 dB Flatness	G = +2, V_O = 0.2 V p-p, R_L = 150 Ω to 2.5 V, R_F = 402 Ω		17		MHz
Slew Rate	G = −1, V_O = 2 V step	90	135		V/µs
Full Power Response	G = +1, V_O = 1 V p-p		65		MHz
Settling Time to 0.1%	G = −1, V_O = 2 V step		55		ns
NOISE/DISTORTION PERFORMANCE					
Total Harmonic Distortion (see Figure 11)	f_C = 5 MHz, V_O = 2 V p-p, G = −1, R_L = 100 Ω to 1.5 V		−47		dB
Input Voltage Noise	f = 10 kHz		16		nV/√Hz
Input Current Noise	f = 10 kHz		600		fA/√Hz
Differential Gain Error (NTSC)	G = +2, V_{CM} = 1 V				
	R_L = 150 Ω to 1.5 V		0.11		%
	R_L = 1 kΩ to 1.5 V		0.09		%
Differential Phase Error (NTSC)	G = +2, V_{CM} = 1 V				
	R_L = 150 Ω to 1.5 V		0.24		Degrees
	R_L = 1 kΩ to 1.5 V		0.10		Degrees
Crosstalk	f = 5 MHz, G = +2		−60		dB
DC PERFORMANCE					
Input Offset Voltage			1.6	10	mV
	T_{MIN} to T_{MAX}			25	mV
Offset Drift			10		µV/°C
Input Bias Current			1.3	2.6	µA
	T_{MIN} to T_{MAX}			3.25	µA
Input Offset Current			0.15	0.8	µA
Open-Loop Gain	R_L = 2 kΩ	80	96		dB
	T_{MIN} to T_{MAX}		94		dB
	R_L = 150 Ω	74	82		dB
	T_{MIN} to T_{MAX}		76		dB
INPUT CHARACTERISTICS					
Input Resistance			290		kΩ
Input Capacitance			1.4		pF
Input Common-Mode Voltage Range			−0.2 to +2.0		V
Common-Mode Rejection Ratio	V_{CM} = 0 V to 1.5 V	72	88		dB
OUTPUT CHARACTERISTICS					
Output Voltage Swing	R_L = 10 kΩ to 1.5 V		0.01 to 2.99		V
	R_L = 2 kΩ to 1.5 V	0.075 to 2.9	0.02 to 2.98		V
	R_L = 150 Ω to 1.5 V	0.20 to 2.75	0.125 to 2.875		V
Output Current	V_{OUT} = 0.5 V to 2.5 V		45		mA
	T_{MIN} to T_{MAX}		45		mA
Short Circuit Current	Sourcing		60		mA
	Sinking		90		mA
Capacitive Load Drive	G = +1		45		pF
POWER SUPPLY					
Operating Range		3		12	V
Quiescent Current/Amplifier			4.2	4.8	mA
Power Supply Rejection Ratio	ΔV_S = +0.5 V	68	80		dB
OPERATING TEMPERATURE RANGE		−40		+85	°C

T_A = 25°C, V_S = ±5 V, R_L = 2 kΩ to ground, unless otherwise noted.

Table 3.

Parameter	Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Small Signal Bandwidth	G = +1, V_O = 0.2 V p-p	70	110		MHz
	G = −1, +2, V_O = 0.2 V p-p		50		MHz
Bandwidth for 0.1 dB Flatness	G = +2, V_O = 0.2 V p-p, R_L = 150 Ω, R_F = 1.1 kΩ		20		MHz
Slew Rate	G = −1, V_O = 2 V step	105	170		V/µs
Full Power Response	G = +1, V_O = 2 V p-p		40		MHz
Settling Time to 0.1%	G = −1, V_O = 2 V step		50		ns
NOISE/DISTORTION PERFORMANCE					
Total Harmonic Distortion (see Figure 11)	f_C = 5 MHz, V_O = 2 V p-p, G = +2		−71		dB
Input Voltage Noise	f = 10 kHz		16		nV/√Hz
Input Current Noise	f = 10 kHz		900		fA/√Hz
Differential Gain Error (NTSC)	G = +2, R_L = 150 Ω		0.02		%
	R_L = 1 kΩ		0.02		%
Differential Phase Error (NTSC)	G = +2, R_L = 150 Ω		0.11		Degrees
	R_L = 1 kΩ		0.02		Degrees
Crosstalk	f = 5 MHz, G = +2		−60		dB
DC PERFORMANCE					
Input Offset Voltage			1.8	11	mV
	T_{MIN} to T_{MAX}			27	mV
Offset Drift			10		µV/°C
Input Bias Current			1.4	2.6	µA
	T_{MIN} to T_{MAX}			3.5	µA
Input Offset Current			0.1	0.75	µA
Open-Loop Gain	R_L = 2 kΩ	88	96		dB
	T_{MIN} to T_{MAX}		96		dB
	R_L = 150 Ω	78	82		dB
	T_{MIN} to T_{MAX}		80		dB
INPUT CHARACTERISTICS					
Input Resistance			290		kΩ
Input Capacitance			1.4		pF
Input Common-Mode Voltage Range			−5.2 to +4.0		V
Common-Mode Rejection Ratio	V_{CM} = −5 V to +3.5 V	72	88		dB
OUTPUT CHARACTERISTICS					
Output Voltage Swing	R_L = 10 kΩ		−4.98 to +4.98		V
	R_L = 2 kΩ	−4.85 to +4.85	−4.97 to +4.97		V
	R_L = 150 Ω	−4.45 to +4.30	−4.60 to +4.60		V
Output Current	V_{OUT} = −4.5 V to +4.5 V		45		mA
	T_{MIN} to T_{MAX}		45		mA
Short Circuit Current	Sourcing		100		mA
	Sinking		160		mA
Capacitive Load Drive	G = +1 (AD8091/AD8092)		50		pF
POWER SUPPLY					
Operating Range		3		12	V
Quiescent Current/Amplifier			4.8	5.5	mA
Power Supply Rejection Ratio	ΔV_S = ±1 V	68	80		dB
OPERATING TEMPERATURE RANGE		−40		+85	°C

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
Supply Voltage	12.6 V
Power Dissipation	See Figure 4
Common-Mode Input Voltage	$\pm V_S$
Differential Input Voltage	±2.5 V
Output Short-Circuit Duration	See Figure 4
Storage Temperature Range	−65°C to +125°C
Operating Temperature Range	−40°C to +85°C
Lead Temperature (Soldering 10 sec)	300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

MAXIMUM POWER DISSIPATION

The maximum safe power dissipation in the AD8091/AD8092 package is limited by the associated rise in junction temperature (T_J) on the die. The plastic encapsulating the die locally reaches the junction temperature. At approximately 150°C, which is the glass transition temperature, the plastic changes its properties. Even temporarily exceeding this temperature limit may change the stresses that the package exerts on the die, permanently shifting the parametric performance of the AD8091/AD8092. Exceeding a junction temperature of 175°C for an extended period of time can result in changes in the silicon devices, potentially causing failure.

The still-air thermal properties of the package (θ_{JA}), the ambient temperature (T_A), and the total power dissipated in the package (P_D) can be used to determine the junction temperature of the die.

The junction temperature can be calculated as

$$T_J = T_A + (P_D \times \theta_{JA})$$

The power dissipated in the package (P_D) is the sum of the quiescent power dissipation and the power dissipated in the package due to the load drive for all outputs. The quiescent power is the voltage between the supply pins (V_S) times the quiescent current (I_S). Assuming that the load (R_L) is referenced to midsupply, then the total drive power is $V_S/2 \times I_{OUT}$, some of which is dissipated in the package and some in the load ($V_{OUT} \times I_{OUT}$). The difference between the total drive power and the load power is the drive power dissipated in the package.

$$P_D = quiescent\ power + (total\ drive\ power - load\ power)$$

$$P_D = (V_S \times I_S) + \left(\left(\frac{V_S}{2} \times \frac{V_{OUT}}{R_L}\right) - \left(\frac{{V_{OUT}}^2}{R_L}\right)\right)$$

RMS output voltages should be considered. If R_L is referenced to $-V_S$, as in single-supply operation, then the total drive power is $V_S \times I_{OUT}$.

If the rms signal levels are indeterminate, then consider the worst case when $V_{OUT} = V_S/4$ for R_L to midsupply

$$P_D = (V_S \times I_S) + \frac{\left(\frac{V_S}{4}\right)^2}{R_L}$$

In single-supply operation with R_L referenced to $-V_S$, the worst case is $V_{OUT} = V_S/2$.

Airflow increases heat dissipation, effectively reducing θ_{JA}. Also, more metal directly in contact with the package leads from metal traces, through holes, ground, and power planes reduces the θ_{JA}. Care must be taken to minimize parasitic capacitances at the input leads of high speed op amps as discussed in the Input Capacitance section.

Figure 4 shows the maximum safe power dissipation in the package vs. the ambient temperature for the SOIC-8 (125°C/W), SOT23-5 (180°C/W), and MSOP-8 (150°C/W) on a JEDEC standard four-layer board.

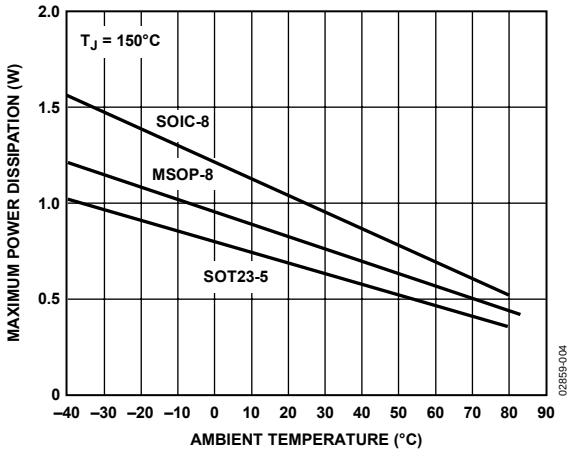


Figure 4. Maximum Power Dissipation vs. Temperature for a Four-Layer Board

TYPICAL PERFORMANCE CHARACTERISTICS

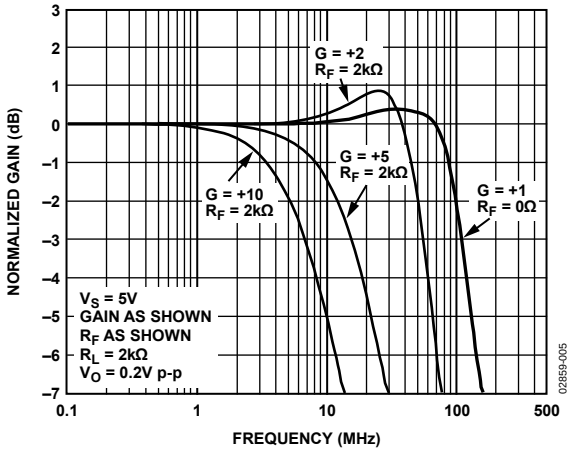


Figure 5. Normalized Gain vs. Frequency; V_S = +5 V

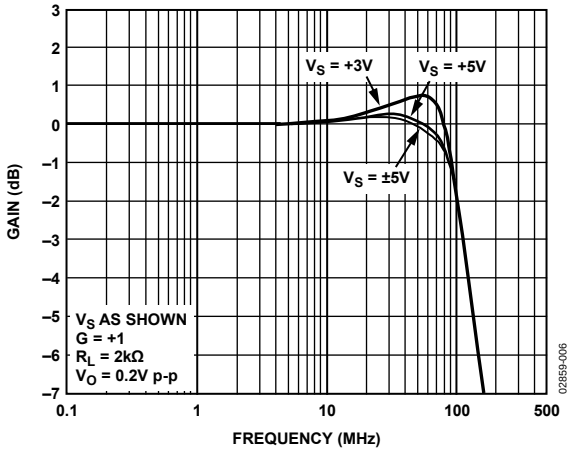


Figure 6. Gain vs. Frequency vs. Supply

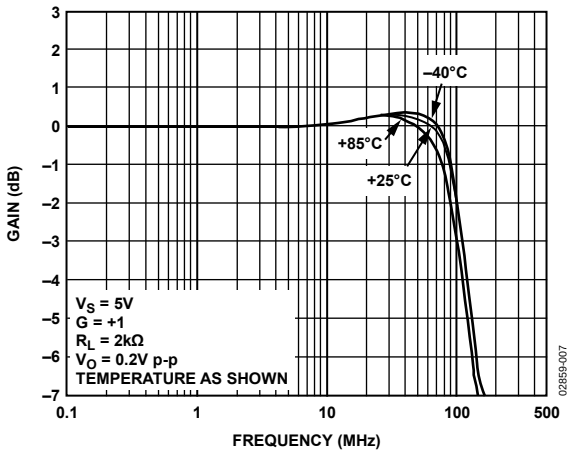


Figure 7. Gain vs. Frequency vs. Temperature

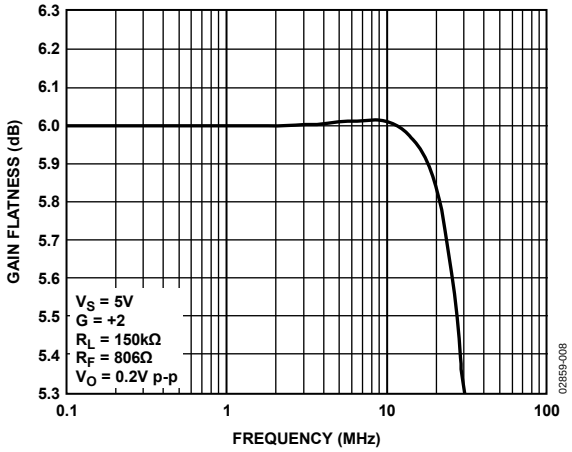


Figure 8. 0.1 dB Gain Flatness vs. Frequency; G = +2

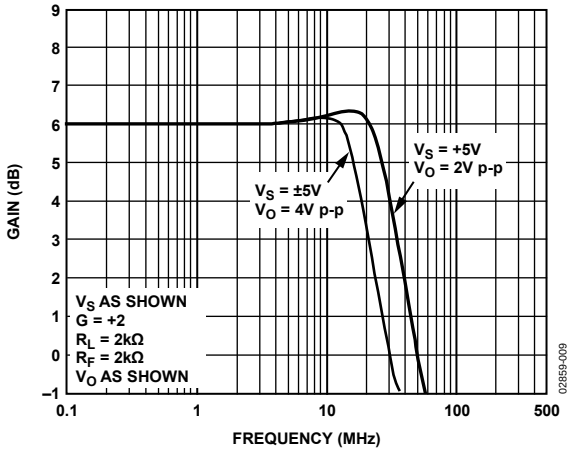


Figure 9. Large Signal Frequency Response; G = +2

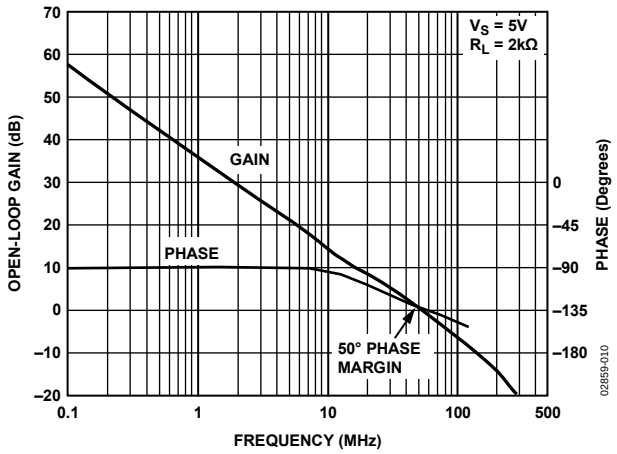


Figure 10. Open-Loop Gain and Phase vs. Frequency

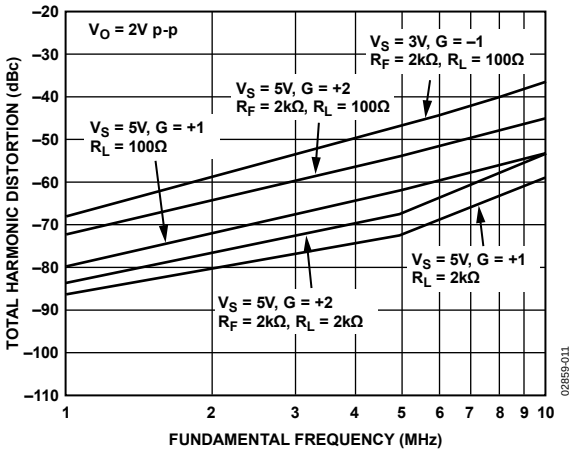


Figure 11. Total Harmonic Distortion

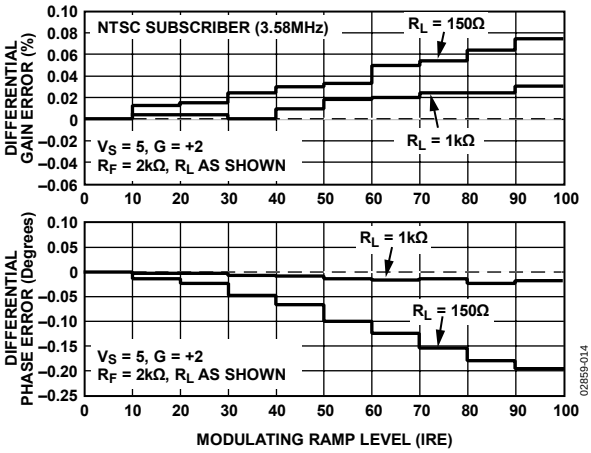


Figure 14. Differential Gain and Phase Errors

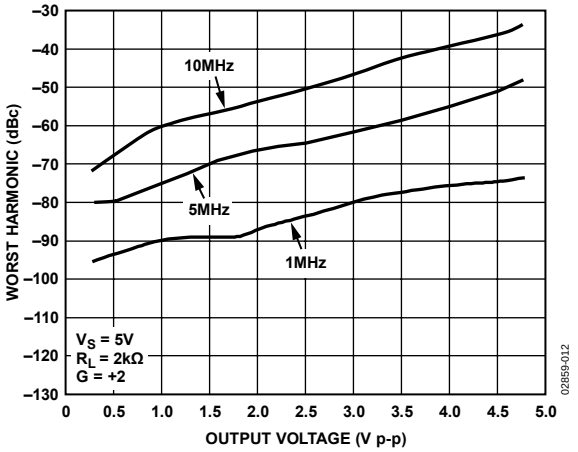


Figure 12. Worst Harmonic vs. Output Voltage

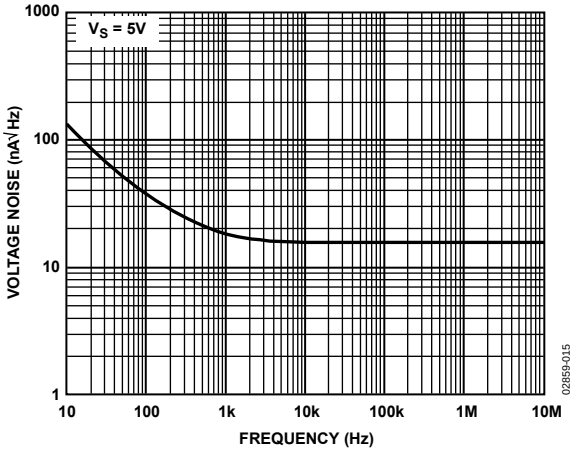


Figure 15. Input Voltage Noise vs. Frequency

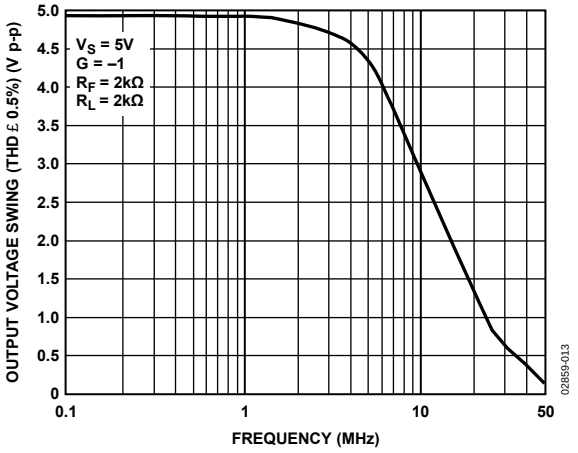


Figure 13. Low Distortion Rail-to-Rail Output Swing

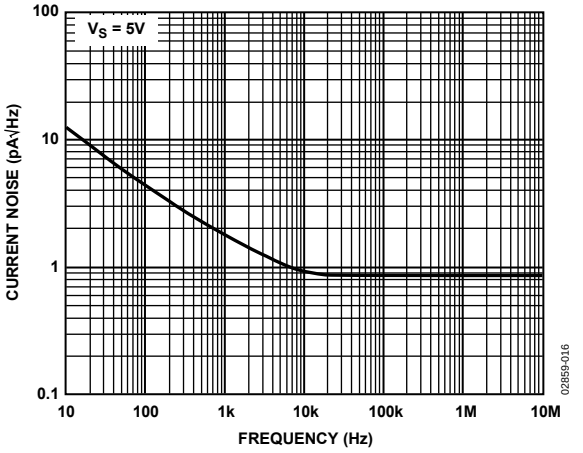


Figure 16. Input Current Noise vs. Frequency

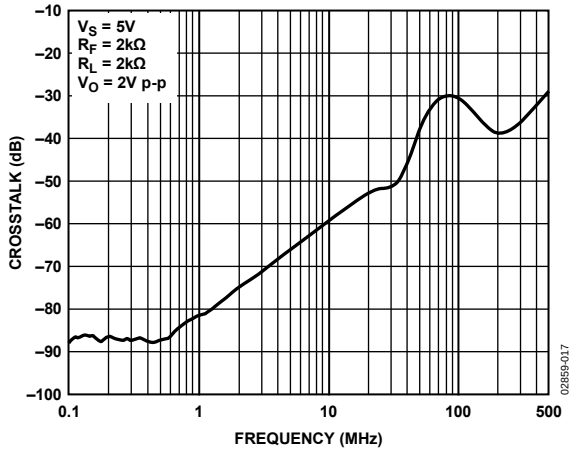


Figure 17. AD8092 Crosstalk (Output-to-Output) vs. Frequency

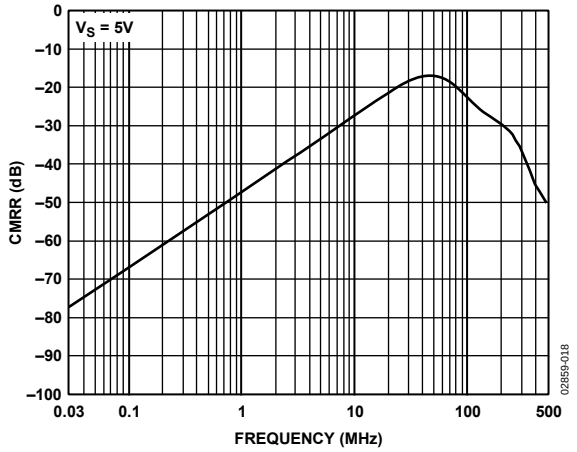


Figure 18. CMRR vs. Frequency

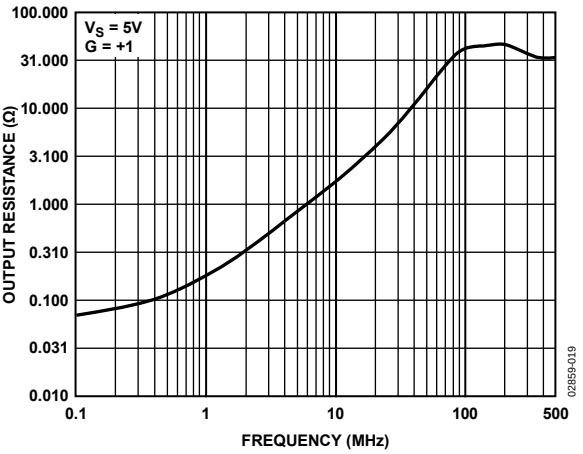


Figure 19. Closed-Loop Output Resistance vs. Frequency

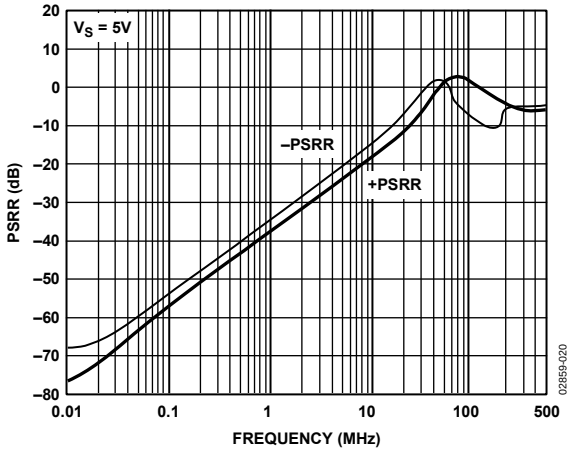


Figure 20. PSRR vs. Frequency

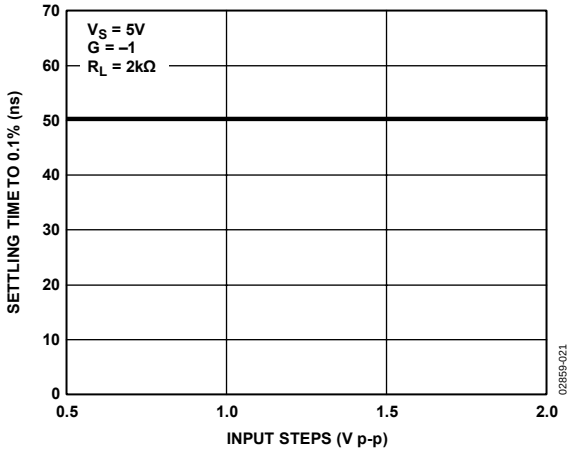


Figure 21. Settling Time vs. Input Step

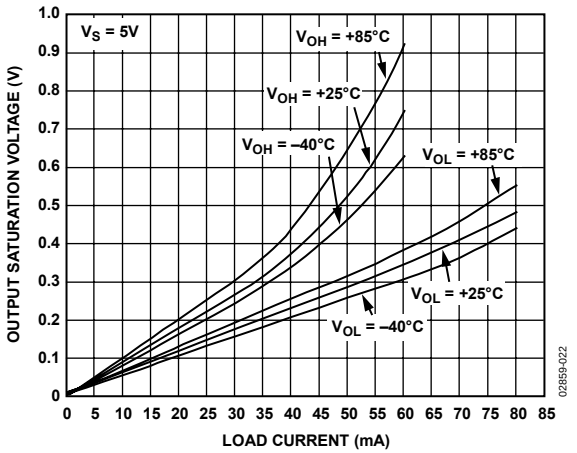


Figure 22. Output Saturation Voltage vs. Load Current

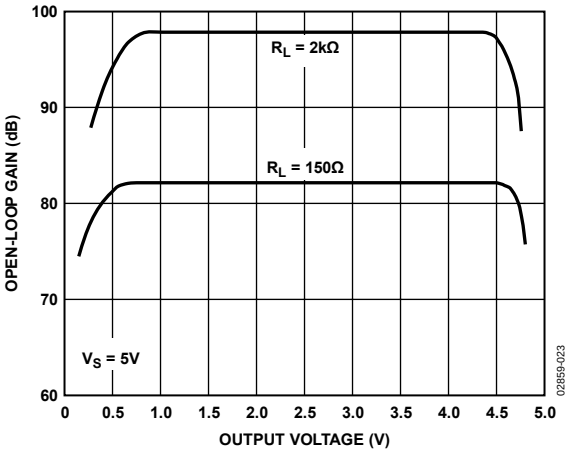


Figure 23. Open-Loop Gain vs. Output Voltage

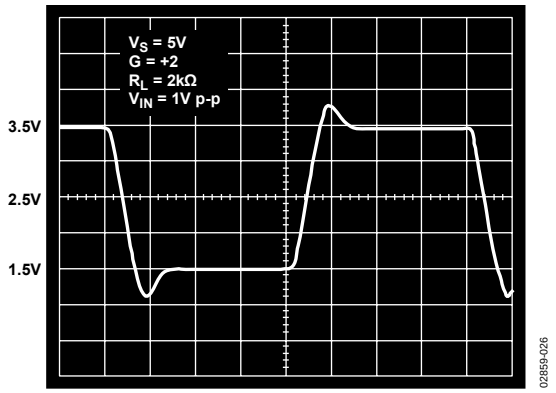


Figure 26. Large Signal Step Response; V_S = +5 V, G = +2

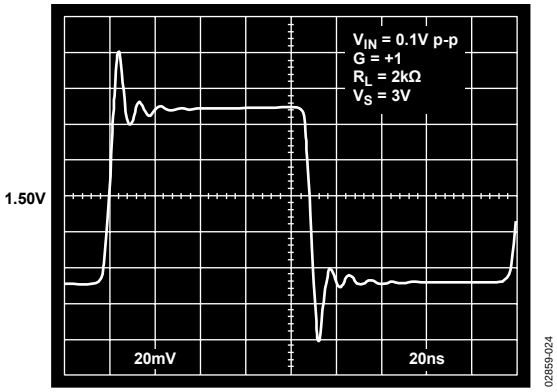


Figure 24. 100 mV Step Response; G = +1

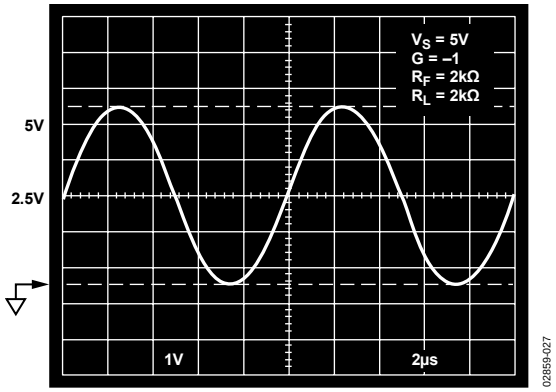


Figure 27. Output Swing; G = –1, R_L = 2 kΩ

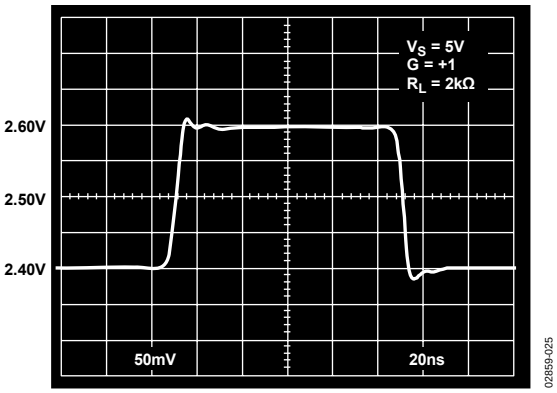


Figure 25. 200 mV Step Response; V_S = +5 V, G = +1

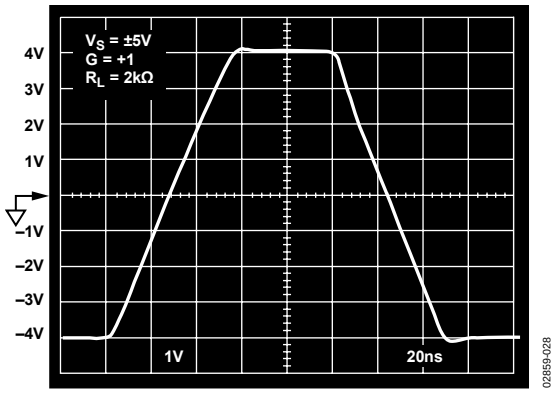


Figure 28. Large Signal Step Response; V_S = ±5 V, G = +1

LAYOUT, GROUNDING, AND BYPASSING CONSIDERATIONS

POWER SUPPLY BYPASSING

Power supply pins are actually inputs, and care must be taken so that a noise-free stable dc voltage is applied. The purpose of bypass capacitors is to create low impedances from the supply to ground at all frequencies, thereby shunting or filtering a majority of the noise.

Decoupling schemes are designed to minimize the bypassing impedance at all frequencies with a parallel combination of capacitors. Chip capacitors of 0.01 µF or 0.001 µF (X7R or NPO) are critical and should be as close as possible to the amplifier package. Larger chip capacitors, such as the 0.1 µF capacitor, can be shared among a few closely spaced active components in the same signal path. A 10 µF tantalum capacitor is less critical for high frequency bypassing and, in most cases, only one per board is needed at the supply inputs.

GROUNDING

A ground plane layer is important in densely packed PC boards to spread the current-minimizing parasitic inductances. However, an understanding of where the current flows in a circuit is critical to implementing effective high speed circuit design. The length of the current path is directly proportional to the magnitude of parasitic inductances and thus the high frequency impedance of the path. High speed currents in an inductive ground return create an unwanted voltage noise.

The lengths of the high frequency bypass capacitor leads are most critical. A parasitic inductance in the bypass grounding works against the low impedance created by the bypass capacitor. Place the ground leads of the bypass capacitors at the same physical location. Because load currents flow from the supplies as well, the ground for the load impedance should be at the same physical location as the bypass capacitor grounds. For the larger value capacitors, which are intended to be effective at lower frequencies, the current return path distance is less critical.

INPUT CAPACITANCE

Along with bypassing and ground, high speed amplifiers can be sensitive to parasitic capacitance between the inputs and ground. A few pF of capacitance reduces the input impedance at high frequencies, in turn increasing the amplifier's gain and causing peaking of the frequency response or even oscillations, if severe enough. It is recommended that the external passive components, which are connected to the input pins, be placed as close as possible to the inputs to avoid parasitic capacitance. The ground and power planes must be kept at a distance of at least 0.05 mm from the input pins on all layers of the board.

INPUT-TO-OUTPUT COUPLING

The input and output signal traces should not be parallel to minimize capacitive coupling between the inputs and output and to avoid any positive feedback.

DRIVING CAPACITIVE LOADS

A highly capacitive load reacts with the output of the amplifiers, causing a loss in phase margin and subsequent peaking or even oscillation, as shown in Figure 29 and Figure 30. There are two methods to effectively minimize its effect.

- Put a small value resistor in series with the output to isolate the load capacitor from the amplifier's output stage.
- Increase the phase margin with higher noise gains or by adding a pole with a parallel resistor and capacitor from –IN to the output.

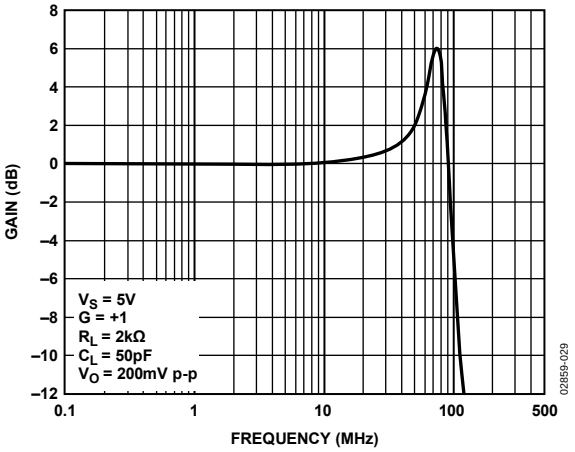


Figure 29. Closed-Loop Frequency Response: C_L = 50 pF

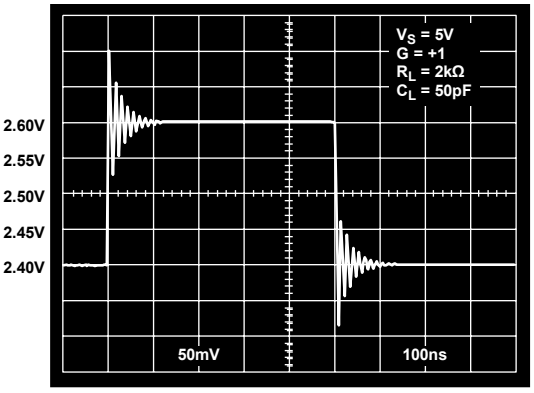


Figure 30. 200 mV Step Response: C_L = 50 pF

As the closed-loop gain is increased, the larger phase margin allows for large capacitor loads with less peaking. Adding a low value resistor in series with the load at lower gains has the same effect. Figure 31 shows the effect of a series resistor for various voltage gains. For large capacitive loads, the frequency response of the amplifier is dominated by the series resistor and capacitive load.

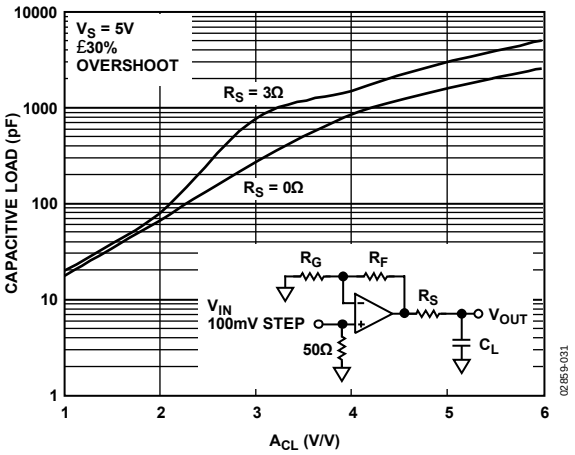


Figure 31. Capacitive Load Drive vs. Closed-Loop Gain

OVERDRIVE RECOVERY

Overdrive of an amplifier occurs when the output range and/or input range is exceeded. The amplifier must recover from this overdrive condition. The AD8091/AD8092 recover within 60 ns from negative overdrive and within 45 ns from positive overdrive, as shown in Figure 32.

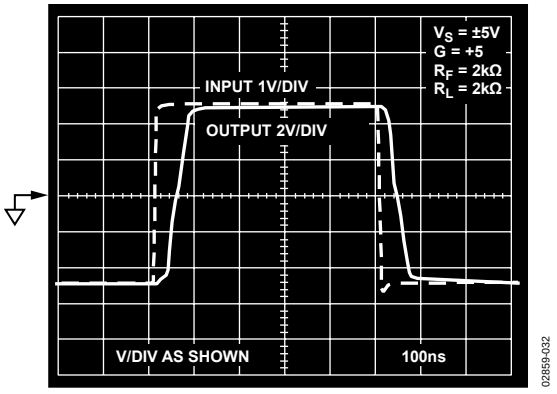


Figure 32. Overdrive Recovery

ACTIVE FILTERS

Active filters at higher frequencies require wider bandwidth op amps to work effectively. Excessive phase shift produced by lower frequency op amps can significantly impact active filter performance.

Figure 33 shows an example of a 2 MHz biquad bandwidth filter that uses three op amps. Such circuits are sometimes used in medical ultrasound systems to lower the noise bandwidth of the analog signal before A/D conversion. Note that the unused amplifiers' inputs should be tied to ground.

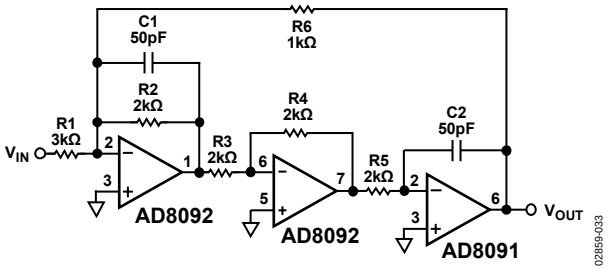


Figure 33. 2 MHz Biquad Band-Pass Filter

The frequency response of the circuit is shown in Figure 34.

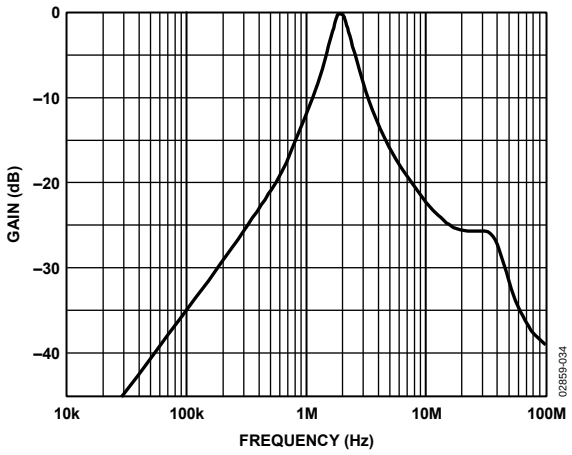


Figure 34. Frequency Response of 2 MHz Band-Pass Biquad Filter

SYNC STRIPPER

Synchronizing pulses are sometimes carried on video signals so as not to require a separate channel to carry the synchronizing information. However, for some functions, such as A/D conversion, it is not desirable to have the sync pulses on the video signal. These pulses reduce the dynamic range of the video signal and do not provide any useful information for such a function.

A sync stripper removes the synchronizing pulses from a video signal while passing all the useful video information. Figure 35 shows a practical single-supply circuit that uses only a single AD8091. It is capable of directly driving a reverse terminated video line.

The video signal plus sync is applied to the noninverting input with the proper termination. The amplifier gain is set equal to 2 via the two 1 kΩ resistors in the feedback circuit. A bias voltage must be applied to R1 for the input signal to have the sync pulses stripped at the proper level.

The blanking level of the input video pulse is the desired place to remove the sync information. The amplifier multiplies this level by 2. This level must be at ground at the output in order for the sync stripping action to take place. Because the gain of the amplifier from the input of R1 to the output is −1, a voltage equal to 2 × V_{BLANK} must be applied to make the blanking level come out at ground.

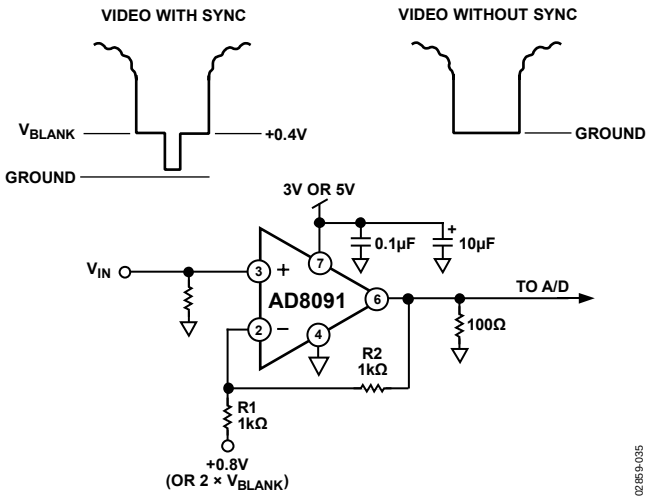


Figure 35. Sync Stripper

SINGLE-SUPPLY COMPOSITE VIDEO LINE DRIVER

Many composite video signals have their blanking level at ground and have video information that is both positive and negative. Such signals require dual-supply amplifiers to pass them. However, by ac level-shifting, a single-supply amplifier can be used to pass these signals. The following complications may arise from such techniques.

Signals of bounded peak-to-peak amplitude that vary in duty cycle require larger dynamic swing capacity than their (bounded) peak-to-peak amplitude after they are ac-coupled. As a worst case, the dynamic signal swing approaches twice the peak-to-peak value. One of two conditions that define the maximum dynamic swing requirements is a signal that is mostly low but goes high with a duty cycle that is a small fraction of a percent. The opposite condition defines the second condition.

The worst case of composite video is not quite this demanding. One bounding condition is a signal that is mostly black for an entire frame but has a white (full amplitude) minimum width spike at least once in a frame.

The other extreme is a full white video signal. The blanking intervals and sync tips of such a signal have negative-going excursions in compliance with the composite video specifications. The combination of horizontal and vertical blanking intervals limit such a signal to being at the highest (white) level for a maximum of about 75% of the time.

As a result of the duty cycles between the two extremes, a 1 V p-p composite video signal that is multiplied by a gain of 2 requires about 3.2 V p-p of dynamic voltage swing at the output for an op amp to pass a composite video signal of arbitrary varying duty cycle without distortion.

Some circuits use a sync tip clamp to hold the sync tips at a relatively constant level to lower the amount of dynamic signal swing required. However, these circuits can have artifacts like sync tip compression unless they are driven by a source with a very low output impedance. The AD8091/AD8092 have adequate signal swing when running on a single 5 V supply to handle an ac-coupled composite video signal.

The input to the circuit shown in Figure 36 is a standard composite (1 V p-p) video signal that has the blanking level at ground. The input network level shifts the video signal by means of ac coupling. The noninverting input of the op amp is biased to half of the supply voltage.

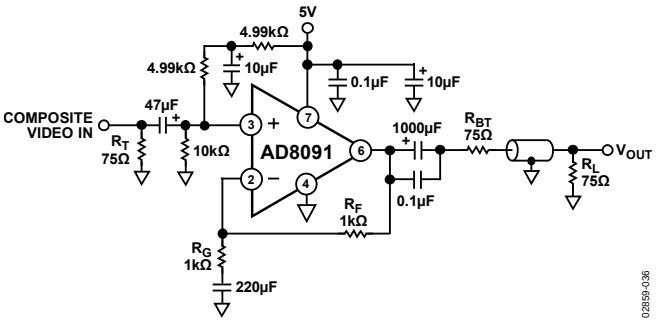
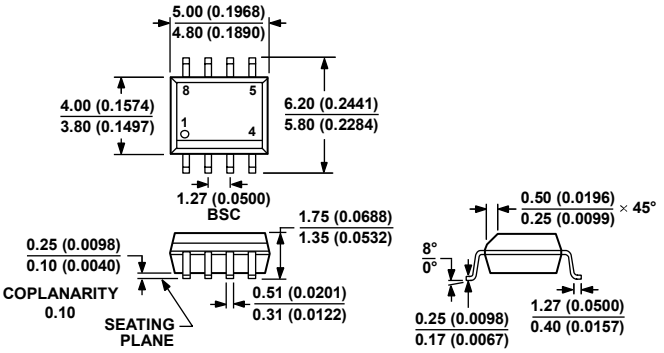


Figure 36. Single-Supply Composite Video Line Driver

The feedback circuit provides unity gain for the dc biasing of the input and provides a gain of 2 for any signals that are in the video bandwidth. The output is ac-coupled and terminated to drive the line.

The capacitor values provide minimum tilt or field time distortion of the video signal. These values are required for video that is considered to be studio or broadcast quality. However, if a lower consumer grade of video, sometimes referred to as consumer video, is all that is desired, the values and the cost of the capacitors can be reduced by as much as a factor of 5 with minimum visible degradation in the picture.

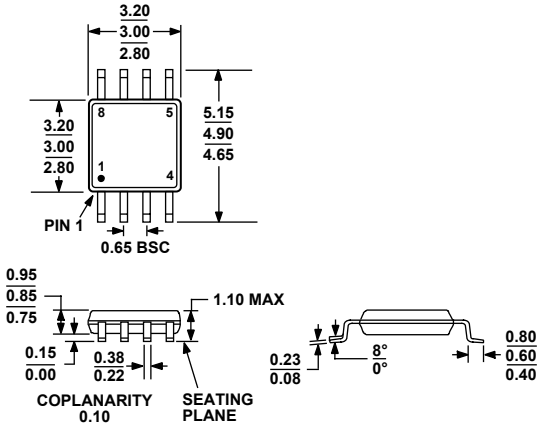
OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-012-AA

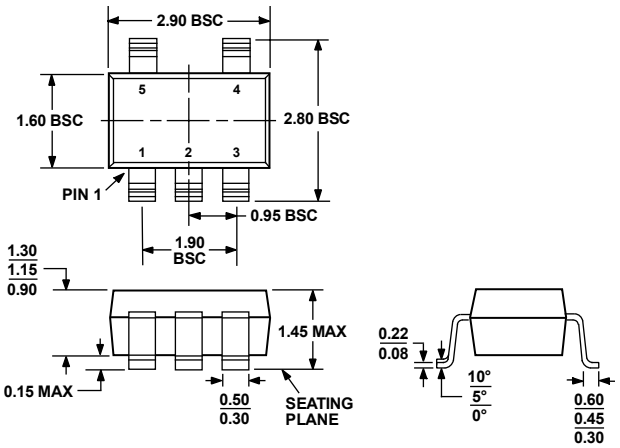
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 37. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body (R-8)
Dimensions shown in millimeters and (inches)



COMPLIANT TO JEDEC STANDARDS MO-187-AA

Figure 38. 8-Lead Mini Small Outline Package [MSOP]
(RM-8)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-178-AA

Figure 39. 5-Lead Small Outline Transistor Package [SOT-23]
(RJ-5)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Branding
AD8091AR	−40°C to +85°C	8-Lead SOIC	R-8	
AD8091AR-REEL	−40°C to +85°C	8-Lead SOIC, 13″ Tape and Reel	R-8	
AD8091AR-REEL7	−40°C to +85°C	8-Lead SOIC, 7″ Tape and Reel	R-8	
AD8091ARZ[1]	−40°C to +85°C	8-Lead SOIC	R-8	
AD8091ARZ-REEL[1]	−40°C to +85°C	8-Lead SOIC, 13″ Tape and Reel	R-8	
AD8091ARZ-REEL7[1]	−40°C to +85°C	8-Lead SOIC, 7″ Tape and Reel	R-8	
AD8091ART-R2	−40°C to +85°C	5-Lead SOT-23	RJ-5	HVA
AD8091ART-REEL	−40°C to +85°C	5-Lead SOT-23, 13″ Tape and Reel	RJ-5	HVA
AD8091ART-REEL7	−40°C to +85°C	5-Lead SOT-23, 7″ Tape and Reel	RJ-5	HVA
AD8091ARTZ-R2[1]	−40°C to +85°C	5-Lead SOT-23	RJ-5	HVA#
AD8091ARTZ-R7[1]	−40°C to +85°C	5-Lead SOT-23, 7″ Tape and Reel	RJ-5	HVA#
AD8091ARTZ-RL[1]	−40°C to +85°C	5-Lead SOT-23, 13″ Tape and Reel	RJ-5	HVA#
AD8092AR	−40°C to +85°C	8-Lead SOIC	R-8	
AD8092AR-REEL	−40°C to +85°C	8-Lead SOIC, 13″ Tape and Reel	R-8	
AD8092AR-REEL7	−40°C to +85°C	8-Lead SOIC, 7″ Tape and Reel	R-8	
AD8092ARZ[1]	−40°C to +85°C	8-Lead SOIC	R-8	
AD8092ARZ-REEL[1]	−40°C to +85°C	8-Lead SOIC, 13″ Tape and Reel	R-8	
AD8092ARZ-REEL7[1]	−40°C to +85°C	8-Lead SOIC, 7″ Tape and Reel	R-8	
AD8092ARM	−40°C to +85°C	8-Lead MSOP	RM-8	HWA
AD8092ARM-REEL	−40°C to +85°C	8-Lead MSOP, 13" Tape and Reel	RM-8	HWA
AD8092ARM-REEL7	−40°C to +85°C	8-Lead MSOP, 7" Tape and Reel	RM-8	HWA
AD8092ARMZ[1]	−40°C to +85°C	8-Lead MSOP	RM-8	HWA#
AD8092ARMZ-REEL[1]	−40°C to +85°C	8-Lead MSOP, 13" Tape and Reel	RM-8	HWA#
AD8092ARMZ-REEL7[1]	−40°C to +85°C	8-Lead MSOP, 7" Tape and Reel	RM-8	HWA#

[1] Z = RoHS Compliant Part. # denotes lead-free, may be top or bottom marked.

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