TABLE OF CONTENTS

REVISION HISTORY

8/2020—Rev. G to Rev. H

Changes to Features Section, Applications Section, Figure 1, and Table 1 ... 1
Change to Endnote 3, Table 2 ... 4
Changes to Timing Specifications Section and Table 4 ... 6
Deleted Table 5 and Figure 3; Renumbered Sequentially ... 6
Changes to Table 5 ... 8
Added Thermal Resistance Section and Table 6; Renumbered Sequentially ... 8
Changes to Figure 30 ... 16
Changes to Table 9 ... 17
Changes to Voltage Reference Input Section and Power Supply Section ... 18
Added Table 5: Renumbered Sequentially ... 6
Changes to Figure 29 ... 14
Changes to Table 9 ... 16
Changes to Voltage Reference Input Section ... 17
Changes to Figure 35 ... 18
Changes to Figure 37 ... 20
Changes to Ordering Guide ... 23

10/2017—Rev. F to Rev. G

Changes to Features Section and Table 1 ... 1
Moved Typical Application Circuit Section and Figure 1 ... 3
Changes to Figure 5 ... 9
Updated Outline Dimensions ... 23
Changes to Ordering Guide ... 24

8/2014—Rev. D to Rev. E

Deleted QFN ... Throughout
Changed Typical Application Diagram Section to Typical Application Circuit Section ... 1
Changes to Features Section ... 1
Added Patent Note, Note 1 ... 1
Changes to Table 1 ... 1
Changes to AC Accuracy Parameter, Table 2 ... 3
Changed nA to µA, Standby Current Parameter, Unit Column, Table 3 ... 4
Changes to Table 8 ... 16
Changes to Power Supply Section ... 17
Updated Outline Dimensions ... 22

4/2016—Rev. E to Rev. F

Changed AD7988-x to AD7988-1/AD7988-5 ... Throughout
Changes to Table 1 ... 1
Changes to Table 2 ... 3
Changes to Table 3 ... 4
Changes to Table 4 ... 5

8/2013—Rev. C to Rev. D

Changes to Features Section ... 1
Changes to Table 3 ... 4
Updated Outline Dimensions ... 22
Changes to Ordering Guide ... 23

8/2012—Rev. B to Rev. C
Changes to Ordering Guide.....23

5/2012—Rev. A to Rev. B
Changes to Table 3.....4
Updated Outline Dimensions.....22

2/2012—Rev. 0 to Rev. A
Added LFCSP Thermal Impedance Values.....7
Updated Outline Dimensions.....23
Changes to Ordering Guide.....23

2/2012—Revision 0: Initial Version

SPECIFICATIONS

VDD = 2.5 V, VIO = 1.71 V to 5.5 V, V_{REF} = 5 V, T_A = −40°C to +125°C, unless otherwise noted.

Table 2.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
RESOLUTION		16			Bits
ANALOG INPUT					
Voltage Range	IN+ − IN−	0		V_{REF}	V
Absolute Input Voltage	IN+	−0.1		V_{REF} + 0.1	V
	IN−	−0.1		+0.1	V
Analog Input CMRR	f_{IN} = 1 kHz		60		dB
Leakage Current at 25°C	Acquisition phase		1		nA
Input Impedance		See the Analog Inputs section			
ACCURACY					
No Missing Codes		16			Bits
Differential Linearity Error	V_{REF} = 5 V	−0.9	±0.4	+0.9	LSB[1]
	V_{REF} = 2.5 V		±0.55		LSB[1]
Integral Linearity Error	V_{REF} = 5 V	−1.25	±0.6	+1.25	LSB[1]
	V_{REF} = 2.5 V		±0.65		LSB[1]
Transition Noise	V_{REF} = 5 V		0.6		LSB[1]
	V_{REF} = 2.5 V		1.0		LSB[1]
Gain Error, T_{MIN} to T_{MAX}[2]			±2		LSB[1]
Gain Error Temperature Drift			±0.35		ppm/°C
Zero Error, T_{MIN} to T_{MAX}[2]		−0.5	±0.08	+0.5	mV
Zero Temperature Drift			0.54		ppm/°C
Power Supply Sensitivity	VDD = 2.5 V ± 5%		±0.1		LSB[1]
THROUGHPUT					
AD7988-1					
Conversion Rate		0		100	kSPS
Transient Response	Full-scale step			500	ns
AD7988-5					
Conversion Rate		0		500	kSPS
Transient Response	Full-scale step			400	ns
AC ACCURACY					
Dynamic Range	V_{REF} = 5 V		92		dB[3]
	V_{REF} = 2.5 V		87		dB[3]
Oversampled Dynamic Range	f_O = 10 kSPS		111		dB[3]
Signal-to-Noise Ratio, SNR	f_{IN} = 10 kHz, V_{REF} = 5 V	90	91.5		dB[3]
	f_{IN} = 10 kHz, V_{REF} = 2.5 V		87		dB[3]
Spurious-Free Dynamic Range, SFDR	f_{IN} = 10 kHz		−110		dB[3]
Total Harmonic Distortion, THD	f_{IN} = 10 kHz		−114		dB[3]
Signal-to-(Noise + Distortion), SINAD	f_{IN} = 10 kHz, V_{REF} = 5 V		91		dB[3]
	f_{IN} = 10 kHz, V_{REF} = 2.5 V		86.5		dB[3]

[1] LSB means least significant bit. With the 5 V input range, 1 LSB is 76.3 µV.
[2] See the Terminology section. These specifications include full temperature range variation, but not the error contribution from the external reference.
[3] All specifications in dB are referred to a full-scale range (FSR). Tested with an input signal at 0.5 dB below full scale, unless otherwise specified.

VDD = 2.5 V, VIO = 1.71 V to 5.5 V, V_{REF} = 5 V, T_A = −40°C to +125°C, unless otherwise noted.

Table 3.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
REFERENCE					
Voltage Range		2.4		5.1	V
Load Current	V_{REF} = 5 V		250		µA
SAMPLING DYNAMICS					
−3 dB Input Bandwidth			10		MHz
Aperture Delay	VDD = 2.5 V		2.0		ns
DIGITAL INPUTS					
Logic Levels					
V_{IL}	VIO > 3 V	−0.3		0.3 × VIO	V
V_{IH}	VIO > 3 V	0.7 × VIO		VIO + 0.3	V
V_{IL}	VIO ≤ 3 V	−0.3		0.1 × VIO	V
V_{IH}	VIO ≤ 3 V	0.9 × VIO		VIO + 0.3	V
I_{IL}		−1		+1	µA
I_{IH}		−1		+1	µA
DIGITAL OUTPUTS					
Data Format		Serial 16 bits straight binary			
Pipeline Delay		Conversion results available immediately after completed conversion			
V_{OL}	I_{SINK} = 500 µA			0.4	V
V_{OH}	I_{SOURCE} = −500 µA	VIO − 0.3			V
POWER SUPPLIES					
VDD		2.375	2.5	2.625	V
VIO		1.71		5.5	V
Standby Current[1, 2]	VDD and VIO = 2.5 V, 25°C		0.35		µA
AD7988-1 Power Dissipation	VDD = 2.625 V, V_{REF} = 5 V, VIO = 3 V				
Total	10 kSPS throughput		70		µW
	100 kSPS throughput		700		µW
				1	mW
VDD Only			400		µW
REF Only			170		µW
VIO Only			130		µW
AD7988-5 Power Dissipation	VDD = 2.625 V, V_{REF} = 5 V, VIO = 3 V				
Total	500 kSPS throughput		3.5	5	mW
VDD Only			2		mW
REF Only			0.85		mW
VIO Only			0.65		mW
Energy per Conversion			7.0		nJ/sample
TEMPERATURE RANGE					
Specified Performance	T_{MIN} to T_{MAX}	−40		+125	°C

[1] With all digital inputs forced to VIO or GND as required.
[2] During the acquisition phase.

TIMING SPECIFICATIONS

VDD = 2.37 V to 2.63 V, VIO = 1.71 V to 5.5 V, T_A = −40°C to +125°C, unless otherwise stated. See Figure 2 for load conditions.

Table 4.

Parameter[1]	Symbol	Min	Typ	Max	Unit
AD7988-1					
Throughput Rate				100	kHz
Conversion Time: CNV Rising Edge to Data Available	t_{CONV}			9.5	µs
Acquisition Time	t_{ACQ}	500			ns
Time Between Conversions	t_{CYC}	10			µs
AD7988-5					
Throughput Rate				500	kHz
Conversion Time: CNV Rising Edge to Data Available	t_{CONV}				
B Grade				1.6	µs
C Grade				1.2	µs
Acquisition Time	t_{ACQ}				
B Grade		400			ns
C Grade		800			ns
Time Between Conversions	t_{CYC}	2			µs
CNV Pulse Width ($\overline{CS}$ Mode)	t_{CNVH}	500			ns
SCK Period ($\overline{CS}$ Mode)	t_{SCK}				
VIO Above 4.5 V		10.5			ns
VIO Above 3 V		12			ns
VIO Above 2.7 V		13			ns
VIO Above 2.3 V		15			ns
VIO Above 1.71 V		22			ns
SCK Period (Chain Mode)	t_{SCK}				
VIO Above 4.5 V		11.5			ns
VIO Above 3 V		13			ns
VIO Above 2.7 V		14			ns
VIO Above 2.3 V		16			ns
VIO Above 1.71 V		23			ns
SCK Low Time	t_{SCKL}				
VIO Above 2.3 V		4.5			ns
VIO Above 1.71 V		6			ns
SCK High Time	t_{SCKH}				
VIO Above 2.3 V		4.5			ns
VIO Above 1.71 V		6			ns
SCK Falling Edge to Data Remains Valid	t_{HSDO}	3			ns
SCK Falling Edge to Data Valid Delay	t_{DSDO}				
VIO Above 4.5 V				9.5	ns
VIO Above 3 V				11	ns
VIO Above 2.7 V				12	ns
VIO Above 2.3 V				14	ns
VIO Above 1.71 V			14	21	ns
CNV or SDI Low to SDO D15 MSB Valid ($\overline{CS}$ Mode)	t_{EN}				
VIO Above 3 V				10	ns
VIO Above 2.3V				15	ns
VIO Above 1.71 V			18	40	ns
CNV or SDI High or Last SCK Falling Edge to SDO High Impedance ($\overline{CS}$ Mode)	t_{DIS}			20	ns
SDI Valid Setup Time from CNV Rising Edge	$t_{SSDICNV}$	5			ns
SDI Valid Hold Time from CNV Rising Edge ($\overline{CS}$ Mode)	$t_{HSDICNV}$				
VIO Above 2.3 V		2			ns
VIO Above 1.71 V		10			ns

Parameter[1]	Symbol	Min	Typ	Max	Unit
SDI Valid Hold Time from CNV Rising Edge (Chain Mode)	$t_{HSDICNV}$	0			ns
SCK Valid Setup Time from CNV Rising Edge (Chain Mode)	$t_{SSCKCNV}$	5			ns
SCK Valid Hold Time from CNV Rising Edge (Chain Mode)	$t_{HSCKCNV}$	5			ns
SDI Valid Setup Time from SCK Falling Edge (Chain Mode)	$t_{SSDISCK}$	2			ns
SDI Valid Hold Time from SCK Falling Edge (Chain Mode)	$t_{HSDISCK}$	3			ns

[1] Timing parameters measured with respect to a falling edge are defined as triggered at x% VIO. Timing parameters measured with respect to a rising edge are defined as triggered at y% VIO. For VIO ≤ 3 V, x = 90 and y = 10. For VIO > 3 V, x = 70 and y = 30. The minimum V_{IH} and maximum V_{IL} are used. See the Digital Inputs Specifications in Table 2.

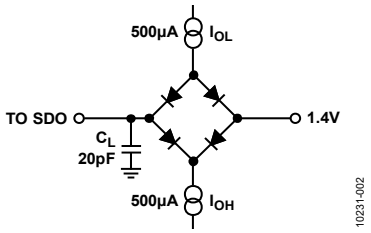


Figure 2. Load Circuit for Digital Interface Timing

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	Rating
Analog Inputs	
IN+,[1] IN−[1] to GND	−0.3 V to V_{REF} + 0.3 V or ±130 mA
Supply Voltage	
REF, VIO to GND	−0.3 V to +6 V
VDD to GND	−0.3 V to +3 V
VDD to VIO	+3 V to −6 V
Digital Inputs to GND	−0.3 V to VIO + 0.3 V
Digital Outputs to GND	−0.3 V to VIO + 0.3 V
Storage Temperature Range	−65°C to +125°C
Junction Temperature	150°C
Reflow Soldering	JEDEC Standard (J-STD-020)

[1] See the Analog Inputs section.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JA} is the natural convection junction to ambient thermal resistance measured in a one cubic foot sealed enclosure. θ_{JC} is the junction to case thermal resistance.

Table 6. Thermal Resistance

Package Type[1]	θ_{JA}	θ_{JC}	Unit
RM-10	200	44	°C/W
CP-10-9	80	15	°C/W

[1] Test Condition 1: thermal impedance simulated values are based upon use of a 2S2P JEDEC PCB. See the Ordering Guide.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

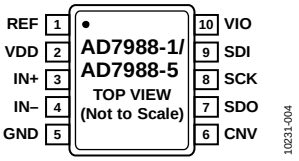


Figure 3. 10-Lead MSOP Pin Configuration

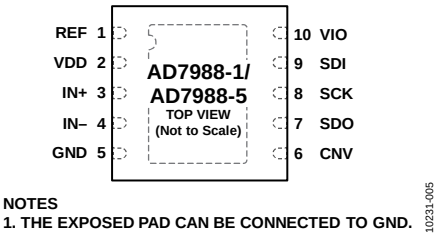


Figure 4. 10-Lead LFCSP Pin Configuration

Table 7. Pin Function Descriptions

Pin No.	Mnemonic	Type[1]	Description
1	REF	AI	Reference Input Voltage. The V_{REF} range is from 2.4 V to 5.1 V. It is referred to the GND pin. The GND pin should be decoupled closely to the REF pin with a 10 µF capacitor.
2	VDD	P	Power Supply.
3	IN+	AI	Analog Input. It is referred to IN−. The voltage range, for example, the difference between IN+ and IN−, is 0 V to V_{REF}.
4	IN−	AI	Analog Input Ground Sense. Connect to the analog ground plane or to a remote sense ground.
5	GND	P	Power Supply Ground.
6	CNV	DI	Convert Input. This input has multiple functions. On its leading edge, it initiates the conversions and selects the interface mode of the part: chain mode or $\overline{CS}$ mode. In $\overline{CS}$ mode, the SDO pin is enabled when CNV is low. In chain mode, the data should be read when CNV is high.
7	SDO	DO	Serial Data Output. The conversion result is output on this pin. It is synchronized to SCK.
8	SCK	DI	Serial Data Clock Input. When the part is selected, the conversion result is shifted out by this clock.
9	SDI	DI	Serial Data Input. This input provides multiple features. It selects the interface mode of the ADC as follows: Chain mode is selected if this pin is low during the CNV rising edge. In this mode, SDI is used as a data input to daisy-chain the conversion results of two or more ADCs onto a single SDO line. The digital data level on SDI is output on SDO with a delay of 16 SCK cycles. $\overline{CS}$ mode is selected if SDI is high during the CNV rising edge. In this mode, either SDI or CNV can enable the serial output signals when low.
10	VIO	P	Input/Output Interface Digital Power. Nominally at the same supply as the host interface (1.8 V, 2.5 V, 3 V, or 5 V).
	EP		Exposed Pad. The exposed pad can be connected to GND.

[1]AI = analog input, DI = digital input, DO = digital output, and P = power.

TERMINOLOGY

Integral Nonlinearity Error (INL)

INL refers to the deviation of each individual code from a line drawn from negative full scale through positive full scale. The point used as negative full scale occurs ½ LSB before the first code transition. Positive full scale is defined as a level 1½ LSB beyond the last code transition. The deviation is measured from the middle of each code to the true straight line (see Figure 29).

Differential Nonlinearity Error (DNL)

In an ideal ADC, code transitions are 1 LSB apart. DNL is the maximum deviation from this ideal value. It is often specified in terms of resolution for which no missing codes are guaranteed.

Offset Error

The first transition should occur at a level ½ LSB above analog ground (38.1 µV for the 0 V to 5 V range). The offset error is the deviation of the actual transition from that point.

Gain Error

The last transition (from 111 … 10 to 111 … 11) should occur for an analog voltage 1½ LSB below the nominal full scale (4.999886 V for the 0 V to 5 V range). The gain error is the deviation of the actual level of the last transition from the ideal level after the offset is adjusted out.

Spurious-Free Dynamic Range (SFDR)

SFDR is the difference, in decibels (dB), between the rms amplitude of the input signal and the peak spurious signal.

Effective Number of Bits (ENOB)

ENOB is a measurement of the resolution with a sine wave input. It is related to SINAD by the following formula:

$$ENOB = (SINAD_{dB} - 1.76)/6.02$$

and is expressed in bits.

Noise-Free Code Resolution

Noise-free code resolution is the number of bits beyond which it is impossible to distinctly resolve individual codes. It is calculated as

$$Noise\text{-}Free\ Code\ Resolution = \log_2(2^N/Peak\text{-}to\text{-}Peak\ Noise)$$

and is expressed in bits.

Effective Resolution

Effective resolution is calculated as

$$Effective\ Resolution = \log_2(2^N/RMS\ Input\ Noise)$$

and is expressed in bits.

Total Harmonic Distortion (THD)

THD is the ratio of the rms sum of the first five harmonic components to the rms value of a full-scale input signal and is expressed in dB.

Dynamic Range

Dynamic range is the ratio of the rms value of the full scale to the total rms noise measured with the inputs shorted together. The value for dynamic range is expressed in dB. It is measured with a signal at −60 dBFS to include all noise sources and DNL artifacts.

Signal-to-Noise Ratio (SNR)

SNR is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, excluding harmonics and dc. The value for SNR is expressed in dB.

Signal-to-(Noise + Distortion) Ratio (SINAD)

SINAD is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc. The value for SINAD is expressed in dB.

Aperture Delay

Aperture delay is the measure of the acquisition performance. It is the time between the rising edge of the CNV input and when the input signal is held for a conversion.

Transient Response

Transient response is the time required for the ADC to accurately acquire its input after a full-scale step function is applied.

TYPICAL PERFORMANCE CHARACTERISTICS

VDD = 2.5 V, V_{REF} = 5.0 V, VIO = 3.3 V, unless otherwise noted.

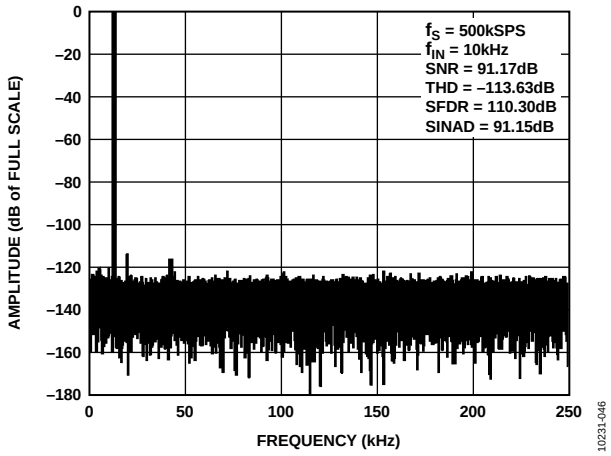


Figure 5. AD7988-5 FFT Plot, V_{REF} = 5 V

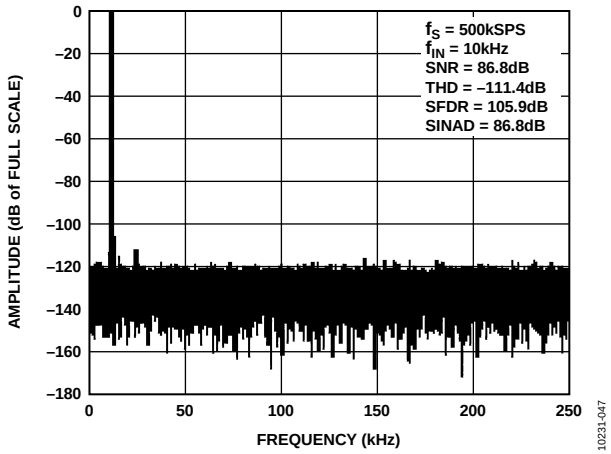


Figure 6. AD7988-5 FFT Plot, V_{REF} = 2.5 V

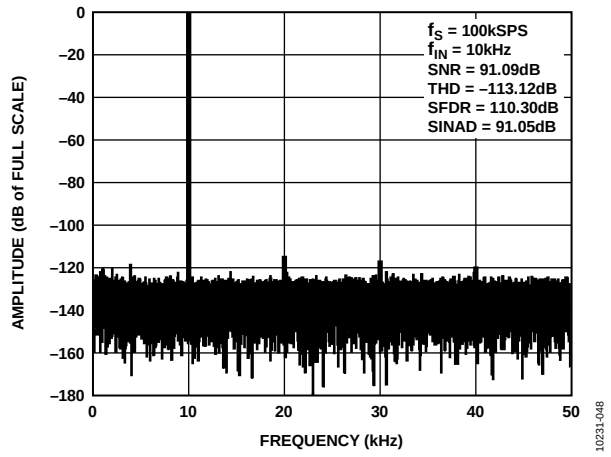


Figure 7. AD7988-1 FFT Plot, V_{REF} = 5 V

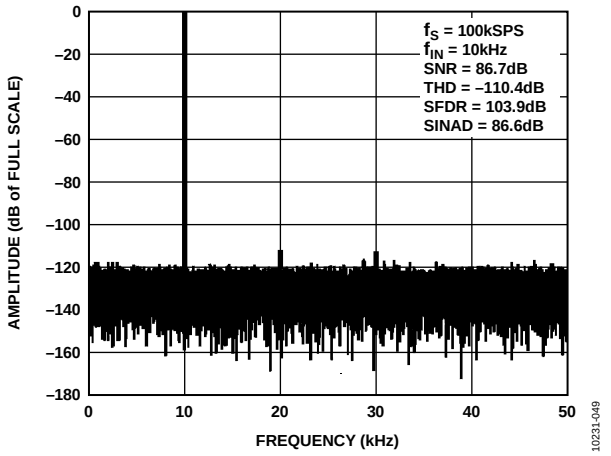


Figure 8. AD7988-1 FFT Plot, V_{REF} = 2.5 V

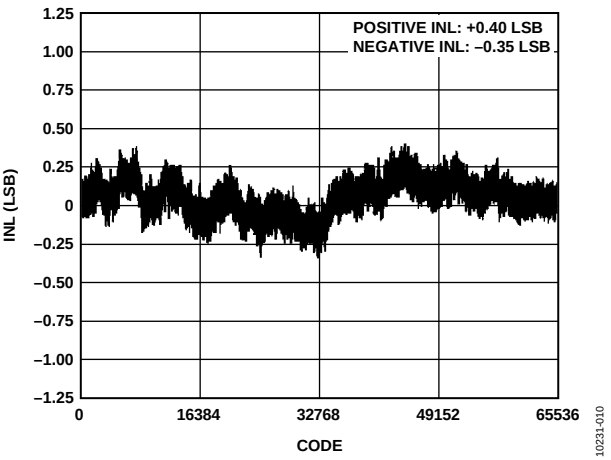


Figure 9. Integral Nonlinearity vs. Code, V_{REF} = 5 V

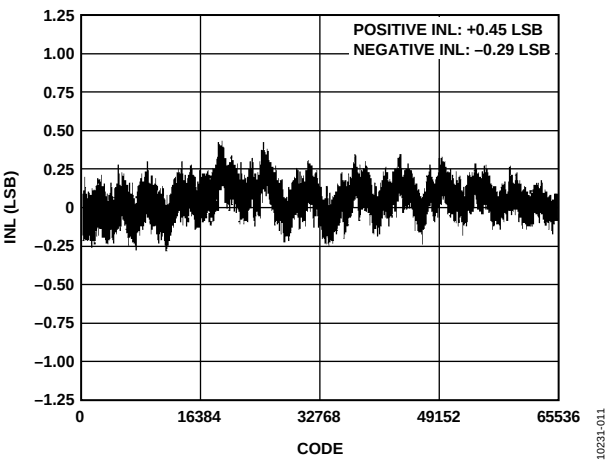


Figure 10. Integral Nonlinearity vs. Code, V_{REF} = 2.5 V

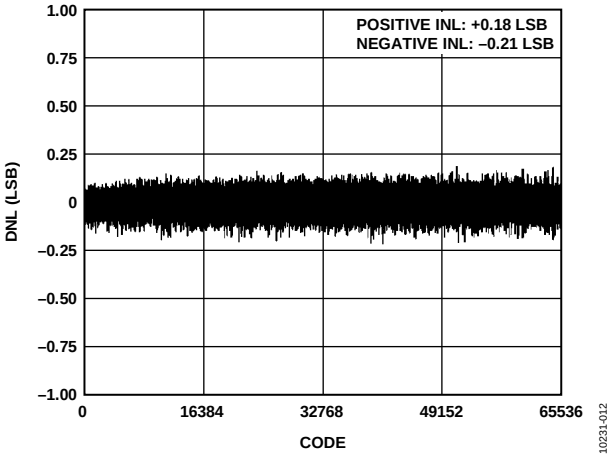


Figure 11. Differential Nonlinearity vs. Code, V_{REF} = 5 V

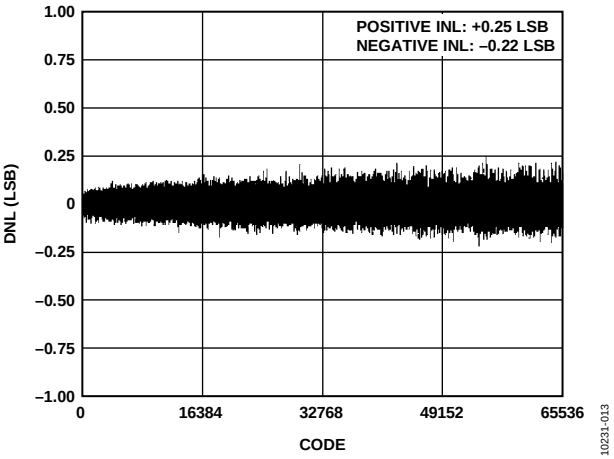


Figure 12. Differential Nonlinearity vs. Code, V_{REF} = 2.5 V

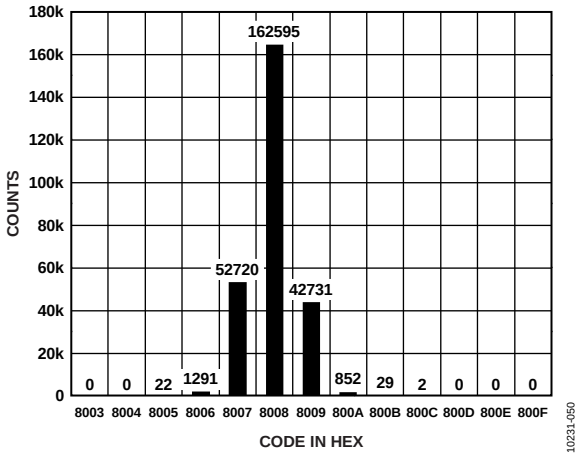


Figure 13. Histogram of a DC Input at the Code Center, V_{REF} = 5 V

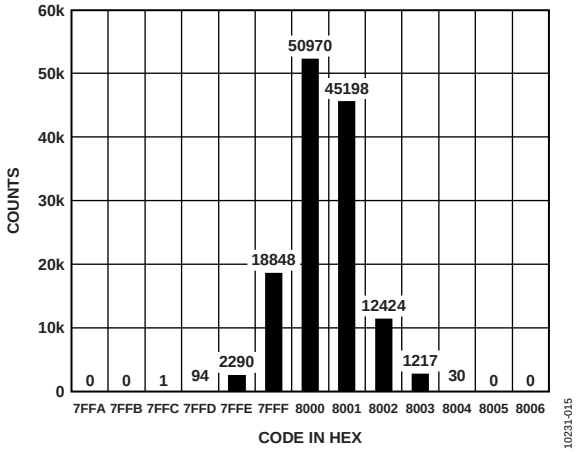


Figure 14. Histogram of a DC Input at the Code Transition, V_{REF} = 2.5 V

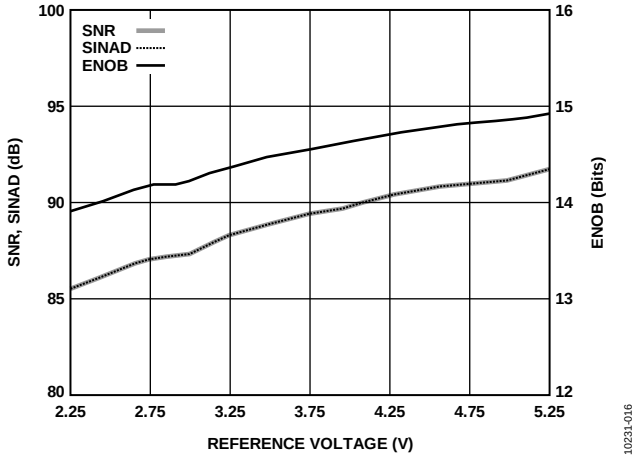


Figure 15. SNR, SINAD, and ENOB vs. Reference Voltage

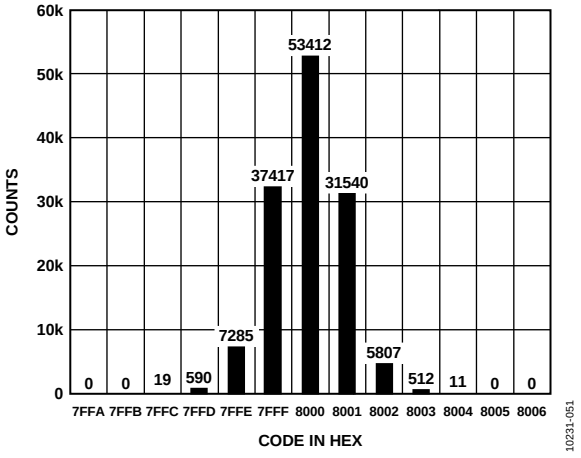


Figure 16. Histogram of a DC Input at the Code Center, V_{REF} = 2.5 V

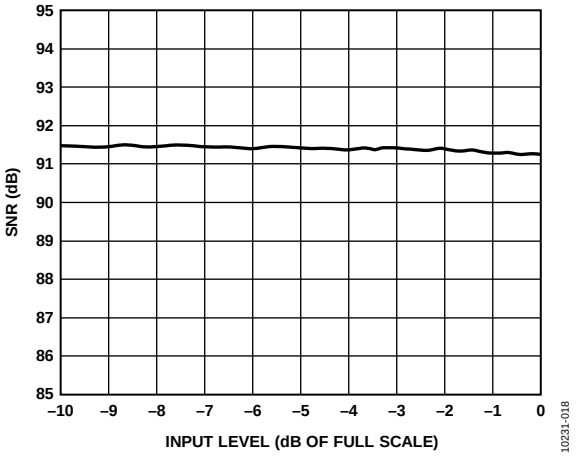


Figure 17. SNR vs. Input Level

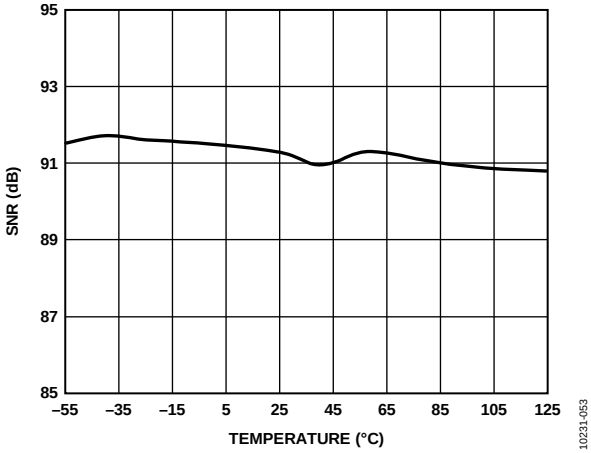


Figure 20. SNR vs. Temperature

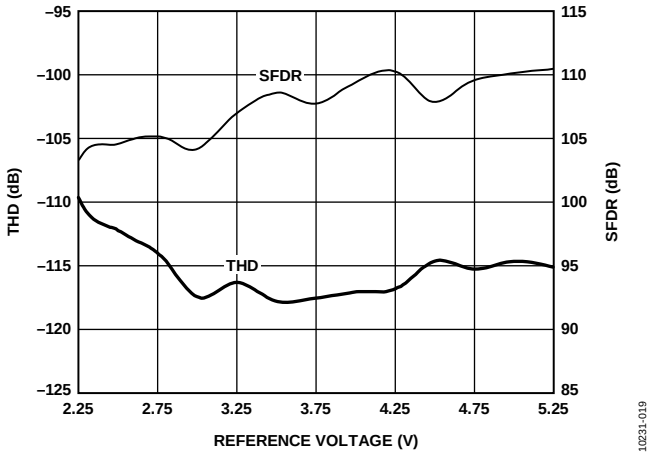


Figure 18. THD, SFDR vs. Reference Voltage

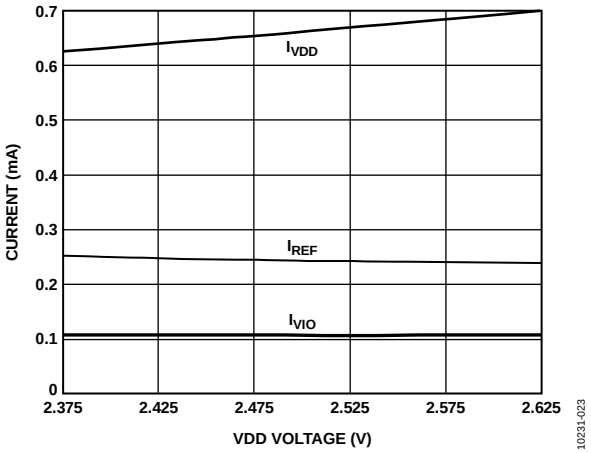


Figure 21. Operating Currents vs. Supply (AD7988-5)

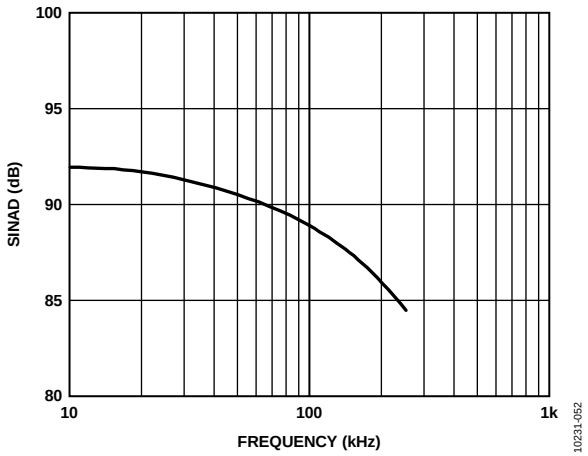


Figure 19. SINAD vs. Frequency

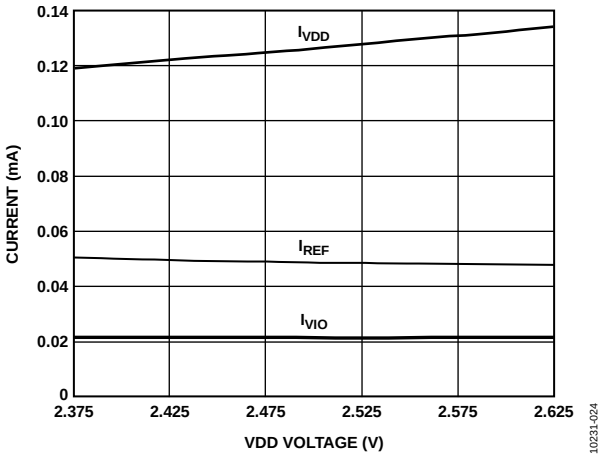


Figure 22. Operating Currents vs. Supply (AD7988-1)

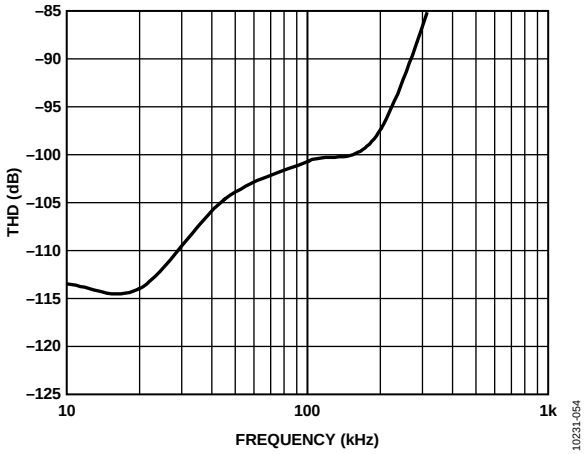


Figure 23. THD vs. Frequency

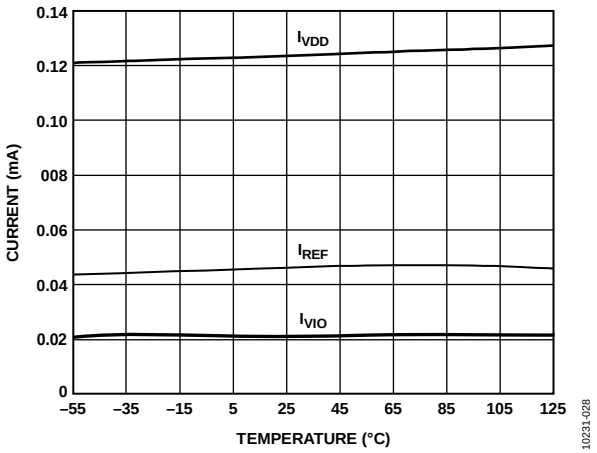


Figure 26. Operating Currents vs. Temperature (AD7988-1)

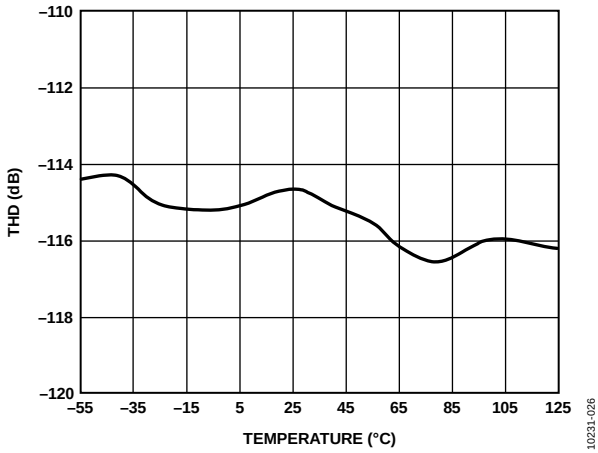


Figure 24. THD vs. Temperature

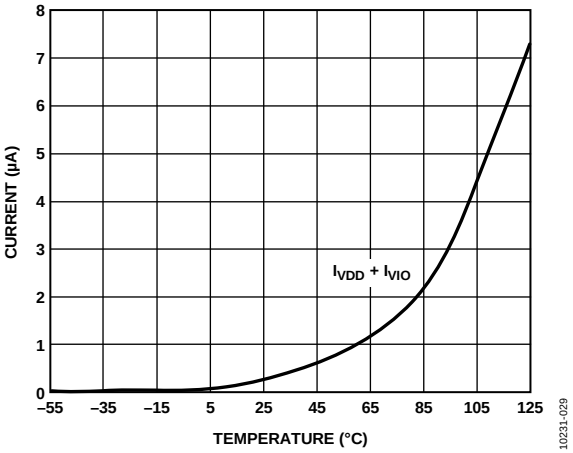


Figure 27. Power-Down Currents vs. Temperature

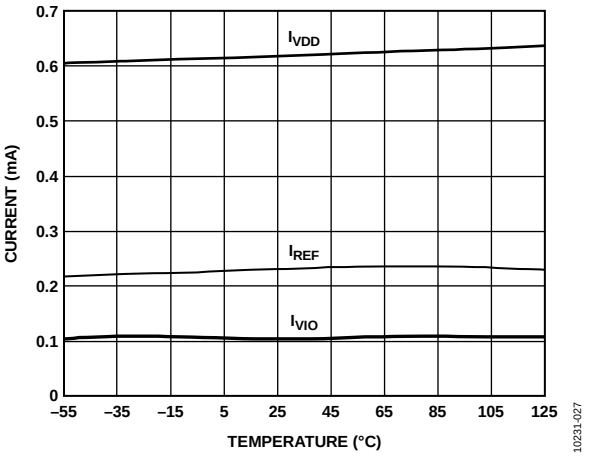


Figure 25. Operating Currents vs. Temperature (AD7988-5)

THEORY OF OPERATION

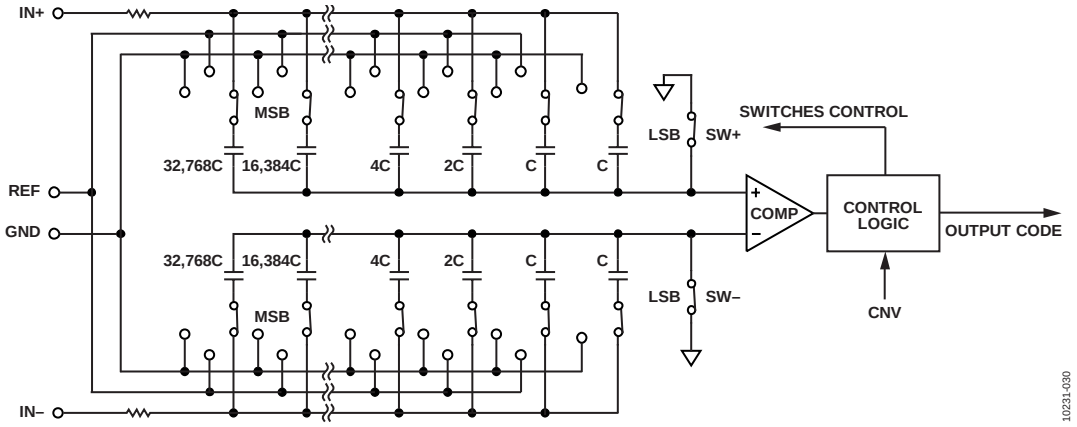


Figure 28. ADC Simplified Schematic

CIRCUIT INFORMATION

The AD7988-1/AD7988-5 devices are fast, low power, single-supply, precise 16-bit ADCs that use a successive approximation architecture.

The AD7988-1 is capable of converting 100,000 samples per second (100 kSPS), whereas the AD7988-5 is capable of a throughput of 500 kSPS, and they power down between conversions. When operating at 10 kSPS, for example, the ADC consumes 70 µW typically, ideal for battery-powered applications.

The AD7988-1/AD7988-5 provide the user with on-chip track-and-hold and does not exhibit any pipeline delay or latency, making it ideal for multiple multiplexed channel applications.

The AD7988-1/AD7988-5 can be interfaced to any 1.8 V to 5 V digital logic family. It is housed in a 10-lead MSOP or a tiny 10-lead LFCSP that combines space savings and allows flexible configurations.

CONVERTER OPERATION

The AD7988-1/AD7988-5 are successive approximation ADCs based on a charge redistribution DAC. Figure 28 shows the simplified schematic of the ADC. The capacitive DAC consists of two identical arrays of 16 binary weighted capacitors, which are connected to the two comparator inputs.

During the acquisition phase, terminals of the array tied to the comparator's input are connected to GND via SW+ and SW−. All independent switches are connected to the analog inputs. Therefore, the capacitor arrays are used as sampling capacitors and acquire the analog signal on the IN+ and IN− inputs. When the acquisition phase is completed and the CNV input goes high, a conversion phase is initiated. When the conversion phase begins, SW+ and SW− are opened first. The two capacitor arrays are then disconnected from the inputs and connected to the GND input. Therefore, the differential voltage between the IN+ and IN− inputs captured at the end of the acquisition phase are applied to the comparator inputs, causing the comparator to become unbalanced. By switching each element of the capacitor array between GND and REF, the comparator input varies by binary weighted voltage steps ($V_{REF}/2$, $V_{REF}/4$ … $V_{REF}/65,536$). The control logic toggles these switches, starting with the MSB, to bring the comparator back into a balanced condition. After the completion of this process, the part returns to the acquisition phase and the control logic generates the ADC output code.

Because the AD7988-1/AD7988-5 have an on-board conversion clock, the serial clock, SCK, is not required for the conversion process.

Transfer Functions

The ideal transfer characteristic for the AD7988-1/AD7988-5 is shown in Figure 29 and Table 8.

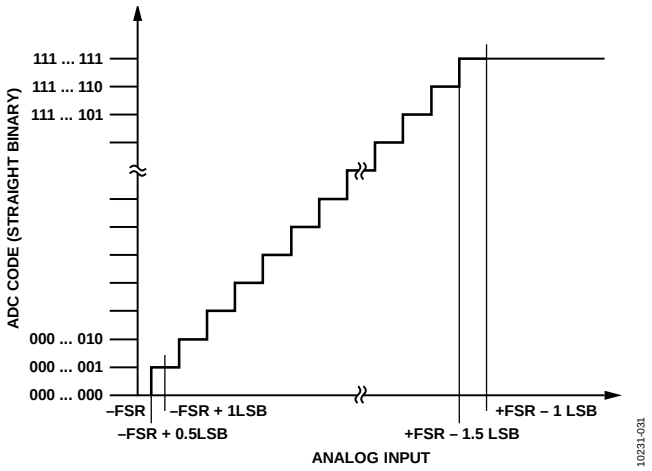


Figure 29. ADC Ideal Transfer Function

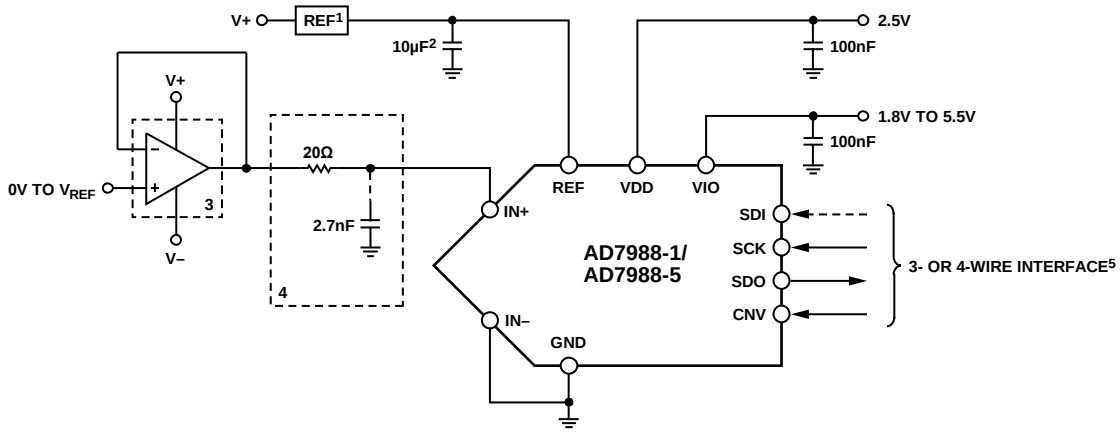
Table 8. Output Codes and Ideal Input Voltages

	Analog Input	
Description	**V_{REF} = 5 V**	**Digital Output Code (Hex)**
FSR – 1 LSB	4.999924 V	FFFF[1]
Midscale + 1 LSB	2.500076 V	8001
Midscale	2.5 V	8000
Midscale – 1 LSB	2.499924 V	7FFF
–FSR + 1 LSB	76.3 µV	0001
–FSR	0 V	0000[2]

[1] This is also the code for an overranged analog input (V_{IN+} – V_{IN-} above V_{REF} – V_{GND}).
[2] This is also the code for an underranged analog input (V_{IN+} – V_{IN-} below V_{GND}).

TYPICAL CONNECTION DIAGRAM

Figure 30 shows an example of the recommended connection diagram for the AD7988-1/AD7988-5 when multiple supplies are available.



[1] SEE THE VOLTAGE REFERENCE INPUT SECTION FOR REFERENCE SELECTION.
[2] C_{REF} IS USUALLY A 10µF CERAMIC CAPACITOR (X5R).
[3] SEE THE DRIVER AMPLIFIER CHOICE SECTION.
[4] RECOMMENDED FILTER CONFIGURATION. SEE THE ANALOG INPUTS SECTION.
[5] SEE THE DIGITAL INTERFACE SECTION FOR THE MOST CONVENIENT INTERFACE MODE.

Figure 30. Typical Application Diagram with Multiple Supplies

ANALOG INPUTS

Figure 31 shows an equivalent circuit of the input structure of the AD7988-1/AD7988-5.

The two diodes, D1 and D2, provide ESD protection for the analog inputs, IN+ and IN−. Care must be taken to ensure that the analog input signal never exceeds the supply rails by more than 0.3 V, because this causes these diodes to become forward-biased and start conducting current. These diodes can handle a forward-biased current of 130 mA maximum. For instance, these conditions may eventually occur when the input buffer's supplies are different from VDD. In such a case (for example, an input buffer with a short circuit), the current limitation can be used to protect the part.

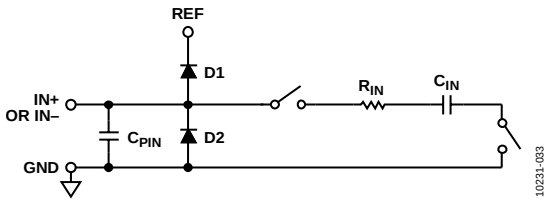


Figure 31. Equivalent Analog Input Circuit

The analog input structure allows the sampling of the true differential signal between IN+ and IN−. By using these differential inputs, signals common to both inputs are rejected.

During the acquisition phase, the impedance of the analog inputs (IN+ and IN−) can be modeled as a parallel combination of Capacitor C_{PIN} and the network formed by the series connection of R_{IN} and C_{IN}. C_{PIN} is primarily the pin capacitance. R_{IN} is typically 400 Ω and is a lumped component made up of serial resistors and the on resistance of the switches. C_{IN} is typically 30 pF and is mainly the ADC sampling capacitor. During the conversion phase, when the switches are opened, the input impedance is limited to C_{PIN}. R_{IN} and C_{IN} make a one-pole, low-pass filter that reduces undesirable aliasing effects and limits the noise.

When the source impedance of the driving circuit is low, the AD7988-1/AD7988-5 can be driven directly. Large source impedances significantly affect the ac performance, especially THD. The dc performances are less sensitive to the input impedance. The maximum source impedance depends on the amount of THD that can be tolerated. The THD degrades as a function of the source impedance and the maximum input frequency.

DRIVER AMPLIFIER CHOICE

Although the AD7988-1/AD7988-5 are easy to drive, the driver amplifier needs to meet the following requirements:

- The noise generated by the driver amplifier must be kept as low as possible to preserve the SNR and transition noise performance of the AD7988-1/AD7988-5. The noise coming from the driver is filtered by the AD7988-1/AD7988-5 analog input circuit's one-pole, low-pass filter made by R_{IN} and C_{IN} or by the external filter, if one is used. Because the typical noise of the AD7988-1/AD7988-5 is 47.3 μV rms, the SNR degradation due to the amplifier is

$$SNR_{LOSS} = 20 \log \left(\frac{47.3}{\sqrt{47.3^2 + \frac{\pi}{2} f_{-3dB} (Ne_N)^2}} \right)$$

- where:
  f_{-3dB} is the input bandwidth in MHz of the AD7988-1/AD7988-5 (10 MHz) or the cutoff frequency of the input filter, if one is used.
  N is the noise gain of the amplifier (for example, 1 in buffer configuration).
  e_N is the equivalent input noise voltage of the op amp, in nV/√Hz.
- For ac applications, the driver should have a THD performance commensurate with the AD7988-1/AD7988-5.
- For multichannel multiplexed applications, the driver amplifier and the AD7988-1/AD7988-5 analog input circuit must settle for a full-scale step onto the capacitor array at a 16-bit level (0.0015%, 15 ppm). In the amplifier data sheet, settling at 0.1% to 0.01% is more commonly specified. This may differ significantly from the settling time at a 16-bit level and should be verified prior to driver selection.

Table 9. Recommended Driver Amplifiers[1]

Amplifier	Typical Application
ADA4805-1	Low noise, small size, and low power
ADA4807-1	Very low noise and high frequency
ADA4627-1	Precision, low noise, and low input bias current
ADA4522-1	Precision, zero drift, and EMI enhanced
ADA4841-1	Low noise, low distortion and low power

[1] For the latest recommended drivers, see the product recommendations listed on the product webpage.

VOLTAGE REFERENCE INPUT

The AD7988-1/AD7988-5 voltage reference input, REF, has a dynamic input impedance and must therefore be driven by a low impedance source with efficient decoupling between the REF and GND pins, as explained in the Layout section.

When REF is driven by a very low impedance source, for example, a reference buffer using the AD8031, the ADA4805-1, or the ADA4807-1, a ceramic chip capacitor is appropriate for optimum performance.

If an unbuffered reference voltage is used, the decoupling value depends on the reference used. For example, a 22 µF (X5R, 1206 size) ceramic chip capacitor is appropriate for optimum performance using a low temperature drift reference, such as the ADR435, ADR445, LTC6655, or ADR4550.

If desired, a reference-decoupling capacitor value as small as 2.2 µF can be used with a minimal impact on performance, especially DNL.

Regardless, there is no need for an additional lower value ceramic decoupling capacitor (for example, 100 nF) between the REF and GND pins.

POWER SUPPLY

The AD7988-1/AD7988-5 use two power supply pins: a core supply, VDD, and a digital input/output interface supply, VIO. VIO allows direct interface with any logic between 1.8 V and 5.0 V. To reduce the number of supplies needed, VIO and VDD can be tied together. When VIO is greater than or equal to VDD, the AD7988-1/AD7988-5 are insensitive to power supply sequencing. In normal operation, if the magnitude of VIO is less than the magnitude of VDD, VIO must be applied before VDD. Additionally, it is very insensitive to power supply variations over a wide frequency range, as shown in Figure 32.

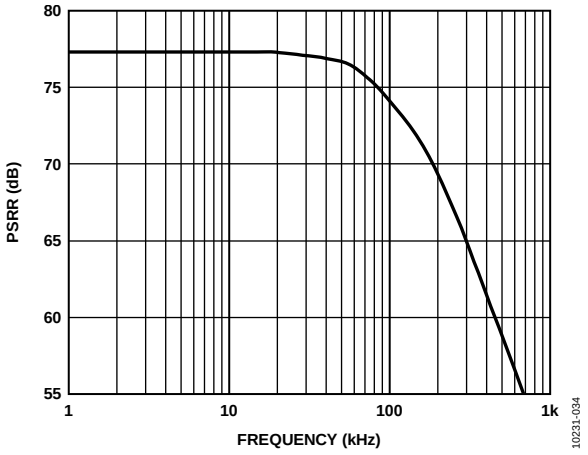


Figure 32. PSRR vs. Frequency

The AD7988-1/AD7988-5 powers down automatically at the end of each conversion phase.

DIGITAL INTERFACE

Although the AD7988-1/AD7988-5 have a reduced number of pins, it offers flexibility in its serial interface modes.

The AD7988-1/AD7988-5, when in $\overline{CS}$ mode, is compatible with SPI, QSPI™, and digital hosts. This interface can use either a 3-wire or 4-wire interface. A 3-wire interface using the CNV, SCK, and SDO signals minimizes wiring connections and is useful, for instance, in isolated applications. A 4-wire interface using the SDI, CNV, SCK, and SDO signals allows CNV, which initiates the conversions, to be independent of the readback timing (SDI). This is useful in low jitter sampling or simultaneous sampling applications.

The AD7988-1/AD7988-5, when in chain mode, provides a daisy-chain feature using the SDI input for cascading multiple ADCs on a single data line, similar to a shift register.

The mode in which the part operates depends on the SDI level when the CNV rising edge occurs. $\overline{CS}$ mode is selected if SDI is high, and chain mode is selected if SDI is low. The SDI hold time is such that when SDI and CNV are connected together, the chain mode is selected.

The user must time out the maximum conversion time prior to readback.

$\overline{CS}$ MODE, 3-WIRE

This mode is typically used when a single AD7988-1or AD7988-5 is connected to an SPI-compatible digital host. The connection diagram is shown in Figure 33, and the corresponding timing is given in Figure 34.

With SDI tied to VIO, a rising edge on CNV initiates a conversion, selects the $\overline{CS}$ mode, and forces SDO to high impedance. When the conversion is complete, the AD7988-1/AD7988-5 enter the acquisition phase and powers down.

When CNV goes low, the MSB is output onto SDO. The remaining data bits are then clocked by subsequent SCK falling edges. The data is valid on both SCK edges. Although the rising edge can be used to capture the data, a digital host using the SCK falling edge allows a faster reading rate, provided that it has an acceptable hold time. After the 16th SCK falling edge or when CNV goes high, whichever is earlier, SDO returns to high impedance.

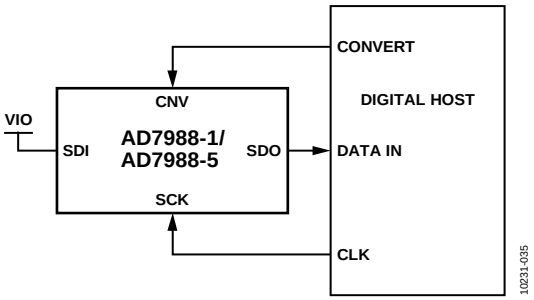


Figure 33. 3-Wire $\overline{CS}$ Mode Connection Diagram

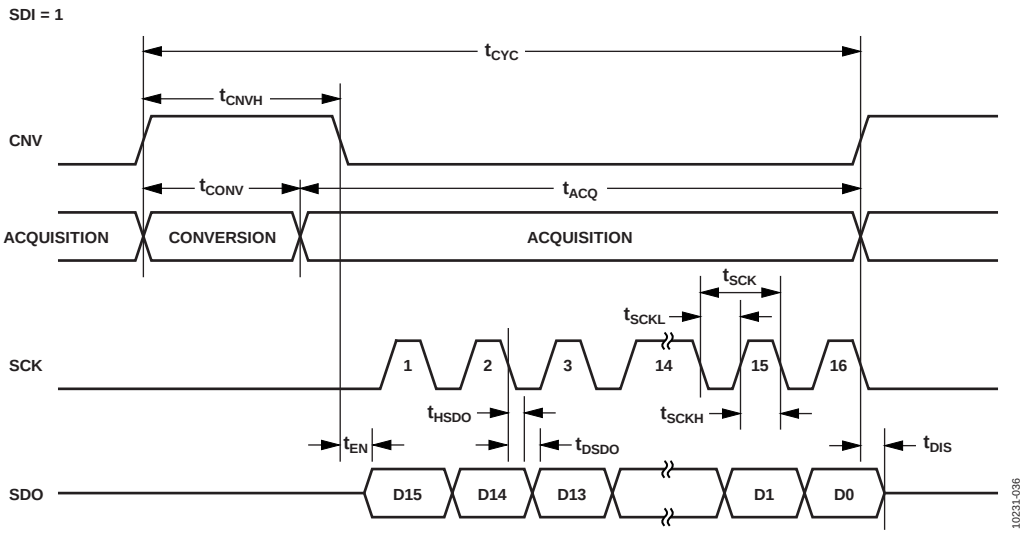


Figure 34. 3-Wire $\overline{CS}$ Mode Serial Interface Timing (SDI High)

$\overline{CS}$ MODE 4-WIRE

This mode is typically used when multiple AD7988-1/AD7988-5 devices are connected to an SPI-compatible digital host.

A connection diagram example using the AD7988-1/AD7988-5 devices are shown in Figure 35, and the corresponding timing is given in Figure 36.

With SDI high, a rising edge on CNV initiates a conversion, selects the $\overline{CS}$ mode, and forces SDO to high impedance. In this mode, CNV must be held high during the conversion phase and the subsequent data readback (if SDI and CNV are low, SDO is driven low). Prior to the minimum conversion time, SDI can be used to select other SPI devices, such as analog multiplexers, but SDI must be returned high before the minimum conversion time elapses and then held high for the maximum conversion time.

When the conversion is complete, the AD7988-1/AD7988-5 enter the acquisition phase and powers down. Each ADC result can be read by bringing its SDI input low, which consequently outputs the MSB onto SDO. The remaining data bits are then clocked by subsequent SCK falling edges. The data is valid on both SCK edges. Although the rising edge can be used to capture the data, a digital host using the SCK falling edge allows a faster reading rate, provided that it has an acceptable hold time. After the 16th SCK falling edge or when SDI goes high, whichever is earlier, SDO returns to high impedance and another AD7988-1 or AD7988-5 can be read.

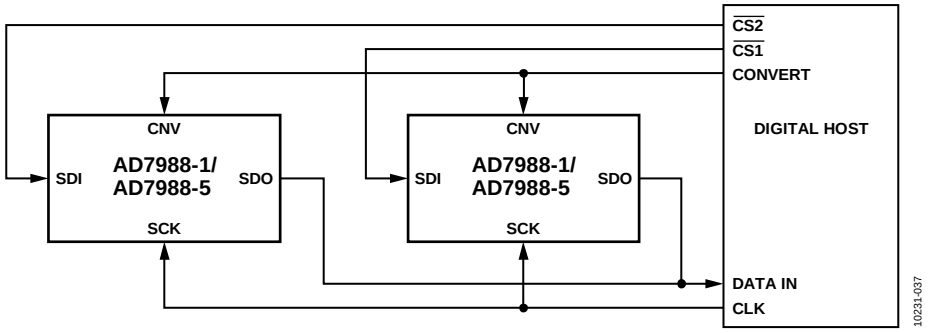


Figure 35. 4-Wire $\overline{CS}$ Mode Connection Diagram

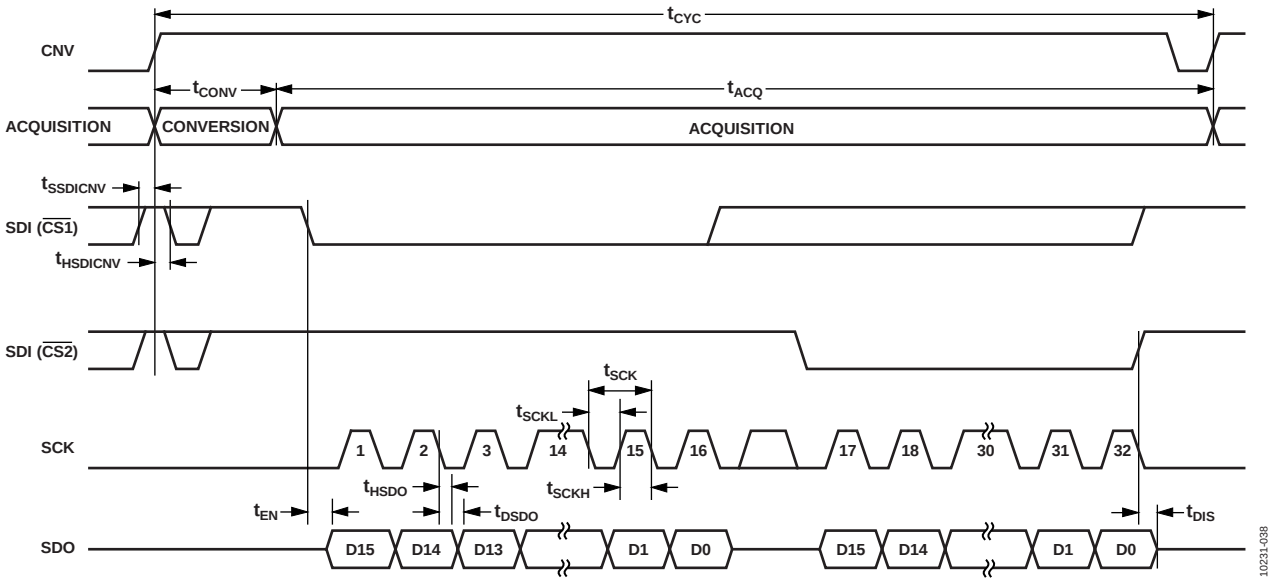


Figure 36. 4-Wire $\overline{CS}$ Mode Serial Interface Timing

CHAIN MODE

This mode can be used to daisy-chain multiple AD7988-1/ AD7988-5 devices on a 3-wire serial interface. This feature is useful for reducing component count and wiring connections, for example, in isolated multiconverter applications or for systems with a limited interfacing capacity. Data readback is analogous to clocking a shift register.

A connection diagram example using the AD7988-1/AD7988-5 devices is shown in Figure 37, and the corresponding timing is given in Figure 38.

When SDI and CNV are low, SDO is driven low. With SCK low, a rising edge on CNV initiates a conversion and selects the chain mode. In this mode, CNV is held high during the conversion phase and the subsequent data readback. When the conversion is complete, the MSB is output onto SDO and the AD7988-1/ AD7988-5 enter the acquisition phase and power down. The remaining data bits stored in the internal shift register are clocked by subsequent SCK falling edges. For each ADC, SDI feeds the input of the internal shift register and is clocked by the SCK falling edge. Each ADC in the chain outputs its data MSB first, and 16 × N clocks are required to read back the N ADCs. The data is valid on both SCK edges. Although the rising edge can be used to capture the data, a digital host using the SCK falling edge allows a faster reading rate and, consequently, more AD7988-1/ AD7988-5 devices in the chain, provided that the digital host has an acceptable hold time. The maximum conversion rate may be reduced due to the total readback time.

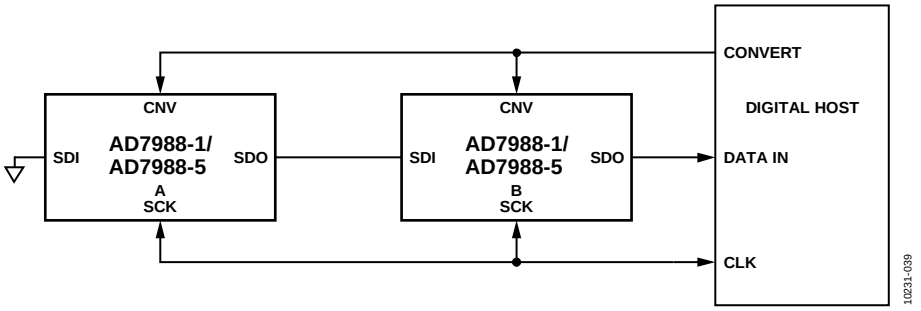


Figure 37. Chain Mode Connection Diagram

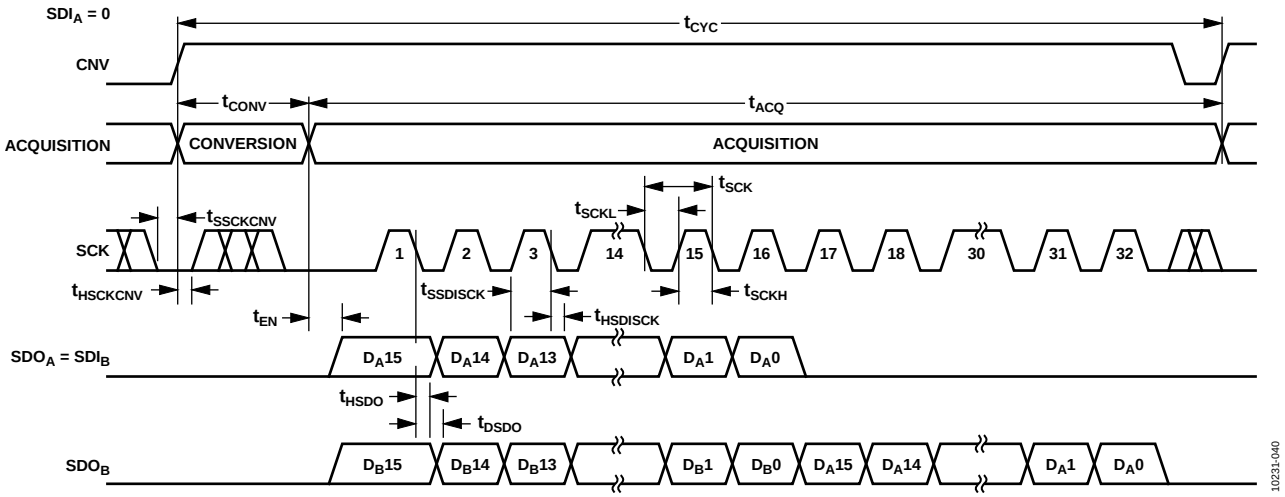


Figure 38. Chain Mode Serial Interface Timing

APPLICATIONS INFORMATION

INTERFACING TO BLACKFIN® DSP

The AD7988-1/AD7988-5 can easily connect to a DSP SPI or SPORT. The SPI configuration is straightforward, using the standard SPI interface as shown in Figure 39.

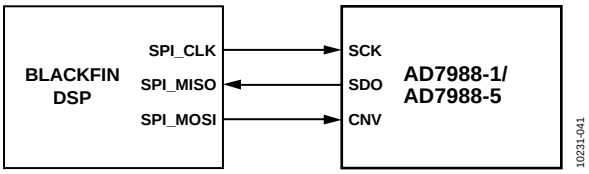


Figure 39. Typical Connection to Blackfin SPI Interface

Similarly, the SPORT interface can be used to interface to this ADC. The SPORT interface has some benefits in that it can use direct memory access (DMA) and provides a lower jitter CNV signal generated from a hardware counter.

Some glue logic may be required between SPORT and the AD7988-1/AD7988-5 interface. The evaluation board for the AD7988-1/AD7988-5 interfaces directly to the SPORT of the Blackfin-based (ADSP-BF527) SDP board. The configuration used for the SPORT interface requires the addition of some glue logic as shown in Figure 40. The SCK input to the ADC was gated off when CNV was high to keep the SCK line static while converting the data, thereby ensuring the best integrity of the result. This approach uses an AND gate and a NOT gate for the SCK path. The other logic gates used on the RSCLK and RFS paths are for delay matching purposes and may not be necessary where path lengths are short.

This is one approach to using the SPORT interface for this ADC; there may be other solutions equal to this approach.

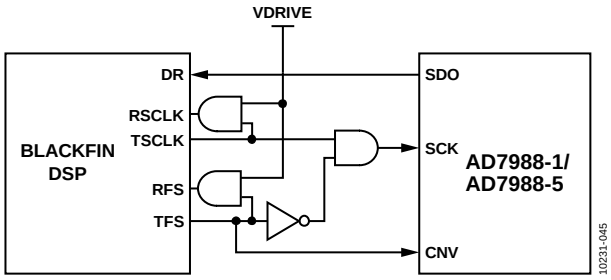


Figure 40. Evaluation Board Connection to Blackfin Sport Interface

LAYOUT

Design the printed circuit board (PCB) that houses the AD7988-1/AD7988-5 so that the analog and digital sections are separated and confined to certain areas of the board. The pinout of the AD7988-1/AD7988-5, with all the analog signals on the left side and all the digital signals on the right side, eases this task.

Avoid running digital lines under the device because these couple noise onto the die, unless a ground plane under the AD7988-1/AD7988-5 is used as a shield. Fast switching signals, such as CNV or clocks, should never run near analog signal paths. Avoid crossover of digital and analog signals.

Using at least one ground plane is recommended. The ground plane can be common or split between the digital and analog section. In the latter case, join the planes underneath the AD7988-1/AD7988-5 devices.

The AD7988-1/AD7988-5 voltage reference input, REF, has a dynamic input impedance. Decouple REF with minimal parasitic inductances by placing the reference decoupling ceramic capacitor close to, but ideally right up against, the REF and GND pins and connecting them with wide, low impedance traces.

Finally, decouple the power supplies of the AD7988-1/AD7988-5, VDD and VIO, with ceramic capacitors, typically 100 nF, placed close to the AD7988-1/AD7988-5 and connected using short and wide traces to provide low impedance paths and to reduce the effect of glitches on the power supply lines.

An example of a layout following these rules is shown in Figure 41 and Figure 42.

EVALUATING THE PERFORMANCE OF THE AD7988-1/AD7988-5

The evaluation board package for the AD7988-1/AD7988-5 (EVAL-AD7988-5SDZ) includes a fully assembled and tested evaluation board, documentation, and software for controlling the board from a PC via the EVAL-SDP-CB1Z.

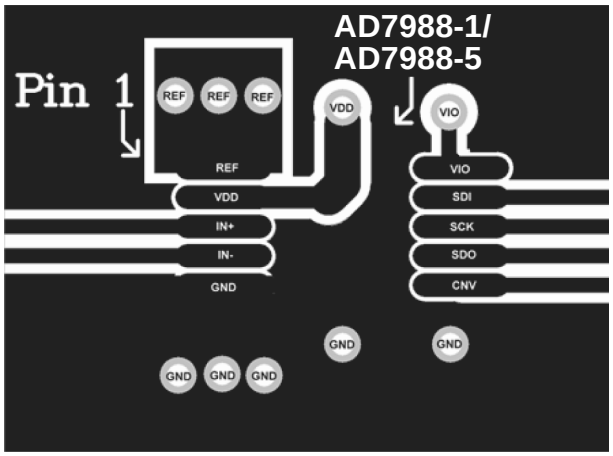


Figure 41. Example Layout of the AD7988-1/AD7988-5 (Top Layer)

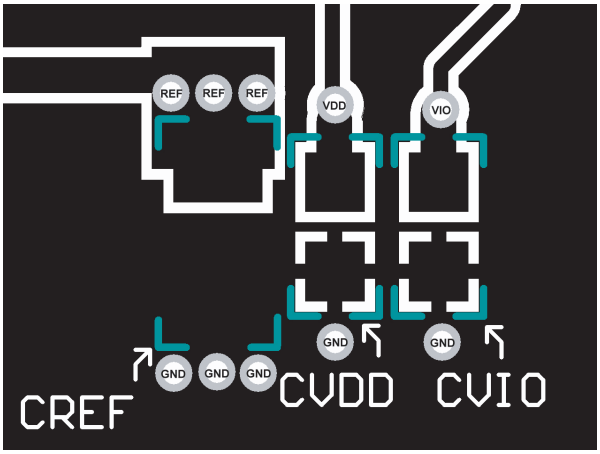
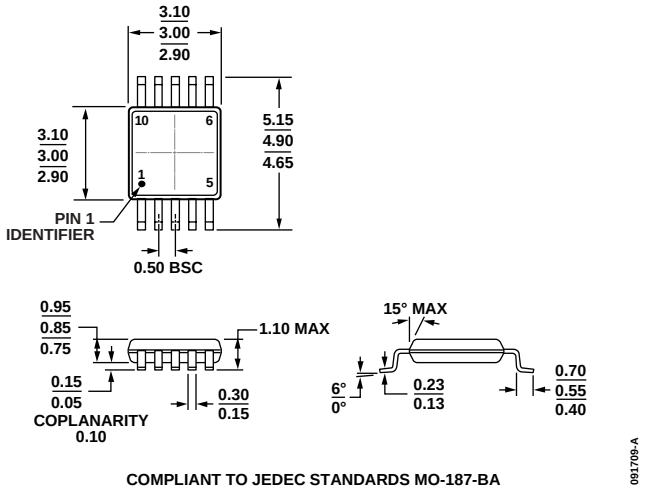


Figure 42. Example Layout of the AD7988-1/AD7988-5 (Bottom Layer)

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-187-BA

Figure 43.10-Lead Mini Small Outline Package [MSOP]
(RM-10)
Dimensions shown in millimeters

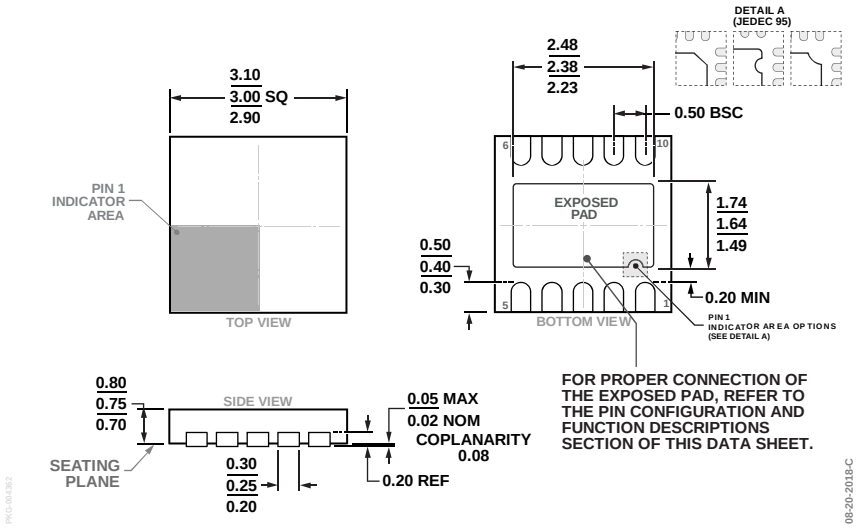


Figure 44. 10-Lead Lead Frame Chip Scale Package [LFCSP]
3 mm × 3 mm Body and 0.75 mm Package Height
(CP-10-9)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1, 2, 3]	Integral Nonlinearity	Temperature Range	Ordering Quantity	Package Description	Package Option	Branding
AD7988-1BRMZ	±1.25 LSB max	−40°C to +125°C	Tube, 50	10-Lead MSOP	RM-10	C7E
AD7988-1BRMZ-RL7	±1.25 LSB max	−40°C to +125°C	Reel, 1,000	10-Lead MSOP	RM-10	C7E
AD7988-1BCPZ-RL	±1.25 LSB max	−40°C to +125°C	Reel, 5,000	10-Lead LFCSP	CP-10-9	C7X
AD7988-1BCPZ-RL7	±1.25 LSB max	−40°C to +125°C	Reel, 1,500	10-Lead LFCSP	CP-10-9	C7X
AD7988-5BRMZ	±1.25 LSB max	−40°C to +125°C	Tube, 50	10-Lead MSOP	RM-10	C7Q
AD7988-5BRMZ-RL7	±1.25 LSB max	−40°C to +125°C	Reel, 1,000	10-Lead MSOP	RM-10	C7Q
AD7988-5BCPZ-RL	±1.25 LSB max	−40°C to +125°C	Reel, 5,000	10-Lead LFCSP	CP-10-9	C7Z
AD7988-5BCPZ-RL7	±1.25 LSB max	−40°C to +125°C	Reel, 1,500	10-Lead LFCSP	CP-10-9	C7Z
AD7988-5CCPZ-RL	±1.25 LSB max	−40°C to +125°C	Reel, 5,000	10-Lead LFCSP	CP-10-9	C8P
AD7988-5CCPZ-RL7	±1.25 LSB max	−40°C to +125°C	Reel, 1,500	10-Lead LFCSP	CP-10-9	C8P
EVAL-AD7988-5SDZ				Evaluation Board with the AD7988-5 Populated; Use for the Evaluation of both the AD7988-1 and the AD7988-5		
EVAL-SDP-CB1Z				System Demonstration Board; Used as a Controller Board for Data Transfer via USB Interface to PC		

[1] Z = RoHS Compliant Part.
[2] The EVAL-AD7988-5SDZ can be used as a standalone evaluation board or in conjunction with the EVAL-SDZ-CB1Z for evaluation and/or demonstration purposes.
[3] The EVAL-SDP-CB1Z allows a PC to control and communicate with all Analog Devices, Inc., evaluation boards ending in the SD designator.