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REVISION HISTORY

8/2017—Rev. H to Rev. I

Added Thermal Resistance Section and Table 3; Renumbered Sequentially	4
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10/2015—Rev. G to Rev. H

Changes to Table 3.....	4
Changes to Notes Section	4

8/2015—Rev. F to Rev. G

Changed NC to DNC.....	Throughout
Added Solder Heat Shift Parameter, Table 1	3
Added Table 3; Renumbered Sequentially	4
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12/2012—Rev. E to Rev. F

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5/2004—Rev. D to Rev. E

Updated Format.....	Universal
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1/2004—Rev. C to Rev. D

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5/2002—Rev. B to Rev. C

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SPECIFICATIONS

$T_A = 25^\circ\text{C}$, $V_{IN} = 5\text{ V}$, unless otherwise noted.

Table 1.

Parameter	AD780AN/AD780AR			AD780CR			AD780BN/AD780BR			Unit
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
OUTPUT VOLTAGE										
2.5 V Out	2.495		2.505	2.4985		2.5015	2.499		2.501	V
3.0 V Out	2.995		3.005	2.9950		3.0050	2.999		3.001	V
SOLDER HEAT SHIFT										
Mean		−1.1			−1.1			−1.1		mV
Sigma		0.4			0.4			0.4		mV
OUTPUT VOLTAGE DRIFT ¹										
−40°C to +85°C			7			7			3	ppm/°C
−55°C to +125°C			20			20				ppm/°C
LINE REGULATION										
2.5 V Output, $4\text{ V} \leq V_{IN} \leq 36\text{ V}$, T_{MIN} to T_{MAX}			10			10			10	μV/V
3.0 V Output, $4.5\text{ V} \leq V_{IN} \leq 36\text{ V}$, T_{MIN} to T_{MAX}			10			10			10	μV/V
LOAD REGULATION, SERIES MODE										
Sourcing $0\text{ mA} < I_{OUT} < 10\text{ mA}$			50			50			50	μV/mA
T_{MIN} to T_{MAX}			75			75			75	μV/mA
Sinking $-10\text{ mA} < I_{OUT} < 0\text{ mA}$			75			75			75	μV/mA
−40°C to +85°C			75			75			75	μV/mA
−55°C to +125°C			150			150			150	μV/mA
LOAD REGULATION, SHUNT MODE										
$I < I_{SHUNT} < 10\text{ mA}$			75			75			75	μV/mA
QUIESCENT CURRENT, 2.5 V SERIES MODE ²										
−40°C to +85°C		0.75	1.0		0.75	1.0		0.75	1.0	mA
−55°C to +125°C		0.8	1.3		0.8	1.3		0.8	1.3	mA
MINIMUM SHUNT CURRENT		0.7	1.0		0.7	1.0		0.7	1.0	mA
OUTPUT NOISE										
0.1 Hz to 10 Hz		4			4			4		μV p-p
Spectral Density, 100 Hz		100			100			100		nV/√Hz
LONG-TERM STABILITY ³		20			20			20		± ppm/1000 Hr
TRIM RANGE	4.0			4.0			4.0			± %
TEMPERATURE PIN										
Voltage Output @ 25°C	500	560	620	500	560	620	500	560	620	mV
Temperature Sensitivity		1.9			1.9			1.9		mV/°C
Output Resistance		3			3			3		kΩ
SHORT-CIRCUIT CURRENT TO GROUND		30			30			30		mA
TEMPERATURE RANGE										
Specified Performance (A, B, C)	−40		+85	−40		+85	−40		+85	°C
Operating Performance (A, B, C) ⁴	−55		+125	−55		+125	−55		+125	°C

¹ Maximum output voltage drift is guaranteed for all packages.

² 3.0 V mode typically adds 100 μA to the quiescent current. Also, I_q increases by 2 μA/V above an input voltage of 5 V.

³ The long-term stability specification is noncumulative. The drift in subsequent 1,000 hour periods is significantly lower than in the first 1,000 hour period.

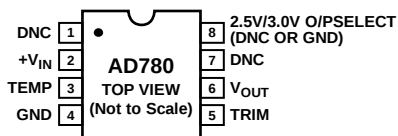
⁴ The operating temperature range is defined as the temperature extremes at which the device will still function. Parts may deviate from their specified performance outside their specified temperature range.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Values
+V _{IN} to Ground	36 V
TRIM Pin to Ground	36 V
TEMP Pin to Ground	36 V
Power Dissipation (25°C)	500 mW
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering 10 sec)	300°C
Output Protection	Output safe for indefinite short to ground and momentary short to V _{IN} .
ESD Classification	Class 1 (1000 V)

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.



NOTES
1. DNC = DO NOT CONNECT TO THIS PIN.

Figure 2. Pin Configuration, 8-Lead PDIP and SOIC Packages

THERMAL RESISTANCE

Thermal performance is directly linked to PCB design and operating environment. Careful attention to PCB thermal design is required.

Table 3. Thermal Resistance¹

Package Type	θ_{JA}	θ_{JC}^2	Unit
N-8	49.8	37.4	°C/W
R-8	160	36.8	°C/W

¹ Values in Table 3 are calculated based on standard JEDEC test conditions unless otherwise specified.

² 100um TIM is used for the θ_{JC} test. TIM is assumed to have 3.6 W/mK.

Table 4. Die Physical Characteristics

Parameter	Value	Units
Die Size	67 × 96	mil
Back Grind Thickness	10	mil
Bond Pad Opening Size	89 × 136	μm
Top Metal Composition	AlCu (0.5%)	%
Passivation	Oxynitride	
Polyimide	None	μm
Die Marker	780	
Substrate Bias	GND	V

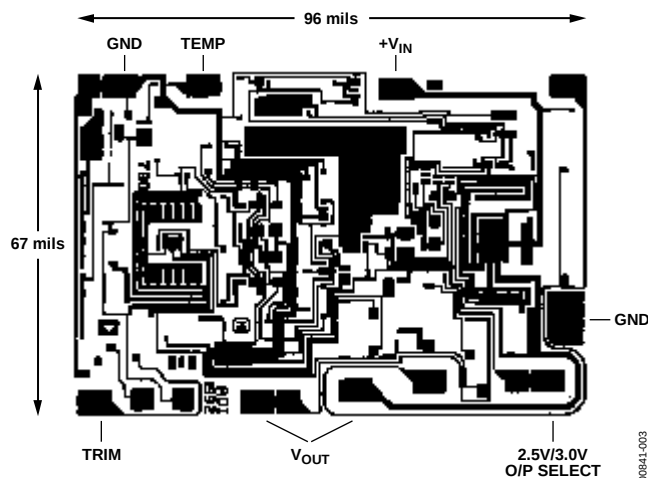


Figure 3. Die Layout

NOTES

Both V_{OUT} pads must be connected to the output.

Die Thickness: The standard thickness of Analog Devices, Inc. bipolar dice is 10 mil ± 1 mil.

Die Dimensions: The dimensions given are the maximum possible die size.

Backing: The standard backside surface is silicon (not plated). Analog Devices does not recommend gold-backed dice for most applications.

Edges: A diamond saw is used to separate wafers into dice, thus providing perpendicular edges halfway through the die. In contrast to scribed dice, this technique provides a more uniform die shape and size. The perpendicular edges facilitate handling (such as tweezer pickup), while the uniform shape and size simplify substrate design and die attach.

Top Surface: The standard top surface of the die is covered by a layer of passivation. All areas are covered except bonding pads and scribe lines.

Surface Metallization: The metallization to Analog Devices bipolar dice is aluminum/copper. The minimum thickness is 10,000 Å.

Bonding Pads: All bonding pads have a minimum size of 4.0 mil by 6.0 mil. The passivation windows have a minimum size of 3.5 mil by 5.3 mil.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

THEORY OF OPERATION

Band gap references are the high performance solution for low supply voltage and low power voltage reference applications. In this technique, a voltage with a positive temperature coefficient is combined with the negative coefficient of a transistor's V_{be} to produce a constant band gap voltage.

In the AD780, the band gap cell contains two NPN transistors (Q6 and Q7) that differ in emitter area by 12 $\times$. The difference in their V_{be} s produces a PTAT current in R5. This, in turn, produces a PTAT voltage across R4 that, when combined with the V_{be} of Q7, produces a voltage (V_{bg}) that does not vary with temperature. Precision laser trimming of the resistors and other patented circuit techniques are used to further enhance the drift performance.

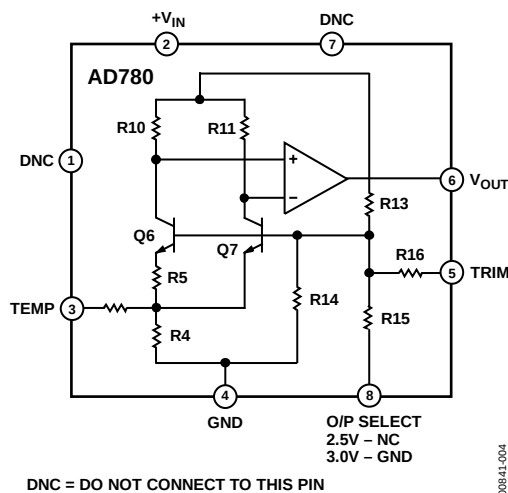


Figure 4. Schematic Diagram

The output voltage of the AD780 is determined by the configuration of Resistors R13, R14, and R15 in the amplifier's feedback loop. This sets the output to either 2.5 V or 3.0 V, depending on whether R15 (Pin 8) is grounded or not connected.

A unique feature of the AD780 is the low headroom design of the high gain amplifier, which produces a precision 3 V output from an input voltage as low as 4.5 V (or 2.5 V from a 4.0 V input). The amplifier design also allows the part to work with $+V_{IN} = V_{OUT}$ when current is forced into the output terminal. This allows the AD780 to work as a 2-terminal shunt regulator, providing a -2.5 V or -3.0 V reference voltage output without external components.

The PTAT voltage is also used to provide the user with a thermometer output voltage (at Pin 3) that increases at a rate of approximately 2 mV/ $^{\circ}$ C.

The DNC (Pin 7) of the AD780 is a 20 k Ω resistor to $+V_{IN}$ that is used solely for production test purposes. Users who are currently using the LT1019 self-heater pin (Pin 7) must take into account the different load on the heater supply.

APPLYING THE AD780

The AD780 can be used without any external components to achieve specified performance. If power is supplied to Pin 2 and Pin 4 is grounded, Pin 6 provides a 2.5 V or 3.0 V output depending on whether Pin 8 is left unconnected or grounded.

A bypass capacitor of 1 μF (+ V_{IN} to GND) should be used if the load capacitance in the application is expected to be greater than 1 nF. The AD780 in 2.5 V mode typically draws 700 μA of I_{q} at 5 V. This increases by $\sim 2 \mu\text{A/V}$ up to 36 V.

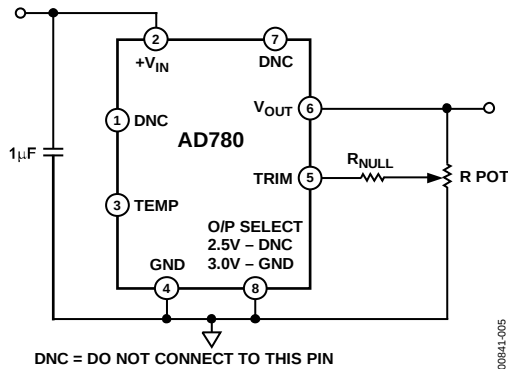


Figure 5. Optional Fine-Trim Circuit

Initial error can be nulled using a single 25 k Ω potentiometer connected between V_{OUT} , TRIM, and GND. This is a coarse trim with an adjustment range of 4%, and is only included here for compatibility purposes with other references. A fine trim can be implemented by inserting a large value resistor (e.g., 1 M Ω to 5 M Ω) in series with the wiper of the potentiometer (see Figure 5). The trim range, expressed as a fraction of the output, is simply greater than or equal to $2.1 \text{ k}\Omega/R_{\text{NULL}}$ for either the 2.5 V or 3.0 V mode.

The external null resistor affects the overall temperature coefficient by a factor equal to the percentage of V_{OUT} nulled.

For example, a 1 mV (0.03%) shift in the output caused by the trim circuit, with a 100 ppm/ $^{\circ}\text{C}$ null resistor, adds less than 0.06 ppm/ $^{\circ}\text{C}$ to the output drift ($0.03\% \times 200 \text{ ppm}/^{\circ}\text{C}$, since the resistors internal to the AD780 also have temperature coefficients of less than 100 ppm/ $^{\circ}\text{C}$).

NOISE PERFORMANCE

The impressive noise performance of the AD780 can be further improved, if desired, by adding two capacitors: a load capacitor (C_1) between the output and ground, and a compensation capacitor (C_2) between the TEMP pin and ground. Suitable values are shown in Figure 6.

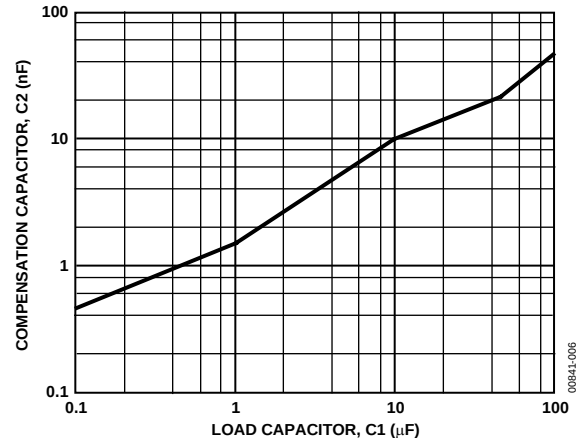


Figure 6. Compensation and Load Capacitor Combinations

C_1 and C_2 also improve the settling performance of the AD780 when subjected to load transients. The improvement in noise performance is shown in Figure 7, Figure 8, Figure 9, and Figure 10.

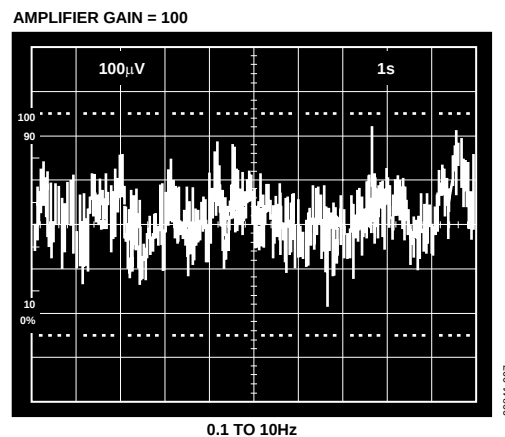


Figure 7. Standalone Noise Performance

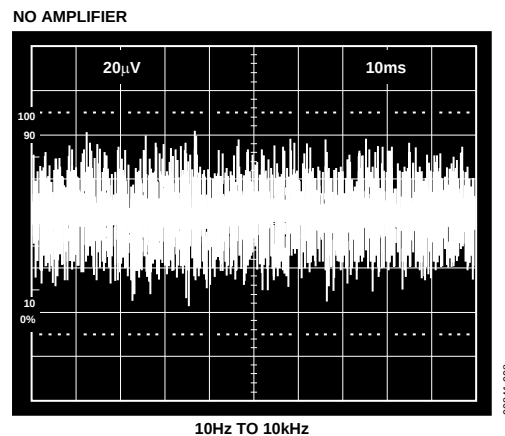


Figure 8. Standalone Noise Performance

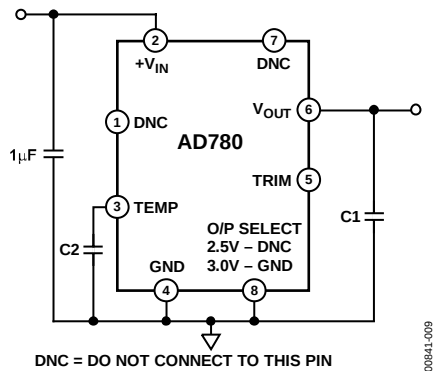


Figure 9. Noise Reduction Circuit

NOISE COMPARISON

The wideband noise performance of the AD780 can also be expressed in ppm. The typical performance with C1 and C2 is 0.6 ppm; without external capacitors, typical performance is 1.2 ppm.

This performance is, respectively, 7× and 3× lower than the specified performance of the LT1019.

NO AMPLIFIER

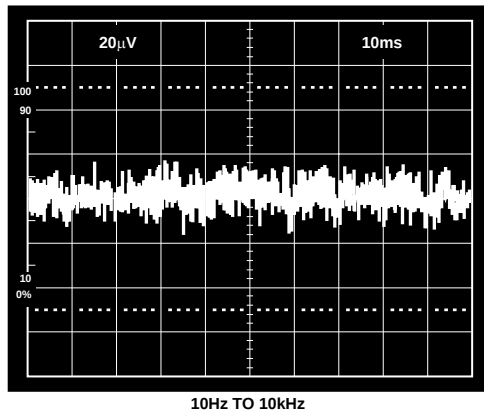


Figure 10. Reduced Noise Performance with C1 = 100 μF, C2 = 100 nF

TEMPERATURE PERFORMANCE

The AD780 provides superior performance over temperature by means of a combination of patented circuit design techniques, precision thin-film resistors, and drift trimming. Temperature performance is specified in terms of ppm/°C; because of nonlinearity in the temperature characteristic, the box test method is used to test and specify the part. The nonlinearity takes the form of the characteristic S-shaped curve shown in Figure 11. The box test method forms a rectangular box around this curve, enclosing the maximum and minimum output voltages over the specified temperature range. The specified drift is equal to the slope of the diagonal of this box.

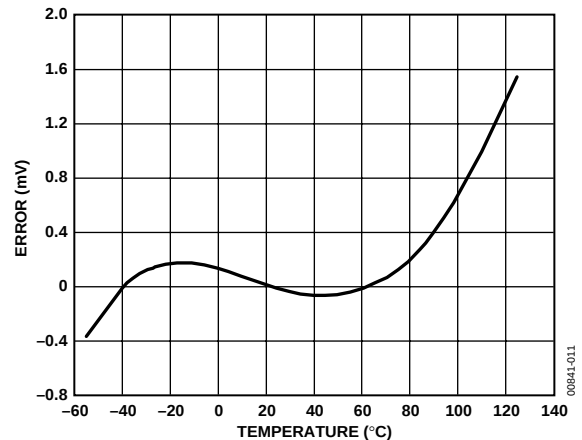


Figure 11. Typical AD780BN Temperature Drift

TEMPERATURE OUTPUT PIN

The AD780 provides a TEMP output (Pin 3) that varies linearly with temperature. This output can be used to monitor changes in system ambient temperature, and to initiate calibration of the system, if desired. The voltage V_{TEMP} is 560 mV at 25°C, and the temperature coefficient is approximately 2 mV/°C.

Figure 12 shows the typical V_{TEMP} characteristic curve over temperature taken at the output of the op amp with a noninverting gain of 5.

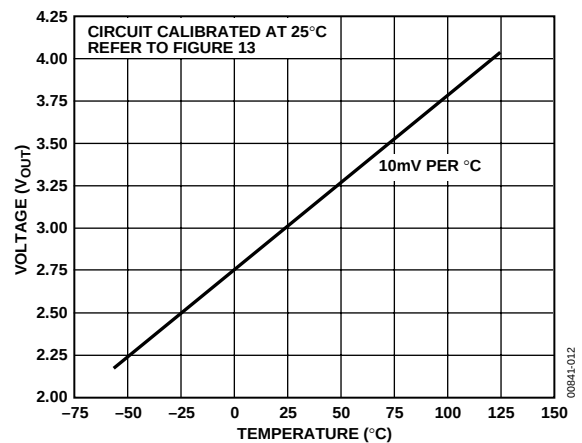


Figure 12. Temperature Pin Transfer Characteristic

Since the TEMP voltage is acquired from the band gap core circuit, current pulled from this pin has a significant effect on V_{OUT} . Care must be taken to buffer the TEMP output with a suitable op amp, for example, an OP07, AD820, or AD711 (all of which would result in less than a 100 μV change in V_{OUT}). The relationship between I_{TEMP} and V_{OUT} is

$$\Delta V_{OUT} = 5.8 \text{ mV}/\mu\text{A } I_{TEMP} \text{ (2.5 V Range)}$$

or

$$\Delta V_{OUT} = 6.9 \text{ mV}/\mu\text{A } I_{TEMP} \text{ (3.0 V Range)}$$

Notice how sensitive the current dependent factor on V_{OUT} is. A large amount of current, even in tens of microamps, drawn from the TEMP pin can cause the V_{OUT} and TEMP output to fail.

The choice of C1 and C2 was dictated primarily by the need for a relatively flat response that rolled off early in the high frequency noise at the output. However, there is considerable margin in the choice of these capacitors. For example, the user can actually put a huge C2 on the TEMP pin with none on the output pin. However, one must either put very little or a lot of capacitance at the TEMP pin. Intermediate values of capacitance can sometimes cause oscillation. In any case, the user should follow the recommendation in Figure 6.

TEMPERATURE TRANSDUCER CIRCUIT

The circuit shown in Figure 13 is a temperature transducer that amplifies the TEMP output voltage by a gain of a little over +5 to provide a wider full-scale output range. The digital potentiometer can be used to adjust the output so it varies by exactly 10 mV/°C.

To minimize resistance changes with temperature, resistors with low temperature coefficients, such as metal film resistors, should be used.

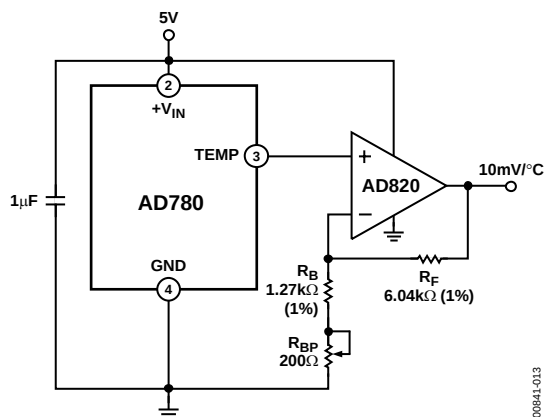


Figure 13. Differential Temperature Transducer

SUPPLY CURRENT OVER TEMPERATURE

The quiescent current of the AD780 varies slightly over temperature and input supply range. The test limit is 1 mA over the industrial and 1.3 mA over the military temperature range. Typical performance with input voltage and temperature variation is shown in Figure 14.

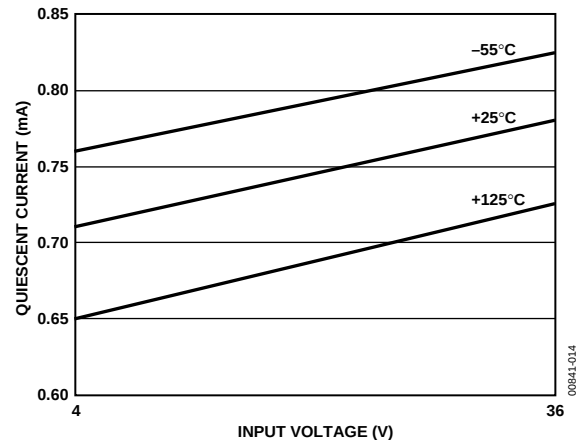


Figure 14. Typical Supply Current over Temperature

TURN-ON TIME

The time required for the output voltage to reach its final value within a specified error band is defined as the turn-on settling time. The two major factors that affect this are the active circuit settling time and the time for the thermal gradients on the chip to stabilize. Typical settling performance is shown in Figure 15. The AD780 settles to within 0.1% of its final value within 10 μs.

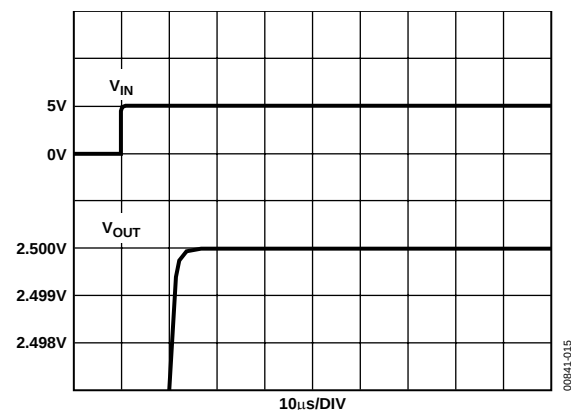


Figure 15. Turn-On Settling Time Performance

DYNAMIC PERFORMANCE

The output stage of the AD780 has been designed to provide superior static and dynamic load regulation.

Figure 16 and Figure 17 show the performance of the AD780 while driving a 0 mA to 10 mA load.

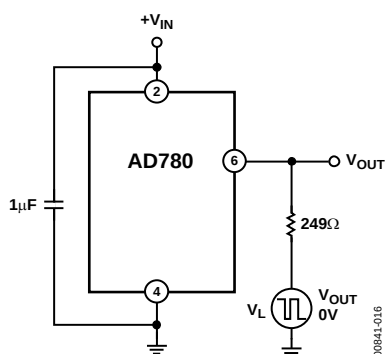


Figure 16. Transient Resistive Load Test Circuit

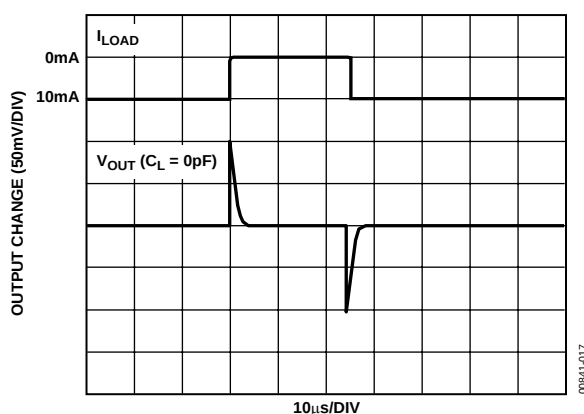


Figure 17. Settling Under Transient Resistive Load

The dynamic load may be resistive and capacitive. For example, the load may be connected via a long capacitive cable. Figure 18 and Figure 19 show the performance of the AD780 driving a 1000 pF, 0 mA to 10 mA load.

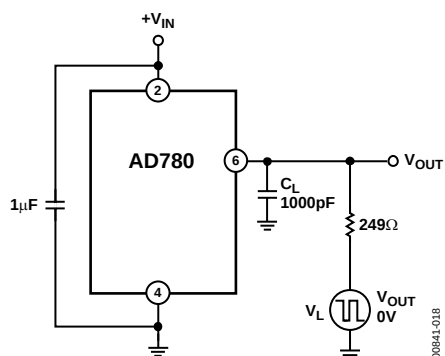


Figure 18. Capacitive Load Transient Response Test Circuit

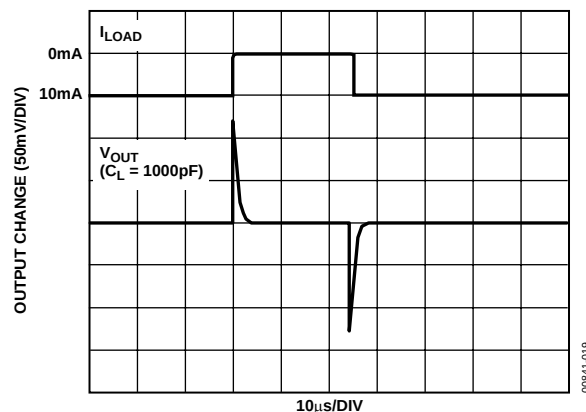


Figure 19. Settling under Dynamic Capacitive Load

LINE REGULATION

Line regulation is a measure of change in output voltage due to a specified change in input voltage. It is intended to simulate worst-case unregulated supply conditions and is measured in $\mu\text{V}/\text{V}$. Figure 20 shows typical performance with $4.0\text{ V} < V_{\text{IN}} < 15.0\text{ V}$.

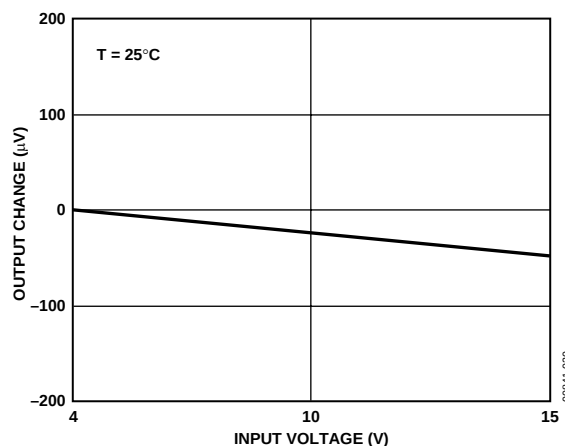


Figure 20. Output Voltage Change vs. Input Voltage

The [AD780](#) is ideally suited to be the reference for most 5 V high resolution ADCs. The [AD780](#) is stable under any capacitive load, has superior dynamic load performance, and its 3.0 V output provides the converter with the maximum dynamic range without requiring an additional and expensive buffer amplifier. One of the many ADCs that the [AD780](#) is suited for is the [AD7884](#), a 16-bit, high speed sampling ADC (see Figure 21). This part previously needed a precision 5 V reference, resistor divider, and buffer amplifier to do this function.



The [AD780](#) is also ideal for use with higher resolution converters, such as the [AD7710/AD7711/AD7712](#) (see Figure 22). While these parts are specified with a 2.5 V internal reference, the [AD780](#) in 3 V mode can be used to improve the absolute accuracy, temperature stability, and dynamic range. It is shown in Figure 22 with the two optional noise reduction capacitors.



4.5 V REFERENCE FROM 5 V SUPPLY

The circuit diagram shows a precision current source. The AD780 is configured with its non-inverting input (pin 3) connected to a voltage divider from V_{SUPPLY} (consisting of a $0.1\mu F$ capacitor and a $1k\Omega$ resistor) and to a feedback network (consisting of a $2.5k\Omega$ resistor and a $0.1\mu F$ capacitor) connected to the output. The inverting input (pin 4) is connected to ground through a $5k\Omega$ resistor and to the base of a 2N2907 transistor through a $4k\Omega$ resistor. The emitter of the transistor is connected to ground through a 0.01% resistor. The collector of the transistor is connected to V_{SUPPLY} and to the output node. The output node is also connected to ground through a $10\mu F$ capacitor and a 3.9Ω resistor. The output voltage is labeled V_{OUT} .

00841-023

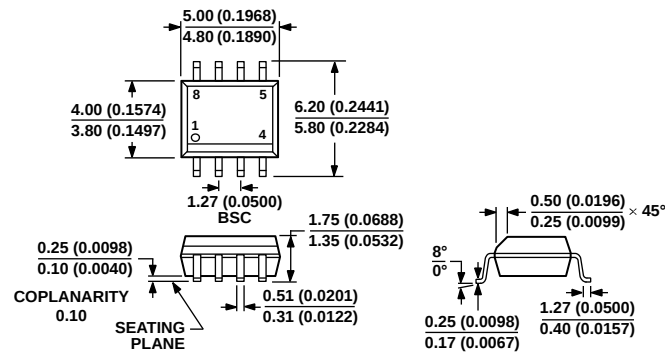
The [AD780](#) can produce a negative output voltage in shunt mode by connecting the input and output to ground, and connecting the GND pin of the [AD780](#) to a negative supply via a bias resistor, as shown in Figure 25.



A precise -2.5 V reference capable of supplying up to 100 mA to a load can be implemented with the [AD780](#) in series mode, using the bootstrap circuit shown in Figure 25.

Downloaded from [Arrow.com](https://www.arrow.com).

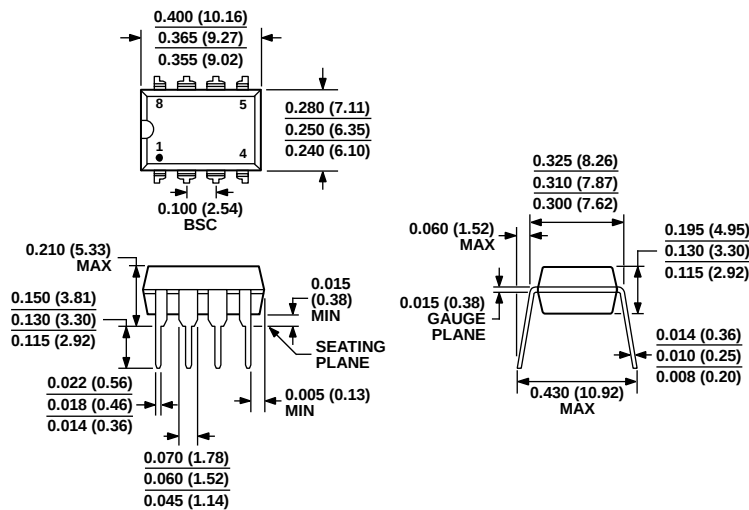
OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-012-AA
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
(IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

012407-A

Figure 26. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body (R-8)
Dimensions shown in millimeters and (inches)



COMPLIANT TO JEDEC STANDARDS MS-001
CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS
(IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.
CORNER LEADS MAY BE CONFIGURED AS WHOLE OR HALF LEADS.

070606-A

Figure 27. 8-Lead Plastic Dual-In-Line Package [PDIP]
Narrow Body
(N-8)
Dimensions shown in inches and (millimeters)

ORDERING GUIDE

Model ¹	Initial Error	Temperature Range	Temperature Coefficient	Package Description	Package Option	Qty. per Tube/Reel/Wafflepack
AD780ANZ	±5.0 mV	−40°C to +85°C	7 ppm/°C	8-Lead PDIP	N-8	50
AD780AR	±5.0 mV	−40°C to +85°C	7 ppm/°C	8-Lead SOIC_N	R-8	98
AD780AR-REEL7	±5.0 mV	−40°C to +85°C	7 ppm/°C	8-Lead SOIC_N	R-8	750
AD780ARZ	±5.0 mV	−40°C to +85°C	7 ppm/°C	8-Lead SOIC_N	R-8	98
AD780ARZ-REEL7	±5.0 mV	−40°C to +85°C	7 ppm/°C	8-Lead SOIC_N	R-8	750
AD780BNZ	±1.0 mV	−40°C to +85°C	3 ppm/°C	8-Lead PDIP	N-8	50
AD780BR	±1.0 mV	−40°C to +85°C	3 ppm/°C	8-Lead SOIC_N	R-8	98
AD780BR-REEL7	±1.0 mV	−40°C to +85°C	3 ppm/°C	8-Lead SOIC_N	R-8	750
AD780BRZ	±1.0 mV	−40°C to +85°C	3 ppm/°C	8-Lead SOIC_N	R-8	98
AD780BRZ-REEL	±1.0 mV	−40°C to +85°C	3 ppm/°C	8-Lead SOIC_N	R-8	2,500
AD780BRZ-REEL7	±1.0 mV	−40°C to +85°C	3 ppm/°C	8-Lead SOIC_N	R-8	750
AD780CRZ	±1.5 mV	−40°C to +85°C	7 ppm/°C	8-Lead SOIC_N	R-8	98
AD780CRZ-REEL7	±1.5 mV	−40°C to +85°C	7 ppm/°C	8-Lead SOIC_N	R-8	750
AD780-001C				DIE		165

¹ Z = RoHS Compliant Part.