AD768* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- AD768 Evaluation Board

DOCUMENTATION

Application Notes

- AN-414: Low Cost, Low Power Devices for HDSL Applications
- AN-912: Driving a Center-Tapped Transformer with a Balanced Current-Output DAC
- AN-932: Power Supply Sequencing

Data Sheet

- AD768: 16-Bit, 30 MSPS D/A Converter Data Sheet

REFERENCE MATERIALS

Solutions Bulletins & Brochures

- Digital to Analog Converters ICs Solutions Bulletin

DESIGN RESOURCES

- AD768 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all AD768 EngineerZone Discussions.

SAMPLE AND BUY

Visit the product page to see pricing options.

TECHNICAL SUPPORT

Submit a technical question or find your regional support number.

DOCUMENT FEEDBACK

Submit feedback for this data sheet.

AD768–SPECIFICATIONS

(T_{MIN} to T_{MAX}, V_{DD} = +5.0 V, V_{EE} = –5.0 V, LADCOM, REFCOM, DCOM = 0 V, IREFIN = 5 mA, CLOCK = 10 MHz, unless otherwise noted)

Parameter	Min	Typ	Max	Units
RESOLUTION	16			Bits
DC ACCURACY[1]				
Linearity Error				
T_A = +25°C	–8	±4	+8	LSB
T_{MIN} to T_{MAX}	–8		+8	LSB
Differential Nonlinearity				
T_A = +25°C	–6	±2	+6	LSB
T_{MIN} to T_{MAX}	–8		+8	LSB
Monotonicity (13-Bit)	GUARANTEED OVER RATED SPECIFICATION TEMPERATURE RANGE			
ANALOG OUTPUT				
Offset Error	–0.2		+0.2	% of FSR
Gain Error	–1.0		+1.0	% of FSR
Full-Scale Output Current[2]		20		mA
Output Compliance Range	–1.2		+5.0	V
Output Resistance	0.8	1.0	1.2	kΩ
Output Capacitance		3		pF
REFERENCE OUTPUT				
Reference Voltage	2.475	2.5	2.525	V
Reference Output Current[3]		+5.0	+15	mA
REFERENCE INPUT				
Reference Input Current	1	5	7	mA
Reference Bandwidth[4]				
Small Signal, IREF = 5 mA ± 0.1 mA		28		MHz
Large Signal, IREF = 4 mA ± 2 mA		9		MHz
TEMPERATURE COEFFICIENTS				
Unipolar Offset Drift	–5		+5	ppm of FSR/°C
Gain Drift[5]	–20		+20	ppm of FSR/°C
Gain Drift[6]	–40		+40	ppm of FSR/°C
Reference Voltage Drift	–30		+30	ppm/°C
DYNAMIC PERFORMANCE[7]				
Maximum Output Update Rate	30	40		MSPS
Output Settling Time (t_{ST}) (to 0.025%)		25	35	ns
Output Propagation Delay (t_{PD})		10		ns
Glitch Impulse		35		pV-s
Output Rise Time (10% to 90%)		5		ns
Output Fall Time (10% to 90%)		5		ns
Output Noise (DB0–DB15 High, into 50 Ω)		3		nV/√Hz
Differential Gain Error		0.01		%
Differential Phase Error		0.01		Degree
DIGITAL INPUTS				
Logic “1” Voltage	3.5			V
Logic “0” Voltage			1.5	V
Logic “1” Current	–10		+10	μA
Logic “0” Current	–10		+10	μA
Input Capacitance		10		pF
Input Setup Time (t_S)	10			ns
Input Hold Time (t_H)	5			ns
Latch Pulse Width (t_{LPW})	10			ns
AC LINEARITY[7]				
Spurious-Free Dynamic Range (SFDR Within a Window)				
F_{OUT} = 1.002 MHz; CLOCK = 10 MHz; 2 MHz Span		86	79	dB
F_{OUT} = 1.002 MHz; CLOCK = 20 MHz; 2 MHz Span		85		dB
F_{OUT} = 5.002 MHz; CLOCK = 30 MHz; 10 MHz Span		78		dB
Spurious-Free Dynamic Range (SFDR to Nyquist)				
F_{OUT} = 1.002 MHz; CLOCK = 10 MHz		74	70	dB
F_{OUT} = 1.002 MHz; CLOCK = 20 MHz		73		dB
F_{OUT} = 5.002 MHz; CLOCK = 30 MHz		67		dB
Total Harmonic Distortion (THD)				
F_{OUT} = 1.002 MHz; CLOCK = 10 MHz		–71	–68	dB
F_{OUT} = 1.002 MHz; CLOCK = 20 MHz		–66		dB
F_{OUT} = 5.002 MHz; CLOCK = 30 MHz		–61		dB

Parameter	Min	Typ	Max	Units
POWER SUPPLY				
Positive Voltage Range	4.75	5	5.25	V
Negative Voltage Range	–5.25	–5	–4.75	V
Positive Supply Current		30	40	mA
Negative Supply Current		63	73	mA
Nominal Power Dissipation		465	600	mW
Power Supply Rejection Ratio (PSRR)	–0.2		+0.2	% of FSR/V
OPERATING RANGE	–40		+85	°C

NOTES
[1]Measured at IOUTA, driving a virtual ground.
[2]Nominal FS output current is 4× the current at IREFIN. Therefore, nominal FS current is 20 mA when IREFIN = 5 mA.
[3]Output current is defined as total current available for IREFIN and any external load.
[4]Reference bandwidth is a function of external cap at NR pin. Refer to compensation section of data sheet for details.
[5]Excludes internal reference drift.
[6]Includes internal reference drift.
[7]Measured as unbuffered voltage output (1 V range) with FS current into 50 Ω load at IOUTB.
Specifications subject to change without notice.

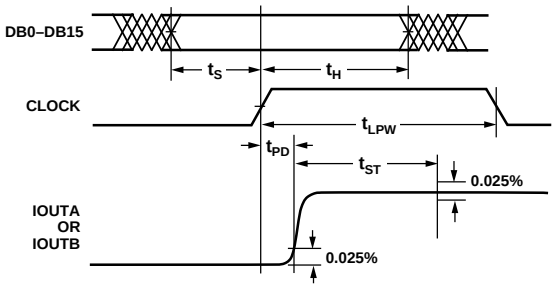
ABSOLUTE MAXIMUM RATINGS*

Parameter	with Respect to	Min	Max	Units
Positive Supply Voltage (V_{DD})	DCOM, REFCOM, LADCOM	–0.5	+6.0	V
Negative Supply Voltage (V_{EE})	DCOM, REFCOM, LADCOM	–6.0	+0.5	V
Analog-to-Other Grounds (REFCOM)	DCOM, LADCOM	–0.5	+0.5	V
Digital-to-Other Grounds (DCOM)	LADCOM, REFCOM	–0.5	+0.5	V
Reference Output (REFOUT)	REFCOM		V_{DD} + 0.5	V
Reference Input Current (IREFIN)			+7.5	mA
Digital Inputs (DB0–DB15, CLOCK)	DCOM	–0.5	V_{DD} + 0.5	V
Analog Outputs (IOUTA, IOUTB)	LADCOM	–2.0	+5.0	V
Maximum Junction Temperature			+150	°C
Storage Temperature		–65	+150	°C
Lead Temperature			+300	°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating for extended periods may affect device reliability.

ORDERING GUIDE

Model	Package Description	Package Option
AD768AR	28-Pin 300 mil SOIC	R-28
AD768ACHIPS	Die	
AD768-EB	AD768 Evaluation Board	



Timing Diagram

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD768 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

WAFER TEST LIMITS[1] (T_A = +25°C, V_{DD} = +5.0 V, V_{EE} = –5.0 V, I_{REFIN} = 5 mA, unless otherwise noted)

Parameter	AD768ACHIPS Limit	Units
Integral Nonlinearity[2]	±8	LSB max
Differential Nonlinearity[2]	±6	LSB max
Offset Error	±0.2	% FSR max
Gain Error	±1.0	% FSR max
Reference Voltage	±1.0	% of nom. 2.5 V max
Positive Supply Current	40	mA max
Negative Supply Current	73	mA max
Power Dissipation	600	mW max

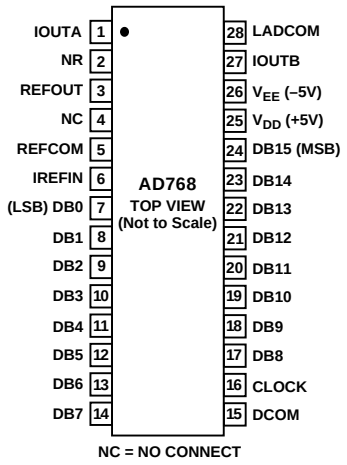
NOTES
[1]Electrical test are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice.
[2]Limits extrapolated from testing of individual bit errors.
[3]Die offers latch control pad. Edge triggered latches become level triggered when latch control and clock pads are high.
[4]Die substrate is connected to V_{EE}.

PIN DESCRIPTIONS

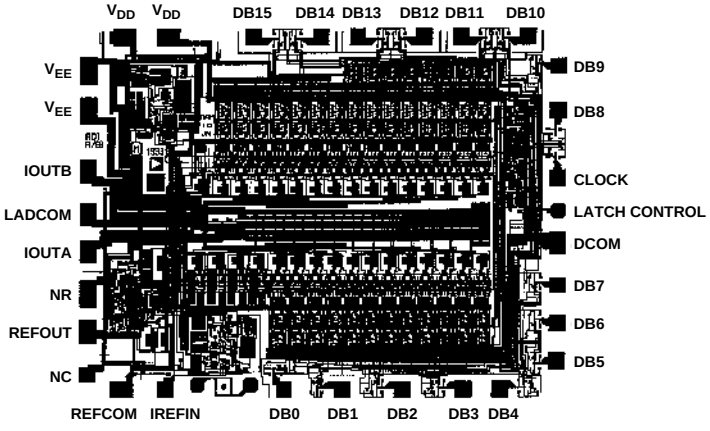
Pin No.	Symbol	Type	Name and Function
1	IOUTA	AO	DAC Current Output. Full-scale current when all data bits are 1s.
2	NR	AI	Noise Reduction Node. Add capacitor for noise reduction.
3	REFOUT	AO	Reference Output Voltage. Nominal value is 2.5 V.
4	NC	NC	No Connect. Reserved for internal use.
5	REFCOM	P	Reference Ground.
6	IREFIN	AI	Reference Input Current. Nominal is 5 mA. DAC full-scale is 4× this current.
7	DB0	DI	Data Bit 0 (LSB).
8–14	DB1–DB7	DI	Data Bits 1–7.
15	DCOM	P	Digital Ground.
16	CLOCK	DI	Clock Input. Data latched on positive edge of clock.
17–23	DB8–DB14	DI	Data Bits 8–14.
24	DB15	DI	Data Bit 15 (MSB).
25	V_{DD}	P	Positive Supply Voltage. Nominal is +5 V.
26	V_{EE}	P	Negative Supply Voltage. Nominal is –5 V.
27	IOUTB	AO	Complementary DAC Current Output. Full-scale current when all data bits are 0s.
28	LADCOM	P	DAC Ladder Common.

Type: AI = Analog Input; DI = Digital Input; AO = Analog Output; P = Power.

PIN CONFIGURATION



DICE CHARACTERISTICS[3, 4]



Die Size:
0.1106 × 0.1417 inch, 15,672 sq. mils
(2.81 × 3.60 mm, 10.116 sq. mm)

DEFINITIONS OF SPECIFICATIONS

Linearity Error (Also Called Integral Nonlinearity or INL)
Linearity error is defined as the maximum deviation of the actual analog output from the ideal output, determined by a straight line drawn from zero to full scale.

Differential Nonlinearity (or DNL)
DNL is the measure of the variation in analog value, normalized to full scale, associated with a 1 LSB change in digital input code.

Monotonicity
A D/A converter is monotonic if the output either increases or remains constant as the digital input increases.

Offset Error
The deviation of the output current from the ideal of zero is called offset error. For IOUTA, 0 mA output is expected when the inputs are all 0s. For IOUTB, 0 mA output is expected when all inputs are set to 1s.

Gain Error
The difference between the actual and ideal output span. The actual span is determined by the output when all inputs are set to 1s minus the output when all inputs are set to 0s. The ideal output current span is 4× the current applied to the IREFIN pin.

Output Compliance Range
The range of allowable voltage at the output of a current-output DAC. Operation beyond the maximum compliance limits may cause either output stage saturation or breakdown, resulting in nonlinear performance.

Temperature Drift
Temperature drift is specified as the maximum change from the ambient (+25°C) value to the value at either T_{MIN} or T_{MAX}. For offset and gain drift, the drift is reported in ppm of full-scale range (FSR) per degree C. For reference drift, the drift is reported in ppm per degree C.

Power Supply Rejection
The maximum change in the full-scale output as the supplies are varied from nominal to minimum and maximum specified voltages.

Settling Time
The time required for the output to reach and remain within a specified error band about its final value, measured from the start of the output transition.

Spurious-Free Dynamic Range
The difference, in dB, between the rms amplitude of the input signal and the peak spurious signal over the specified bandwidth.

Total Harmonic Distortion
THD is the ratio of the rms sum of the first six harmonic components to the rms value of the measured input signal. It is expressed as a percentage or in decibels (dB).

Glitch Impulse
Asymmetrical switching times in a DAC give rise to undesired output transients which are quantified by a glitch impulse. It is specified as the net area of the glitch in pV-sec.

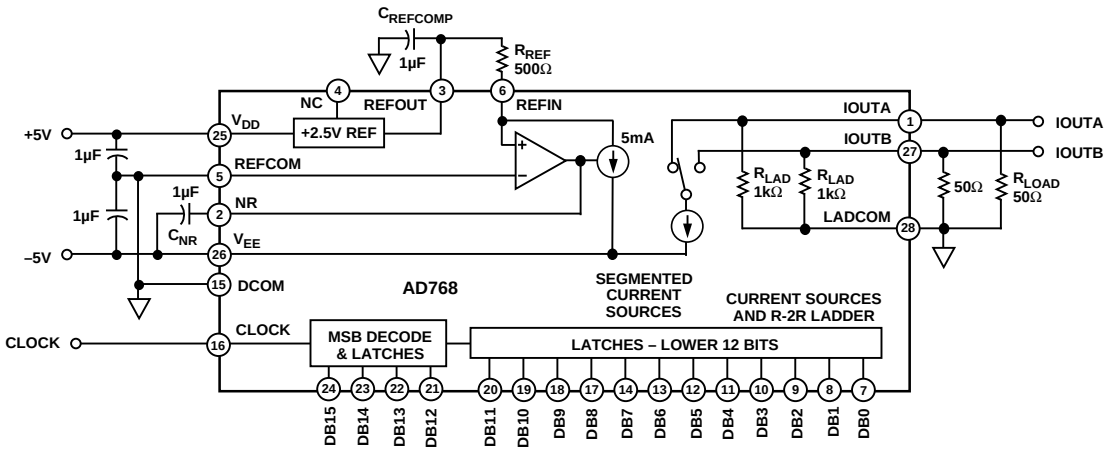


Figure 1. Functional Block Diagram and Basic Hookup

FUNCTIONAL DESCRIPTION

The AD768 is a current-output DAC with a nominal full-scale current of 20 mA and a 1 kΩ output impedance. Differential outputs are provided to support single-ended or differential applications. The DAC architecture combines segmented current sources for the top four bits (MSBs) and a 1 kΩ R-2R ladder for the lower 12 bits (LSBs). The DAC current sources are implemented with laser-trimmable thin film resistors for excellent dc linearity. A proprietary switching technique is utilized to reduce glitch energy and maximize dynamic accuracy.

The digital interface offers CMOS compatible edge-triggered input latches that interface readily to CMOS logic and supports clock rates up to 40 MSPS. A temperature compensated 2.5 V bandgap reference is integrated on-chip to drive the AD768 reference input current with the use of a single external resistor. The functional block diagram in Figure 1 is a simple representation of the internal circuitry to aid the understanding of the AD768's operation. The DAC transfer function is described, and followed by a detailed description of each key portion of the circuit. Typical circuit configurations are shown in the section APPLYING THE AD768.

DAC TRANSFER FUNCTION

The AD768 may be used in either current-output mode with the output connected to a virtual ground, or voltage-output mode with the output connected to a resistive load.

In current output mode,

$$I_{OUT} = (DAC\ CODE/65536) \times (I_{REFIN} \times 4)$$

In voltage output mode,

$$V_{OUT} = I_{OUT} \times R_{LOAD} \| R_{LAD}$$

where:

DAC CODE is the decimal representation of the DAC inputs; an integer between 0 and 65535.

I_{REFIN} is the current applied at the IREFIN pin, determined by V_{REF}/R_{REF}.

Substituting for I_{OUT} and I_{REFIN},

$$V_{OUT} = -V_{REF} \times (DAC\ CODE/65536) \times 4 \times [(R_{LOAD} \| R_{LAD})/R_{REF}]$$

These equations clarify an important aspect of the AD768 transfer function; the full-scale current output of the DAC is proportional to a current input. The voltage output is then a function of the ratio of $(R_{LOAD} \| R_{LAD})/R_{REF}$, allowing for cancellation of resistor drift by selection of resistors with matched characteristics.

REFERENCE INPUT

The IREFIN pin is a current input node with low impedance to REFCOM. This input current sets the magnitude of the DAC current sources such that the full-scale output current is exactly four times the current applied at IREFIN. For the nominal input current of 5 mA, the nominal full-scale output current is 20 mA.

The 5 mA reference input current can be generated from the on-chip 2.5 V reference with an external resistor of 500 Ω from REFOUT to IREFIN. If desired, a variety of external reference voltages may be used based on the selection of an appropriate resistor. However, to maintain stability of the reference amplifier, the external impedance at IREFIN must be kept below 1 kΩ.

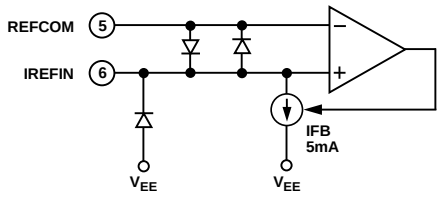


Figure 2. Equivalent Reference Input Circuit

The I_{REFIN} current can be varied from 1 mA to 7 mA which subsequently will result in a proportional change in the DAC full-scale. Since the operating currents within the DAC vary with I_{REFIN}, so does the power dissipation. Figure 3 illustrates that relationship.

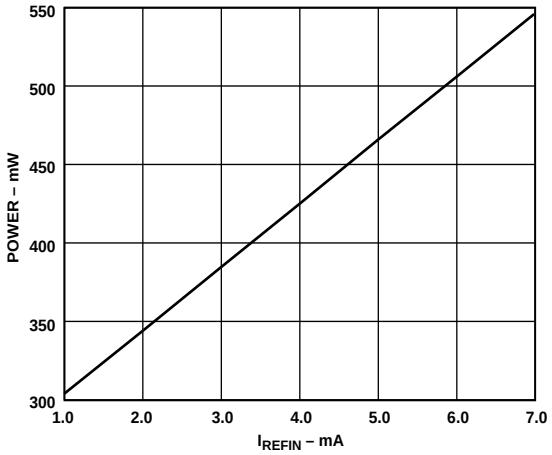


Figure 3. Power Dissipation vs. I_{REFIN} Current

Note the AD768 is optimized for operation at an input current of 5 mA. Both linearity and dynamic performance at other input currents may be somewhat degraded. Figure 4 shows typical dc linearity over a range of input currents. Figure 5 shows typical SFDR (to Nyquist) performance over a range of input currents and CLOCK input rates for a 1 MHz output frequency.

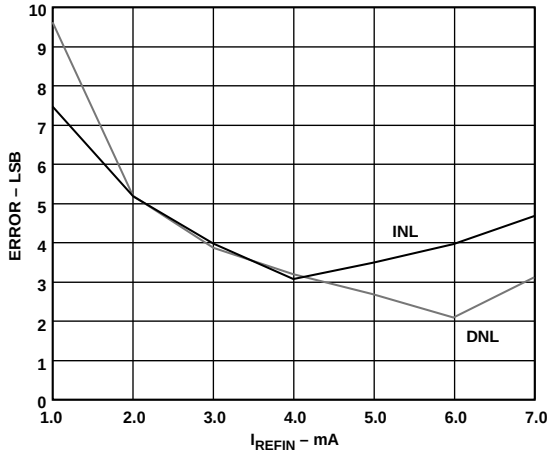


Figure 4. INL/DNL vs. I_{REFIN} Current

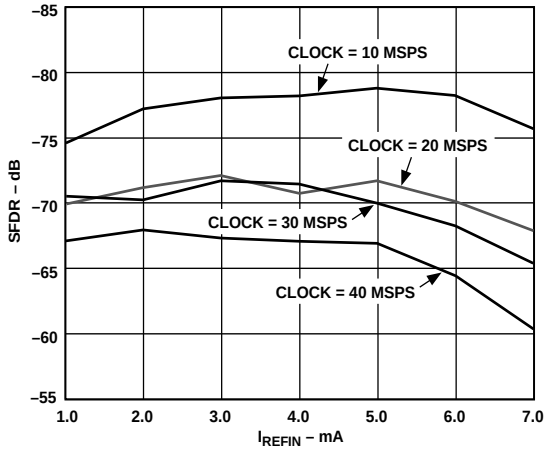


Figure 5. SFDR (to Nyquist) vs. I_{REFIN} @ F_{OUT} = 1 MHz

REFERENCE OUTPUT

The internal 2.5 V bandgap reference is provided for generation of the I_{REFIN} current, and must be compensated externally with a capacitor of 0.1 µF or greater from REFOUT to REFCOM. If an external reference is used, REFOUT should be tied directly to the positive supply voltage, V_{DD}. This effectively turns off the internal reference, eliminating the need for the external capacitor at REFOUT. The reference is specified to drive a nominal load of 5 mA with a maximum of 15 mA. Operation with a heavier load will result in degradation of supply rejection and reference voltage accuracy. Therefore, the reference output should be buffered with an amplifier when additional load current is required. A properly sized pull-up resistor can also be used to source additional current to the load. The resistors value should be selected such that REFOUT will always source a minimum of 5 mA to IREFIN and the additional load.

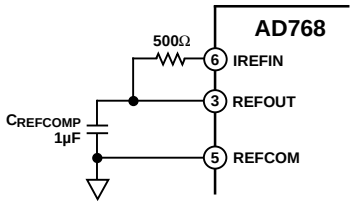


Figure 6. Typical Reference Hookup

TEMPERATURE CONSIDERATIONS

Note that the reference plays a key role in the overall temperature performance of the AD768. Any drift of I_{REFIN} shows up directly in I_{OUT}. When the output is taken as a current, the drift of I_{REFIN} (which depends on both V_{REF} and R_{REF}) must be minimized. This can be done by using the internal temperature compensated reference for V_{REF} and a low temperature coefficient resistor for R_{REF}. If the output is taken as a voltage, it is a function of a resistor ratio, not an absolute resistor value. By selecting resistors with matched temperature coefficients for R_{REF} and R_{LOAD}, the drift in the resistor values will cancel, providing optimal drift performance.

REFERENCE NOISE REDUCTION AND MULTIPLYING BANDWIDTH

For application flexibility and multiplying capabilities, the reference amplifier is designed to offer adjustable bandwidth that can be reduced by connecting an external capacitor from the NR node to the negative supply pin, V_{EE}. This capacitor limits the bandwidth and acts as a filter to reduce the noise contribution from the reference amplifier.

The noise reduction capacitor, C_{NR}, is not required for stability and does not affect the settling time of the DAC output. Without this capacitor, the I_{REFIN} bandwidth is 15 MHz allowing high frequency modulation of the DAC full-scale range through the reference input node. Figure 7 shows the relationship between the external noise reduction capacitor and the –3 dB bandwidth of the reference amplifier.

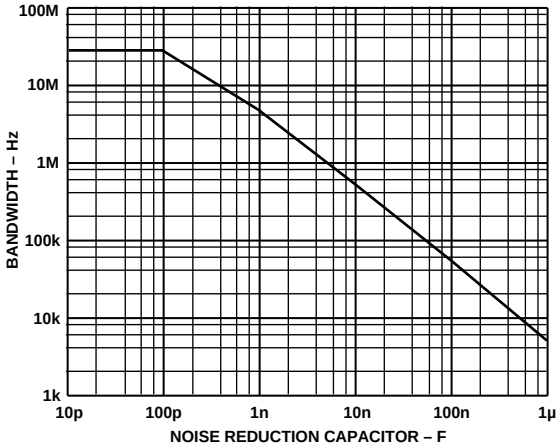


Figure 7. External Noise Reduction Capacitor vs. –3 dB Bandwidth

The sensitivity of the NR node requires that care be taken in capacitor placement. The capacitor should be located as physically close to the package pins as possible and lead lengths should be minimized. For this purpose, the use of a chip capacitor is recommended. For applications that do not require high frequency modulation at IREFIN, it is recommended that a capacitor on the order of 1 µF be connected from NR to V_{EE}. If the reference input is purely dc, noise may be minimized with multiple capacitors, such as 1 µF and 0.1 µF, to more effectively filter both high and low frequency disturbances.

ANALOG OUTPUTS

The AD768 offers two analog outputs; IOUTA is trimmed for optimal INL and DNL performance and has a full-scale output when all bits are high. For applications that require the specified dc accuracy, IOUTA should be used. IOUTB is the complementary output with full-scale output when all bits are low. Both IOUTA and IOUTB provide similar dynamic performance. Refer to Figures 8 and 9 for typical INL and DNL performance curves. The outputs can also be used differentially. Refer to the section “Applying the AD768” for examples of various output configurations.

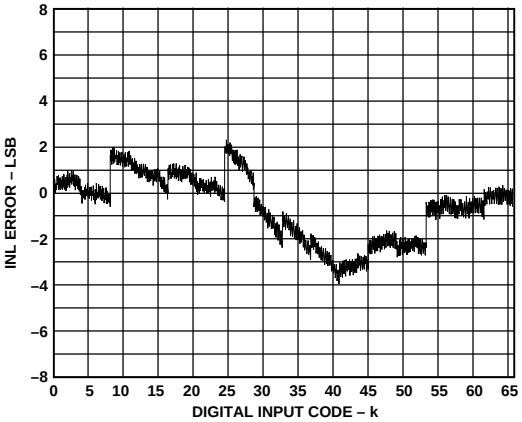


Figure 8. Typical INL Performance

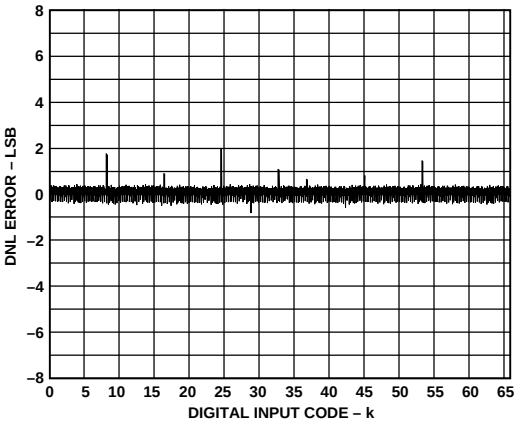


Figure 9. Typical DNL Performance

The outputs have a compliance range of –1.2 V to +5.0 V with respect to LADCOM. The current steering output stages will remain functional over this range. Operation beyond the maximum compliance limits may cause either output stage saturation or breakdown, resulting in nonlinear performance. The rated dc and ac performance specifications are for an output voltage of 0 V to –1 V.

The current in LADCOM is proportional to I_{REFIN} and has been carefully configured to be independent of digital code when the output is connected to a virtual ground. This minimizes any detrimental effects of ladder ground resistance on linearity. For optimal dc linearity, IOUTA should be connected directly to a virtual ground, and IOUTB should be grounded. An example of this configuration is provided in the section "Buffered Voltage Output." If IOUTA is driving a resistive load directly, then IOUTB should be terminated with an equal impedance. This will ensure the current in LADCOM remains constant with digital code, and is recommended for improved dc linearity in the unbuffered voltage output configuration.

As shown in Figure 10, there is an equivalent output impedance of 1 kΩ in parallel with 3 pF at each output terminal. If the output voltage deviates from the ladder common voltage, an error current flows through this 1 kΩ impedance. This is a linear effect which does not change with input code, so it appears as a gain error. With 50 Ω output termination, the resulting gain error is approximately –5%. An example of this configuration is provided in the section Unbuffered Voltage Output.

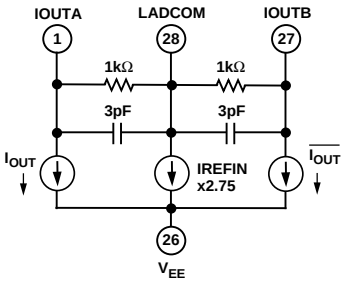


Figure 10. Equivalent Analog Output Circuit

DIGITAL INPUTS

The AD768 digital inputs consist of 16 data input pins and a clock pin. The 16-bit parallel data inputs follow standard positive binary coding, where DB15 is the most significant bit (MSB) and DB0 is the least significant bit (LSB). IOUTA produces full-scale output current when all data bits are at logic 1. IOUTB is the complementary output, with full-scale when all data bits are at logic 0. The full-scale current is split between the two outputs as a function of the input code.

The digital interface is implemented using an edge-triggered master slave latch. The DAC output is updated following the rising edge of the clock, and is designed to support a clock rate as high as 40 MSPS. The clock can be operated at any duty cycle that meets the specified minimum latch pulse width. The setup and hold times can also be varied within the clock cycle as long as the specified minimums are met, although the location of these transition edges may affect digital feedthrough. The digital inputs are CMOS compatible with logic thresholds set to approximately half the positive supply voltage. The small input current requirements allow for easy interfacing to unbuffered CMOS logic. Figure 11 shows the equivalent digital input circuit.

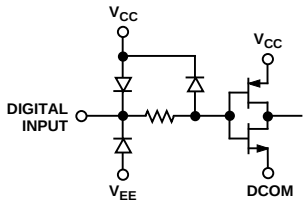


Figure 11. Equivalent Digital Input Circuit

Digital input signals to the DAC should be isolated from the analog output as much as possible. Interconnect distances to the DAC inputs should be kept as short as possible. Termination resistors may improve performance if the digital lines become too long. To minimize digital feedthrough, the inputs should be free from glitches and ringing, and may be further improved with a reduction of edge speed.

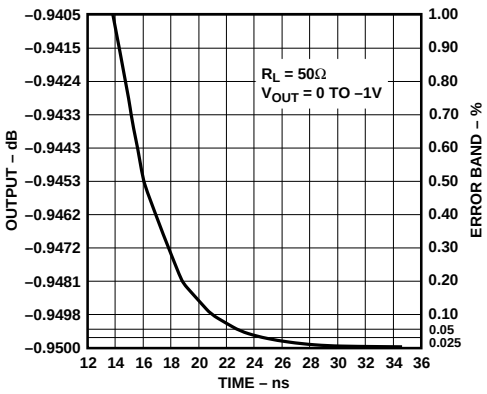


Figure 12. Settling Time

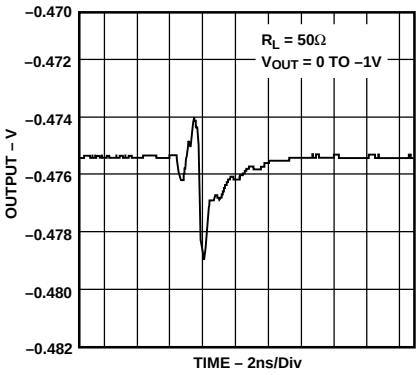


Figure 13. Glitch Impulse at Major Carry

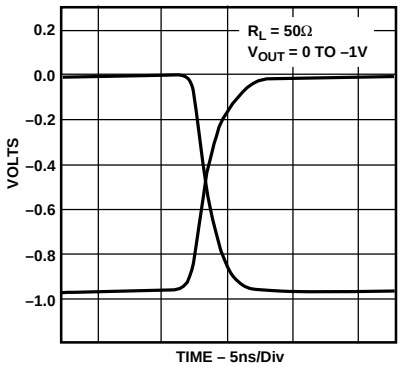


Figure 14. Rise and Fall Characteristics

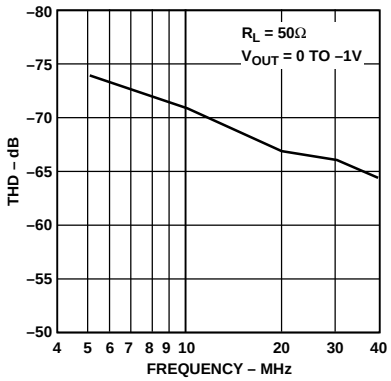


Figure 15. THD vs. Clock Frequency at F_{OUT} = 1 MHz

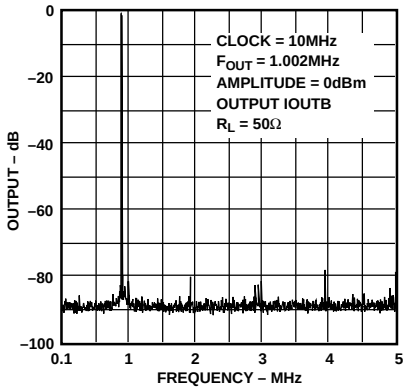


Figure 16. Typical Spectral Performance

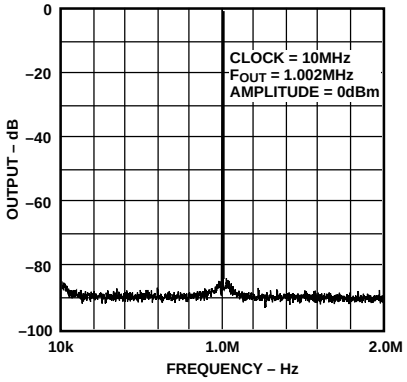


Figure 17. Typical SFDR (With a Window)

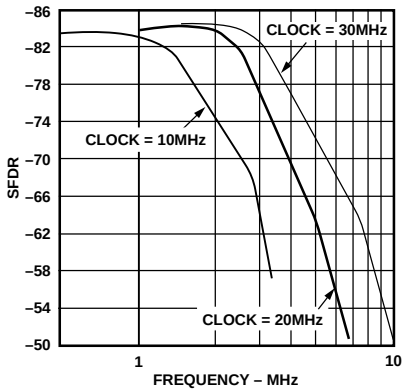


Figure 18. SFDR (Within a Window) vs. F_{OUT}

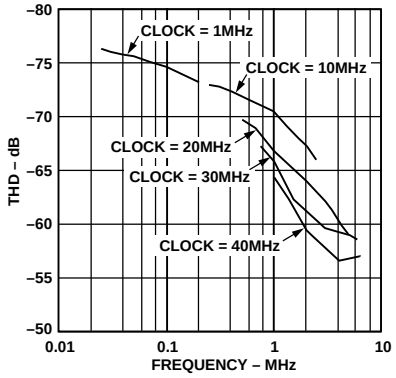


Figure 19. THD vs. F_{OUT}

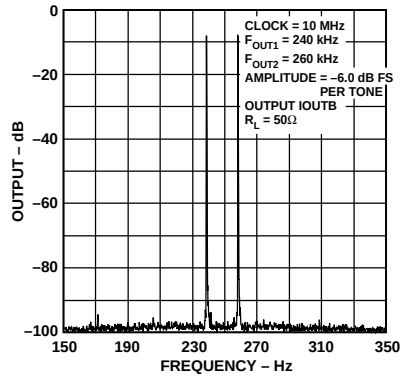


Figure 20. Intermodulation Distortion

APPLYING THE AD768

OUTPUT CONFIGURATIONS

The following sections illustrate some typical output configurations for the AD768. While most figures take the output at IOUTA, IOUTB can be interchanged in all cases. Unless otherwise noted, it is assumed that I_{REFIN} and full-scale currents are set to nominal values.

For application that require the specified dc accuracies, proper resistor selection is required. In addition to absolute resistor tolerances, resistor self-heating can result in unexpected errors. For optimal INL, the buffered voltage output is recommended as shown in Figure 23. In this configuration, self-heating of R_{FB} may cause a change in gain, producing a bow in the INL curve. This effect can be minimized by selection of a low temperature coefficient resistor.

UNBUFFERED VOLTAGE OUTPUT CONFIGURATIONS

Figure 21 shows the AD768 configured to provide a unipolar output range of approximately 0 V to –1 V. The nominal full-scale current of 20 mA flows through the parallel combination of the 50 Ω R_L resistor and the 1 kΩ DAC output resistance (from the R-2R ladder), for a combined 47.6 Ω. This produces an ideal full-scale voltage of –0.952 V with respect to LADCOM. In addition, the 1 kΩ DAC output resistance has a tolerance of ±20% which may vary the full-scale gain by ±1%. This linear variation results in a gain error which can be easily compensated for by adjusting I_{REFIN}.

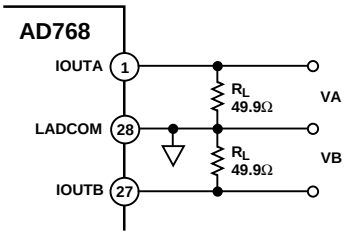


Figure 21. 0 V to –1 V Unbuffered Voltage Output

In this configuration, it is important to note the restrictions from the output compliance limits. The maximum negative voltage compliance is –1.2 V, prohibiting use of a 100 Ω load to produce a 0 V to –2 V output swing. One additional consideration for operation in this mode is integral nonlinearity. As the voltage at the output node changes, the finite output impedance of the DAC current steering switches gives rise to small changes in the output current that vary with output voltage, producing a bow (up to 8 LSBs) in the INL. For optimal INL performance, the buffered voltage output mode is recommended.

The INL is also slightly dependent on the termination of the unused output (IOUTB) as described in the ANALOG OUTPUT section. To eliminate this effect, IOUTB should be terminated with the same impedance as IOUTA, so both outputs see the same resistive divider to ground. This will keep the current in LADCOM constant, minimizing any code-dependent IR drops within the DAC ladder that may give rise to additional nonlinearities.

AC-Coupled Output

Configuring the output as shown in Figure 22 provides a bipolar output signal from the AD768 without requiring the use of a summing amplifier. The ac load impedance presented to the DAC output is the parallel combination of the AD768's output impedance, R_L, and bias resistor R_B. The nominal output swing with the values given in Figure 22 is ±0.5 V assuming $R_B >> R_L$. The gain of the circuit will be a function of the tolerances of the impedances R_{LAD}, R_B, and R_L.

Choosing the value of R_B and C will depend primarily on the desired –3 dB high pass cutoff frequency and the bias current, I_B, of the subsequent stage connected to R_B. The –3 dB frequency can be approximated by the equation,

$$f_{-3\,dB} = 1/[2 \times \pi \times (R_B + R_L \| R_{LAD}) \times C].$$

The dc offset of the output is a function of the bias current of the subsequent stage and the value of R_B. For example, if C = 390 pF, R_B = 20 kΩ, and I_B = 1.0 µA, the –3 dB frequency is approximately 20.4 kHz and the dc offset would be 20 mV.

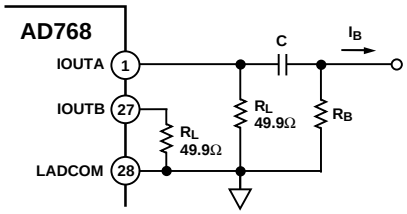


Figure 22. 0.5 V to –0.5 V Unbuffered AC-Coupled Output

BUFFERED VOLTAGE OUTPUT CONFIGURATIONS

Unipolar Configuration

For positive output voltages, or voltage ranges greater than allowed by output compliance limits, some type of external buffer is needed. A wide variety of amplifiers may be selected based on considerations such as speed, accuracy and cost. The AD9631 is an excellent choice when dynamic performance is important, offering low distortion up to 10 MHz. Figure 23 shows the implementation of 0 V to +2 V full-scale unipolar buffered voltage output. The amplifier establishes a summing node at ground for the DAC output. The buffered output voltage results from the DAC output current flowing through the amplifier's feedback resistor, R_{FB}. In this case, the 20 mA full-scale current across R_{FB} (100 Ω) produces an output voltage range of 0 V through +2 V. The same configuration using a precision amplifier such as the AD845 is recommended for optimal dc linearity.

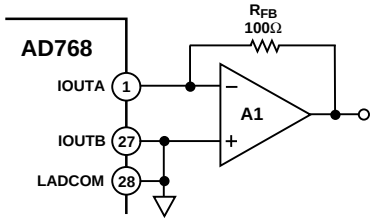


Figure 23. Unipolar 0 V to +2 V Buffered Voltage Output

Buffered Output Using a Current Divider

The configuration shown in Figure 23 may not be possible in cases where the amplifier cannot supply the requisite 20 mA feedback current. As an alternative, Figure 24 shows amplifier A1 in conjunction with a resistive current divider. The values of R_{FF} and R_L are chosen to limit the current, I_3, which must be supplied by A1. Current, I_2, is shunted to ground through resistor, R_L. The parallel combination of R_{FF} and R_L should not exceed 60 Ω to avoid exceeding the specified compliance voltage.

For the values given in Figure 24, I_3 equals 4 mA, which results in a nominal unipolar output swing of 0 V to 2 V. Note, since A1 has an inverting gain of approximately –4 and a noise gain of +5, A1's distortion and noise performance should be considered.

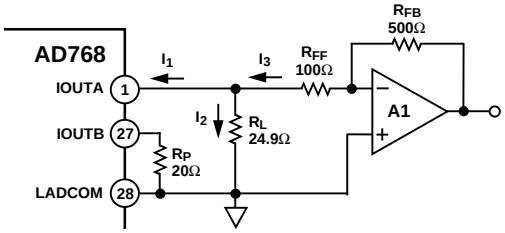


Figure 24. 0 V to 2 V Buffered Unipolar Output Using a Current Divider

Bipolar Configuration

Bipolar mode is accomplished by providing an offset current, $I_{BIPOLAR}$, to the I/V amplifier's (A1) summing junction. By setting $I_{BIPOLAR}$ to exactly half the full-scale current flowing through R_{FB}, the resulting output voltage will be symmetrical about the summing junction voltage, typically ground. Figure 25 shows the implementation for a bipolar ±2.5 V buffered voltage output. The resistor divider sets the full-scale current for I_{DAC} to 5 mA. The internal 2.5 V reference generates a 2.5 mA $I_{BIPOLAR}$ current across R_{BIP}. An output voltage of 0 V is produced when the DAC is set to half scale (100. . .0) such that the 2.5 mA current, I_{DAC}, is exactly offset by $I_{BIPOLAR}$. As the DAC is varied from zero to full-scale, the output voltage swings from –2.5 V to +2.5 V. Note, in configurations that require more than 15 mA of total current from REFOUT, an external buffer is required.

Op amps such as the AD811, AD8001, and AD9631 are good selections for superior dynamic performance. In dc applications, op amps such as the AD845 or AD797 may be more appropriate.

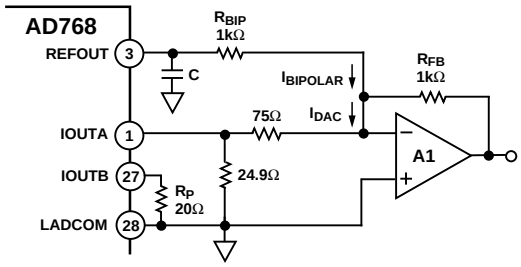


Figure 25. Bipolar ±2.5 V Buffered Voltage Output

DIFFERENTIAL OUTPUT CONFIGURATIONS

AC Coupling via a Transformer

Applications that do not require baseband operation typically use transformer coupling. Transformer coupling the complementary outputs of the AD768 to a load has the inherent benefit of providing electrical isolation while consuming no additional power. Also, a properly applied transformer should not degrade the AD768's output signal with respect to noise and distortion, since the transformer is a passive device. Figure 26 shows a center-tapped output transformer that provides the necessary dc load conditions at the outputs IOUTA and IOUTB to drive a ±0.5 V signal into a 50 Ω load. In this particular circuit, the center-tapped transformer has an impedance ratio of 4 that corresponds to a turns ratio of 2. Hence, any load, R_L, referred to the primary side is multiplied by a factor of 4 (i.e., in this case 200 Ω). To avoid dc current from flowing into the R-2R ladder of the DAC, the center tap of the transformer should be connected to LADCOM.

In order to comply with the minimum voltage compliance of –1.2 V, the maximum differential resistance seen between IOUTA and IOUTB should not exceed 240 Ω. Note that the differential resistance consists of the load R_L, referred to the primary side of the transformer in parallel with any added differential resistance, R_{DIFF}, across the two outputs. R_{DIFF} is typically added to the primary side of the transformer to match the effective primary source impedance to the load (i.e., in this case 200 Ω).

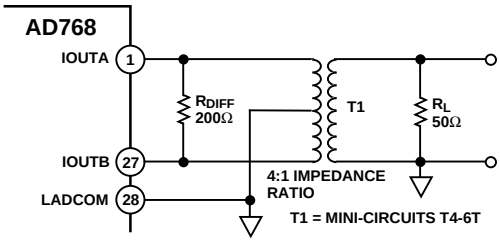


Figure 26. Differential Output Using a Transformer

DC COUPLING VIA AN AMPLIFIER

A dc differential to single-ended conversion can be easily accomplished using the circuit shown in Figure 27. This circuit will attenuate both ac and dc common-mode error sources due to the differential nature of the circuit. Thus, common-mode noise (i.e., clock feedthrough) as well as dc unipolar offset errors will be significantly reduced. Also, excellent temperature stability can be obtained by using temperature tracking, thin film resistors for R and R_{REF}. The design equations for the circuit are provided such that the voltage output swing and IREF can be optimized for a given application.

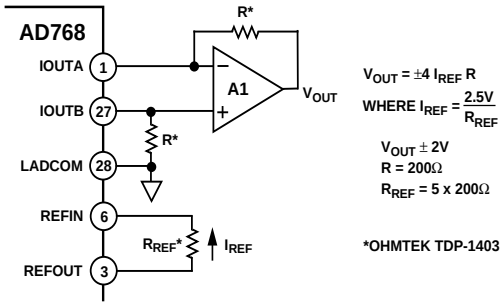


Figure 27. DC Differential to Single-Ended Conversion

POWER AND GROUNDING CONSIDERATIONS

In systems seeking to simultaneously achieve high speed and high accuracy, the implementation and construction of the printed circuit board design is often as important as the circuit design. Proper RF techniques must be used in device selection, placement and routing, and supply bypassing and grounding.

Maintaining low noise on power supplies and ground is critical to obtaining optimum results from the AD768. Figure 28 provides an illustration of the recommended printed circuit board ground plane layout which is implemented on the AD768 evaluation board.

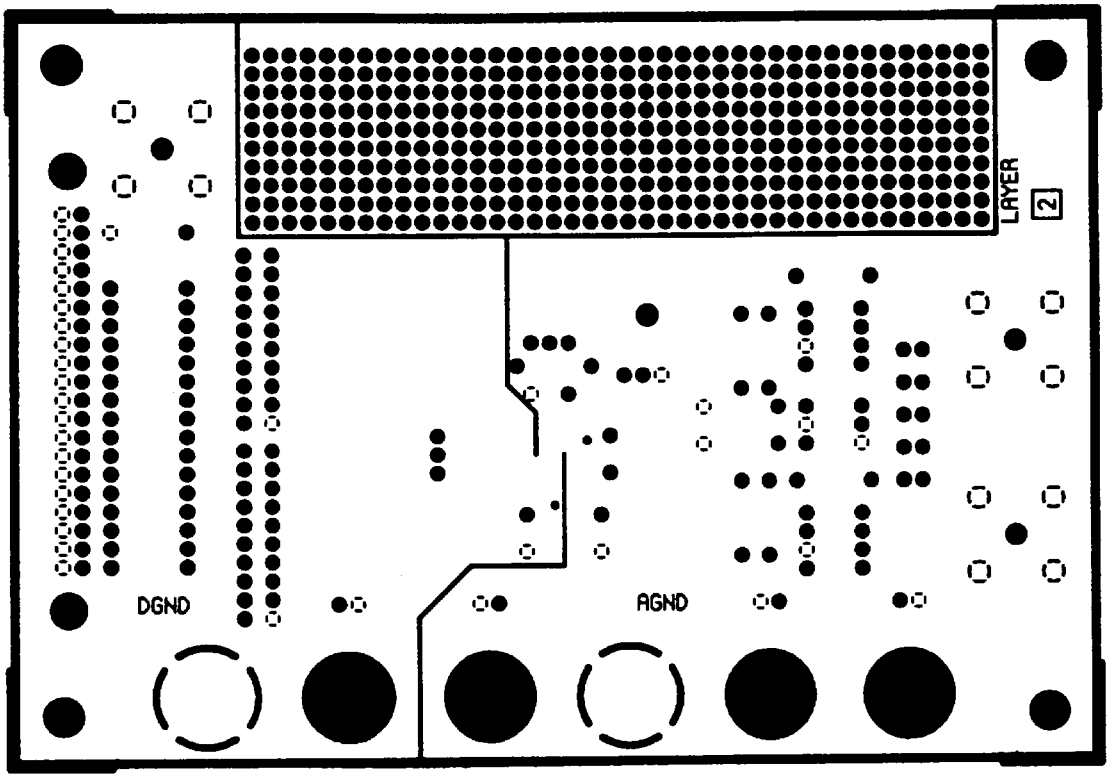


Figure 28. Printed Circuit Board Ground Plane Layout

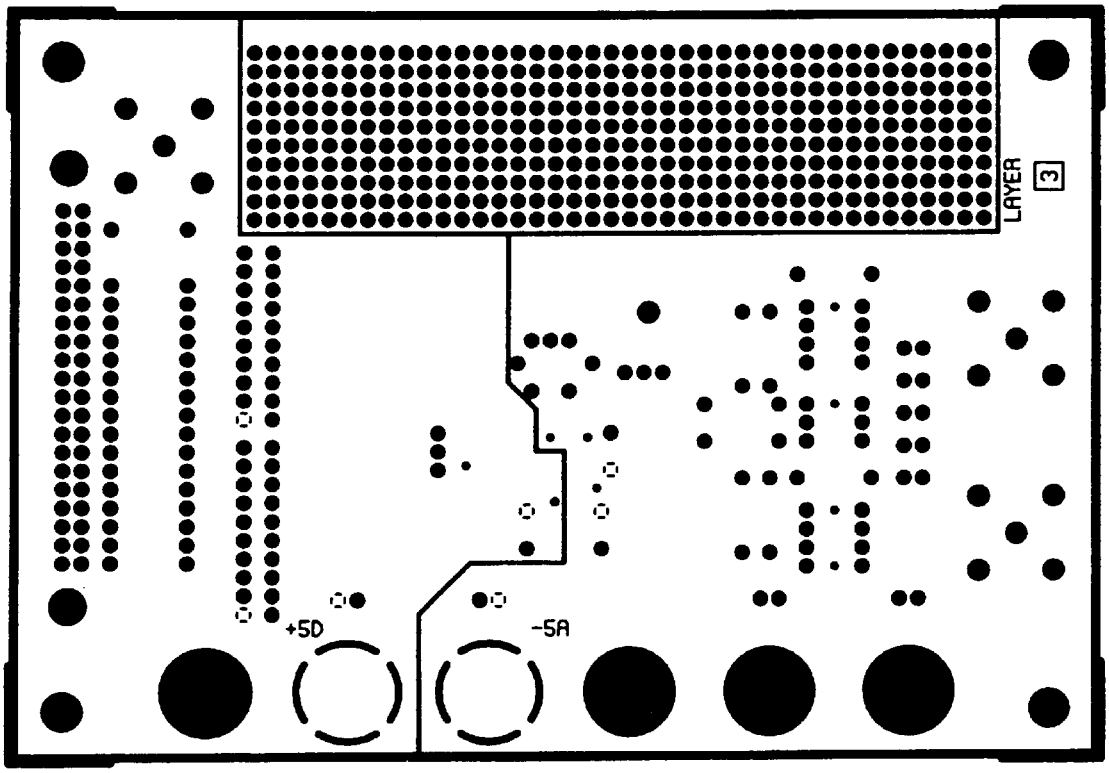


Figure 29. Printed Circuit Board Power Plane Layout

If properly implemented, ground planes can perform a host of functions on high speed circuit boards: bypassing, shielding, current transport, etc. In mixed signal design, the analog and digital portions of the board should be distinct from each other, with the analog ground plane confined to the areas covering analog signal traces and the digital ground plane confined to areas covering the digital interconnects.

All analog ground pins of the DAC, reference, and other analog output components, should be tied directly to the analog ground plane. The two ground planes should be connected by a path 1/4 to 1/2 inch wide underneath or within 1/2 inch of the DAC as shown in Figure 28. Care should be taken to ensure that the ground plane is uninterrupted over crucial signal paths. On the digital side, this includes the digital input lines running to the DAC as well as any clock signals. On the analog side, this includes the DAC output signal, reference signal, and the supply feeders.

The use of wide runs or planes in the routing of power lines is also recommended. This serves the dual role of providing a low series impedance power supply to the part, as well as, providing some "free" capacitive decoupling to the appropriate ground plane. Figure 29 illustrates the power plane layout used in the AD768 evaluation board. The AD768 evaluation board uses a four layer P.C. board which illustrates good layout practices as discussed above.

It is essential that care be taken in the layout of signal and power ground interconnects to avoid inducing extraneous voltage drops in the signal ground paths. It is recommended that all connections be short, direct and as physically close to the package as possible, in order to minimize the sharing of conduction paths between different currents. When runs exceed an inch in length, some type of termination resistor should be considered. The necessity and value of this resistor will be dependent upon the logic family used.

For maximum ac performance, the DAC should be mounted directly to the circuit board; sockets should be avoided since they introduce unwanted capacitive coupling between adjacent pins of the device.

POWER SUPPLY AND DECOUPLING

One of the most important external components associated with high speed designs are the capacitors used to bypass the power supplies. Both selection and placement of these capacitors can be critical and, to a large extent, dependent upon the specifics of the system configuration. The dominant consideration in the selection of bypass capacitors for the AD768 is the minimization of the series resistance and inductance. Many capacitors will begin to look inductive at 20 MHz and above. Ceramic and film type capacitors generally feature lower series inductance than tantalum or electrolytic types.

It is recommended that each power supply to the AD768 be decoupled by a 0.1 µF capacitor located as close to the device pins as possible. Surface-mount chip capacitors, by virtue of their low parasitic inductance, are preferable to through-hole types. Some series inductance between the DAC supply pins and the power supply plane may help to provide additional filtering of high frequency power supply noise. This inductance can be generated by using small ferrite beads.

A clean digital supply may be generated using the circuit shown in Figure 30. The circuit consists of a differential LC filter with separate power supply and return lines. Lower noise can be attained using low ESR (Equivalent Series Resistance) type electrolytic and tantalum capacitors.

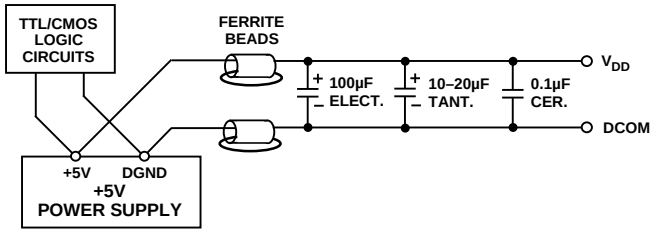


Figure 30. Differential LC Filter for Single +5 V Applications

APPLICATIONS

USING THE AD768 AS A MULTIPLYING DAC

The AD768 can be easily configured as a multiplying DAC since I_{REFIN} can be modulated from 1 mA to 7 mA. The reference amplifier sets the maximum multiplying bandwidth to 15 MHz, while any external capacitor to the NR node serves to limit the bandwidth according to Figure 7. I_{REFIN} can be easily modulated by properly scaling and summing into the IREFIN node the modulating signal. Figure 31 demonstrates how the modulating signal VMOD can be properly scaled and converted to a current via R_{REFMOD} such that its peak current does not exceed 3.0 mA. Figure 32 shows the AD768's typical distortion versus the reference channel frequency.

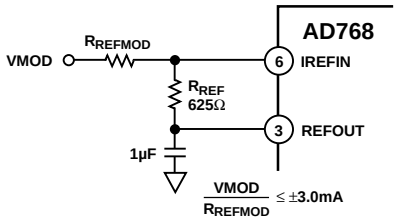


Figure 31. Typical Multiplying DAC Application

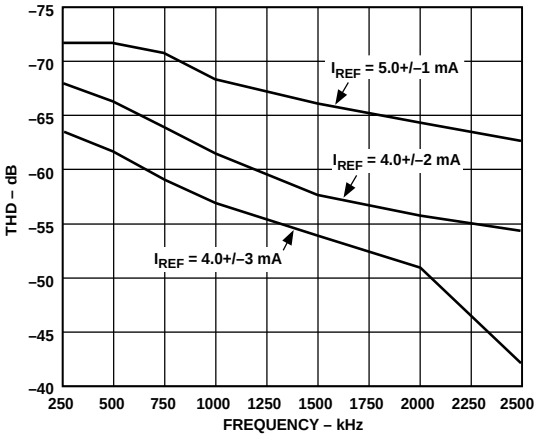


Figure 32. Reference Channel Distortion vs. Frequency

AD768 IN MULTITONE TRANSMITTERS (FOR ADSL)

Communications applications frequently require aspects of component performance that differ significantly from the simple, single tone signals used in typical SNR and THD tests. This is particularly true for spread-spectrum and frequency division multiplexed (FDM) type signals, where information content is held in a number of small signal components spread across the frequency band. In these applications, a combination of wide dynamic range, good fine-scale linearity, and low intermodulation distortion is required. Unfortunately, a part's full scale SNR and THD performance may not be a reliable indicator of how it will perform in these multitone applications.

One example of an FDM communications system is the DMT (discrete multitone) ADSL (Asymmetrical Digital Subscriber Line) standard currently being considered by ANSI. Figure 33 shows a block diagram of a transmitter function.

The digital bits are used to QAM modulate each of approximately 200 discrete tones. An inverse FFT turns this modulated frequency domain information into 512 time points at a 2.2 MSPS sample rate. These time points are then put through an FIR interpolation filter to upsample (in this case to 4.4 MSPS). The bit stream is run through the AD768, which is followed by a 4th order analog smoothing filter, then run to the line-driving circuitry

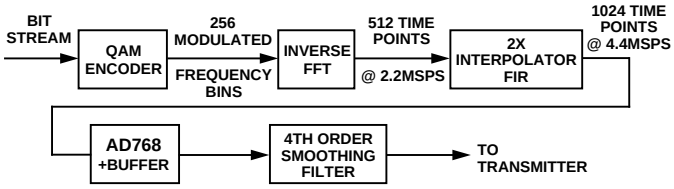


Figure 33. Typical DMT ADSL Transmit Chain

Figure 34a shows a frequency domain representation of a test vector run through this system, while 34b shows the time domain representation. (Clearly the frequency domain picture is more informative.) We wish to optimize the SINAD of each 4 kHz frequency band: this is a function of both noise (wideband and quantization) and distortion (simple harmonic and intermod).

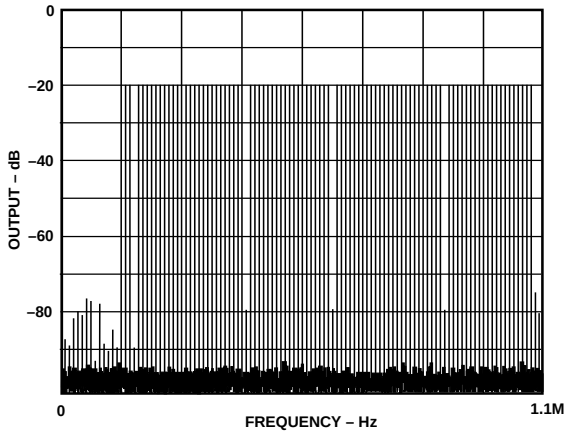


Figure 34a. Output Spectrum of ADSL Test Vector

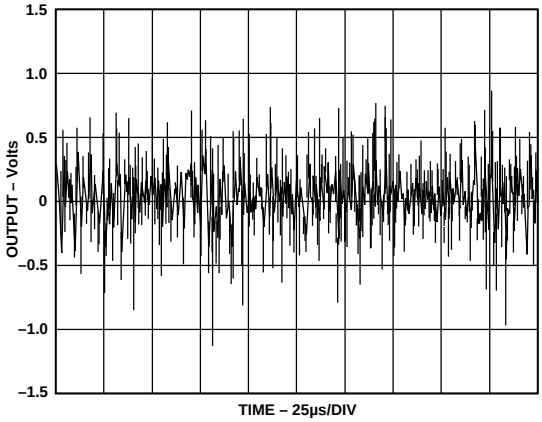


Figure 34b. Time Domain Output Signal of ADSL Test Vector

Table I and II show the available SNR and THD at the output of the filter vs. frequency bin for the ADSL application. The AD768's combination of 16-bit dynamic range and 14-bit linearity provides excellent performance for the DMT signal. Its fast input rate would support even faster rates of oversampling, if one were interested in trading off digital filter complexity in the interpolator for a simplified analog filter.

Table I. SNR vs. Frequency

Frequency	SNR
151 kHz	70.1 dB
349 kHz	69.7 dB
500 kHz	69.4 dB
1 MHz	69.8 dB

Table II. THD vs. Frequency

Frequency	THD
160 kHz	–68.9 dBc
418 kHz	–64.0 dBc
640 kHz	–64.3 dBc
893 kHz	–63.8 dBc

AD768 EVALUATION BOARD

GENERAL DESCRIPTION

The AD768-EB is an evaluation board for the AD768 16-bit 30 Msps D/A converter. Careful attention to layout and circuit design combined with analog and digital prototyping areas allows the user to easily and effectively evaluate the AD768 in any application where high resolution, high speed conversion is required.

The digital inputs to the AD768-EB may be driven directly using the standard 40-pin IDC connector. An external clock is also required. These signals may be applied from a user's bench, or they can be generated from a circuit built on the prototyping area. The analog outputs from the AD768-EB are available on BNC connectors. These outputs may be configured to use either resistors, op amps, or a transformer.

OPERATING PROCEDURE AND FUNCTIONAL DESCRIPTION

Power

Power may be supplied to the AD768-EB by applying either wires or banana plugs to the metal binding posts included on the printed circuit board.

DGND. Digital Ground. The digital ground and the analog ground are connected together underneath the AD768. Optimal performance can be obtained with separate analog and digital supplies. For evaluation purposes, a single-supply which makes a second analog and digital ground connection at the supply is acceptable.

+5D. The +5 V (±5%) digital supply should be capable of supplying 50 mA.

–5A. The –5 V (±5%) analog supply should be capable of supplying –75 mA.

AGND. Analog ground. The analog ground and the digital ground are connected together underneath the AD768. Optimal performance can be obtained with separate analog and digital supplies. For evaluation purposes, a single-supply which makes a second analog and digital ground connection at the supply is acceptable.

$-V_{EE}$. Negative analog supply; typically –5 V to –15 V. This supply is used as the negative supply rail for the external op amps. For the AD811 supplied with the AD768-EB, a supply capable of supplying –20 mA (excluding external load requirements) is required.

$+V_{CC}$. Positive analog supply; typically +5 V to +15 V. This supply is used as the positive supply rail for the external op amps. For the AD811 supplied with the AD768-EB, a supply capable of supplying +20 mA (excluding external load requirements) is required.

Analog Outputs

The analog output(s) from the AD768-EB are available on BNC jacks "A" and "B." The complementary current outputs from the AD768 can be configured using either resistors, op amps, or a transformer. Only the "A" portion of the AD768-EB is populated and shipped from the factory. The "B" side, or complementary output, may be populated by the user if so desired.

JP1. Buffered op amp output "A". Jumper JP1 should be installed if the buffered op amp output is desired. **When JP1 is installed, JP2 and JP3 must be removed** for proper operation. The output, available on the "A" connector, has a nominal voltage swing of 0 V to 2 V and is in-phase with the digital input. This is the factory default setting.

JP2. Bipolar 50 Ω transformer output. If jumper JP2 is installed, a transformer coupled output is available on the "A" connector. **When JP2 is installed, JP1 and JP3 must be removed** for proper operation. The transformer acts both as a differential-to-single-ended converter and as an impedance transformer. For proper operation, **the transformer must be terminated with a 50 Ω resistor**. R2 must be replaced with the 100 Ω resistor, R7. An additional 100 Ω resistor and the transformer are included with the AD768-EB. The additional 100 Ω resistor must be soldered into the appropriate position labeled "R3" and the transformer must be inserted into the socket labeled "T1." The nominal output voltage into a 50 Ω load is 1 V p-p centered on a common-mode voltage of 0 V.

JP3. Resistor output "A." JP3 is used to connect the resistor R2 to the "A" output. U2 should be removed from its socket. Using a 24.9 Ω resistor for R2, the output is an unbuffered 0 V to –0.5 V output that is out of phase with the digital input. Resistor R2 may be replaced with other values, but careful attention to the recommended output compliance range should be observed. **When JP3 is installed, JP1 and JP2 must be removed for proper operation**.

JP4. Resistor output "B." JP4 is used to connect the resistor R3 to the "A" output. U3 should be removed from its socket. The AD768-EB is shipped from the factory with resistor R3 shorted to ground. A different value selected by the user can be installed for R3 to generate an unbuffered output that is in-phase with the digital input. Careful attention to the recommended output compliance range should be observed when selecting the value of R3. **When JP4 is installed, JP5 must be removed for proper operation**.

JP5. Buffered op amp output "B." Jumper JP5 should be installed if the buffered op amp output is desired. **When JP5 is installed, JP4 must be removed for proper operation**. The output is available on the "B" connector and has a nominal voltage swing determined by the combination of resistors R3, R9, and R10. This op amp is not provided with the AD768-EB.

Reference

Either the internal reference of the AD768 or an external reference may be selected on the AD768-EB. R12 is used to adjust the full-scale output current of the AD768.

SW2. Internal/External reference select switch. When SW2 is in position 1, the internal reference of the AD768 is selected. When SW2 is in position 2, an external reference must be provided by the user.

Level-Shifting the Analog Output

Resistor sockets R8 and R6 can be populated with an appropriately valued resistor to add dc offset current to an output which uses the op amp configuration. As an example, to generate a bipolar output signal, a 1.25 kΩ resistor installed into the "R8" socket level-shifts the normally unipolar output by –1 V. The factory defaults for R8 and R6 are open circuits.

Clock Input
An external sample clock must be provided to either the BNC connector labeled "CLOCK" or on Pin 33 of the IDC connector. This clock must comply with the logic levels outlined in the AD768 data sheet. The "CLOCK" input is terminated with a removable 51 Ω resistor. The IDC connector clock connection is unterminated.

SW1. Clock source select switch. When SW1 is in position 1, Pin 33 of the IDC connected is applied to the CLOCK input of the AD768. When SW2 is in position 2, the "CLOCK" BNC connector is applied to the CLOCK input of the AD768.

Digital Inputs
The digital inputs of the AD768, DB0–DB15, are available via J1, a 40-pin IDC connector. These inputs should comply with the specifications given in the AD768 data sheet.

Layout Considerations
Figures 28 and 29 show the AD768-EB ground and power plane layouts. Figures 35–38 show the schematic diagram, trace routing, silk screening, and component layout for the AD768 4 layer evaluation board.

Separate ground and power planes have several advantages for high speed layouts. (For further information outlining these advantages, see the application note "Design and Layout of a Video Graphics System for Reduced EMI" [E1309] available from Analog Devices [(617) 461-3392].) A solid ground plane can be used if the digital return current can be routed such that it does not modulate the analog ground plane. If this is not possible, it may be necessary to split the ground plane in order to force currents to flow in a controlled direction. This type of grounding scheme is shown in the Figure 28. The ground plane is separated into analog and digital planes that are joined together under the AD768. In any case, the AD768 should be treated as an analog component and a common ground connection should be made underneath the AD768 despite some pins being labeled "digital" ground and some as "analog" ground.

A complete parts list for the AD768 evaluation board is given in Table IV.

Table III. Summary of Jumper Functionality

Installed	Jumper Function
Jumper	
JP1	Buffered Output A
JP2	50 Ω Transformer Output
JP3 (STBY)	Unbuffered Output A
JP4	Unbuffered Output B
JP5	Buffered Output B

Table IV. AD768-EB Parts List

Reference	Value / Part Type	Package	Qty/Bd
U1	AD768	28-Pin SOIC	1
U2	AD811	8-Pin DIP	1
T1	Mini-Circuits T4–6T	Not Installed	1
A, B, CLOCK	BNC JACKs, Small	Small, Vertical	3
JP1–5	Header	2-Pin	5
SW1, 2	SPDT, Secme	0.1" × 0.3"	2
J1	40-Pin IDC Connector	R.A., Male, w/ Latches	1
R1	500 Ω	1/4 W, 0.01%, Vishay	1
R2	25 Ω	1/4 W, 0.01%, Vishay	1
R3, R13–21, & R23–29	Wire Jumpers		17
R5	500 Ω	1/4 W, 0.01%, Vishay	1
R7	100 Ω	1/4 W, 0.01%, Vishay	1
R11	51 Ω	1/8 W, 5%, Carbon	1
R12	10 kΩ Pot.	3266 W	1
C1–4	1 µF Ceram. Cap.	Leaded	4
C5–8, C10, 12, 14, & C16–19		0.1 µF Chip Cap, 1206	11
C9, 11, 13, 15	22 µF Tant. Cap., 25 V	Teardrop, 0.1" Spacing	4

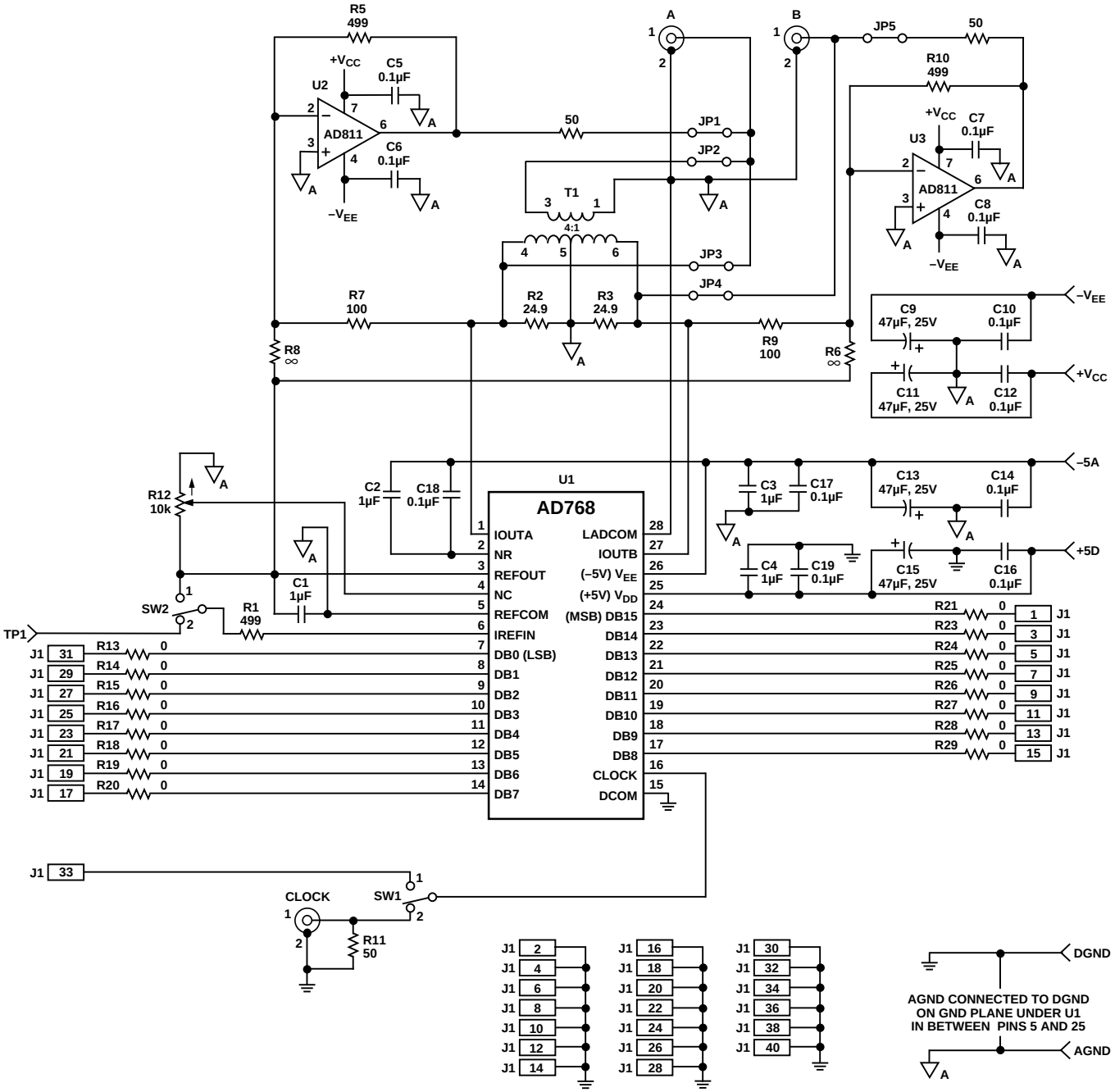


Figure 35. AD768 Evaluation Board Schematic

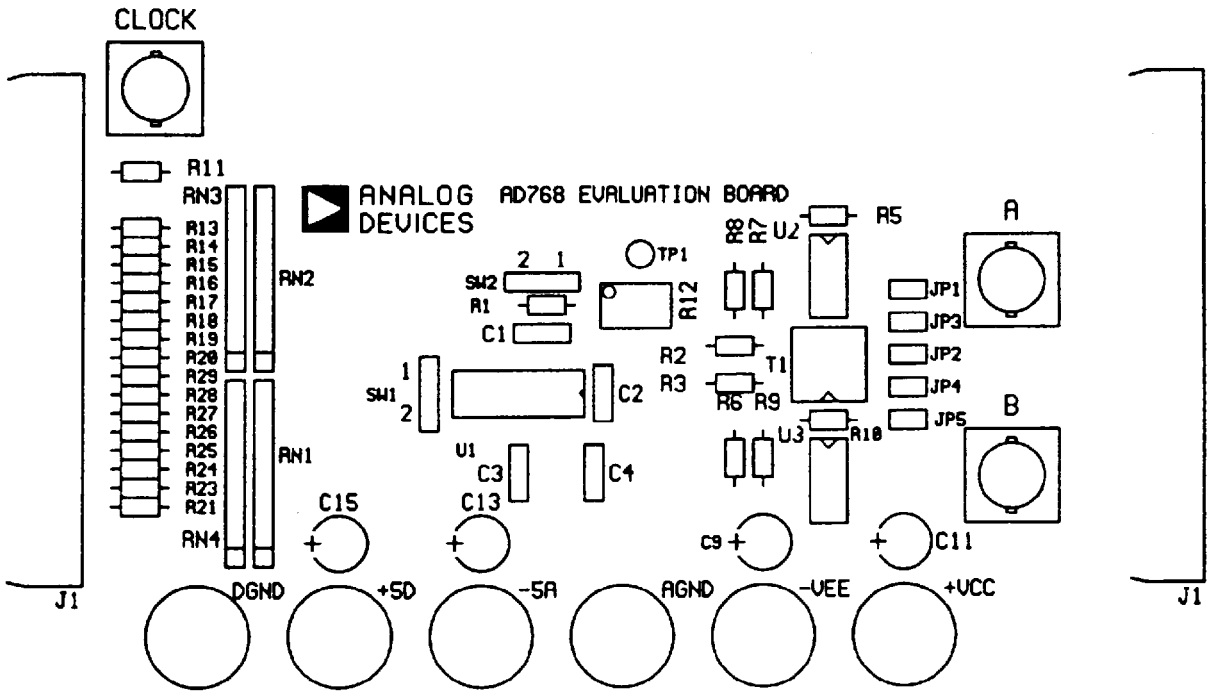


Figure 36. Silkscreen Layer (Not to Scale)

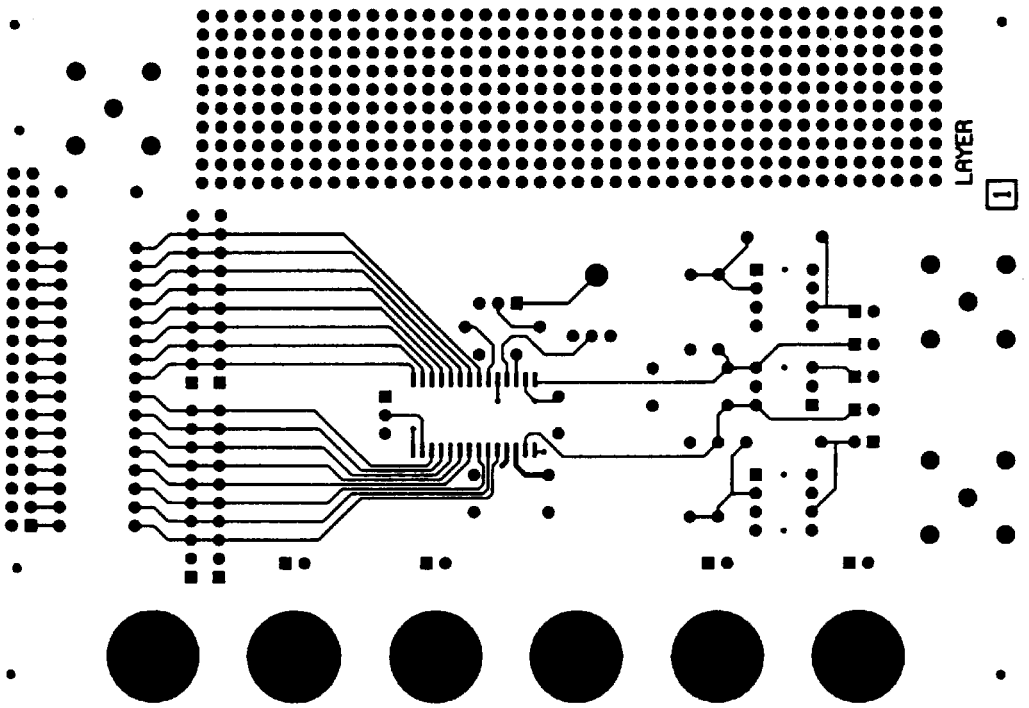


Figure 37. Component Side PCB Layout (Not to Scale)

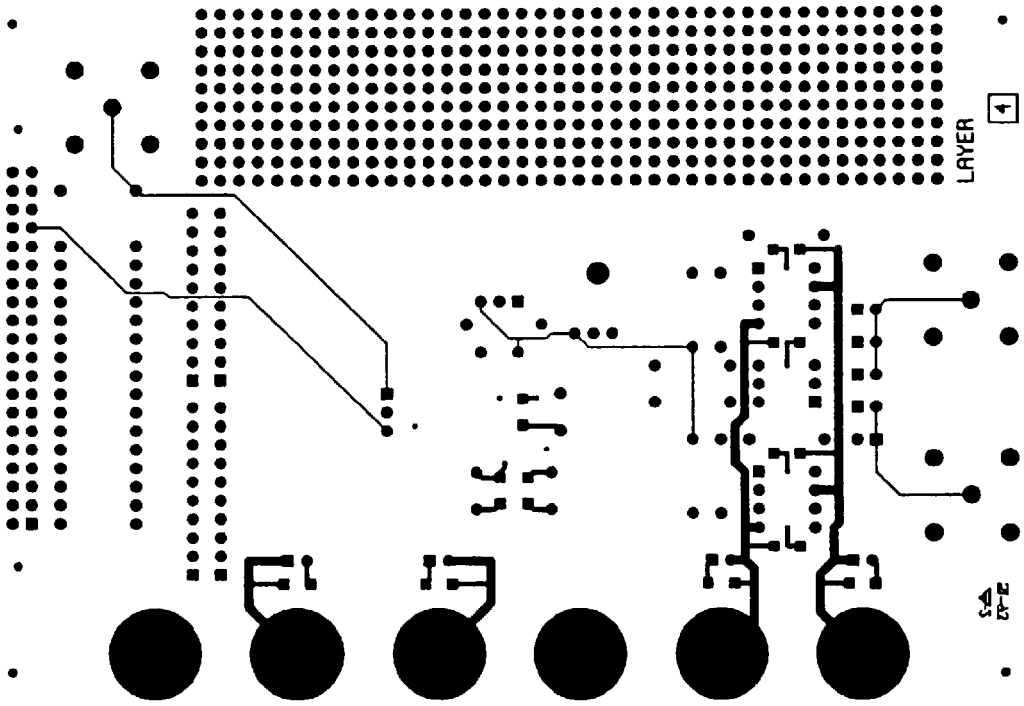
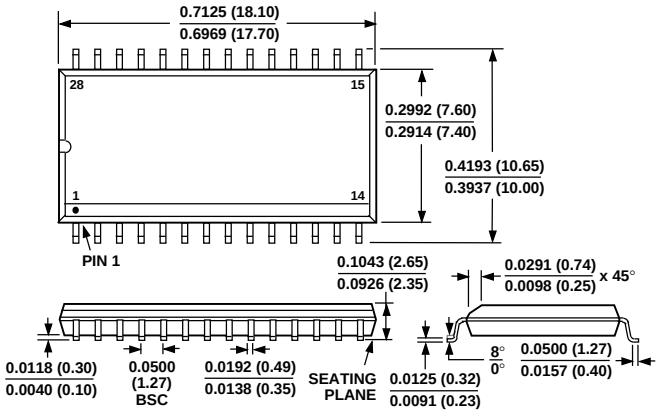


Figure 38. Solder Side PCB Layout (Not to Scale)

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

R-28
300 Mil 28-Pin SOIC



C1941a–5–6/96

PRINTED IN U.S.A.