

74VHCT138A

3-to-8 Decoder/Demultiplexer

Features

- High Speed: $t_{PD} = 7.6\text{ns}$ (Typ.) at $V_{CC} = 5\text{V}$
- Low power dissipation: $I_{CC} = 4\mu\text{A}$ (Max.) at $T_A = 25^\circ\text{C}$
- Power down protection is provided on all inputs and outputs
- Pin and function compatible with 74HCT138

General Description

The VHCT138A is an advanced high speed CMOS 3-to-8 DECODER fabricated with silicon gate CMOS technology. It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

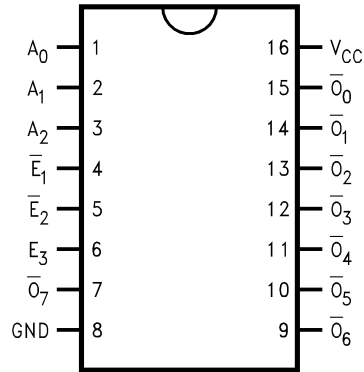
When the device is enabled, 3 Binary Select inputs (A_0 , A_1 and A_2) determine which one of the outputs (\overline{O}_0 – \overline{O}_7) will go LOW. When enable input E_3 is held LOW or either \overline{E}_1 or \overline{E}_2 is held HIGH, decoding function is inhibited and all outputs go HIGH. E_3 , \overline{E}_1 and \overline{E}_2 inputs are provided to ease cascade connection and for use as an address decoder for memory systems. Protection circuits ensure that 0V to 7V can be applied to the input pins without regard to the supply voltage and to the output pins with $V_{CC} = 0\text{V}$. These circuits prevent device destruction due to mismatched supply and input/output voltages. This device can be used to interface 3V to 5V systems and two supply systems such as battery backup.

Ordering Information

| Order Number | Package Number | Package Description |
|---------------|----------------|--|
| 74VHCT138AM | M16A | 16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow |
| 74VHCT138ASJ | M16D | 16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide |
| 74VHCT138AMTC | MTC16 | 16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide |

Surface mount packages are also available on Tape and Reel. Specify by appending the suffix letter "X" to the ordering number.

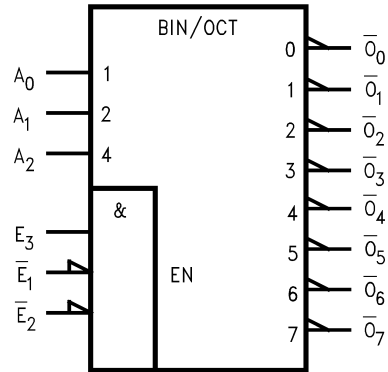
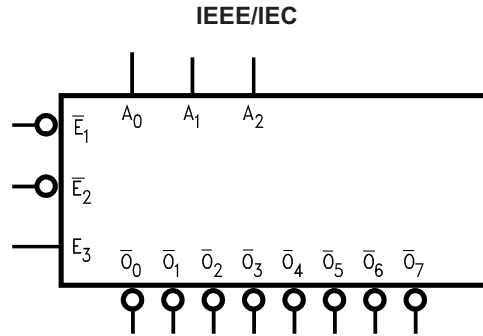
Connection Diagram



Pin Description

| Pin Names | Description |
|---------------------------|----------------|
| A_0 – A_2 | Address Inputs |
| \bar{E}_1 – \bar{E}_2 | Enable Inputs |
| E_3 | Enable Input |
| \bar{O}_0 – \bar{O}_7 | Outputs |

Logic Symbols



Truth Table

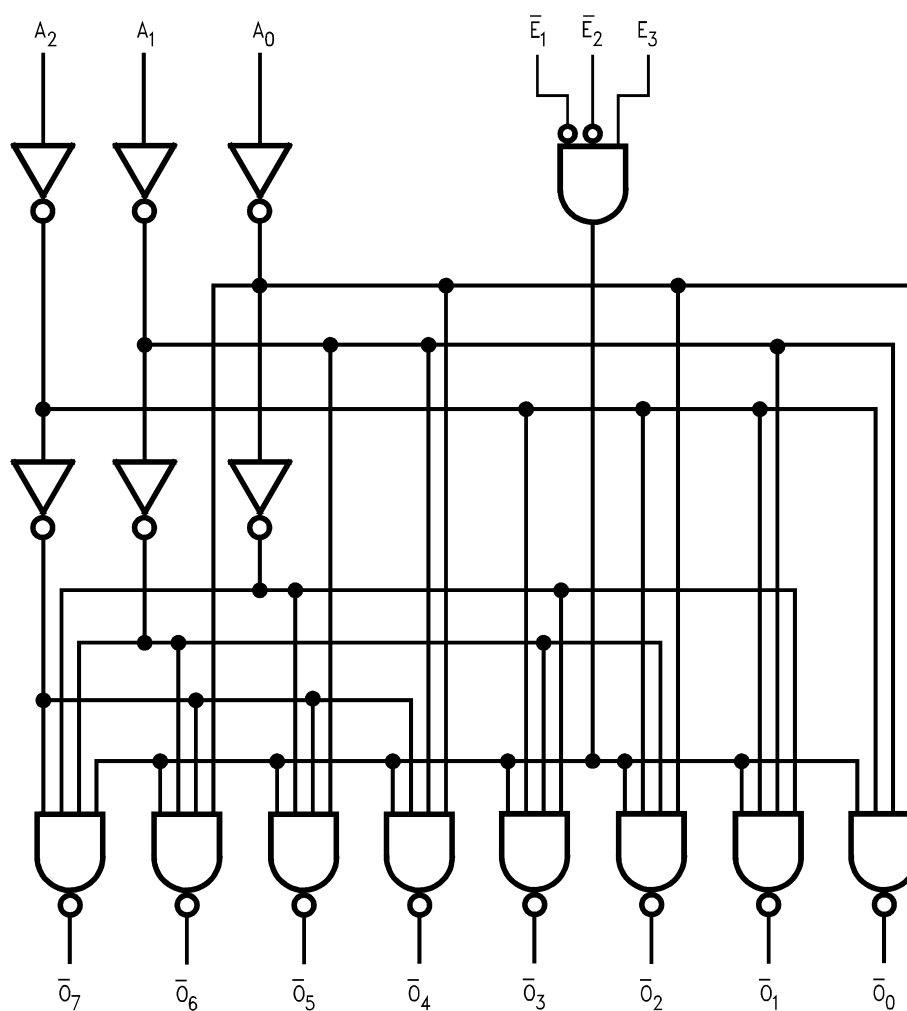
| Inputs | | | | | | Outputs | | | | | | | |
|-------------|-------------|-------|-------|-------|-------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|
| \bar{E}_1 | \bar{E}_2 | E_3 | A_0 | A_1 | A_2 | \bar{O}_0 | \bar{O}_1 | \bar{O}_2 | \bar{O}_3 | \bar{O}_4 | \bar{O}_5 | \bar{O}_6 | \bar{O}_7 |
| H | X | X | X | X | X | H | H | H | H | H | H | H | H |
| X | H | X | X | X | X | H | H | H | H | H | H | H | H |
| X | X | L | X | X | X | H | H | H | H | H | H | H | H |
| L | L | H | L | L | L | L | H | H | H | H | H | H | H |
| L | L | H | H | L | L | H | L | H | H | H | H | H | H |
| L | L | H | L | H | L | H | H | L | H | H | H | H | H |
| L | L | H | H | H | L | H | H | H | L | H | H | H | H |
| L | L | H | L | L | H | H | H | H | H | L | H | H | H |
| L | L | H | H | L | H | H | H | H | H | H | L | H | H |
| L | L | H | L | H | H | H | H | H | H | H | H | L | H |
| L | L | H | H | H | H | H | H | H | H | H | H | H | L |

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

| Symbol | Parameter | Rating |
|-----------|--|---|
| V_{CC} | Supply Voltage | –0.5V to +7.0V |
| V_{IN} | DC Input Voltage | –0.5V to +7.0V |
| V_{OUT} | DC Output Voltage Note 1 Note 2 | –0.5V to 7.0V –0.5V to $V_{CC} + 0.5V$ |
| I_{IK} | Input Diode Current | –20mA |
| I_{OK} | Output Diode Current ⁽³⁾ | ±20mA |
| I_{OUT} | DC Output Current | ±25mA |
| I_{CC} | DC V_{CC} /GND Current | ±75mA |
| T_{STG} | Storage Temperature | –65°C to +150°C |
| T_L | Lead Temperature (Soldering, 10 seconds) | 260°C |

Recommended Operating Conditions⁽⁴⁾

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

| Symbol | Parameter | Rating |
|------------|--|------------------------------|
| V_{CC} | Supply Voltage | 4.5V to +5.5V |
| V_{IN} | Input Voltage | 0V to +5.5V |
| V_{OUT} | Output Voltage Note 1 Note 2 | 0V to 5.5V 0V to V_{CC} |
| T_{OPR} | Operating Temperature | –40°C to +85°C |
| t_r, t_f | Input Rise and Fall Time, $V_{CC} = 5.0V \pm 0.5V$ | 0 ~ 20ns/V |

Notes:

1. $V_{CC} = 0V$.
2. HIGH or LOW state. I_{OUT} absolute maximum rating must be observed.
3. $V_{OUT} < GND$, $V_{OUT} > V_{CC}$ (Outputs Active).
4. Unused inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

| Symbol | Parameter | V _{CC} (V) | Conditions | T _A = 25°C | | | T _A = -40°C to +85°C | | Units |
|------------------|--------------------------------|---------------------|---|-----------------------|------|------|---------------------------------|------|-------|
| | | | | Min. | Typ. | Max. | Min. | Max. | |
| V _{IH} | HIGH Level Input Voltage | 4.5 – 5.5 | | 2.0 | | | 2.0 | | V |
| V _{IL} | LOW Level Input Voltage | 4.5 – 5.5 | | | | 0.8 | | 0.8 | V |
| V _{OH} | HIGH Level Output Voltage | 4.5 | V _{IN} = V _{IH} or V _{IL} I _{OH} = -50μA | 4.4 | 4.5 | | 4.4 | | V |
| | | | I _{OH} = -8mA | 3.94 | | | 3.80 | | |
| V _{OL} | LOW Level Output Voltage | 4.5 | V _{IN} = V _{IH} or V _{IL} I _{OL} = 50μA | | 0.0 | 0.1 | | 0.1 | V |
| | | | I _{OL} = 8mA | | | 0.36 | | 0.44 | |
| I _{IN} | Input Leakage Current | 0 – 5.5 | V _{IN} = 5.5V or GND | | | ±0.1 | | ±1.0 | μA |
| I _{CC} | Quiescent Supply Current | 5.5 | V _{IN} = V _{CC} or GND | | | 4.0 | | 20.0 | μA |
| I _{CCT} | Maximum I _{CC} /Input | 5.5 | V _{IN} = 3.4V, All other inputs = V _{CC} or GND | | | 1.35 | | 1.50 | mA |
| I _{OFF} | Output Leakage Current | 0 | V _{OUT} = 5.5V | | | 0.5 | | 5.0 | μA |

AC Electrical Characteristics

| Symbol | Parameter | V _{CC} (V) | Conditions | T _A = 25°C | | | T _A = -40°C to +85°C | | Units |
|-------------------------------------|---|---------------------|------------------------|-----------------------|------|------|---------------------------------|------|-------|
| | | | | Min. | Typ. | Max. | Min. | Max. | |
| t _{PLH} , t _{PHL} | Propagation Delay, A _n to O _n | 5.0 ± 0.5 | C _L = 15pF | | 7.6 | 10.4 | 1.0 | 12.0 | ns |
| | | | C _L = 50pF | | 8.1 | 11.4 | 1.0 | 13.0 | |
| t _{PLH} , t _{PHL} | Propagation Delay, E ₃ to O _n | 5.0 ± 0.5 | C _L = 15pF | | 6.6 | 9.1 | 1.0 | 10.5 | ns |
| | | | C _L = 50pF | | 7.1 | 10.1 | 1.0 | 11.5 | |
| t _{PLH} , t _{PHL} | Propagation Delay, E ₁ or E ₂ to O _n | 5.0 ± 0.5 | C _L = 15pF | | 7.0 | 9.6 | 1.0 | 11.0 | ns |
| | | | C _L = 50pF | | 7.5 | 10.6 | 1.0 | 12.0 | |
| C _{IN} | Input Capacitance | | V _{CC} = Open | | 4 | 10 | | 10 | pF |
| C _{PD} | Power Dissipation Capacitance | | ⁽⁵⁾ | | 49 | | | | pF |

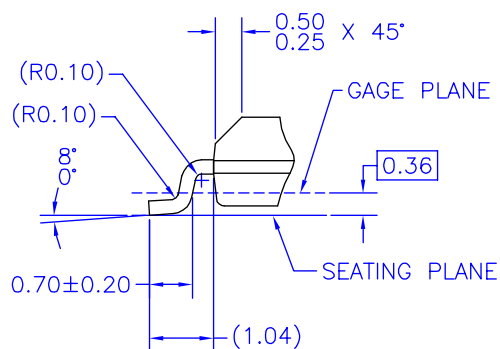
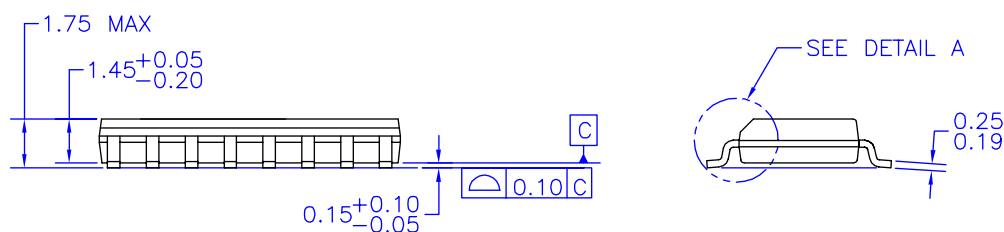
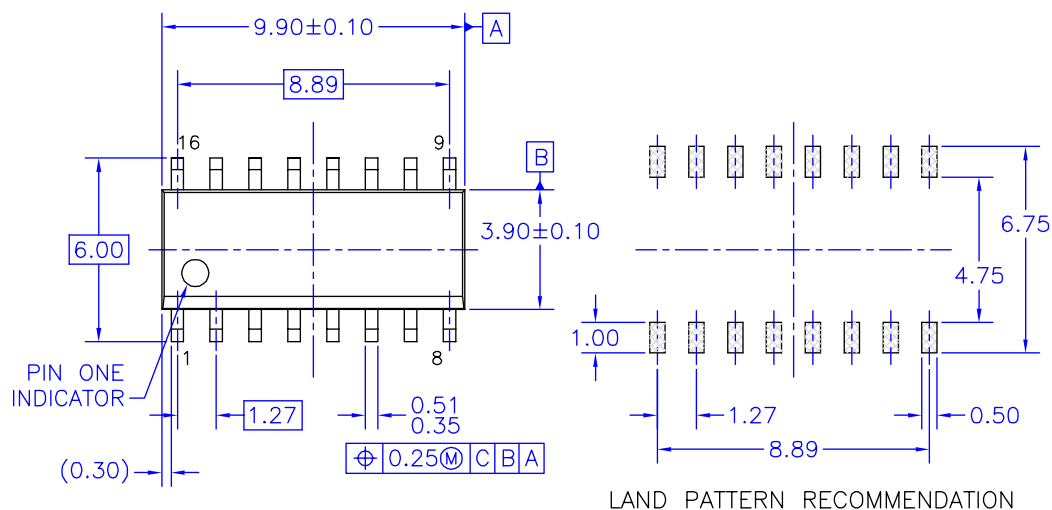
Note:

5. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation:

$$I_{CC} (\text{Opr.}) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

Physical Dimensions

Dimensions are in millimeters unless otherwise noted.



NOTES: UNLESS OTHERWISE SPECIFIED

- A) THIS PACKAGE CONFORMS TO JEDEC MS-012, VARIATION AC, ISSUE C, DATED MAY 1990.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.
- D) STANDARD LEAD FINISH:
200 MICROINCHES / 5.08 MICRONS MIN.
LEAD/TIN (SOLDER) ON COPPER.

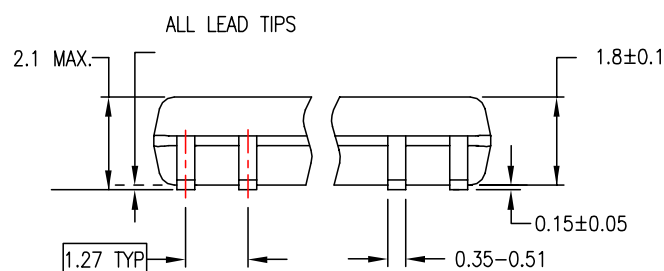
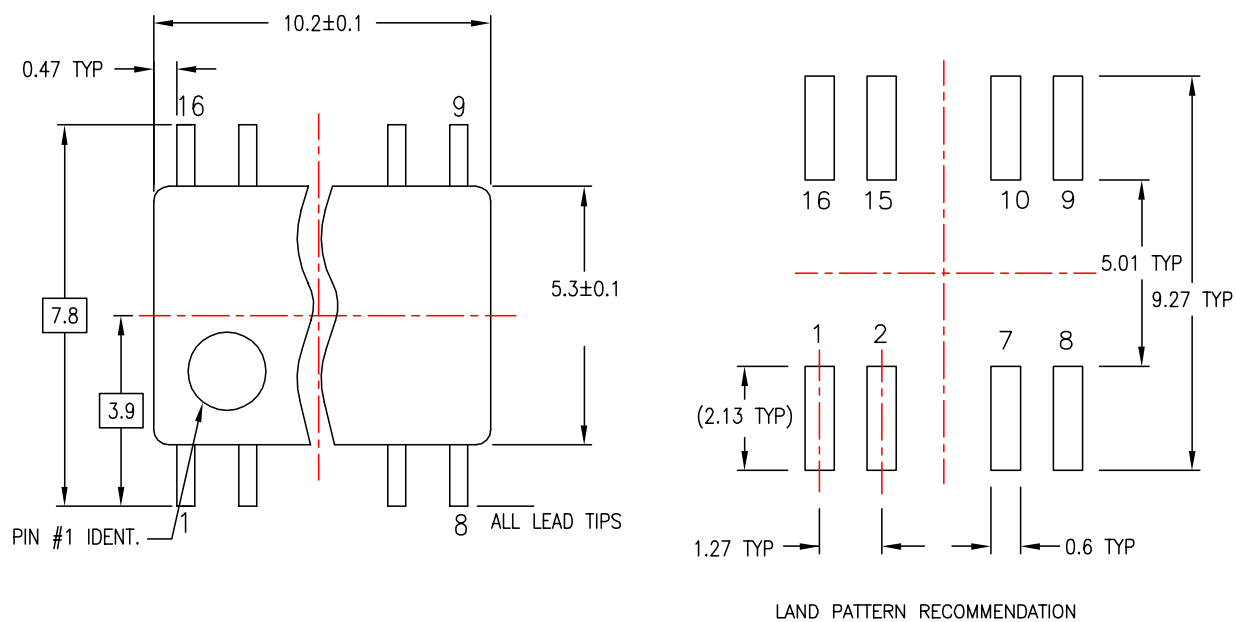
DETAIL A
SCALE: 2:1

M16AREVK

Figure 1. 16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow Package Number M16A

Physical Dimensions (Continued)

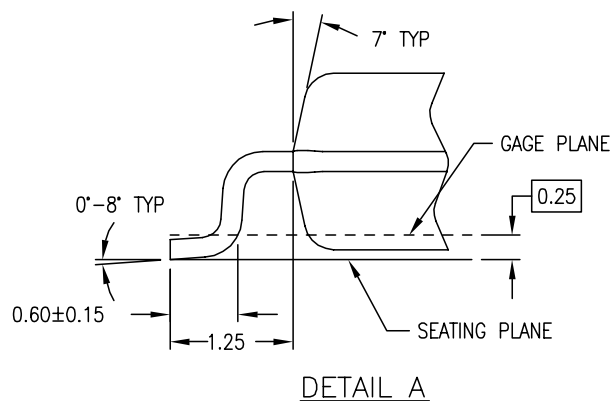
Dimensions are in millimeters unless otherwise noted.



DIMENSIONS ARE IN MILLIMETERS

NOTES:

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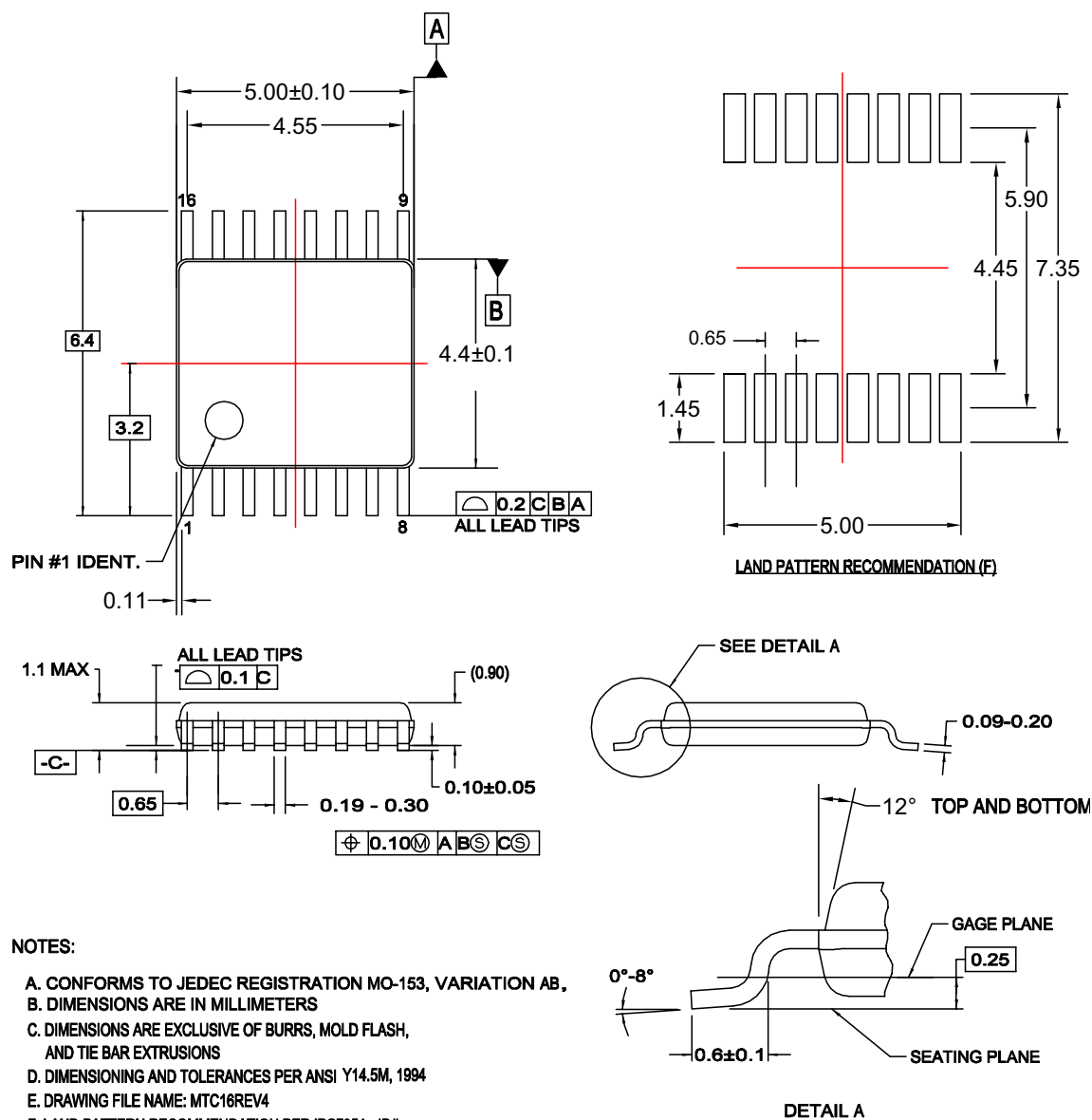


M16DREVC

**Figure 2. 16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M16D**

Physical Dimensions (Continued)

Dimensions are in millimeters unless otherwise noted.




MTC16rev4

Figure 3. 16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide Package Number MTC16

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