

74VHC175 Quad D-Type Flip-Flop

Features

- High Speed: $f_{MAX} = 210\text{MHz}$ (Typ.) at $V_{CC} = 5\text{V}$
- Low power dissipation: $I_{CC} = 4\mu\text{A}$ (Max.) at $T_A = 25^\circ\text{C}$
- High noise immunity: $V_{NIH} = V_{NIL} = 28\% V_{CC}$ (Min.)
- Power down protection is provided on all inputs
- Low noise: $V_{OLP} = 0.8\text{V}$ (Max.)
- Pin and function compatible with 74HC175

General Description

The VHC175 is an advanced high-speed CMOS device fabricated with silicon gate CMOS technology. It achieves the high-speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

The VHC175 is a high-speed quad D-type flip-flop. The device is useful for general flip-flop requirements where clock and clear inputs are common. The information on the D inputs is stored during the LOW-to-HIGH clock transition. Both true and complemented outputs of each flip-flop are provided. A Master Reset input resets all flip-flops, independent of the Clock or D inputs, when LOW.

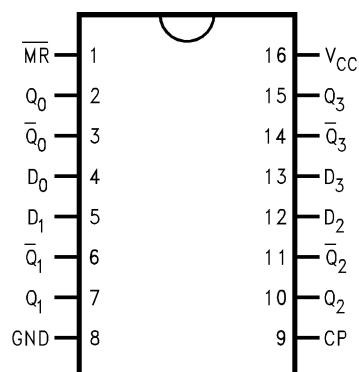
An input protection circuit insures that 0V to 7V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5V to 3V systems and two supply systems such as battery backup. This circuit prevents device destruction due to mismatched supply and input voltages.

Ordering Information

Order Number	Package Number	Package Description
74VHC175M	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
74VHC175SJ	M16D	16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74VHC175MTC	MTC16	16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Surface mount packages are also available on Tape and Reel. Specify by appending the suffix letter "X" to the ordering number.

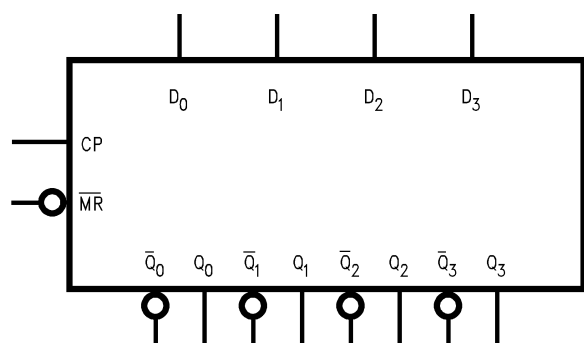
Connection Diagram



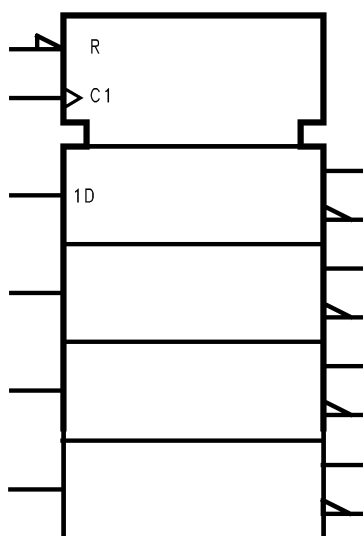
Pin Description

Pin Names	Description
D_0-D_3	Data Inputs
CP	Clock Pulse Input
MR	Master Reset Input
Q_0-Q_3	True Outputs
$\overline{Q_0}-\overline{Q_3}$	Complement Outputs

Logic Symbol



IEEE/IEC



Functional Description

The VHC175 consists of four edge-triggered D flip-flops with individual D inputs and Q and \bar{Q} outputs. The Clock and Master Reset are common. The four flip-flops will store the state of their individual D inputs on the LOW-to-HIGH clock (CP) transition, causing individual Q and \bar{Q} outputs to follow. A LOW input on the Master Reset (\overline{MR}) will force all Q outputs LOW and \bar{Q} outputs HIGH independent of Clock or Data inputs. The VHC175 is useful for general logic applications where a common Master Reset and Clock are acceptable.

Truth Table

Inputs @ t_n , $\overline{MR} = H$		Outputs @ t_{n+1}	
D_n		Q_n	\bar{Q}_n
L		L	H
H		H	L

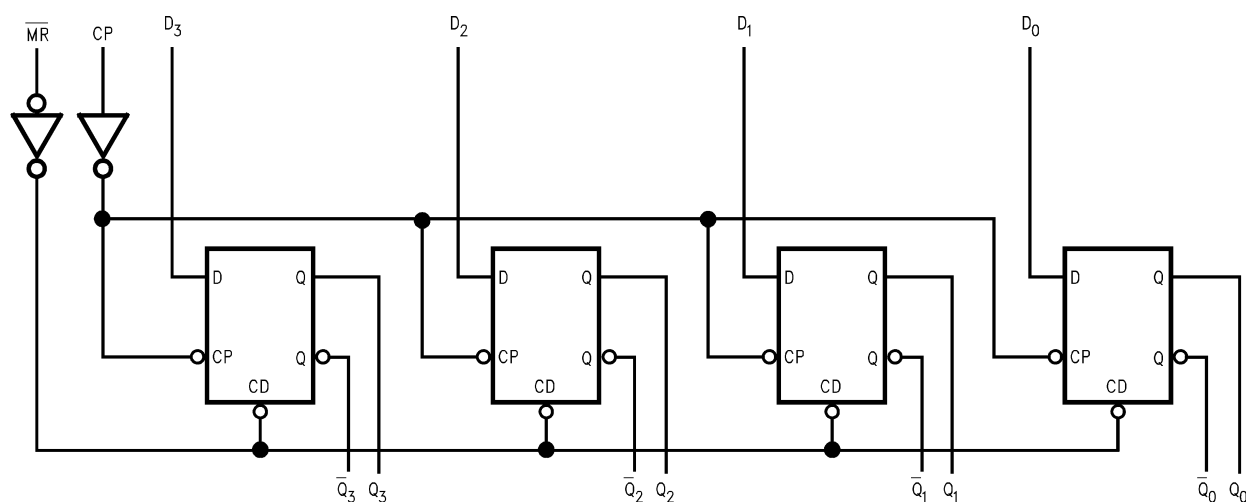
H = HIGH Voltage Level

L = LOW Voltage Level

t_n = Bit Time before Clock Pulse

t_{n+1} = Bit Time after Clock Pulse

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Rating
V_{CC}	Supply Voltage	-0.5V to +7.0V
V_{IN}	DC Input Voltage	-0.5V to +7.0V
V_{OUT}	DC Output Voltage	-0.5V to $V_{CC} + 0.5V$
I_{IK}	Input Diode Current	-20mA
I_{OK}	Output Diode Current	$\pm 20mA$
I_{OUT}	DC Output Current	$\pm 25mA$
I_{CC}	DC V_{CC} / GND Current	$\pm 50mA$
T_{STG}	Storage Temperature	-65°C to +150°C
T_L	Lead Temperature (Soldering, 10 seconds)	260°C

Recommended Operating Conditions⁽¹⁾

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Rating
V_{CC}	Supply Voltage	2.0V to +5.5V
V_{IN}	Input Voltage	0V to +5.5V
V_{OUT}	Output Voltage	0V to V_{CC}
T_{OPR}	Operating Temperature	-40°C to +85°C
t_r, t_f	Input Rise and Fall Time, $V_{CC} = 3.3V \pm 0.3V$ $V_{CC} = 5.0V \pm 0.5V$	0ns/V ~ 100ns/V 0ns/V ~ 20ns/V

Note:

1. Unused inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Symbol	Parameter	V _{CC} (V)	Conditions		T _A = 25°C			T _A = -40°C to +85°C		Units	
					Min.	Typ.	Max.	Min.	Max.		
V _{IH}	HIGH Level Input Voltage	2.0			1.50			1.50		V	
		3.0–5.5			0.7 x V _{CC}			0.7 x V _{CC}			
V _{IL}	LOW Level Input Voltage	2.0					0.50		0.50	V	
		3.0–5.5					0.3 x V _{CC}		0.3 x V _{CC}		
V _{OH}	HIGH Level Output Voltage	2.0	V _{IN} = V _{IH} or V _{IL}	I _{OH} = -50μA	1.9	2.0		1.9		V	
		3.0			2.9	3.0		2.9			
		4.5			4.4	4.5		4.4			
		3.0				I _{OH} = -4mA	2.58		2.48		
		4.5				I _{OH} = -8mA	3.94		3.80		
V _{OL}	LOW Level Output Voltage	2.0	V _{IN} = V _{IH} or V _{IL}	I _{OL} = 50μA		0.0	0.1		0.1	V	
		3.0				0.0	0.1		0.1		
		4.5				0.0	0.1		0.1		
		3.0				I _{OL} = 4mA		0.36	0.44		
		4.5				I _{OL} = 8mA		0.36	0.44		
I _{IN}	Input Leakage Current	0–5.5	V _{IN} = 5.5V or GND				±0.1		±1.0	μA	
I _{CC}	Quiescent Supply Current	5.5	V _{IN} = V _{CC} or GND				4.0		40.0	μA	

Noise Characteristics

Symbol	Parameter	V_{CC} (V)	$T_A = 25^\circ\text{C}$		Units	Conditions
			Typ.	Limits		
$V_{OLP}^{(2)}$	Quiet Output Maximum Dynamic V_{OL}	5.0	0.4	0.8	V	$C_L = 50\text{pF}$
$V_{OLV}^{(2)}$	Quiet Output Minimum Dynamic V_{OL}	5.0	–0.4	–0.8	V	$C_L = 50\text{pF}$
$V_{IHD}^{(2)}$	Minimum HIGH Level Dynamic Input Voltage	5.0		3.5	V	$C_L = 50\text{pF}$
$V_{ILD}^{(2)}$	Maximum LOW Level Dynamic Input Voltage	5.0		1.5	V	$C_L = 50\text{pF}$

Note:

2. Parameter guaranteed by design.

AC Electrical Characteristics

Symbol	Parameter	V _{CC} (V)	Conditions	T _A = 25°C			T _A = -40°C to +85°C		Units
				Min.	Typ.	Max.	Min.	Max.	
f _{MAX}	Maximum Clock Frequency	3.3 ± 0.3	C _L = 15pF	90	140		75		MHz
			C _L = 50pF	50	75		45		
		5.0 ± 0.5	C _L = 15pF	150	210		125		MHz
			C _L = 50pF	85	115		75		
t _{PLH} , t _{PHL}	Propagation Delay Time, (CP to Q _n or \overline{Q}_n)	3.3 ± 0.3	C _L = 15pF		7.5	11.5	1.0	13.5	ns
			C _L = 50pF		10.0	15.0	1.0	17.0	
		5.0 ± 0.5	C _L = 15pF		4.8	7.3	1.0	8.5	ns
			C _L = 50pF		6.3	9.3	1.0	10.5	
t _{PLH} , t _{PHL}	Propagation Delay Time, (MR to Q _n or \overline{Q}_n)	3.3 ± 0.3	C _L = 15pF		6.3	10.1	1.0	12.0	ns
			C _L = 50pF		8.8	13.6	1.0	15.5	
		5.0 ± 0.5	C _L = 15pF		4.3	6.4	1.0	7.5	ns
			C _L = 50pF		5.8	8.4	1.0	9.5	
t _{OSLH} , t _{OSHL}	Output to Output Skew	3.3 ± 0.3	C _L = 50pF			1.5		1.5	
		5.0 ± 0.5	C _L = 50pF ⁽³⁾			1.0		1.0	
C _{IN}	Input Capacitance		V _{CC} = Open		4	10		10	pF
C _{PD}	Power Dissipation Capacitance		⁽⁴⁾		44				pF

Notes:

3. Parameter guaranteed by design. $t_{OSLH} = |t_{PLHmax} - t_{PLHmin}|$; $t_{OSHL} = |t_{PHLmax} - t_{PHLmin}|$.

4. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained from the equation:

I_{CC} (opr.) = C_{PD} • V_{CC} • f_{IN} + I_{CC}/4 (per F/F), and the total C_{PD} when n pcs of the Flip-Flop operate can be calculated by the following equation: C_{PD} (total) = 30 + 14 • n

AC Operating Requirements

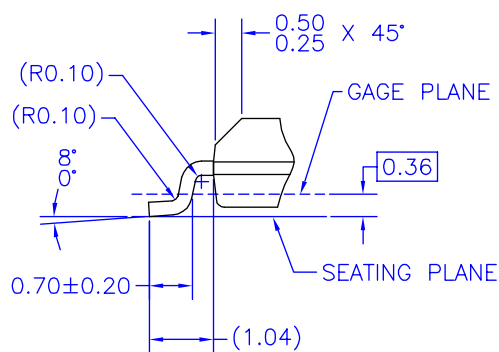
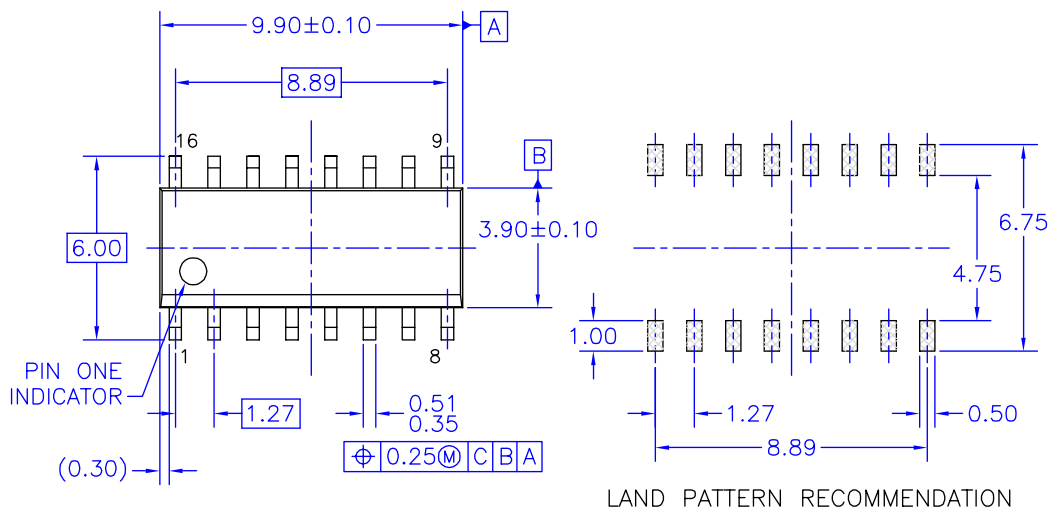
Symbol	Parameter	V _{CC} (V) ⁽⁵⁾	T _A = 25°C		T _A = −40°C to +85°C		Units
			Typ.	Guaranteed Minimum			
t _W (L), t _W (H)	Minimum Pulse Width (CP)	3.3		5.0	5.0	ns	
		5.0		5.0	5.0		
t _W (L)	Minimum Pulse Width (\overline{MR})	3.3		5.0	5.0	ns	
		5.0		5.0	5.0		
t _S	Minimum Setup Time (Dn to CP)	3.3		5.0	5.0	ns	
		5.0		4.0	4.0		
t _H	Minimum Hold Time (Dn to CP)	3.3		1.0	1.0	ns	
		5.0		1.0	1.0		
t _{REC}	Minimum Removal Time (\overline{MR})	3.3		5.0	5.0	ns	
		5.0		5.0	5.0		

Note:

5. V_{CC} is 3.3 ± 0.3V or 5.0 ± 0.5V

Physical Dimensions

Dimensions are in millimeters unless otherwise noted.



DETAIL A
SCALE: 2:1

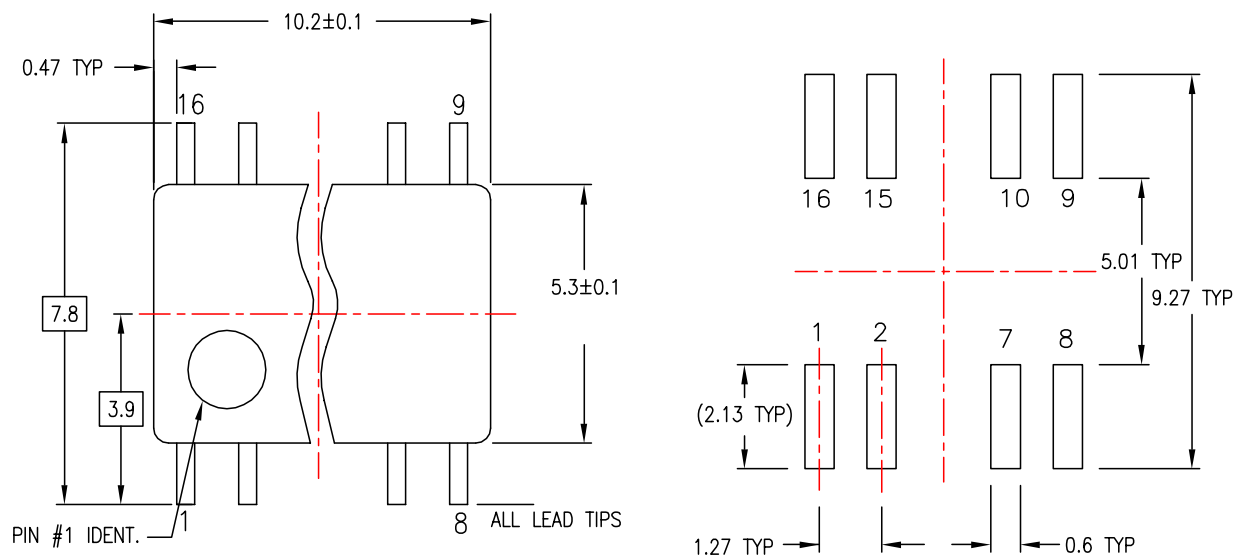
NOTES: UNLESS OTHERWISE SPECIFIED

- A) THIS PACKAGE CONFORMS TO JEDEC MS-012, VARIATION AC, ISSUE C, DATED MAY 1990.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.
- D) STANDARD LEAD FINISH:
200 MICROINCHES / 5.08 MICRONS MIN.
LEAD/TIN (SOLDER) ON COPPER.

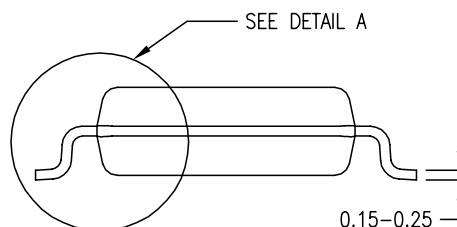
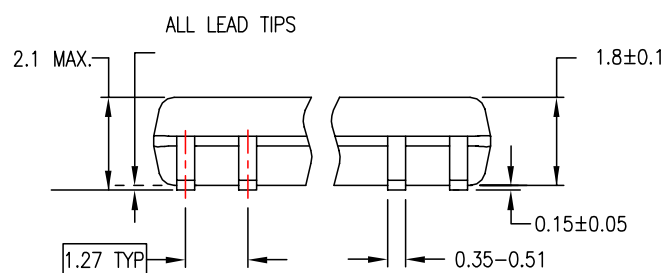
M16AREVK

Figure 1. 16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow Package Number M16A

Dimensions are in millimeters unless otherwise noted.



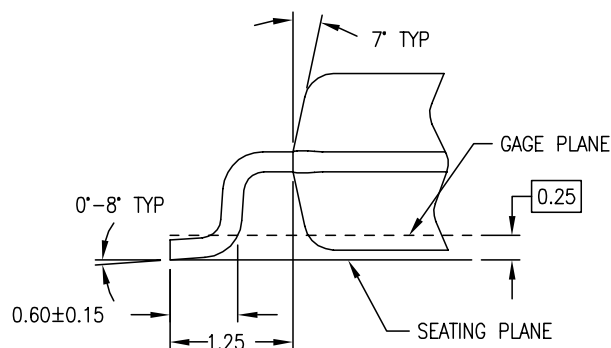
LAND PATTERN RECOMMENDATION



DIMENSIONS ARE IN MILLIMETERS

NOTES:

- A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.



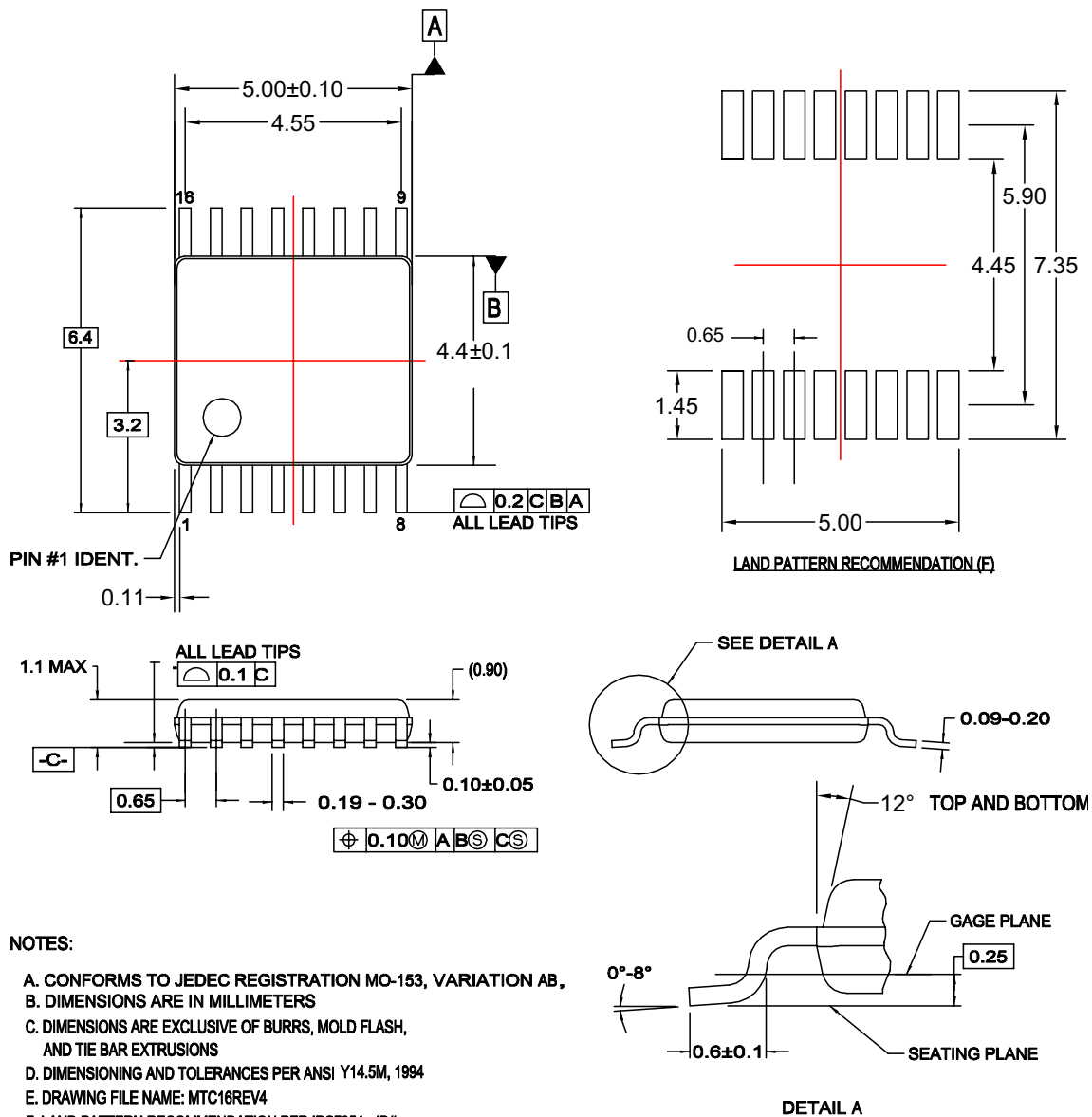
DETAIL A

M16DREVC

**Figure 2. 16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M16D**

Physical Dimensions (Continued)

Dimensions are in millimeters unless otherwise noted.




MTC16rev4

Figure 3. 16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide Package Number MTC16

TRADEMARKS

The following are registered and unregistered trademarks Fairchild Semiconductor owns or is authorized to use and is not intended to be an exhaustive list of all such trademarks.

ACE [®]	<i>i-Lo</i> [™]	Power-SPM [™]	TinyBoost [™]
Across the board. Around the world. [™]	ImpliedDisconnect [™]	PowerTrench [®]	TinyBuck [™]
ActiveArray [™]	IntelliMAX [™]	Programmable Active Droop [™]	TinyLogic [®]
Bottomless [™]	ISOPLANAR [™]	QFET [®]	TINYOPTO [™]
Build it Now [™]	MICROCOUPLER [™]	QS [™]	TinyPower [™]
CoolFET [™]	MicroPak [™]	QT Optoelectronics [™]	TinyWire [™]
CROSSVOLT [™]	MICROWIRE [™]	Quiet Series [™]	TruTranslation [™]
CTL [™]	Motion-SPM [™]	RapidConfigure [™]	μSerDes [™]
Current Transfer Logic [™]	MSX [™]	RapidConnect [™]	UHC [®]
DOVE [™]	MSXPro [™]	ScalarPump [™]	UniFET [™]
E ² CMOS [™]	OCX [™]	SMART START [™]	VCX [™]
EcoSPARK [®]	OCXPro [™]	SPM [®]	Wire [™]
EnSigna [™]	OPTOLOGIC [®]	STEALTH [™]	
FACT Quiet Series [™]	OPTOPLANAR [®]	SuperFET [™]	
FACT [®]	PACMAN [™]	SuperSOT [™] -3	
FAST [®]	PDP-SPM [™]	SuperSOT [™] -6	
FASTr [™]	POP [™]	SuperSOT [™] -8	
FPS [™]	Power220 [®]	SyncFET [™]	
FRFET [®]	Power247 [®]	TCM [™]	
GlobalOptoisolator [™]	PowerEdge [™]	The Power Franchise [®]	
GTO [™]	PowerSaver [™]		
HiSeC [™]			

DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS. THESE SPECIFICATIONS DO NOT EXPAND THE TERMS OF FAIRCHILD'S WORLDWIDE TERMS AND CONDITIONS, SPECIFICALLY THE WARRANTY THEREIN, WHICH COVERS THESE PRODUCTS.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION.

As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild Semiconductor. The datasheet is printed for reference information only.

Rev. I26

ON Semiconductor and  are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of ON Semiconductor's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using ON Semiconductor products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by ON Semiconductor. "Typical" parameters which may be provided in ON Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. ON Semiconductor does not convey any license under its patent rights nor the rights of others. ON Semiconductor products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use ON Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold ON Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that ON Semiconductor was negligent regarding the design or manufacture of the part. ON Semiconductor is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor
19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
USA/Canada

Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910

Japan Customer Focus Center
Phone: 81-3-5817-1050

ON Semiconductor Website: www.onsemi.com

Order Literature: <http://www.onsemi.com/orderlit>

For additional information, please contact your local
Sales Representative