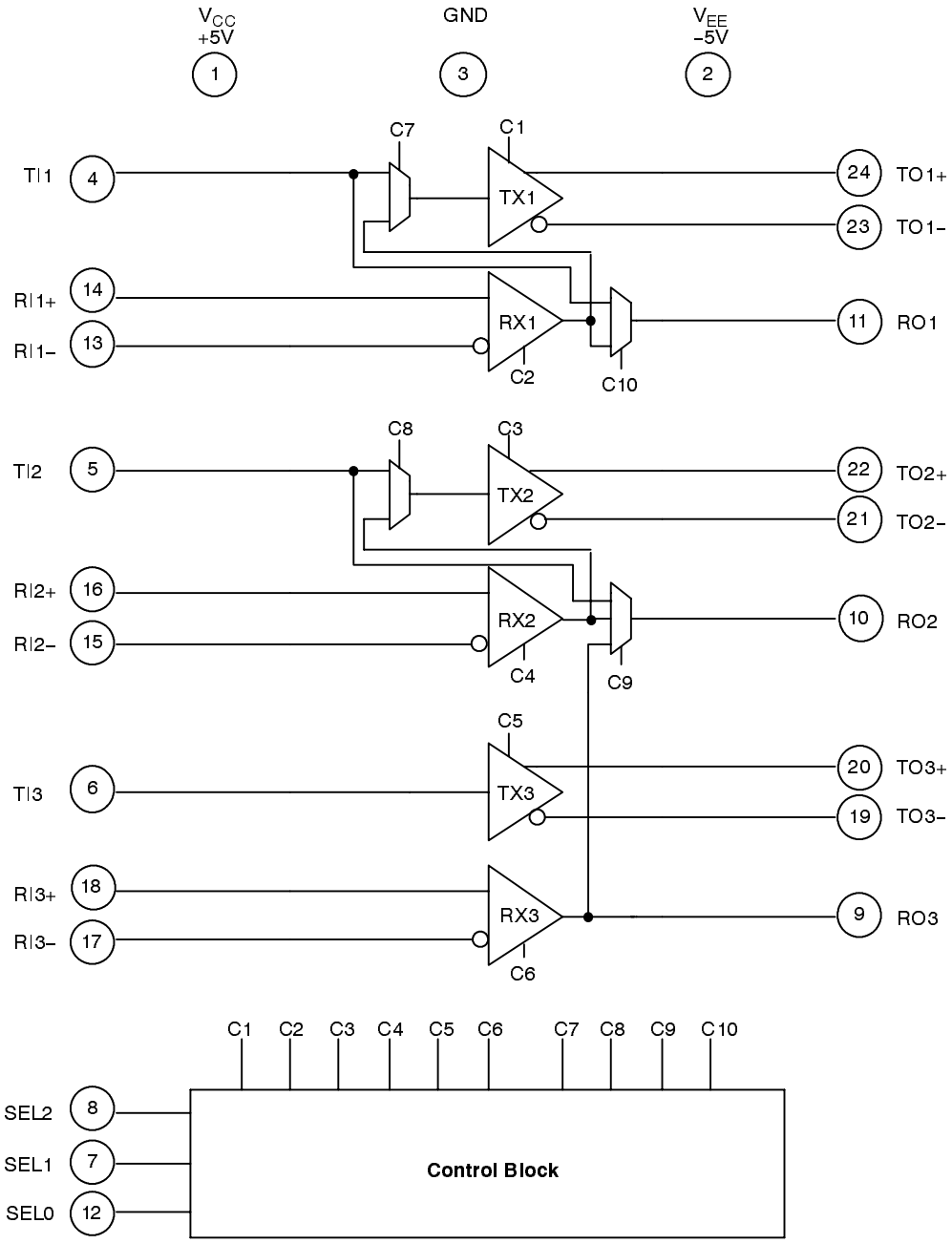
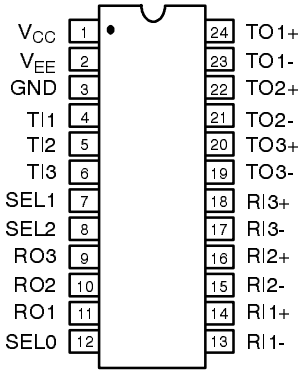
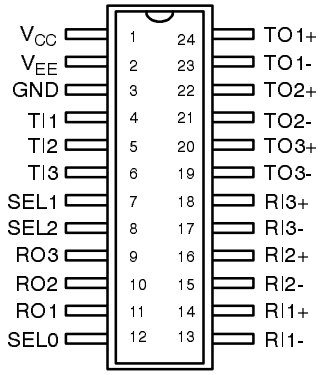


Figure 1. XR−T3590 Block Diagram

PIN CONFIGURATIONS



24 Lead PDIP (0.600")



24 Lead SOIC (0.300")

PIN DESCRIPTION

Pin #	Symbol	Type	Signal	Description
1	V_{CC}			+5 V (±0.25 V).
2	V_{EE}			-5 V (±0.25 V).
3	GND			Ground.
4	TI1	I	TTL	Transmitter 1 input.
5	TI2	I	TTL	Transmitter 2 input.
6	TI3	I	TTL	Transmitter 3 input.
7	SEL1	I	TTL	Mode select 1. (see *Table 1* for details)
8	SEL2	I	TTL	Mode select 2. (see *Table 1* for details)
9	RO3	O	TTL	Receiver 3 output.
10	RO2	O	TTL	Receiver 2 output.
11	RO1	O	TTL	Receiver 1 output.
12	SEL0	I	TTL	Mode select 0. (see *Table 1* for details)
13	RI1-	I	V.35	Receiver 1 negative input.
14	RI1+	I	V.35	Receiver 1 positive input.
15	RI2-	I	V.35	Receiver 2 negative input.
16	RI2+	I	V.35	Receiver 2 positive input.
17	RI3-	I	V.35	Receiver 3 negative input.
18	RI3+	I	V.35	Receiver 3 positive input.
19	TO3-	O	V.35	Transmitter 3 negative output.
20	TO3+	O	V.35	Transmitter 3 positive output.
21	TO2-	O	V.35	Transmitter 2 negative output.
22	TO2+	O	V.35	Transmitter 2 positive output.
23	TO1-	O	V.35	Transmitter 1 negative output.
24	TO1+	O	V.35	Transmitter 1 positive output.

DC ELECTRICAL CHARACTERISTICS

Test Conditions: V_{CC} = **+5.0V** ± 5%, V_{EE}=**-5.0V** ± 5%, T_A = **25°C**[1],driver and receiver are enabled unless otherwise specified. (See *Figure 2.*)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
$\|V_{OD}\|$	Transmitter Differential Output Voltage	***0.44***	0.55	***0.66***	V	-4V≤V_{OS}≤+4V
V_{OC}	Transmitter Common-Mode Output Voltage	***-0.3***	0	***+0.3***	V	V_{OS} = 0 V
I_{OH}	Transmitter Output High Current	**-12.6**	-11	***-9.4***	mA	
I_{OL}	Transmitter Output Low Current	**9.4**	11	**12.6**	mA	
I_{OZ}	Transmitter Output Leakage Current		±1	±100	µA	V_{TO+} = ±5V, V_{TO-} = ±5V While driver disabled
R_O	Transmitter Output Impedance		50		KΩ	
V_{TH}	Differential Receiver Input Threshold Voltage			*150*	mV	F=10 Mbps
V_{HYST}	Receiver Input Hysterisis		30		mV	V_{OS}=0V
I_{IN}	Receiver Input Current			***±0.4***	mA	-5V≤V_{RI}+, V_{RI}-≤5V
R_{IN}	Receiver Input Impedance Differential		35		KΩ	-5V≤V_{RI}+, V_{RI}-≤5V
V_{OH}	Receiver Output High Voltage	***3***	4.5		V	I_{OH}=-4mA
V_{OL}	Receiver Output Low Voltage		0.4	***0.8***	V	I_{OL}=4mA
I_{OSC}	Receiver Output Short-Circuit Current		13		mA	0≤V_O≤V_{CC}
I_{OZR}	Receiver Three-State Output Current			***±10***	µA	Receiver Disabled 0≤V_O≤V_{CC}
V_{IH}	Logic Input High Voltage	***2***			V	TIn, SEL2-0
V_{IL}	Logic Input Low Voltage			***0.8***	V	TIn, SEL2-0
I_{IN}	Logic Input Current		***±2.5***	***±10***	µA	TIn, SEL2-0
I_{CC}	V_{CC} Supply Current		36 250	***50***	mA µA	All On, Loaded, F=10Mbps All Off
I_{EE}	V_{EE} Supply Current		–38 –180	***–50***	mA µA	All On All Off

Notes

[1] *All currents flowing into the device pins are marked positive. All current flowing out of the device pins are marked negative.* ***Bold face parameters*** *are covered by production test and guaranteed over the operating temperature range. Italicized parameters are guaranteed over the full operating temperature range.*

Specifications are subject to change without notice

AC ELECTRICAL CHARACTERISTICS

Test Conditions: V_{CC} = **+5.0V** ± 5%, V_{EE}=**-5.0V** ± 5%, T_A = **25°C**[1], driver and receiver are enabled unless otherwise specified.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
T_R, T_F	Transmitter Rise or Fall Time		5	***30***	ns	V_{OS}=0V
T_{TPLH}	Transmitter Input to Output Propagation Delay		25	***40***	ns	V_{OS}=0V
T_{TPHL}	Transmitter Input to Output Propagation Delay		27	***40***	ns	V_{OS}=0V
T_{OSKEW}	Transmitter Output to Output Skew		***3***		ns	V_{OS}=0V
T_{RPLH}	Receiver Input to Output Propagation Delay (rising)		37	***50***	ns	V_{OS}=0V
T_{RPHL}	Receiver Input to Output Propagation Delay (falling)		35	***50***	ns	V_{OS}=0V
T_{ISKEW}	Differential Receiver Skew (T_{RPLH} – T_{RPHL})		***2***		ns	V_{OS}=0V
T_{ZL}	Receiver Enable to Output Low		34		ns	
T_{ZH}	Receiver Enable to Output High		37		ns	
T_{LZ}	Receiver Disable to Output Low		55		ns	
T_{HZ}	Receiver Disable to Output High		57		ns	

Notes

[1] All currents flowing into the device pins are marked positive. All current flowing out of the device pins are marked negative.

***Bold face parameters** are covered by production test and guaranteed over the operating temperature range. Italicized parameters are guaranteed over the full operating temperature range.*

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . -65°C to +150°C
Operating Temperature . . . . . -40°C to +85°C
Supply Voltage . . . . . ±7V

SEL2	SEL1	SEL0	Drivers On	Receivers On	Description
0	0	0			All off
0	0	1		1, 2, 3	All receivers on
0	1	0	1, 2, 3	1, 2	DCE mode
0	1	1	1, 2, 3	1, 2	DCE mode with mirrored loopback
1	0	0	1, 2	1, 2, 3	DTE mode
1	0	1	1, 2	1, 2, 3	DTE mode with mirrored loopback
1	1	0	1, 2, 3	1, 2, 3	All on
1	1	1	1, 2, 3		All drivers on

Note: *The driver and receiver outputs which are not on, are placed in Hi-Z state.*

Table 1. Function Table

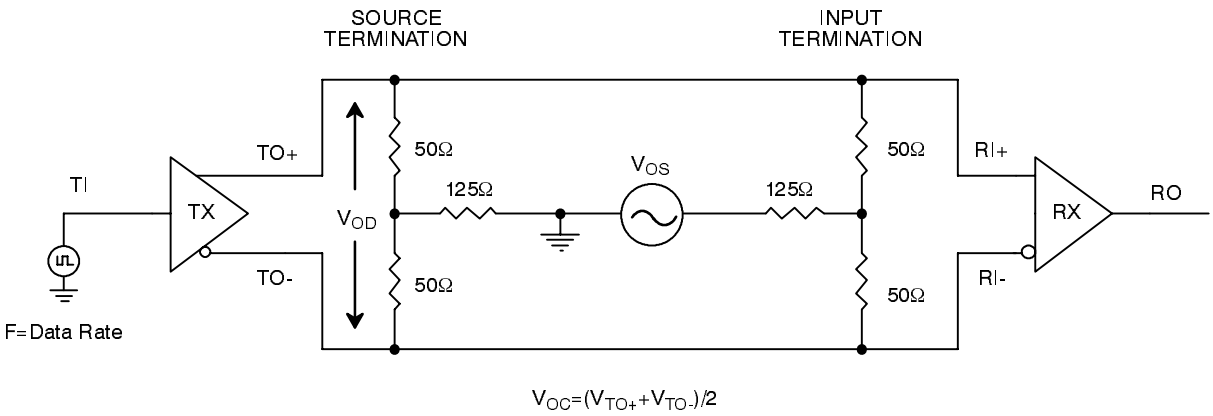


Figure 2. XR-T3590 Test Circuit

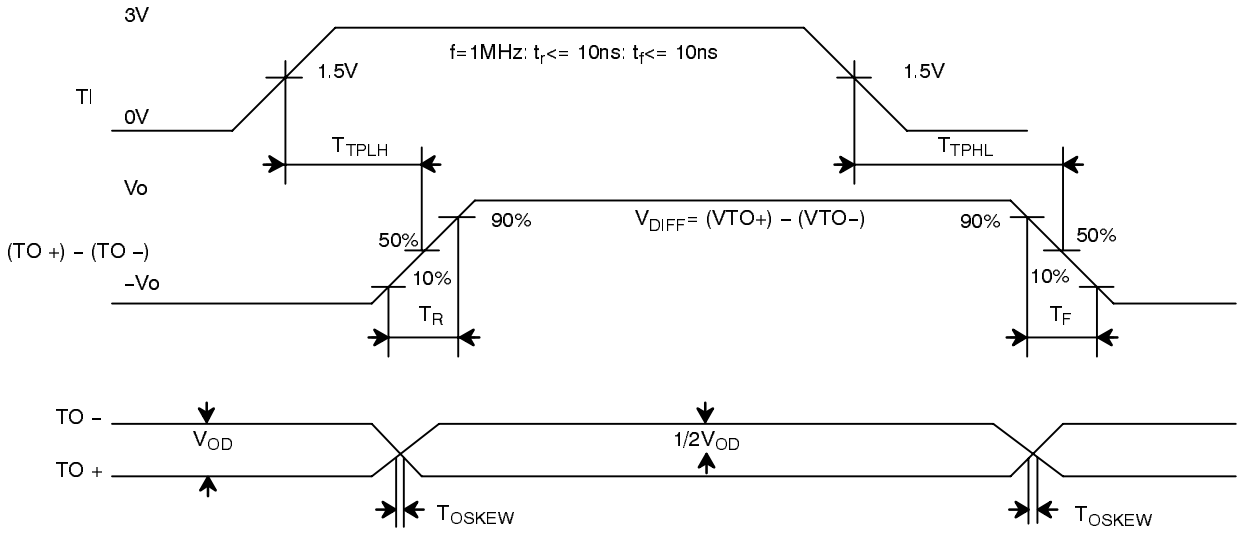


Figure 3. V.35 Transmitter Propagation Delays

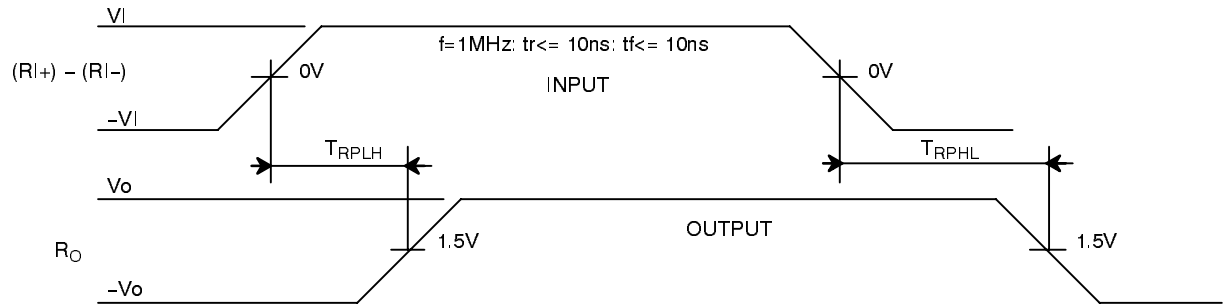


Figure 4. V.35 Receiver Propagation Delays

Cable Termination

For proper operation, the differential inputs and outputs of the XR-T3590 must be properly terminated. This is a requirement to assure full adherence to V.35 electrical signal specifications. The following diagram is a proposed termination configuration:

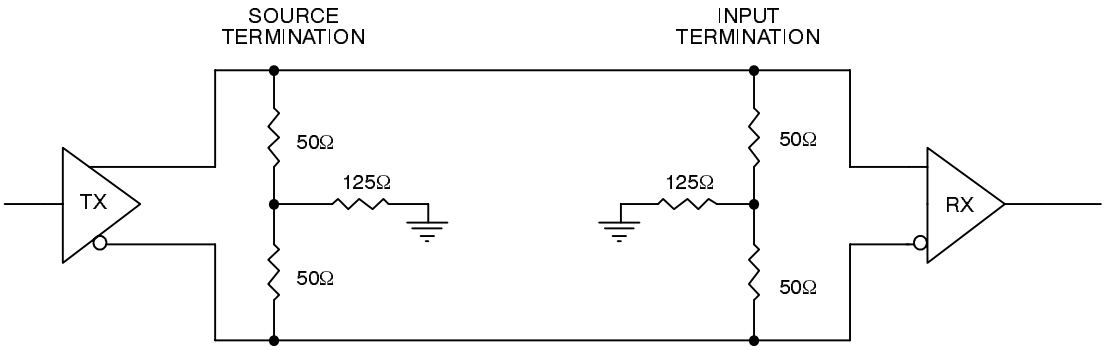


Figure 5. Proposed Source And Input Terminations

Note: *In order to implement the terminations proposed above, standard 1/8W surface mount or through hole 5% resistors can be used. Furthermore, appropriate resistor networks can be used as well.*

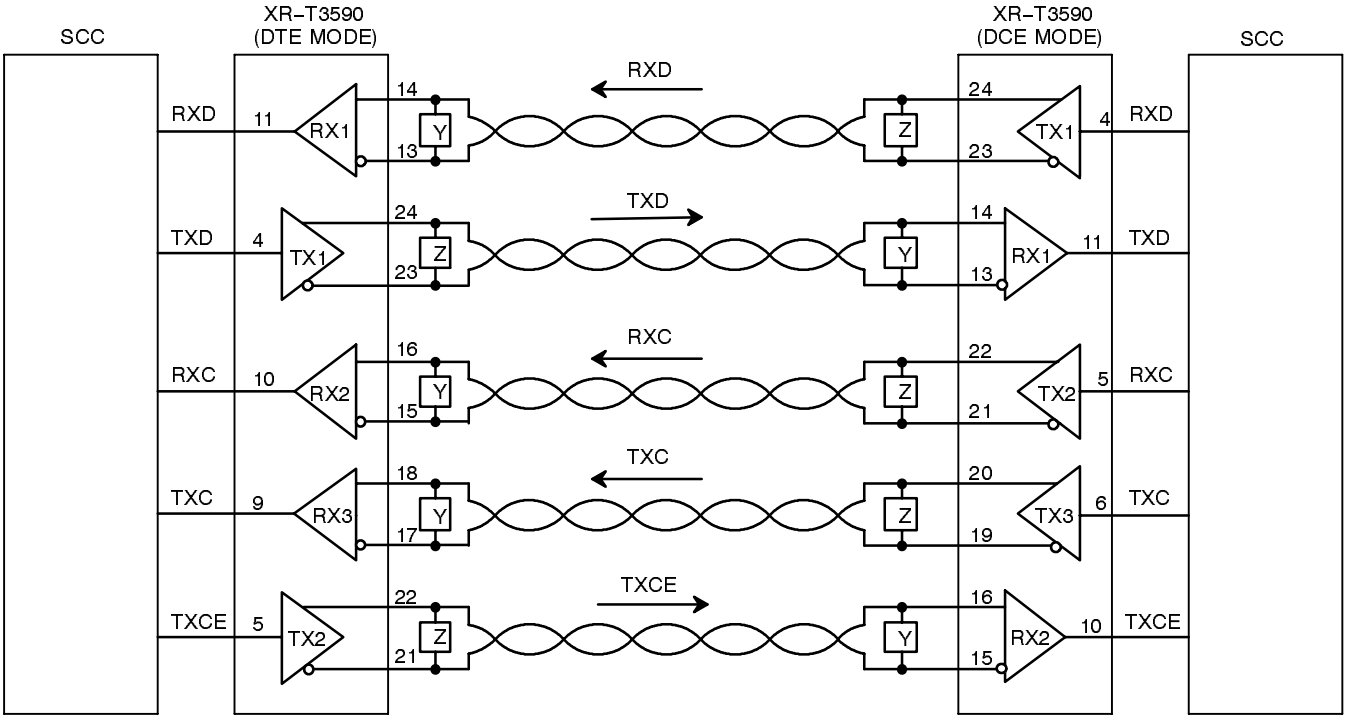


Figure 6. Typical V.35 Clock And Data Configuration

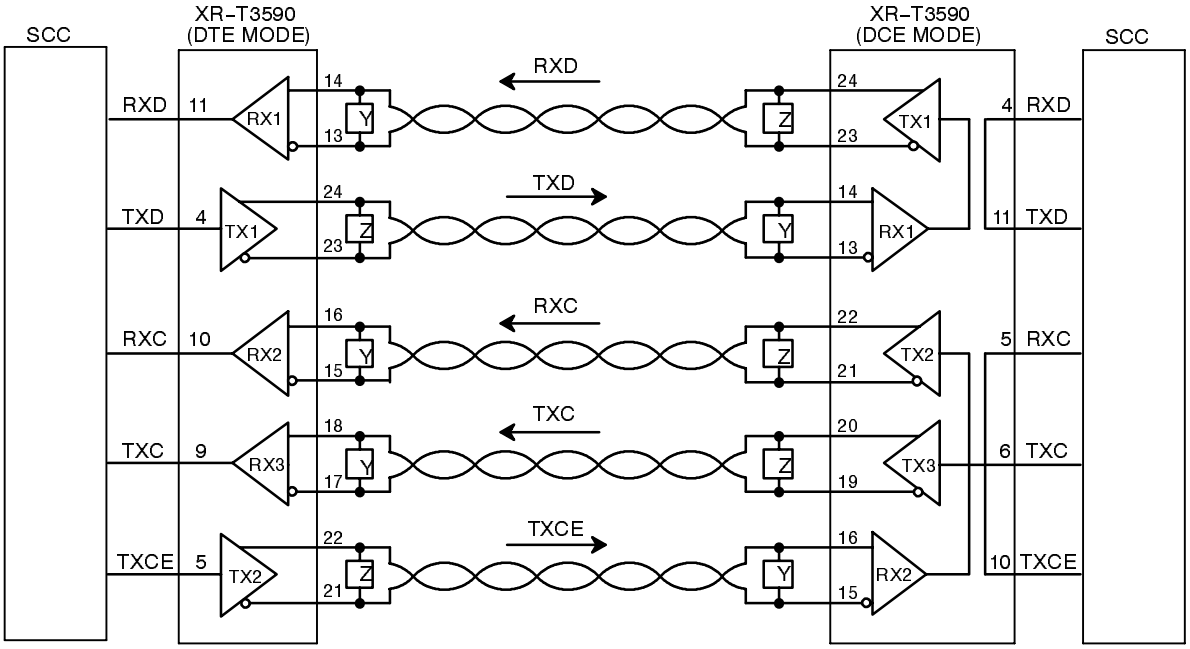


Figure 7. Typical V.35 Configuration During DCE Mirrored Loop Back

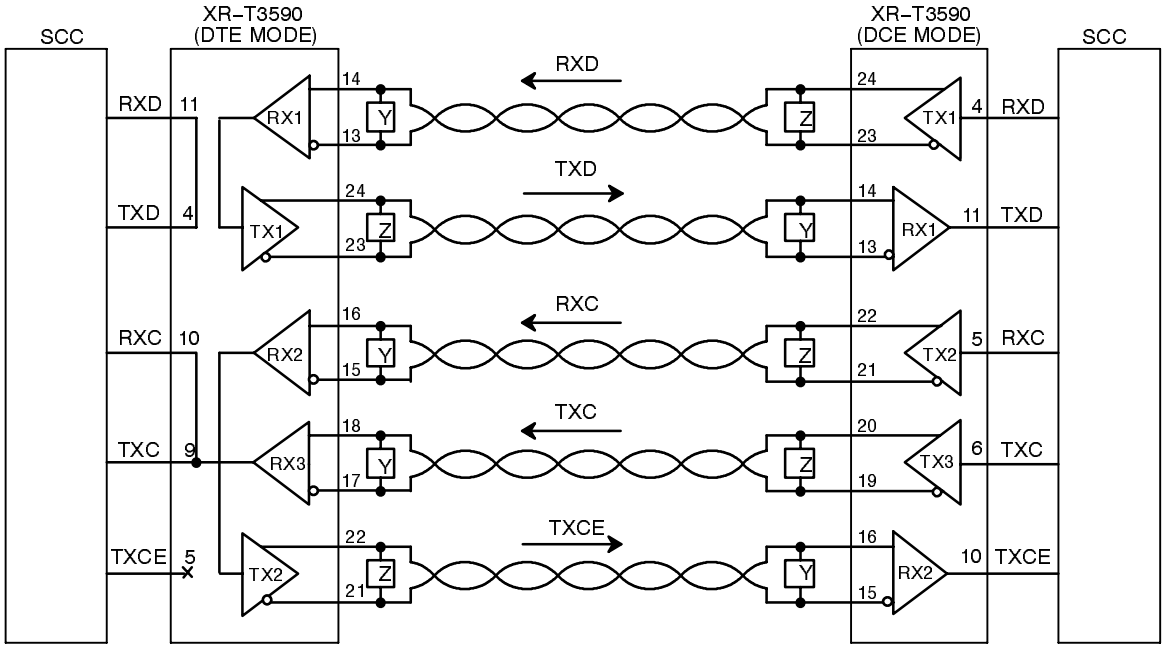


Figure 8. Typical V.35 Configuration During DTE Mirrored Loop Back

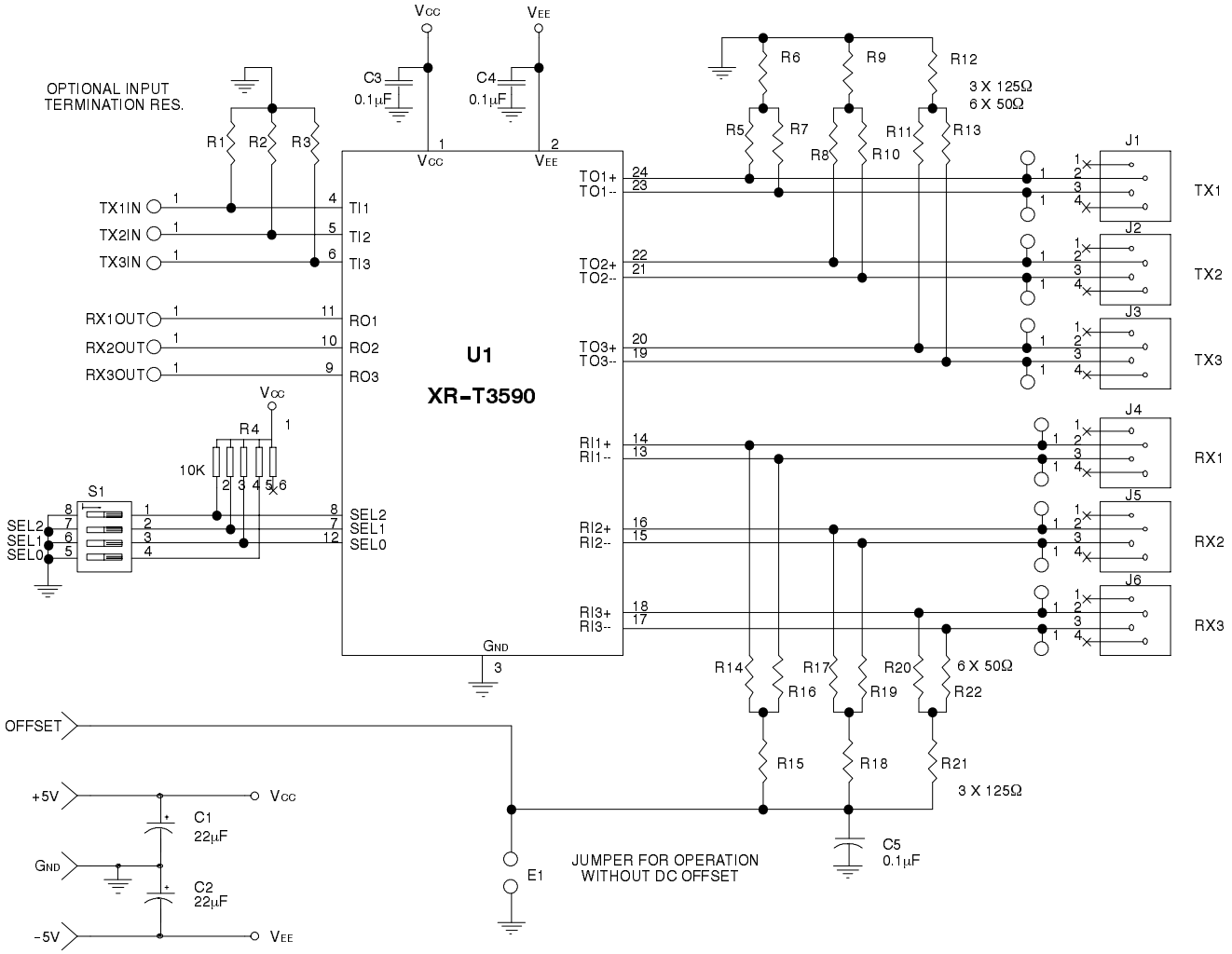
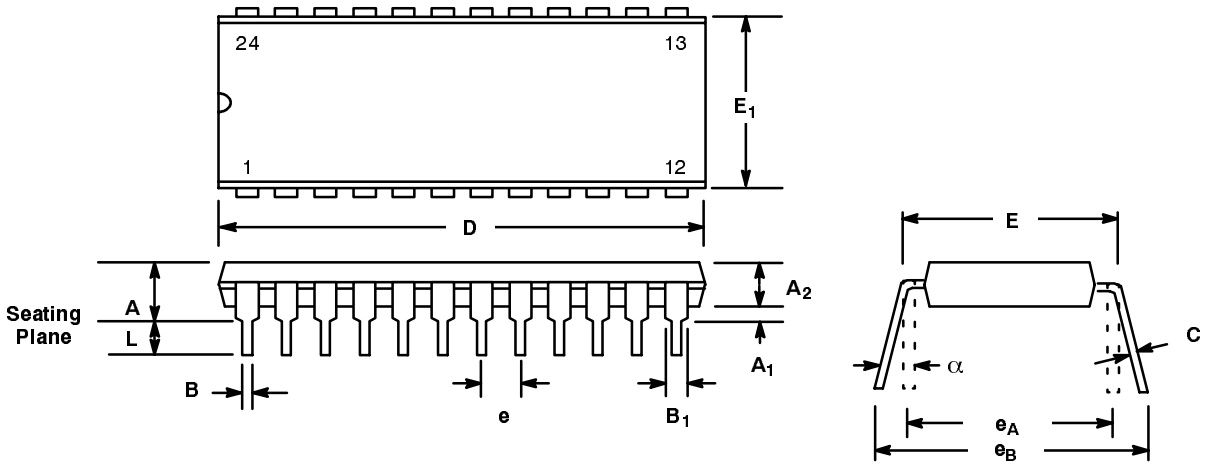


Figure 9. XR-T3590 Demo Board

24 LEAD PLASTIC DUAL-IN-LINE (600 MIL PDIP)

Rev. 1.00

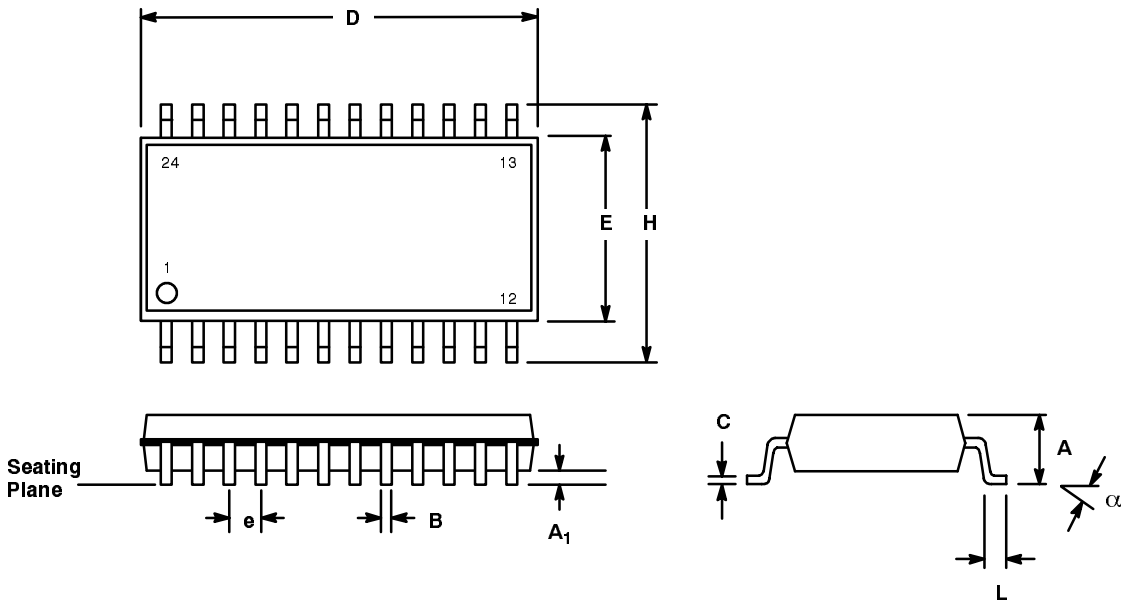


SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.160	0.250	4.06	6.35
A_1	0.015	0.070	0.38	1.78
A_2	0.125	0.195	3.18	4.95
B	0.014	0.024	0.36	0.56
B_1	0.030	0.070	0.76	1.78
C	0.008	0.014	0.20	0.38
D	1.150	1.290	29.21	32.77
E	0.600	0.625	15.24	15.88
E_1	0.485	0.580	12.32	14.73
e	0.100 BSC		2.54 BSC	
e_A	0.600 BSC		15.24 BSC	
e_B	0.600	0.700	15.24	17.78
L	0.115	0.200	2.92	5.08
α	0°	15°	0°	15°

Note: The control dimension is the inch column

24 LEAD SMALL OUTLINE
(300 MIL JEDEC SOIC)

Rev. 1.00



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.093	0.104	2.35	2.65
A1	0.004	0.012	0.10	0.30
B	0.013	0.020	0.33	0.51
C	0.009	0.013	0.23	0.32
D	0.598	0.614	15.20	15.60
E	0.291	0.299	7.40	7.60
e	0.050 BSC		1.27 BSC	
H	0.394	0.419	10.00	10.65
L	0.016	0.050	0.40	1.27
α	0°	8°	0°	8°

Note: The control dimension is the millimeter column

Notes

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Datasheet November 1998