

Contents

1	Block diagram and pin description	5
2	Electrical specifications	7
2.1	Absolute maximum ratings	7
2.2	Thermal data	8
2.3	Electrical characteristics	9
2.4	Electrical characteristics curves	19
3	Application information	21
3.1	GND protection network against reverse battery	21
3.1.1	Solution 1: resistor in the ground line (RGND only)	21
3.1.2	Solution 2: diode (DGND) in the ground line	22
3.2	Load dump protection	22
3.3	MCU I/Os protection	22
3.4	Maximum demagnetization energy (VCC = 24 V)	23
4	Package and PCB thermal data	24
4.1	PowerSSO-24 thermal data	24
5	Package and packing information	27
5.1	PowerSSO-24 mechanical data	27
5.2	PowerSSO-24 packing information	30
6	Order codes	31
7	Revision history	32

List of tables

Table 1.	Pin function	5
Table 2.	Suggested connections for unused and not connected pins	6
Table 3.	Absolute maximum ratings	7
Table 4.	Thermal data.	8
Table 5.	Power section	9
Table 6.	Switching ($V_{CC} = 24\text{ V}$; $T_j = 25\text{ °C}$)	9
Table 7.	Logic inputs.	10
Table 8.	Protections and diagnostics	11
Table 9.	Current sense ($8\text{ V} < V_{CC} < 36\text{ V}$)	11
Table 10.	Open-load detection ($V_{FR_STBY} = 5\text{ V}$)	13
Table 11.	Truth table.	17
Table 12.	Electrical transient requirements (part 1)	18
Table 13.	Electrical transient requirements (part 2)	18
Table 14.	Electrical transient requirements (part 3)	18
Table 15.	Thermal parameters	26
Table 16.	PowerSSO-24 mechanical data	28
Table 17.	Device summary	31
Table 18.	Document revision history	32

List of figures

Figure 1.	Block diagram	5
Figure 2.	Configuration diagram PowerSSO-24 (top view)	6
Figure 3.	Current and voltage conventions	7
Figure 4.	T_{reset} definition	10
Figure 5.	T_{stby} definition	11
Figure 6.	Current sense delay characteristics	13
Figure 7.	Open-load off-state delay timing	13
Figure 8.	Output stuck to V_{CC} detection delay time at FR_{STBY} activation	14
Figure 9.	Switching characteristics	14
Figure 10.	Delay response time between rising edge of output current and rising edge of current sense	15
Figure 11.	Output voltage drop limitation	15
Figure 12.	Device behavior in overload condition	16
Figure 13.	Off-state output current	19
Figure 14.	High level input current	19
Figure 15.	Input clamp voltage	19
Figure 16.	Input low level voltage	19
Figure 17.	Input high level voltage	19
Figure 18.	Input hysteresis voltage	19
Figure 19.	On-state resistance vs T_{case}	20
Figure 20.	On-state resistance vs V_{CC}	20
Figure 21.	I_{LIMH} vs T_{case}	20
Figure 22.	Turn-on voltage slope	20
Figure 23.	Turn-off voltage slope	20
Figure 24.	Application schematic	21
Figure 25.	Maximum turn-off current versus inductance	23
Figure 26.	PowerSSO-24 PC board	24
Figure 27.	$R_{\text{thj-amb}}$ vs PCB copper area in open box free air condition (one channel ON)	24
Figure 28.	PowerSSO-24 thermal impedance junction ambient single pulse (one channel ON)	25
Figure 29.	Thermal fitting model of a double channel HSD in PowerSSO-24	25
Figure 30.	PowerSSO-24 package dimensions	27
Figure 31.	PowerSSO-24 tube shipment (no suffix)	30
Figure 32.	PowerSSO-24 tape and reel shipment (suffix "TR")	30

1 Block diagram and pin description

Figure 1. Block diagram

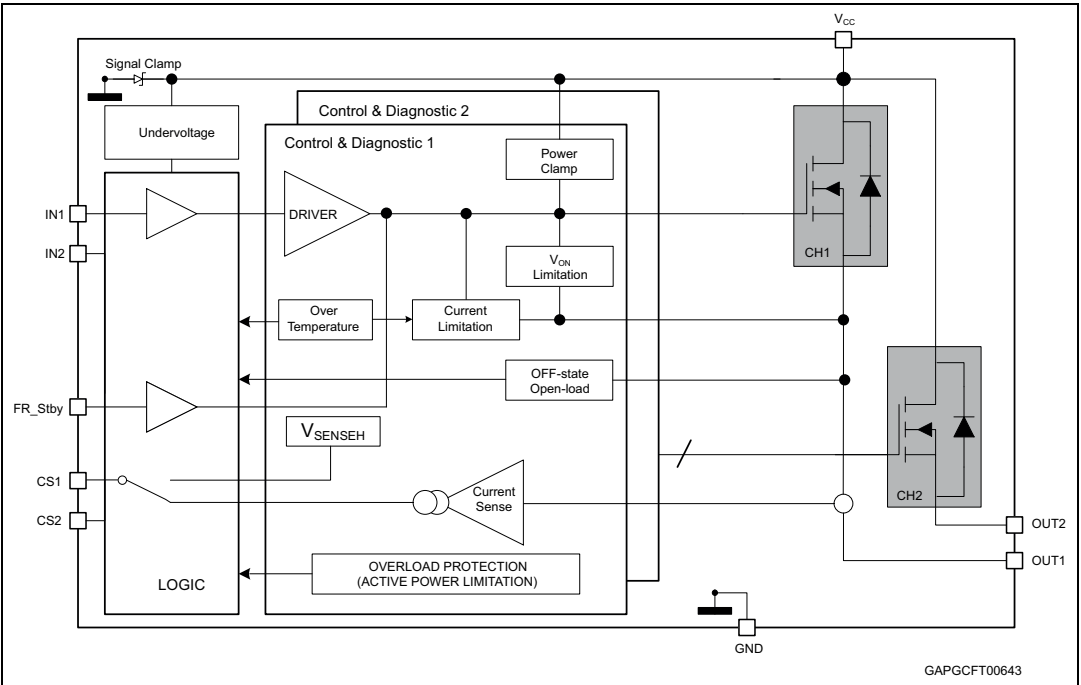


Table 1. Pin function

Name	Function
V _{CC}	Battery connection
OUT _{1,2}	Power output
GND	Ground connection
IN _{1,2}	Voltage controlled input pins with hysteresis, CMOS compatible. They control output switch state
CS _{1,2}	Analog current sense pins, they deliver a current proportional to the load current
FR_Stby	In case of latch-off for overtemperature/overcurrent conditions, a low pulse on the FR_Stby pin is needed to reset the channel. The device enters in standby mode if all inputs and the FR_Stby pin are low.

Figure 2. Configuration diagram PowerSSO-24 (top view)

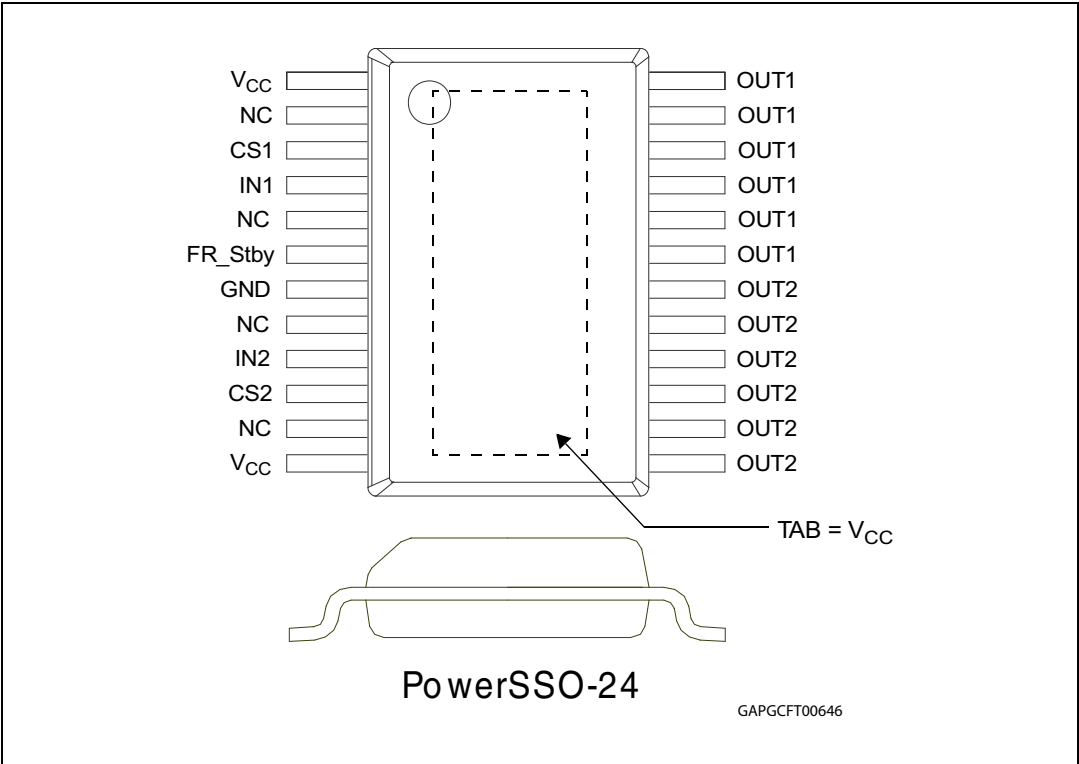


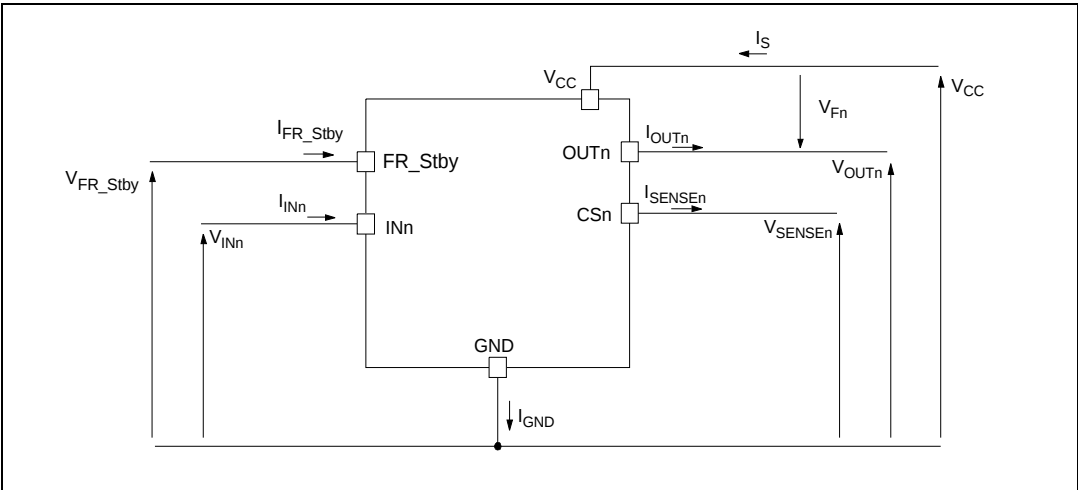
Table 2. Suggested connections for unused and not connected pins

Connection / pin	Current Sense	N.C.	Output	Input	FR_Stby
Floating	Not allowed	X ⁽¹⁾	X	X	X
To ground	Through 10 kΩ resistor	X	Not allowed	Through 10 kΩ resistor	Through 10 kΩ

1. X: do not care.

2 Electrical specifications

Figure 3. Current and voltage conventions



Note: $V_{Fn} = V_{OUTn} - V_{CC}$ during reverse battery condition.

2.1 Absolute maximum ratings

Stressing the device above the ratings listed in [Table 3](#) may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to the conditions reported in this section for extended periods may affect device reliability.

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	DC supply voltage	58	V
$-V_{CC}$	Reverse DC supply voltage	0.3	V
$-I_{GND}$	DC reverse ground pin current	200	mA
I_{OUT}	DC output current	Internally limited	A
$-I_{OUT}$	Reverse DC output current	30	A
I_{IN}	DC input current	-1 to 10	mA
I_{FR_Stby}	Fault reset standby DC input current	-1 to 1.5	mA
$-I_{CSENSE}$	DC reverse CS pin current	200	mA
V_{CSENSE}	Current sense maximum voltage	$V_{CC} - 58$ to $+V_{CC}$	V
E_{MAX}	Maximum switching energy $L = 50 \text{ mH}$; $V_{bat} = 32 \text{ V}$; $T_{jstart} = 150^\circ\text{C}$; $I_{OUT} = 2 \text{ A}$	210	mJ

Table 3. Absolute maximum ratings (continued)

Symbol	Parameter	Value	Unit
L_{smax}	Maximum strain inductance in short circuit condition $R_L = 300\text{ m}\Omega$, $V_{batt} = 32\text{ V}$, $T_{jstart} = 150^\circ\text{C}$, $I_{out} = I_{LMHmax}$	40	μH
V_{ESD}	Electrostatic discharge (Human Body Model: $R = 1.5\text{ k}\Omega$; $C = 100\text{ pF}$)		
	– $IN_{1,2}$	4000	V
	– $CS_{1,2}$	2000	V
	– FR_Stby	4000	V
	– $OUT_{1,2}$	5000	V
	– V_{CC}	5000	V
V_{ESD}	Charge device model (CDM-AEC-Q100-011)	750	V
T_j	Junction operating temperature	-40 to 150	$^\circ\text{C}$
T_{stg}	Storage temperature	-55 to 150	$^\circ\text{C}$

2.2 Thermal data

Table 4. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case (max.) (with one channel ON)	2.4	$^\circ\text{C/W}$
$R_{thj-amb}$	Thermal resistance junction-ambient (max.)	See Figure 27	$^\circ\text{C/W}$

2.3 Electrical characteristics

8 V < V_{CC} < 36 V; -40°C < T_j < 150°C, unless otherwise specified.

Table 5. Power section

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{CC}	Operating supply voltage		8	24	36	V
V_{USD}	Undervoltage shutdown			3.5	5	V
$V_{USDhyst}$	Undervoltage shutdown hysteresis			0.5		V
R_{ON}	On-state resistance ⁽¹⁾	$I_{OUT} = 2\text{ A}$; $T_j = 25^\circ\text{C}$		50		mΩ
		$I_{OUT} = 2\text{ A}$; $T_j = 150^\circ\text{C}$			100	
V_{clamp}	Clamp voltage	$I_S = 20\text{ mA}$	58	64	70	V
I_S	Supply current	Off-state; $V_{CC} = 24\text{ V}$; $T_j = 25^\circ\text{C}$; $V_{IN} = V_{OUT} = V_{SENSE} = 0\text{ V}$		2 ⁽²⁾	5 ⁽²⁾	μA
		On-state; $V_{CC} = 24\text{ V}$; $V_{IN} = 5\text{ V}$; $I_{OUT} = 0\text{ A}$		4.2	6	mA
$I_{L(off)}$	Off-state output current	$V_{IN} = V_{OUT} = 0\text{ V}$; $V_{CC} = 24\text{ V}$; $T_j = 25^\circ\text{C}$	0	0.01	3	μA
		$V_{IN} = V_{OUT} = 0\text{ V}$; $V_{CC} = 24\text{ V}$; $T_j = 125^\circ\text{C}$	0		5	
V_F	Output - V_{CC} diode voltage	$-I_{OUT} = 2\text{ A}$; $T_j = 150^\circ\text{C}$			0.7	V

1. For each channel

2. PowerMOS leakage included

Table 6. Switching ($V_{CC} = 24\text{ V}$; $T_j = 25^\circ\text{C}$)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$R_L = 12\ \Omega$		30		μs
$t_{d(off)}$	Turn-off delay time	$R_L = 12\ \Omega$		40		μs
$dV_{OUT}/dt_{(on)}$	Turn-on voltage slope	$R_L = 12\ \Omega$	0.7 V/μs			V/μs
$dV_{OUT}/dt_{(off)}$	Turn-off voltage slope	$R_L = 12\ \Omega$	0.8 V/μs			V/μs
W_{ON}	Switching energy losses during t_{won}	$R_L = 12\ \Omega$		0.5		mJ
W_{OFF}	Switching energy losses during t_{woff}	$R_L = 12\ \Omega$		0.3		mJ

Table 7. Logic inputs

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IL}	Input low level voltage				0.9	V
I_{IL}	Low level input current	$V_{IN} = 0.9\text{ V}$	1			μA
V_{IH}	Input high level voltage		2.1			V
I_{IH}	High level input current	$V_{IN} = 2.1\text{ V}$			10	μA
$V_{I(hyst)}$	Input hysteresis voltage		0.25			V
V_{ICL}	Input clamp voltage	$I_{IN} = 1\text{ mA}$	5.5		7	V
		$I_{IN} = -1\text{ mA}$		-0.7		V
$V_{FR_Stby_L}$	Fault reset standby low level voltage				0.9	V
$I_{FR_Stby_L}$	Low level fault reset standby current	$V_{FR_Stby} = 0.9\text{ V}$	1			μA
$V_{FR_Stby_H}$	Fault reset standby high level voltage		2.1			V
$I_{FR_Stby_H}$	High level fault reset standby current	$V_{FR_Stby} = 2.1\text{ V}$			10	μA
$V_{FR_Stby(hyst)}$	Fault reset standby hysteresis voltage		0.25			V
$V_{FR_Stby_CL}$	Fault reset standby clamp voltage	$I_{FR_Stby} = 15\text{ mA (t < 10 ms)}$	11		15	V
		$I_{FR_Stby} = -1\text{ mA}$		-0.7		V
t_{reset}	Overload latch-off reset time	See Figure 4	2		24	μs
t_{stby}	Standby delay	See Figure 5	120		1200	μs

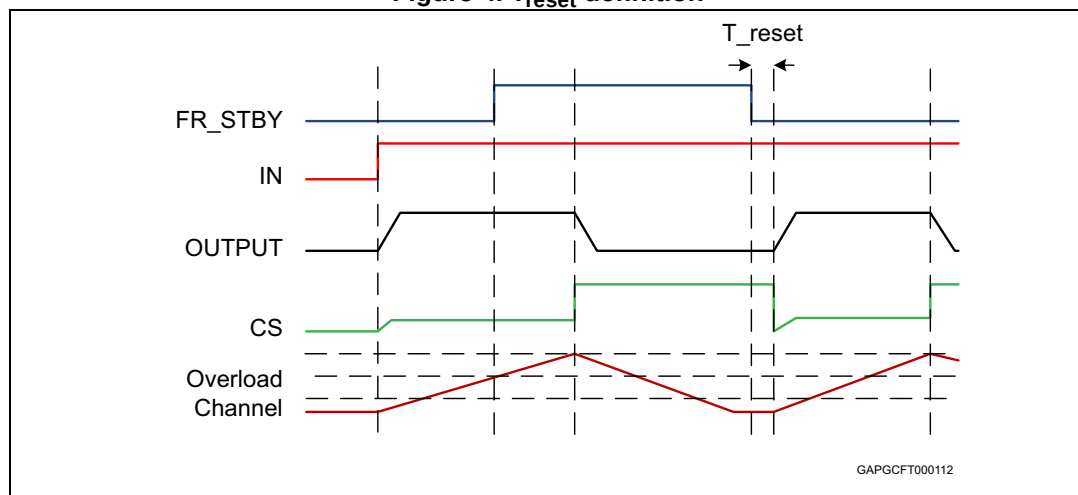
Figure 4. T_{reset} definition

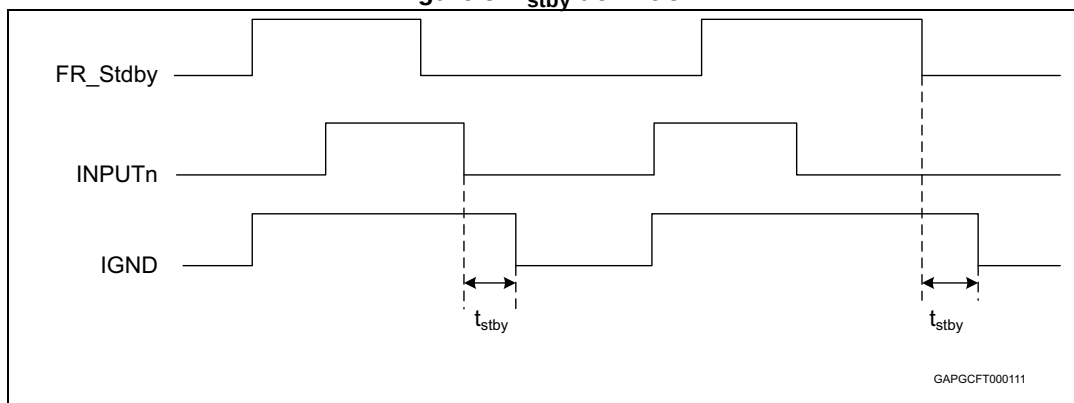
Figure 5. T_{stby} definition

Table 8. Protections and diagnostics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{limH}	DC short circuit current	$V_{CC} = 24\text{ V}$	24	34	46	A
		$5\text{ V} < V_{CC} < 36\text{ V}$			46	A
I_{limL}	Short circuit current during thermal cycling	$V_{CC} = 24\text{ V};$ $T_R < T_j < T_{TSD}$		8.5		A
T_{TSD}	Shutdown temperature		150	175	200	°C
T_R	Reset temperature		$T_{RS} + 1$	$T_{RS} + 5$		°C
T_{RS}	Thermal reset of status		135			°C
T_{HYST}	Thermal hysteresis ($T_{TSD} - T_R$)			7		°C
V_{DEMAC}	Turn-off output voltage clamp	$I_{OUT} = 2\text{ A}; V_{IN} = 0;$ $L = 6\text{ mH}$	$V_{CC} - 58$	$V_{CC} - 64$	$V_{CC} - 70$	V
V_{ON}	Output voltage drop limitation	$I_{OUT} = 100\text{ mA}$		25		mV

Table 9. Current sense ($8\text{ V} < V_{CC} < 36\text{ V}$)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
K_{ol}		$I_{OUT} = 10\text{ mA}; V_{SENSE} = 0.5\text{ V};$ $T_j = -40^\circ\text{C to } 150^\circ\text{C}$ $T_j = 25^\circ\text{C to } 150^\circ\text{C}$	564 972	2800	5563 4895	
K_{led}		$I_{OUT} = 50\text{ mA}; V_{SENSE} = 0.5\text{ V};$ $T_j = -40^\circ\text{C to } 150^\circ\text{C}$ $T_j = 25^\circ\text{C to } 150^\circ\text{C}$	1193 1416	2650	4268 3958	
dK/K_{totled}	Current sense ratio drift	$I_{OUT} = 12\text{ mA to } 60\text{ mA};$ $V_{SENSE} = 0.5\text{ V}; I_{cal} = 35\text{ mA}$	-35		35	%
K_0	I_{OUT}/I_{SENSE}	$I_{OUT} = 100\text{ mA}; V_{SENSE} = 0.5\text{ V};$ $T_j = -40^\circ\text{C to } 150^\circ\text{C}$	1409	2540	3726	
$dK_0/K_0^{(1)}$	Current sense ratio drift	$I_{OUT} = 100\text{ mA}; V_{SENSE} = 0.5\text{ V};$ $T_j = -40^\circ\text{C to } 150^\circ\text{C}$	-20		20	%

Table 9. Current sense (8 V < V_{CC} < 36 V) (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
K ₁	I _{OUT} /I _{SENSE}	I _{OUT} = 0.7 A; V _{SENSE} = 2 V; T _J = -40 °C to 150 °C	1597	2190	2764	
dK ₁ /K ₁ ⁽¹⁾	Current sense ratio drift	I _{OUT} = 0.7 A; V _{SENSE} = 2 V; T _J = -40 °C to 150 °C	-15		15	%
K ₂	I _{OUT} /I _{SENSE}	I _{OUT} = 2 A; V _{SENSE} = 2 V; T _J = -40 °C...150 °C	1850	2190	2550	
dK ₂ /K ₂ ⁽¹⁾	Current sense ratio drift	I _{OUT} = 2 A; V _{SENSE} = 2 V; T _J = -40 °C to 150 °C	-10		+10	%
K ₃	I _{OUT} /I _{SENSE}	I _{OUT} = 8 A; V _{SENSE} = 4 V; T _J = -40 °C to 150 °C	2050	2190	2280	
dK ₃ /K ₃ ⁽¹⁾	Current sense ratio drift	I _{OUT} = 8 A; V _{SENSE} = 4 V; T _J = -40 °C to 150 °C	-3		3	%
I _{SENSE0}	Analog sense leakage current	I _{OUT} = 0 A; V _{SENSE} = 0 V; V _{IN} = 0 V; T _J = -40 °C to 150 °C	0		1	μA
		I _{OUT} = 0 A; V _{SENSE} = 0 V; V _{IN} = 5 V; T _J = -40 °C to 150 °C	0		2	μA
V _{SENSE}	Max analog sense output voltage	I _{OUT} = 8 A; R _{SENSE} = 3.9 kΩ	5			V
V _{SENSEH}	Analog sense output voltage in fault condition ⁽²⁾	V _{CC} = 24 V; R _{SENSE} = 3.9 kΩ	7.5	8.5	9.5	V
I _{SENSEH}	Analog sense output current in fault condition ⁽²⁾	V _{CC} = 24 V; V _{SENSE} = 5 V	4.9	7	12	mA
t _{DSENSE2H}	Delay response time from rising edge of INPUT pins	V _{SENSE} < 4 V; 0.15 A < I _{OUT} < 8 A; I _{SENSE} = 90 % of I _{SENSE max} (see Figure 6)		150	300	μs
Δt _{DSENSE2H}	Delay response time between rising edge of output current and rising edge of current sense	V _{SENSE} < 4 V; I _{SENSE} = 90% of I _{SENSEMAX} , I _{OUT} = 90% of I _{OUTMAX} I _{OUTMAX} = 2 A (see Figure 10)			250	μs
t _{DSENSE2L}	Delay response time from falling edge of INPUT pins	V _{SENSE} < 4 V, 0.15 A < I _{OUT} < 8 A I _{SENSE} = 10 % of I _{SENSE max} (see Figure 6)		5	20	μs

1. Parameter guaranteed by design; it is not tested.

2. Fault condition includes: power limitation, overtemperature and open load in off-state condition.

Table 10. Open-load detection ($V_{FR_STBY} = 5\text{ V}$)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{OL}	Open-load off-state voltage detection threshold	$V_{IN} = 0\text{ V}$; $8\text{ V} < V_{CC} < 36\text{ V}$	2	—	4	V
t_{DSTKON}	Output short circuit to V_{CC} detection delay at turn off	See Figure 7	180	—	1800	μs
$I_{L(off2)}$	Off-state output current at $V_{OUT} = 4\text{ V}$	$V_{IN} = 0\text{ V}$; $V_{SENSE} = 0\text{ V}$; V_{OUT} rising from 0 V to 4 V	-120	—	0	μA
t_{d_vol}	Delay response from output rising edge to V_{SENSE} rising edge in openload	$V_{OUT} = 4\text{ V}$; $V_{IN} = 0\text{ V}$; $V_{SENSE} = 90\%$ of V_{SENSEH} $R_{sense} = 3.9\text{ K}$		—	20	μs
t_{DFRSTK_ON}	Output short circuit to V_{CC} detection delay at FRSTBY activation	See Figure 10 ; Input _{1,2} = low		—	50	μs

Figure 6. Current sense delay characteristics

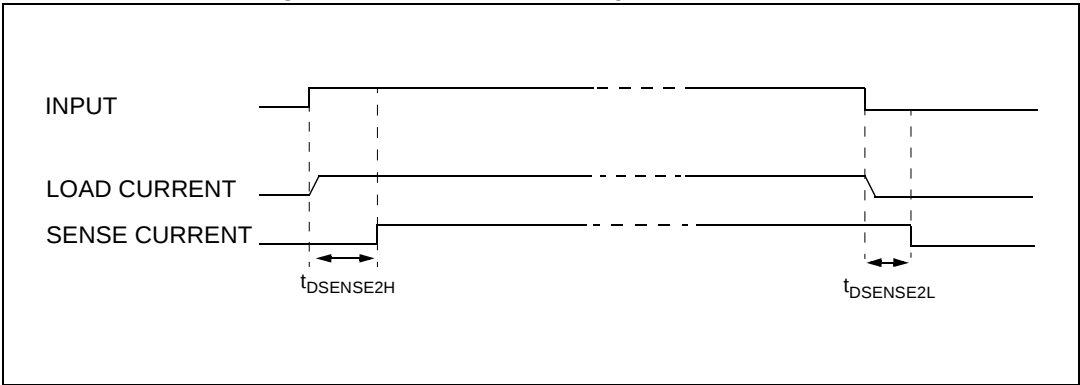
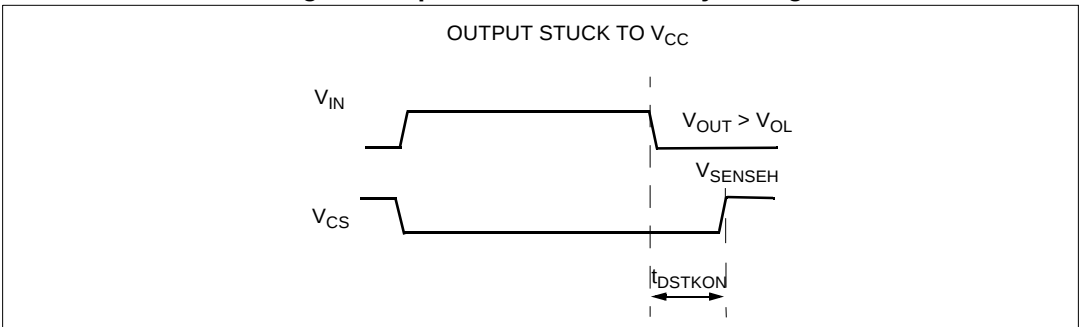


Figure 7. Open-load off-state delay timing



1. $V_{fr_stby} = \text{high}$.

Figure 8. Output stuck to V_{CC} detection delay time at FR_{STBY} activation

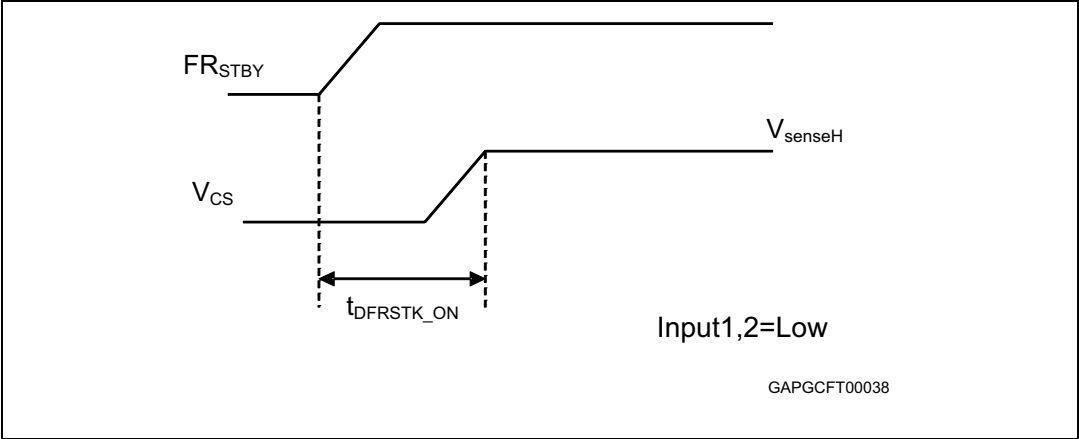


Figure 9. Switching characteristics

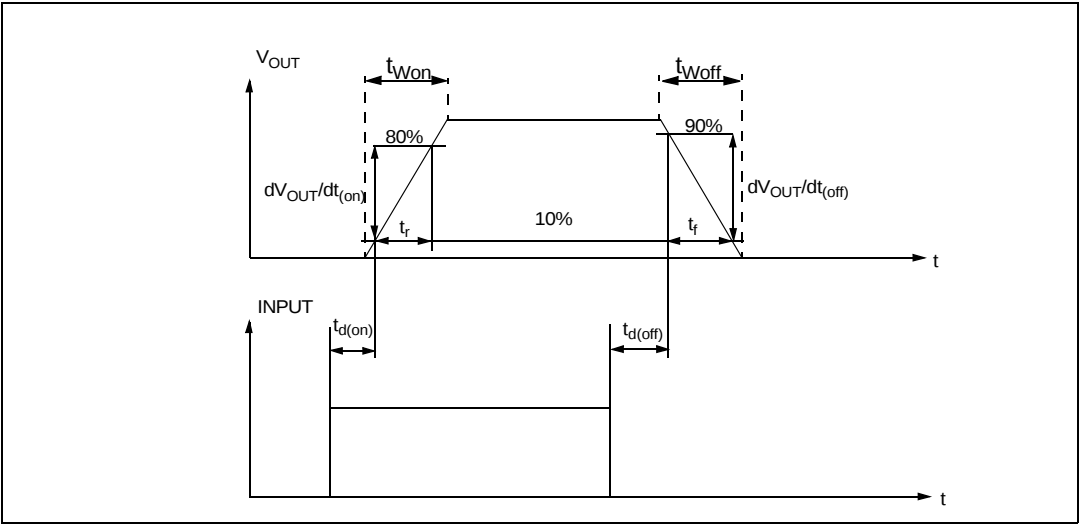


Figure 10. Delay response time between rising edge of output current and rising edge of current sense

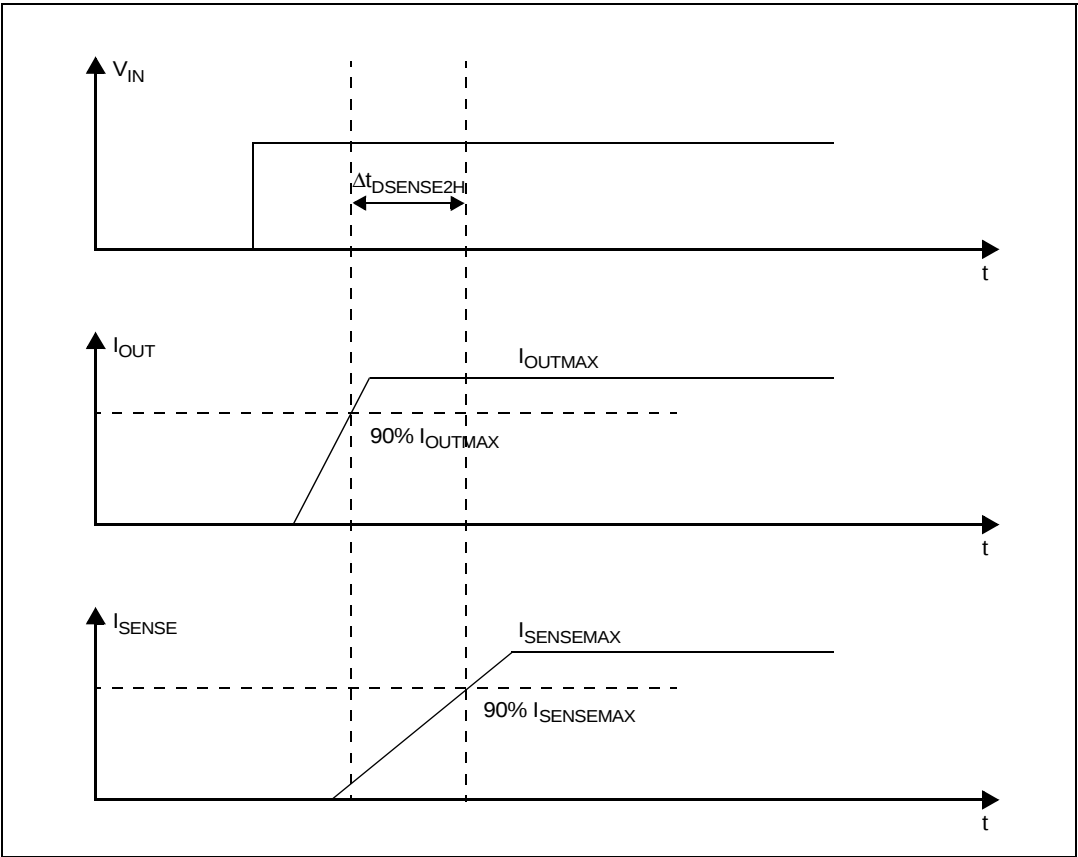


Figure 11. Output voltage drop limitation

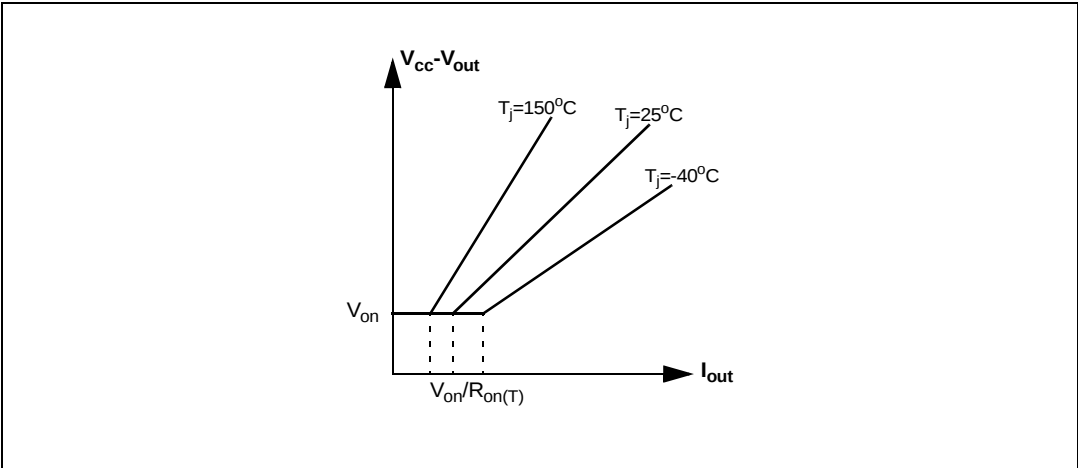


Figure 12. Device behavior in overload condition

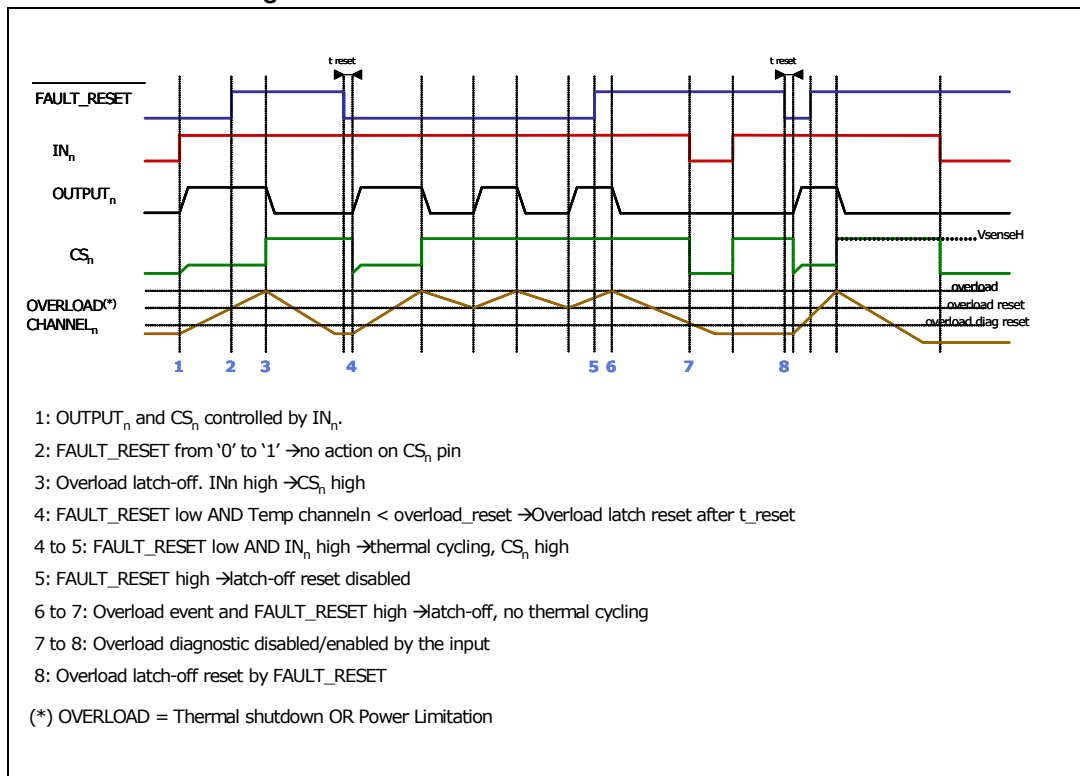


Table 11. Truth table

Conditions	Fault reset standby	Input	Output	Sense
Standby	L	L	L	0
Normal operation	X	L	L	0
	X	H	H	Nominal
Overload	X	L	L	0
	X	H	H	> Nominal
Overtemperature / short to ground	X	L	L	0
	L	H	Cycling	V_{SENSEH}
	H	H	Latched	V_{SENSEH}
Undervoltage	X	X	L	0
Short to V_{BAT}	L	L	H	0
	H	L	H	V_{SENSEH}
	X	H	H	< Nominal
Open load off-state (with pull-up)	L	L	H	0
	H	L	H	V_{SENSEH}
	X	H	H	0
Negative output voltage clamp	X	L	Negative	0

Table 12. Electrical transient requirements (part 1)

ISO 7637-2: 2004(E) Test pulse	Test levels ⁽¹⁾		Number of pulses or test times	Burst cycle/pulse repetition time		Delays and impedance
	III	IV				
1	- 450 V	- 600 V	5000 pulses	0.5 s	5 s	1 ms, 50 Ω
2a	+ 37 V	+ 50 V	5000 pulses	0.2 s	5 s	50 μ s, 2 Ω
3a	- 150 V	- 200 V	1h	90 ms	100 ms	0.1 μ s, 50 Ω
3b	+ 150 V	+ 200 V	1h	90 ms	100 ms	0.1 μ s, 50 Ω
4	- 12 V	- 16 V	1 pulse			100 ms, 0.01 Ω
5b ⁽¹⁾	+ 123 V	+ 174 V	1 pulse			350 ms, 1 Ω

1. Valid in case of external load dump clamp: 58 V maximum referred to ground.

Table 13. Electrical transient requirements (part 2)

ISO 7637-2: 2004(E) Test pulse	Test level results ⁽¹⁾	
	III	IV
1	C	C
2a	C	C
3a	C	C
3b ⁽²⁾	E	E
3b ⁽³⁾	C	C
4	C	C
5b ⁽⁴⁾	C	C

1. In order to guarantee the ISO transient classes a minimum 10 k Ω protection resistors are needed on logic pins.
2. Without capacitor between V_{CC} and GND.
3. With 10 nF between V_{CC} and GND.
4. External load dump clamp, 58 V maximum, referred to ground.

Table 14. Electrical transient requirements (part 3)

Class	Contents
C	All functions of the device are performed as designed after exposure to disturbance.
E	One or more functions of the device are not performed as designed after exposure to disturbance and cannot be returned to proper operation without replacing the device.

2.4 Electrical characteristics curves

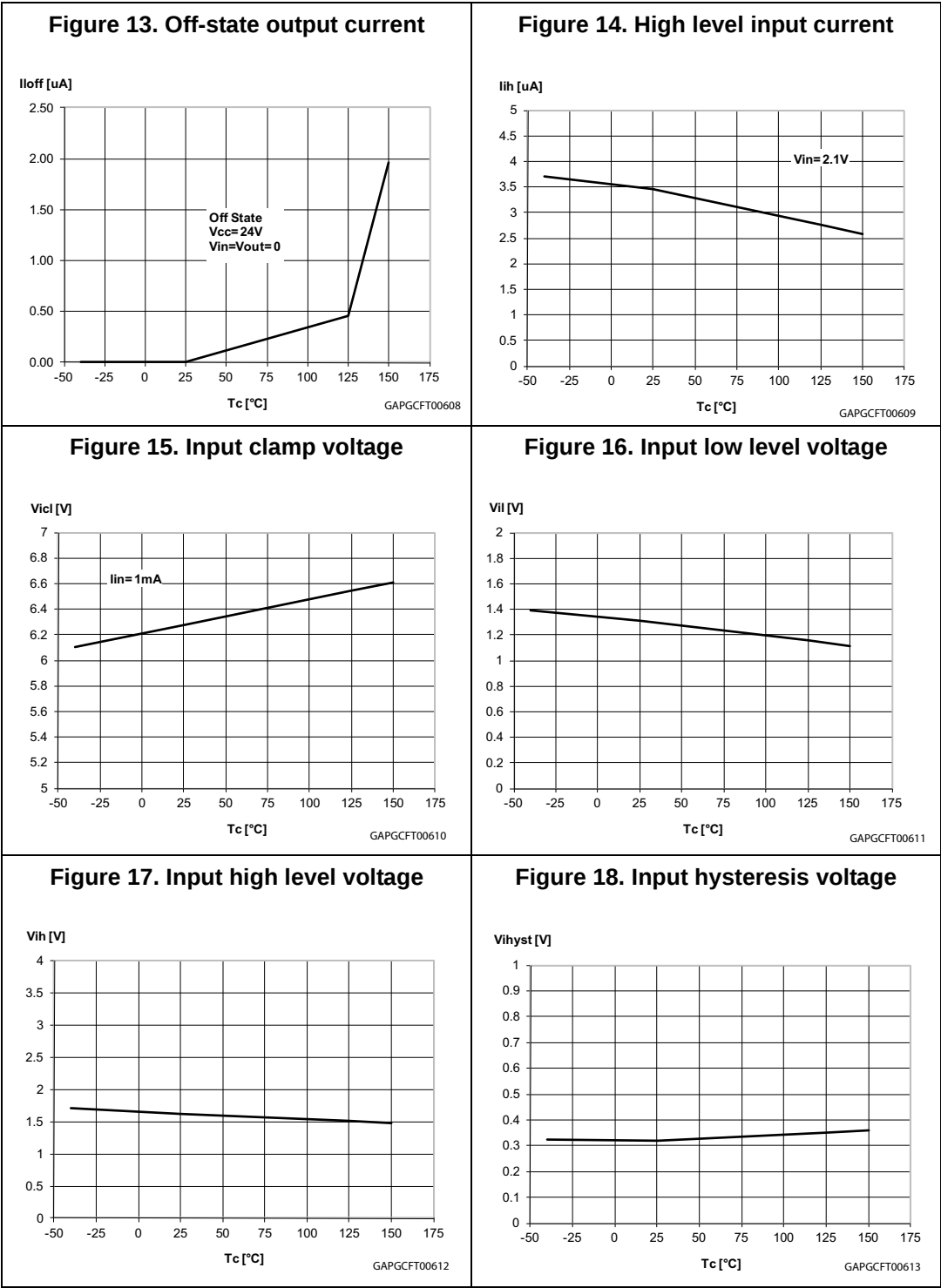


Figure 19. On-state resistance vs T_{case}

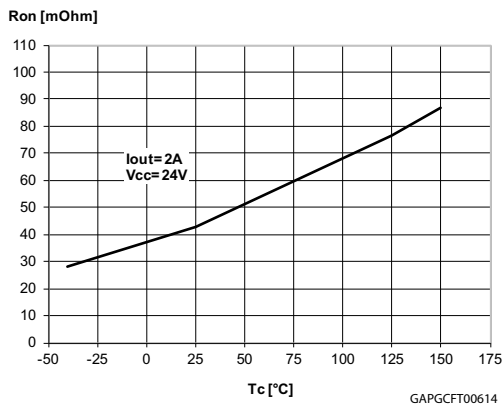


Figure 20. On-state resistance vs V_{CC}

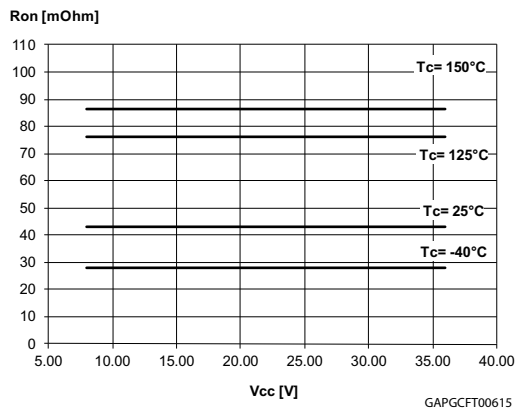


Figure 21. I_{LIMH} vs T_{case}

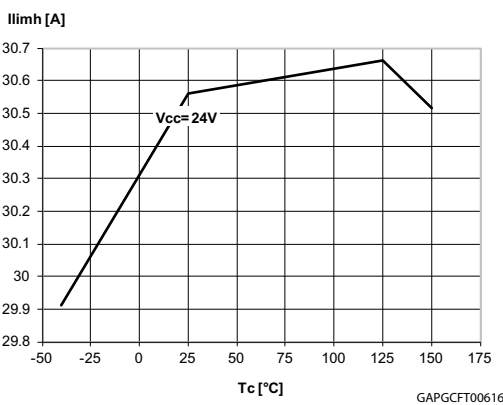


Figure 22. Turn-on voltage slope

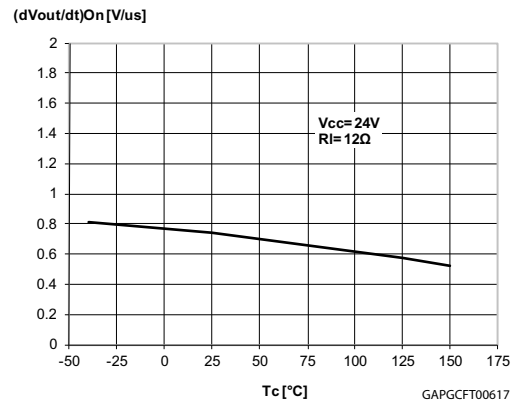
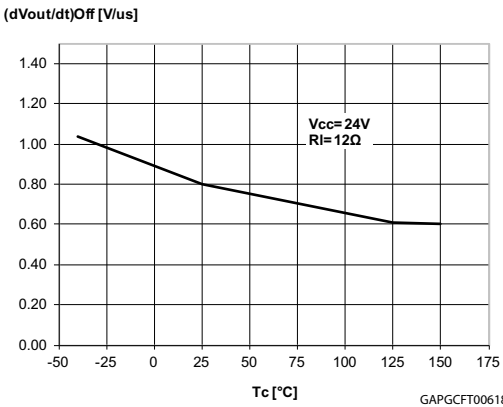
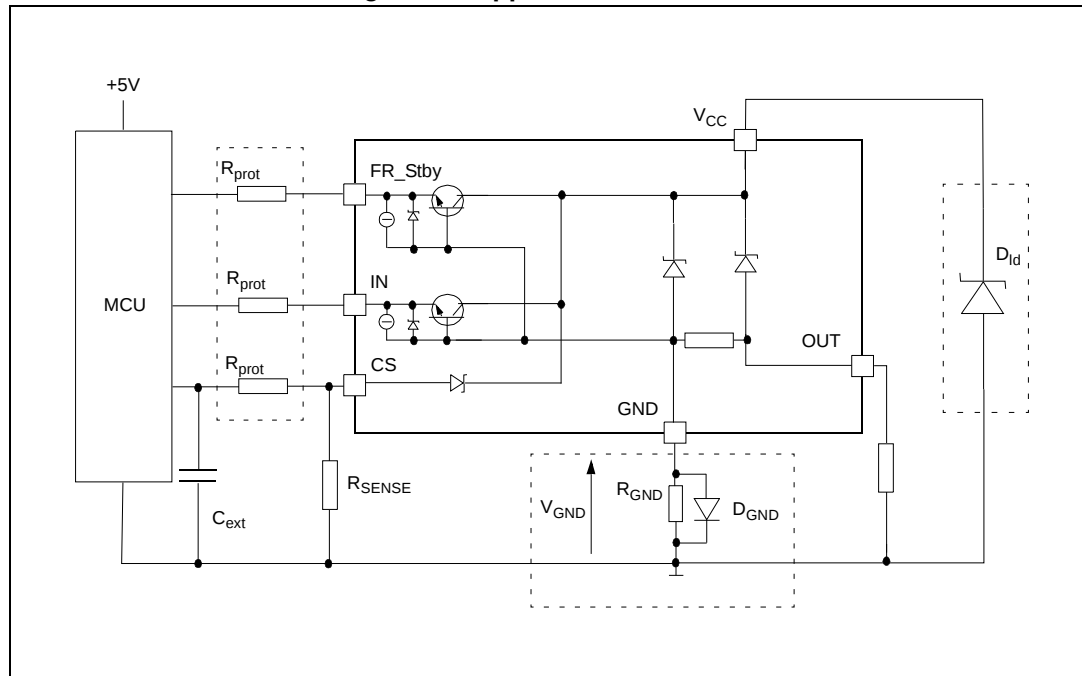


Figure 23. Turn-off voltage slope



3 Application information

Figure 24. Application schematic



3.1 GND protection network against reverse battery

3.1.1 Solution 1: resistor in the ground line (R_{GND} only)

This solution can be used with any type of load.

The following equations are an indication on how to size the R_{GND} resistor.

1. $R_{GND} \leq 600 \text{ mV} / (I_{S(on)max})$.
2. $R_{GND} \geq (-V_{CC}) / (-I_{GND})$

where $-I_{\text{GND}}$ is the DC reverse ground pin current and can be found in the absolute maximum rating section of the device datasheet.

Power dissipation in R_{GND} (when $V_{CC} < 0$: during reverse battery situations) is:

$$P_D = (-V_{CC})^2 / R_{GND}$$

This resistor can be shared amongst several different HSDs. Please note that the value of this resistor should be calculated with formula (1) where $I_{S(on)max}$ becomes the sum of the maximum on-state currents of the different devices.

Please note that if the microprocessor ground is not shared by the device ground then the R_{GND} will produce a shift ($I_{S(on)max} * R_{GND}$) in the input thresholds and the status output values. This shift will vary depending on how many devices are ON in the case of several high side drivers sharing the same R_{GND} .

If the calculated power dissipation leads to a large resistor or several devices have to share the same resistor then ST suggests Solution 2 is used (see below).

3.1.2 Solution 2: diode (D_{GND}) in the ground line

A resistor ($R_{GND} = 4.7 \text{ k}\Omega$) should be inserted in parallel to D_{GND} if the device drives an inductive load.

This small signal diode can be safely shared amongst several different HSDs. Also in this case, the presence of the ground network will produce a shift ($\approx 600 \text{ mV}$) in the input threshold and in the status output values, if the microprocessor ground is not common to the device ground. This shift will not vary if more than one HSD shares the same diode/resistor network.

3.2 Load dump protection

D_{ld} is necessary (Voltage Transient Suppressor) if the load dump peak voltage exceeds to V_{CC} max DC rating. The same applies if the device is subject to transients on the V_{CC} line that are greater than the ones shown in the ISO T/R 7637/2 table.

3.3 MCU I/Os protection

If a ground protection network is used and negative transients are present on the V_{CC} line, the control pins will be pulled negative. ST suggests that a resistor (R_{prot}) be inserted in line to prevent the microcontroller I/O pins from latching-up.

The value of these resistors is a compromise between the leakage current of microcontroller and the current required by the HSD I/Os (Input levels compatibility) with the latch-up limit of microcontroller I/Os.

$$-V_{CCpeak}/I_{latchup} \leq R_{prot} \leq (V_{OH\mu C} - V_{IH} - V_{GND}) / I_{IHmax}$$

Calculation example:

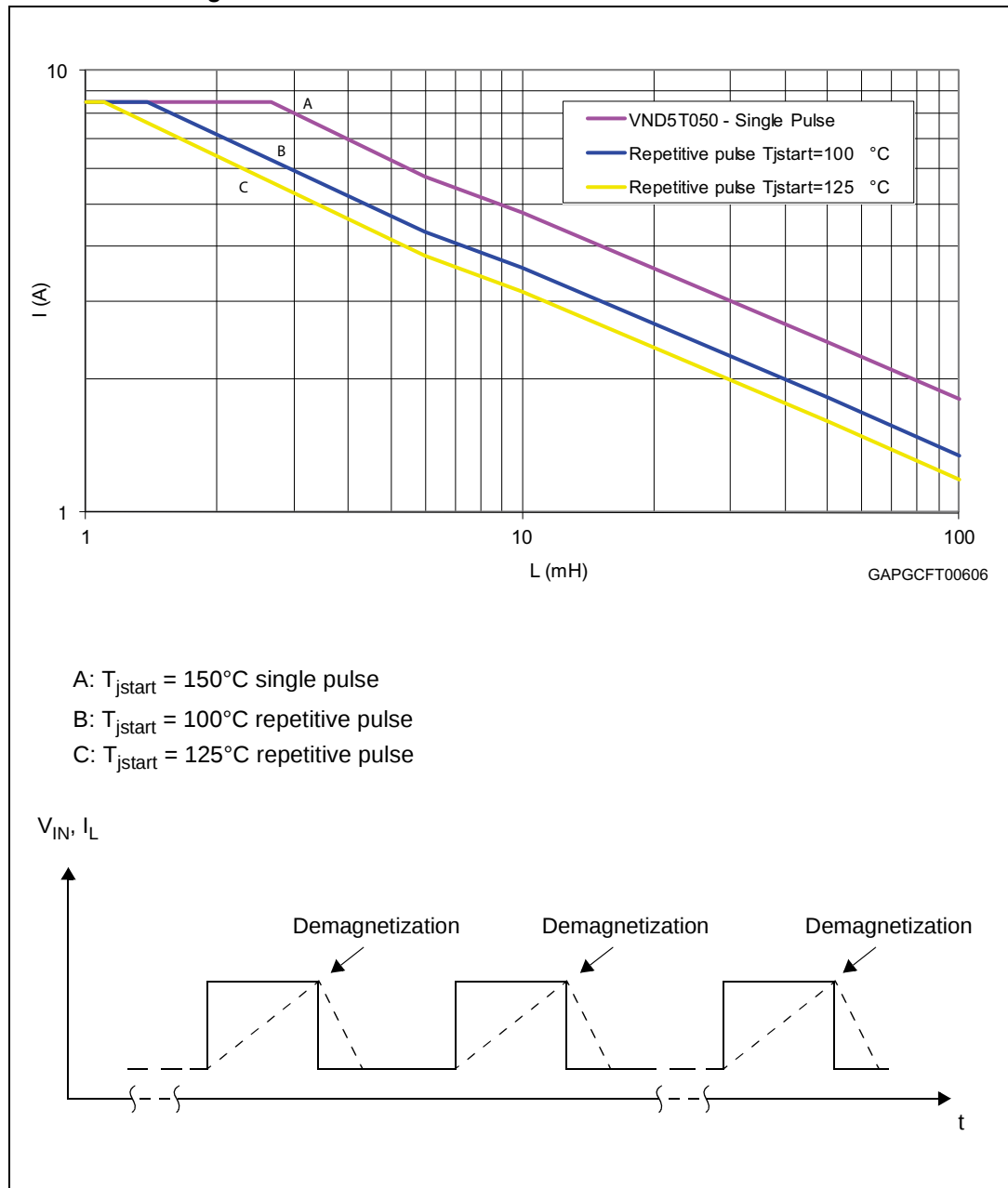
For $V_{CCpeak} = -600 \text{ V}$ and $I_{latchup} \geq 20 \text{ mA}$; $V_{OH\mu C} \geq 4.5 \text{ V}$

$$30 \text{ k}\Omega \leq R_{prot} \leq 180 \text{ k}\Omega.$$

Recommended R_{prot} value is $60 \text{ k}\Omega$.

3.4 Maximum demagnetization energy ($V_{CC} = 24\text{ V}$)

Figure 25. Maximum turn-off current versus inductance



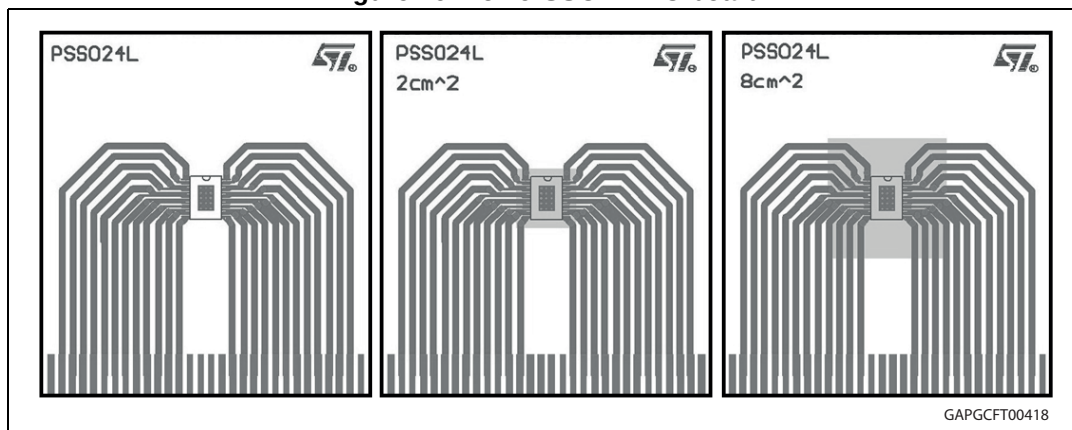
- A: $T_{jstart} = 150\text{ °C}$ single pulse
 B: $T_{jstart} = 100\text{ °C}$ repetitive pulse
 C: $T_{jstart} = 125\text{ °C}$ repetitive pulse

1. Values are generated with $R_L = 0\text{ }\Omega$.
 In case of repetitive pulses, T_{jstart} (at the beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves A and B.

4 Package and PCB thermal data

4.1 PowerSSO-24 thermal data

Figure 26. PowerSSO-24 PC board



1. Layout condition of R_{th} and Z_{th} measurements (board finish thickness 1.6 mm $\pm$ 10%; board double layer; board dimension 77x86; board Material FR4; Cu thickness 0.070mm (front and back side); thermal vias separation 1.2 mm; thermal via diameter 0.3 mm $\pm$ 0.08 mm; Cu thickness on vias 0.025 mm; footprint dimension 4.1 mm x 6.5 mm).

Figure 27. $R_{thj-amb}$ vs PCB copper area in open box free air condition (one channel ON)

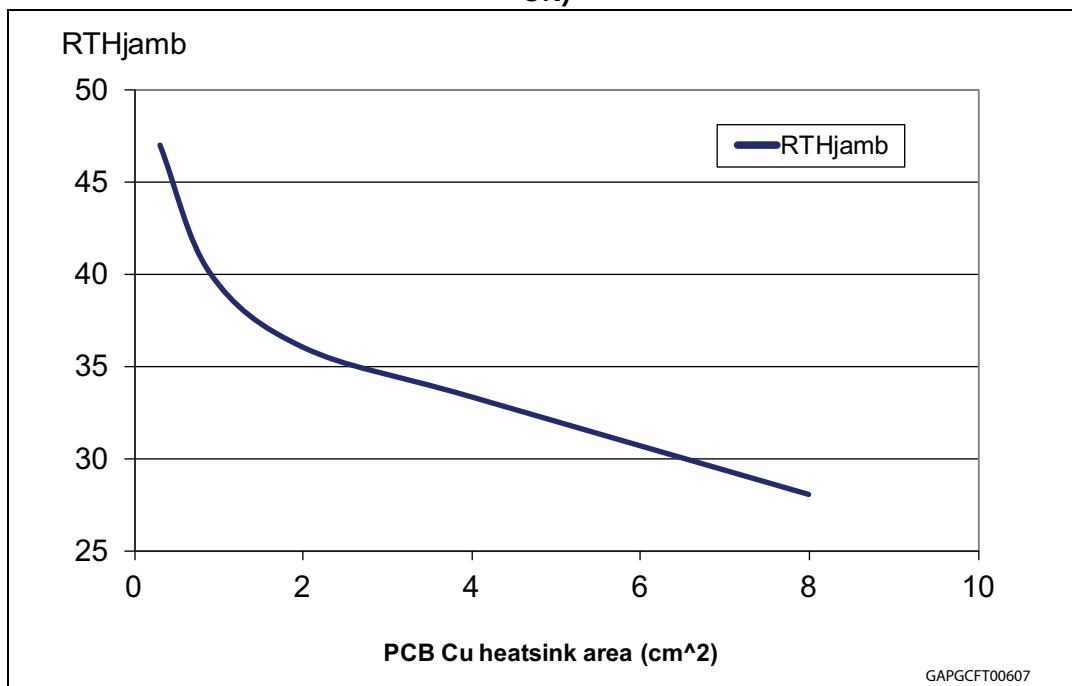


Figure 28. PowerSSO-24 thermal impedance junction ambient single pulse (one channel ON)

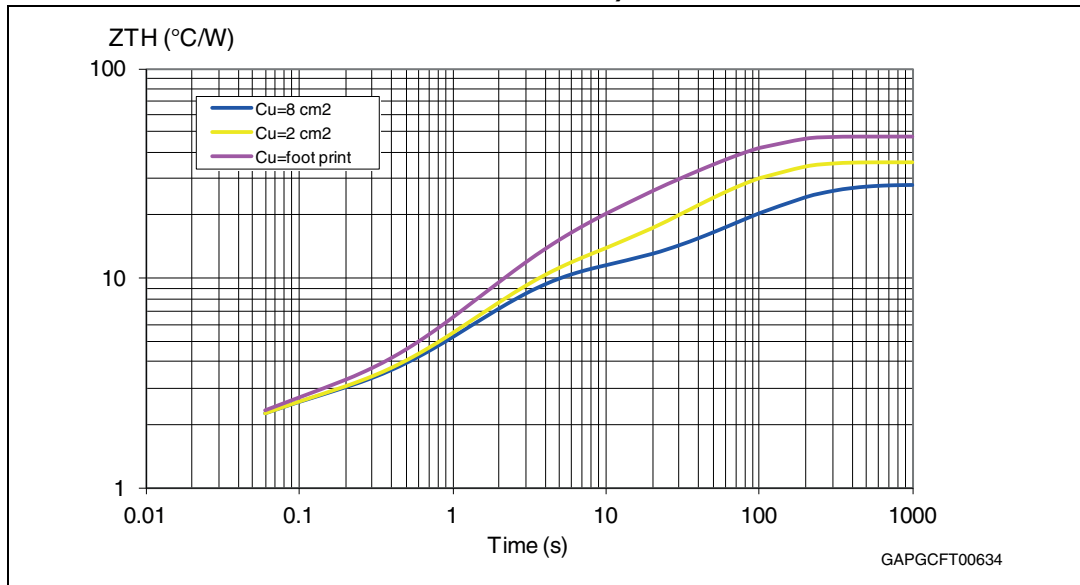
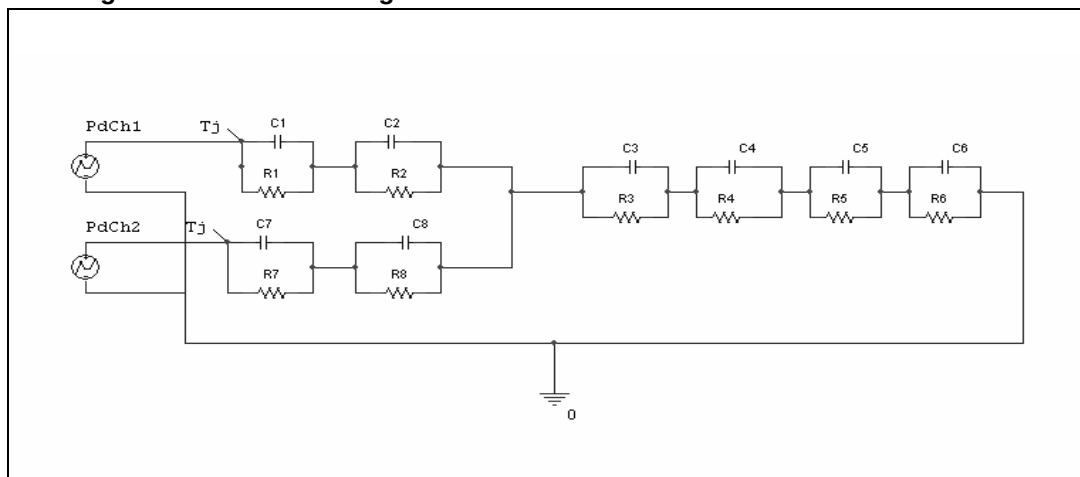


Figure 29. Thermal fitting model of a double channel HSD in PowerSSO-24



1. The fitting model is a simplified thermal tool and is valid for transient evolutions where the embedded protections (power limitation or thermal cycling during thermal shutdown) are not triggered

Equation 1: Pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

$$\text{where } \delta = t_p / T$$

Table 15. Thermal parameters

Area/island (cm ²)	Footprint	2	8
R1 = R7 (°C/W)	0.6		
R2 = R8 (°C/W)	0.75		
R3 (°C/W)	1		
R4 (°C/W)	7.7		
R5 (°C/W)	9	9	8
R6 (°C/W)	28	17	10
C1 = C7 (W.s/°C)	0.005		
C2 = C8 (W.s/°C)	0.01		
C3 (W.s/°C)	0.05		
C4 (W.s/°C)	0.3		
C5 (W.s/°C)	1	4	9
C6 (W.s/°C)	2.2	5	17

5 Package and packing information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com.

ECOPACK[®] is an ST trademark.

5.1 PowerSSO-24 mechanical data

Figure 30. PowerSSO-24 package dimensions

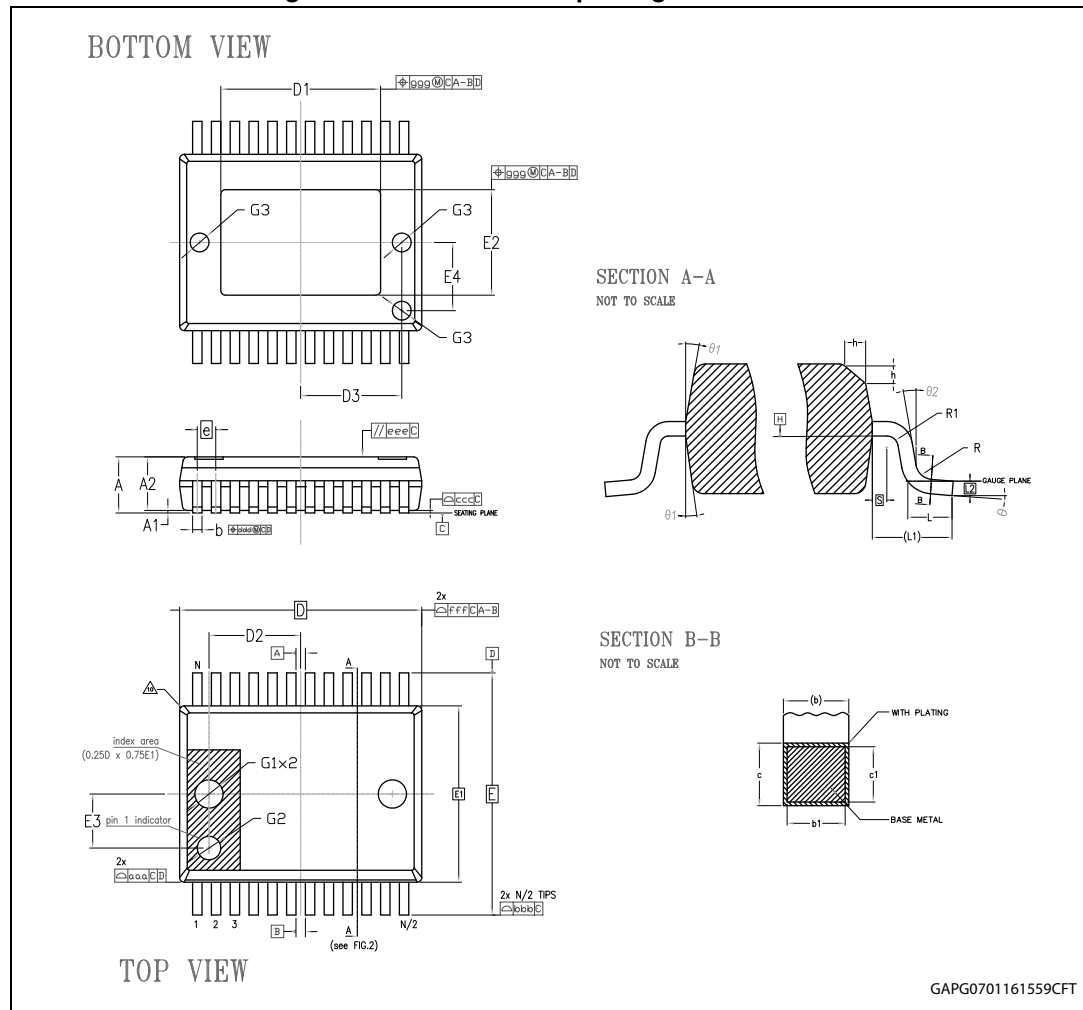


Table 16. PowerSSO-24 mechanical data

Symbol	Millimeters		
	Min.	Typ.	Max.
Θ	0°		8°
$\Theta 1$	5°		10°
$\Theta 2$	0°		
A			2.45
A1	0.00		0.10
A2	2.15		2.35
b	0.33		0.51
b1	0.28	0.40	0.48
c	0.23		0.32
c1	0.20	0.20	0.30
D	10.30 BSC		
D1	6.50		7.10
D2		3.65	
D3		4.30	
e	0.80 BSC		
E	10.30 BSC		
E1	7.50 BSC		
E2	4.10		4.70
E3		2.30	
E4		2.90	
G1		1.20	
G2		1.00	
G3		0.80	
h	0.30		0.40
L	0.55	0.70	0.85
L1	1.40		
L2	0.25 BSC		
N	24		
R	0.30		
R1	0.20		
S	0.25		
Tolerance of form and position			
aaa	0.20		

Table 16. PowerSSO-24 mechanical data (continued)

Symbol	Millimeters		
	Min.	Typ.	Max.
bbb		0.20	
ccc		0.10	
ddd		0.20	
eee		0.10	
fff		0.20	
ggg		0.15	

5.2 PowerSSO-24 packing information

Figure 31. PowerSSO-24 tube shipment (no suffix)

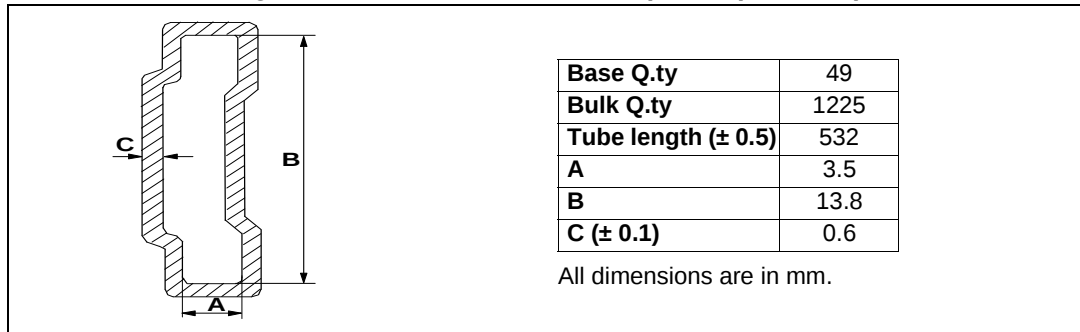
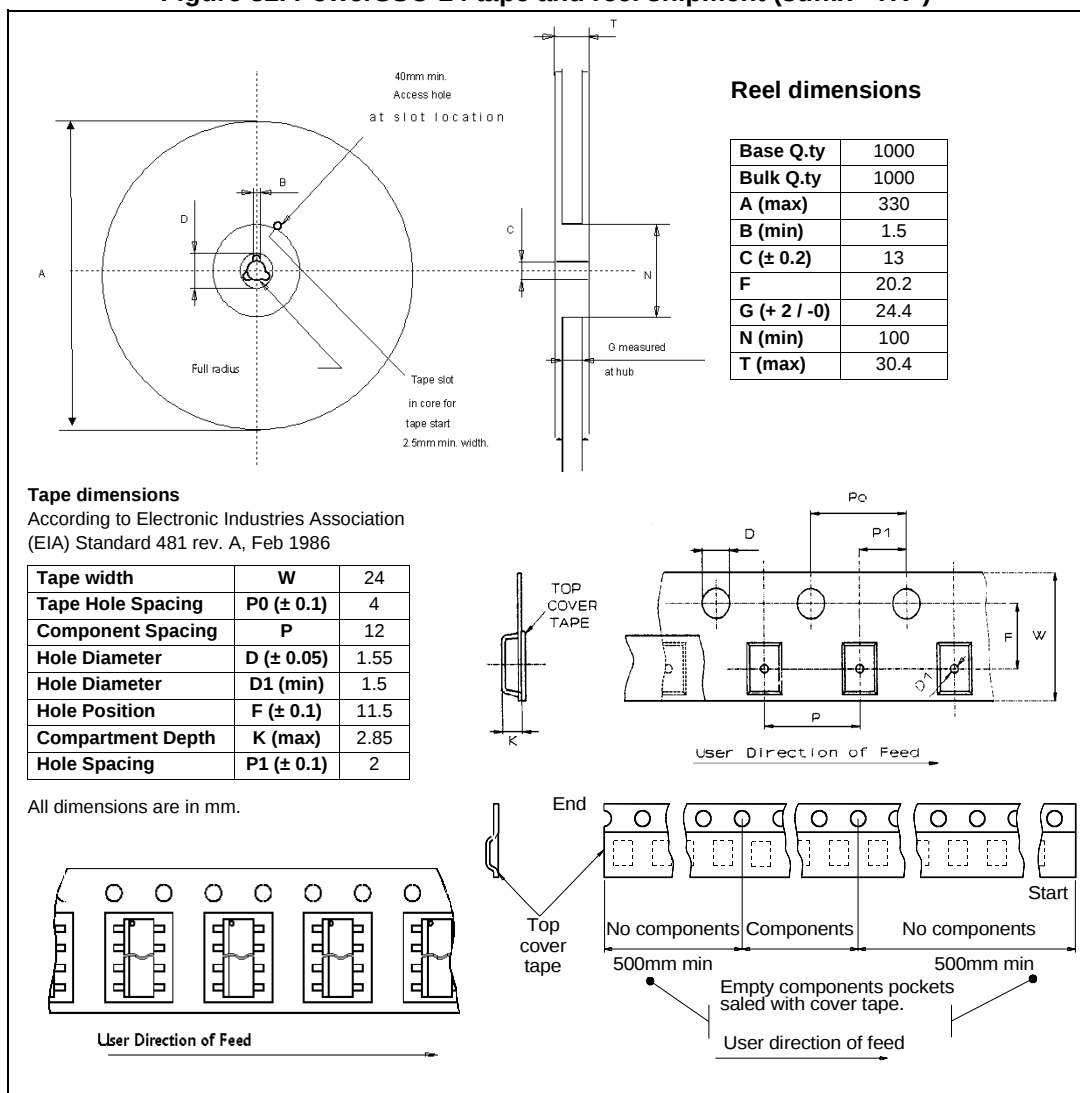


Figure 32. PowerSSO-24 tape and reel shipment (suffix "TR")



6 Order codes

Table 17. Device summary

Package	Order codes	
	Tube	Tape and reel
PowerSSO-24	VND5T050AK-E	VND5T050AKTR-E

7 Revision history

Table 18. Document revision history

Date	Revision	Changes
07-Feb-2012	1	Initial release.
30-Mar-2012	2	Updated Table 2: Suggested connections for unused and not connected pins Table 9: Current sense (8 V < V_{CC} < 36 V) : – dK ₀ /K ₀ : updated test condition from I _{OUT} = 100 A to I _{OUT} = 100 mA Table 13: Electrical transient requirements (part 2) : – added note
18-Sep-2013	3	Updated disclaimer.
24-Feb-2016	4	Table 4: Thermal data : – R _{thj-case} : updated value Updated Section 5.1: PowerSSO-24 mechanical data

IMPORTANT NOTICE – PLEASE READ CAREFULLY

STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST's terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers' products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2016 STMicroelectronics – All rights reserved

