1 Characteristics

Table 1. Absolute ratings

Symbol	Parameter		Value	Unit
V_{PP}[1]	Peak pulse voltage	ISO 10605 (C = 150 pF, R = 330 Ω): Air discharge Contact discharge ISO 10605 (C = 300 pF, R = 330 Ω): Air discharge Contact discharge	 25 15 15 15	kV
T_{stg}	Storage temperature range		-55 to +150	°C
T_j	Operating junction temperature range		-40 to +150	°C
T_L	Lead solder temperature (10 seconds duration)		260	°C

1. For a surge greater than the maximum values, the diode will fail in short-circuit.

Figure 2. Electrical characteristics (definitions)

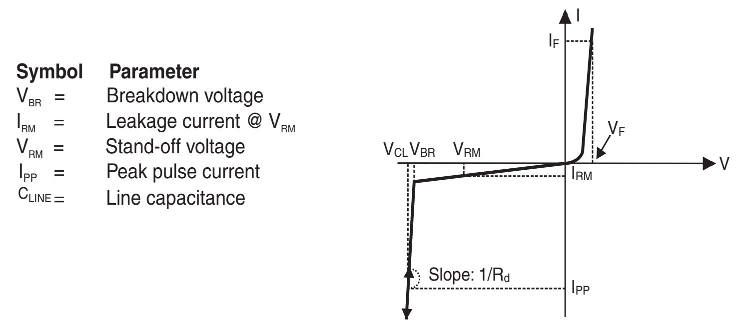


Table 2. Electrical characteristics (T_{amb} = 25 °C)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{RM}	Leakage current	V_{RM} = 5.25 V		10	150	nA
V_{BR}	Breakdown voltage between V_{BUS} and GND	I_R = 1 mA	6			V
V_F	Forward voltage	I_F = 10 mA			1.1	V
V_{CL}	Clamping voltage	I_{PP} = 1 A, 8/20 µs Any I/O pin to GND			12	V
		I_{PP} = 5 A, 8/20 µs Any I/O pin to GND			17	V
$C_{i/o\text{-}GND}$	Capacitance between I/O and GND	V_R = 1.65 V		2.5	3.5	pF
$\Delta C_{i/o\text{-}GND}$	Interline capacitance matching between I/O and GND			0.015		
$C_{i/o\text{-}i/o}$	Capacitance between I/O	V_R = 1.65 V		1.2	1.7	pF
$\Delta C_{i/o\text{-}i/o}$	Interline capacitance matching between I/O			0.04		

Figure 3. Capacitance versus voltage (typical values)

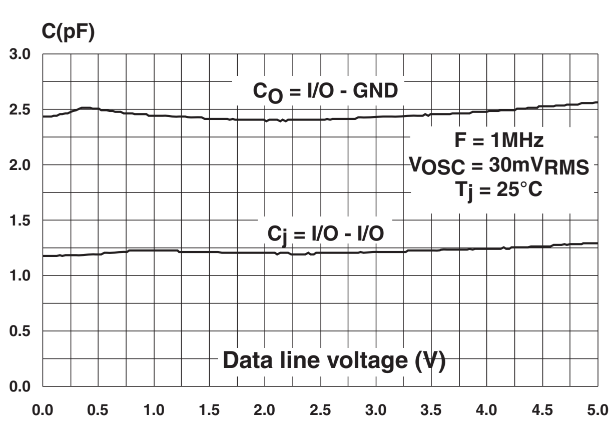


Figure 4. Line capacitance versus frequency (typical values)

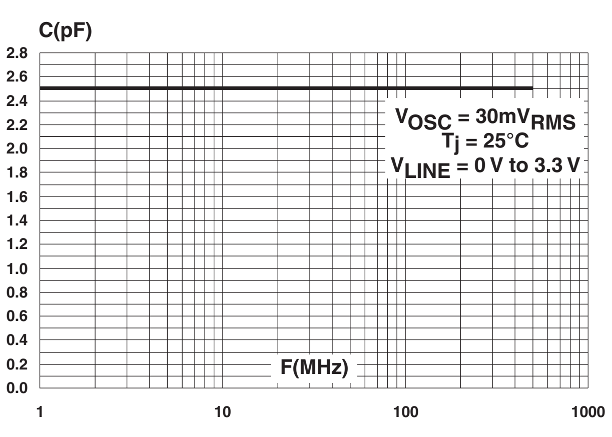


Figure 5. Relative variation of leakage current versus junction temperature (typical values)

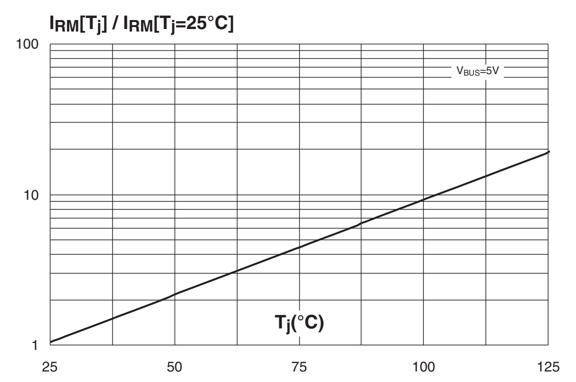


Figure 6. Frequency response

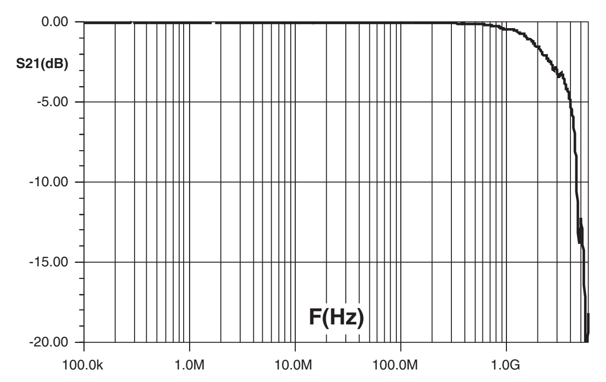


Figure 7. ESD response to ISO10605, C= 150 pF, R = 330 Ω (+15 kV air discharge)

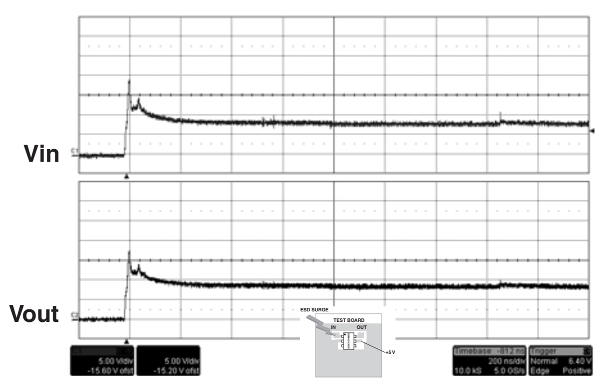


Figure 8. ESD response to ISO10605, C = 150 pF, R = 330 Ω (-15 kV air discharge)

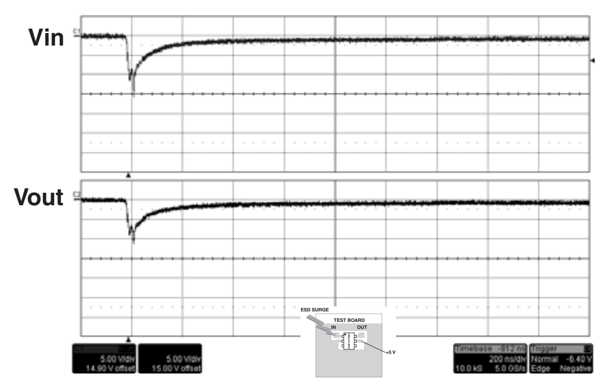
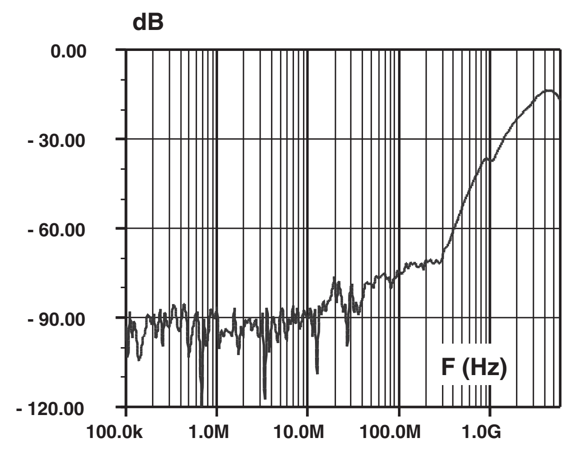


Figure 9. Analog crosstalk results

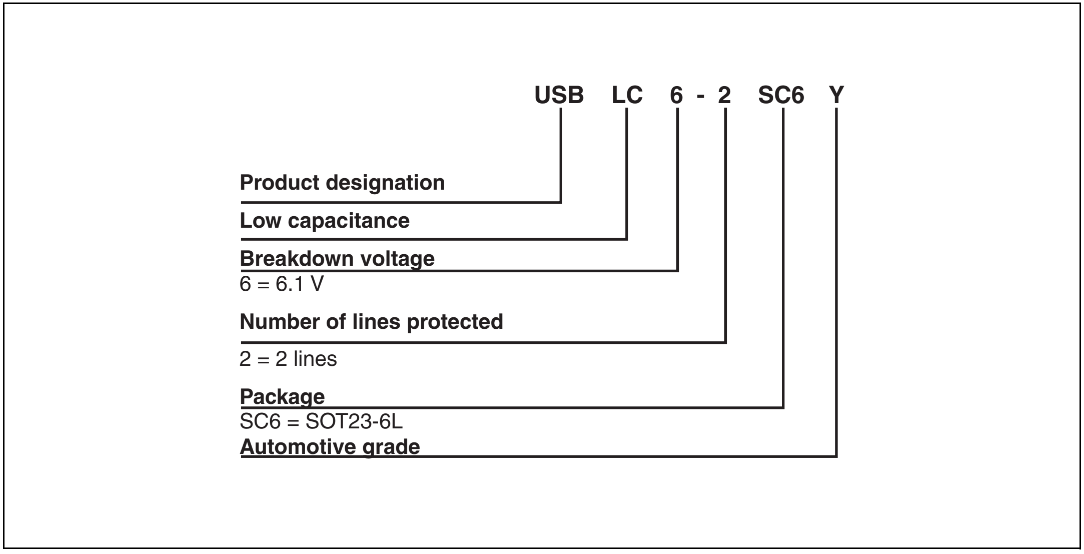


2 Application and design guidelines

More information is available in the STMicroelectronics Application note AN2689, “Protection of automotive electronics from electrical hazards, guidelines for design and component selection”.

3 Ordering information scheme

Figure 10. Ordering information scheme

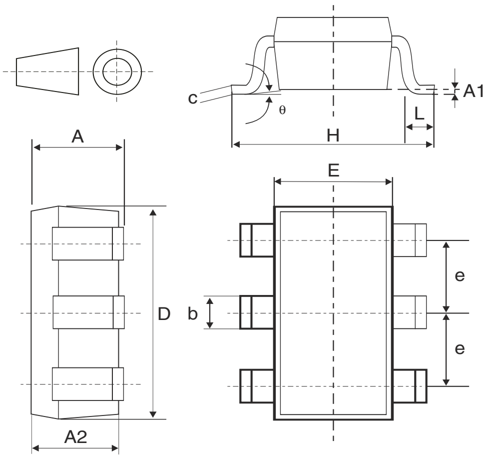


4 Package information

- Epoxy meets UL94, V0
- Lead-free package

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

Table 3. SOT23-6L dimensions



Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.90		1.45	0.035		0.057
A1	0		0.15	0		0.006
A2	0.90		1.30	0.035		0.051
b	0.30		0.50	0.012		0.020
c	0.09		0.20	0.004		0.008
D	2.80		3.05	0.11		0.118
E	1.50		1.75	0.059		0.069
e		0.95			0.037	
H	2.60		3.00	0.102		0.118
L	0.30		0.60	0.012		0.024
θ	0°		10°	0°		10°

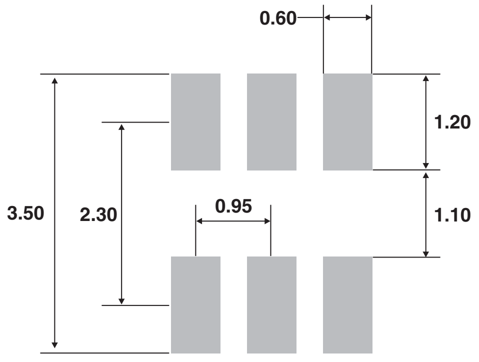


Figure 11. SOT23-6L footprint

5 Recommendation on PCB assembly

5.1 Solder paste

1. Use halide-free flux, qualification ROL0 according to ANSI/J-STD-004.
2. “No clean” solder paste recommended.
3. Offers a high tack force to resist component displacement during PCB movement.
4. Use solder paste with fine particles: powder particle size 20-45 µm.

5.2 Placement

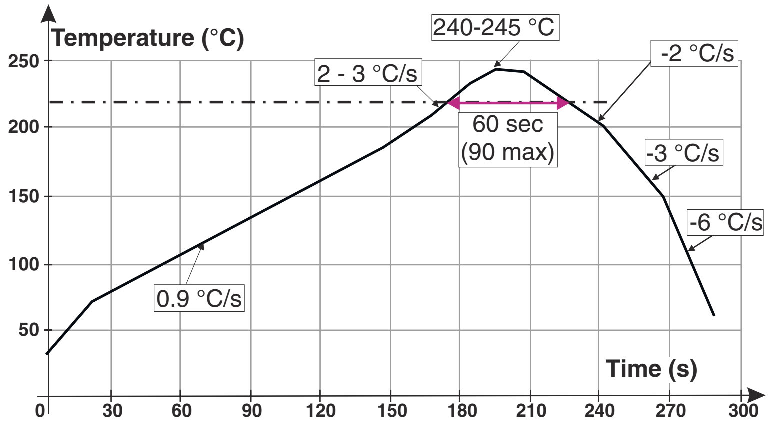
1. Manual positioning is not recommended.
2. It is recommended to use the lead recognition capabilities of the placement system, not the outline centering.
3. Standard tolerance of ± 0.05 mm is recommended.
4. 3.5 N placement force is recommended. Too much placement force can lead to squeezed out solder paste and cause solder joints to short. Too low placement force can lead to insufficient contact between package and solder paste that could cause open solder joints or badly centered packages.
5. To improve the package placement accuracy, a bottom side optical control should be performed with a high resolution tool.
6. For assembly, a perfect supporting of the PCB (all the more on flexible PCB) is recommended during solder paste printing, pick and place and reflow soldering by using optimized tools.

5.3 PCB design preference

1. To control the solder paste amount, the closed via is recommended instead of open vias.
2. The position of tracks and open vias in the solder area should be well balanced. The symmetrical layout is recommended, in case any tilt phenomena caused by asymmetrical solder paste amount due to the solder flow away.

5.4 Reflow profile

Figure 12. ST ECOPACK® recommended soldering reflow profile for PCB mounting



Note: Minimize air convection currents in the reflow oven to avoid component movement.

6 Ordering information

Table 4. Ordering information

Order code	Marking	Package	Weight	Base qty	Delivery mode
USBLC6-2SC6Y	UL2Y	SOT23-6L	16.7 mg	3000	Tape and reel

7 Revision history

Table 5. Document revision history

Date	Revision	Changes
16-May-2012	1	First issue.
06-Sep-2012	2	Updated dimensions A max., b min. and L min. in *Table 3*.

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