Ball Configuration

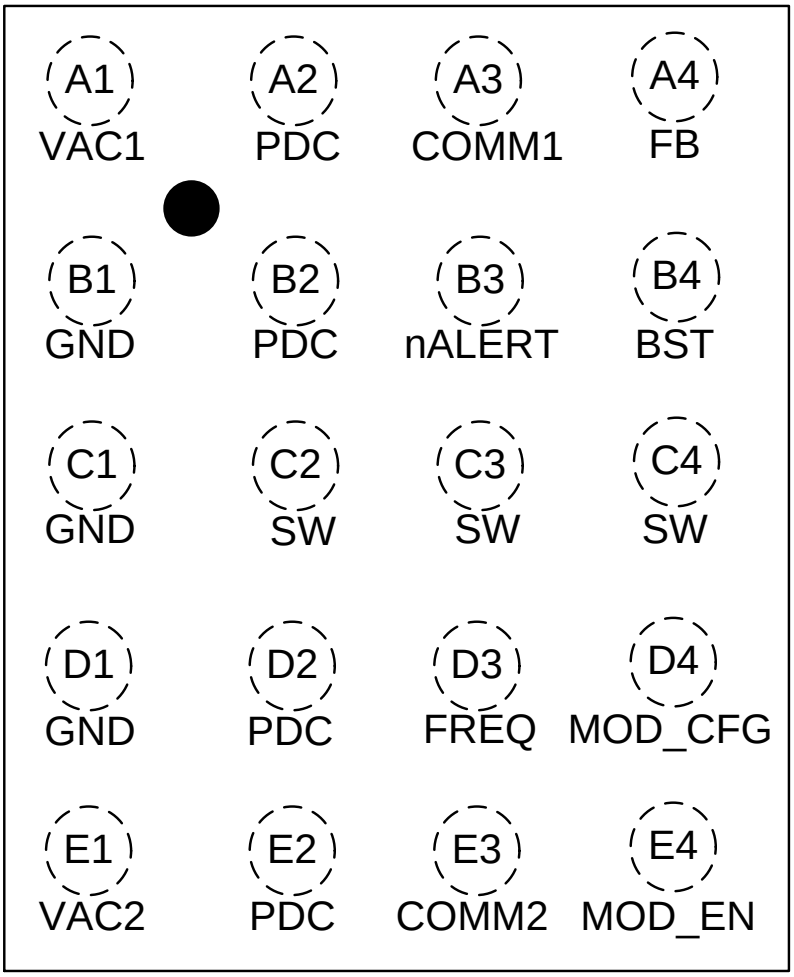


Figure 1: TS51223 Ball Configuration
(Top view with ball 1 designator)

Ball Description

Ball Number	Ball Name	Function	Description
A1	VAC1	Coil input	AC power input from the resonator coil
A2, B2, D2, E2	PDC	Input power	Rectified input voltage
C2, C3, C4	SW	Switching node	BUCK regulator switching node
B4	BST	Bootstrap capacitor	Bootstrap capacitor for buck regulator high-side driver, capacitor between BST pin and SW pin
A3	COMM1	Load modulation switch	Pull-down for VAC1 modulation capacitor
B1, C1, D1	GND	Power ground	Ground
D3	FREQ	Frequency detector output	Open drain output signal, divided-by-8 version of the frequency of the input AC power signal
A4	FB	Feedback input	BUCK feedback input. Use external resistors to set the output voltage.
E1	VAC2	Coil input	AC power input from the resonator coil
B3	nALERT	MCU interrupt output/reset signal	Active low open drain output activated when TX sends an ALERT command
D4	MOD_CFG	Modulation configuration	Configures the internal modulator to start up in standalone mode or in bypass mode. Also configures the PDC voltage in standalone mode.
E3	COMM2	Load modulation switch	Pull-down for VAC2 modulation capacitor
E4	MOD_EN	MCU modulation input	Active high Input to the modulator selection logic, with internal 100kΩ pulldown. If repeated transitions are detected on this pin, the integrated modulator is bypassed and MOD_EN controls the COMM switches.

Functional Block Diagram

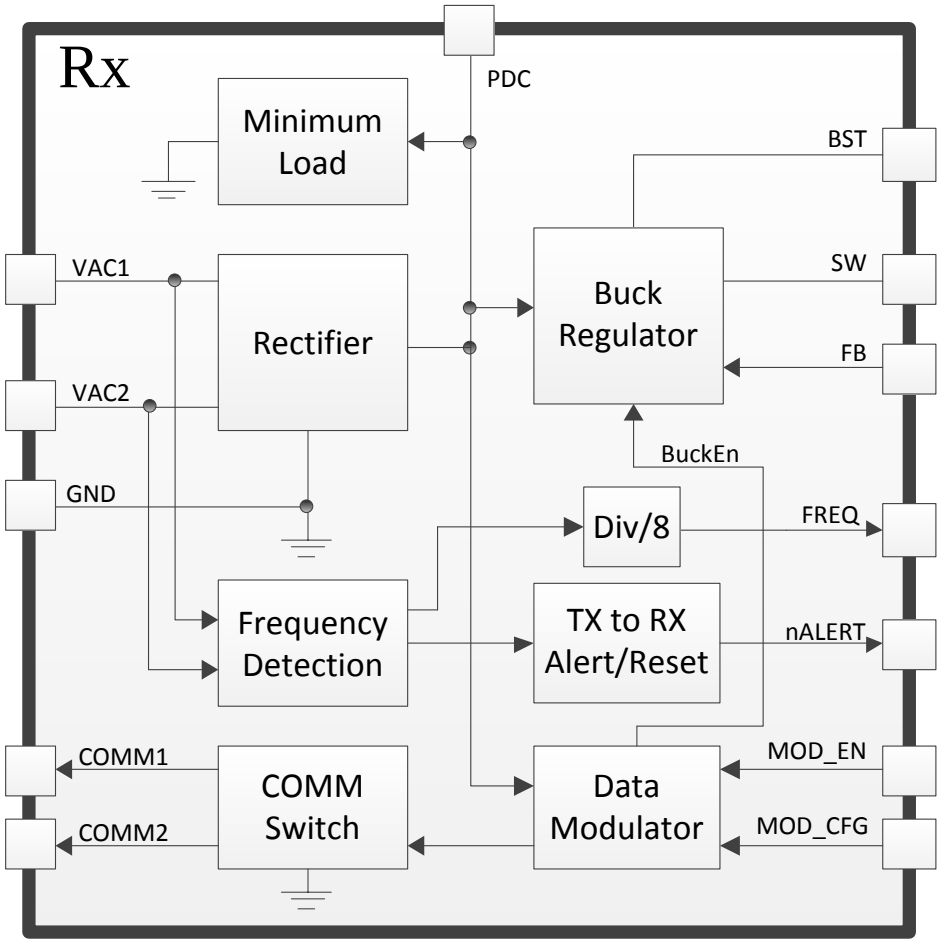


Figure 2: TS51223 Block Diagram

Absolute Maximum Ratings

Over operating free–air temperature range unless otherwise noted [1, 2]

Parameter	Value	Unit
VAC1, VAC2, PDC, COMM1, COMM2	-0.3 to 42	V
BST	-0.3 to (PDC+6)	V
SW	-1 to 42	V
FB, FREQ, nALERT, MOD_EN, MOD_CFG	-0.3 to 6	V
Electrostatic Discharge—Human Body Model	±2	kV
Electrostatic Discharge—Machine Model	±500	V
Peak IR Reflow Temperature (10 to 30 seconds)	260	°C

Notes:

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to network ground terminal.

Recommended Operating Conditions

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Rectified Voltage	V_{PDC}		3.5	12	40	V
Bridge Current	I_{BR}				300	mA
Rectification Frequency	F_{BR}		100	1000	6780	kHz
Output Voltage	V_{OUT}	$V_{PDC} > V_{OUT}/DUTY_{MAX.}$	1.5	5	24	V
Output Current	I_{OUT_MAX}				400	mA
COMM Current	I_{COMM}				50	mA
PDC Capacitance [1]	C_{IN}		2.2	10		µF
BUCK Output Capacitance[1]	C_{OUT}	F_{SW}=1.3MHz, I_{OUT_MAX}= 50mA	8.8	44		µF
BUCK Output Capacitance[1]	C_{OUT}	F_{SW}=1.3MHz, I_{OUT_MAX} = 400mA	20	44		µF
BUCK Bootstrap Capacitor	C_{BST}		17.6	47		nF
Output Filter Inductor	L_{OUT}	F_{SW}=1.3MHz, I_{OUT_MAX} = 50mA	1.5	3.3		µH
Output Filter Inductor	L_{OUT}	F_{SW}=1.3MHz, I_{OUT_MAX} = 400mA	1.5	4.7		µH
RX Coil	L_{IN}	F_{BR} = 1MHz		11		µH
RX Series Resonant Capacitor	C_s	F_{BR} = 1MHz		10		nF
COMM Modulation Capacitors	C_{C1}, C_{C2}	F_{BR} = 1MHz		1		nF

Notes:

(1) Specified capacitance includes allowance for voltage derating, tolerance, temperature, and aging. Select capacitors that meet the specified minimum capacitance.

Electrical Characteristics

Electrical Characteristics, T_J = -40°C to 85°C, unless otherwise noted

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Synchronous Rectifier						
Low-Side Bridge FET drain-source on-state resistance	R_{DSON_BR}			400		mΩ
High-Side Bridge Diode Forward Voltage	V_{D_BR}	I_{BR} = 150mA		500		mV
Capacitive Modulation Switches						
COMM FET drain-source on-state resistance	R_{DSON_COMM}	I_{COMM} = 50mA		10		Ω
Power On Reset						
Power On Reset Voltage	$V_{PDC-POR}$	Internal Logic Reset Clear, internal logic/modulator ready.	2.7	3.0	3.4	V
Power On Reset Hysteresis	$V_{PDC-POR\_HYST}$	(1)		0.35		V
Quiescent Current						
Quiescent Current, PWM mode	Idd_{PWM}	PDC current, Buck Regulator PWM mode, V_{PDC}=12V, VAC1=VAC2=0V, I_{LOAD}=0A, MOD_EN=0, Vout set to 5V.		15		mA
Quiescent Current, PFM mode	Idd_{PFM}	PDC current, Buck Regulator PFM mode, V_{PDC}=12V, VAC1=VAC2=0V, I_{LOAD}=0A, MOD_EN=0, Vout set to 0.9V.		4		mA
Quiescent Current, Buck Off, 10mA Current Source Off	$Idd_{BK\_10mA\_OFF}$	PDC current, Buck Regulator OFF, V_{PDC}=4.5V, VAC1=VAC2=0V, MOD_EN=0, 10mA current source off.		3		mA
Quiescent Current, Buck Off, 10mA Current Source On	Idd_{BK_OFF}	PDC current, Buck Regulator OFF, V_{PDC}=4.5V, VAC1=VAC2=0V, MOD_EN=0, 10mA current source on.		13		mA

Electrical Characteristics (continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Buck Regulator Input						
PDC Under-voltage Lockout	$V_{PDC-UVLO}$	Buck Regulator = Off,		4.3		V
PDC Under-voltage Lockout Hysteresis	$V_{PDC-UVLO-HYST}$	(1) Buck Regulator = Off		350		mV
MOD_EN Digital Input Thresholds						
High Level Input Voltage	V_{IH}	MCU VIO_{MAX} = 1.8V	1.3		5.5	V
Low Level Input Voltage	V_{IL}		0		0.54	V
Pull Down Resistance	R_{PD}		68	100	144	kΩ
FREQ, nALERT Open Drain Output						
High Level Output Leakage	I_{OH_LEAK}	VIO = 5V		0.01	1	µA
Low Level Output Voltage	V_{OD_OL}	I_{SINK} = 3mA			0.1	V
Thermal Protection Thresholds						
Thermal shutdown junction temperature	T_{SD}	(1)		130	146	°C
Thermal shutdown hysteresis	T_{SD_HYST}	(1)		10		°C

Notes:

(1) This parameter is not tested in production.

Regulator Characteristics

Electrical Characteristics, T_J = -40°C to 85°C, V_{PDC}=12V, F_{SW}=1.3MHz, L_{OUT}=4.7µH, C_{OUT}=44µF, C_{BST}=22nF, unless otherwise noted

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
PWM Mode Output Voltage Accuracy	$V_{OUT-PWM}$	I_{OUT} = 150mA	V_{OUT} - 2%	V_{OUT}	V_{OUT} + 2%	V
PFM Mode Output Voltage Accuracy	$V_{OUT-PFM}$	I_{OUT} = 0A	V_{OUT} - 0%	V_{OUT} + 3%	V_{OUT} + 6.5%	V
High-Side Switch ON Resistance	R_{DSON_HS}	I_{SW} = -0.15A (1)		450		mΩ
Low-Side Switch ON Resistance	R_{DSON_LS}	I_{SW} = 0.15A (1)		300		mΩ
Output Over Current Detect	I_{OCD}	High Side Switch Current (I_{OUT_MAX} = 400mA).	1100	1320	1760	mA
Feedback Reference Voltage	FB_{TH}	(2)	0.886	0.900	0.914	V
Soft Start Ramp Time	T_{SS}	15% to 85% * V_{OUT}		2.5		ms
PFM Mode Feedback Comparator Threshold	V_{FB-PFM}			V_{OUT} + 1%		V
VOUT Over Voltage Threshold	V_{OUT-OV}		V_{OUT}	V_{OUT} + 4%	V_{OUT} + 7%	V
VOUT Over Voltage Hysteresis	V_{OUT-OV_HYST}		0.5% * V_{OUT}	1% * V_{OUT}	2% * V_{OUT}	V
Maximum SW Duty Cycle	$DUTY_{MAX}$	(3)	95	96	99	%
Buck Regulator Switching Frequency	F_{sw}		1.17	1.3	1.43	MHz

Notes:

(1) R_{DSON} is characterized at 400mA and tested at lower current in production.

(2) The ratio of V_{PDC} to V_{OUT} cannot exceed 16.

(3) Regulator SW pin is forced off for 240ns every 8 cycles to ensure the BST cap is replenished.

Functional Description

TS51223 is a fully-integrated wireless power receiver that can operate as a single-chip solution in proprietary applications. It can also operate in conjunction with a wireless charger controller or an application microcontroller to support the Qi, PMA or A4WP standards as well as proprietary standards up to 2W for 5V output and up to 5W for higher output voltages. Operating in conjunction with TS80002 as a wireless power transmitter and with a charging controller on the RX side, TS51223 can support bidirectional communication for data upload from the RX to the TX side. A TX to RX alert or reset function is also included so TS80002 can issue an interrupt or a reset signal to the RX MCU if the RX MCU becomes unresponsive.

Rectifier

TS51223 includes a high-efficiency rectifier to convert the input AC power signal to a DC output level for powering a high-efficiency step-down DC-DC converter and an integrated data modulator. The rectifier bridge is built to minimize power dissipation across load current of interest. The primary side of the bridge can stand-off up to 40V with AC input running at 6.78MHz. On the secondary side, a capacitive load on the PDC pin is used to filter the voltage signal on both sides of the bridge rectifier. The integrated data modulator and the external MCU communicate to the transmitter side using the capacitive modulation scheme.

Integrated Modulator

The integrated Data Modulator can be configured to operate in standalone or bypass mode. In standalone mode, the integrated modulator sends data messages to the TX side using a proprietary protocol to control the rectified voltage level on the PDC pin. In bypass mode, the external MCU controls the data packets to the TX side. For example, if the device is configured for standalone mode at power up, the system can receive power without external MCU support, and once PDC is high enough to operate the buck regulator and the MCU, the MCU can take over the communication with the transmitter by bypassing the integrated modulator. Modulator mode reverts back to the standalone mode when the MCU communication with the transmitter stalls. When the PDC output load current is low (buck regulator is off), an internal 10mA load is enabled to allow data communication to take place in optimal conditions.

40V Input Buck Regulator

The integrated Buck regulator is a current-mode synchronous step-down power supply with integrated power switches, internal compensation, and fault protection. It is powered by the DC output of the Wireless power receiver bridge. The regulator is designed to handle a wide range of input and output voltages. The regulator is optimized for high efficiency power conversion with low R_{DSON} integrated synchronous switches. Low power at light output loads is attained by the regulator automatic transitions between PFM and PWM modes. The regulator is configured with external feedback resistors to set the output voltage, V_{OUT}. The regulator automatically turns off when the RX AC power input is removed.

Device Power up Timing

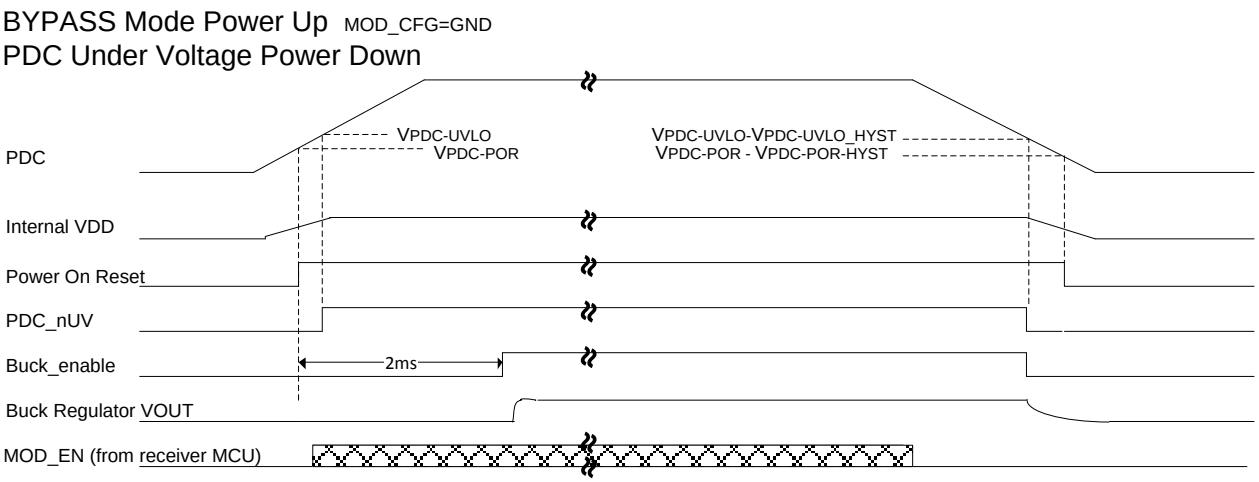


Figure 3: Bypass Mode Power Up

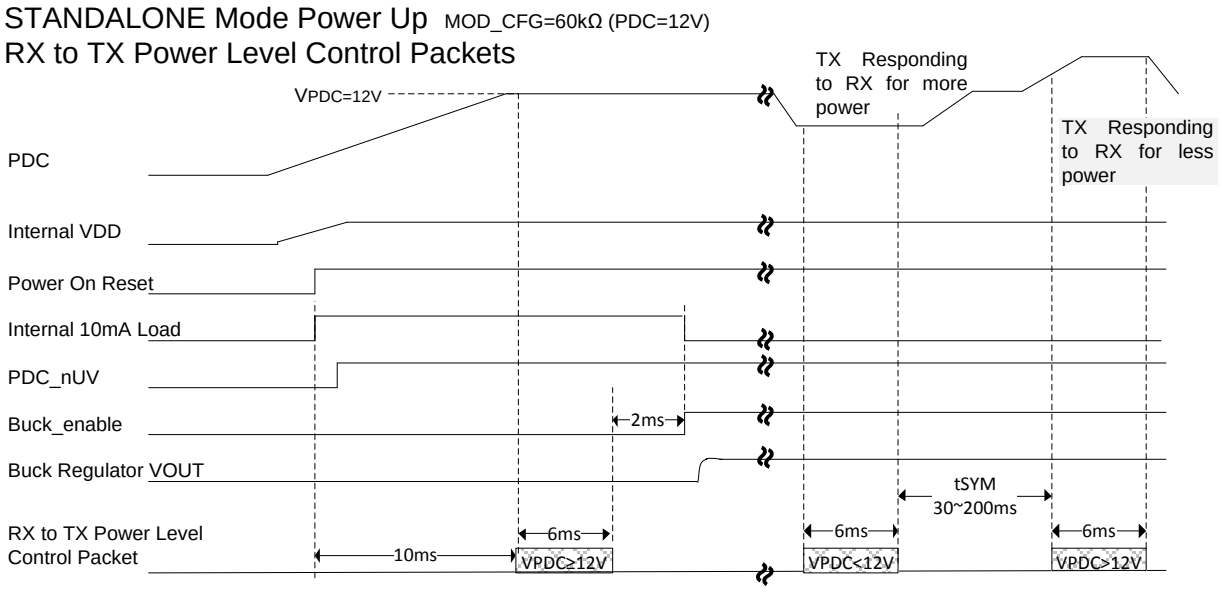


Figure 4: Standalone Mode Power Up

VAC Signal Loss & Buck Control, BYPASS Mode MOD_CFG=GND

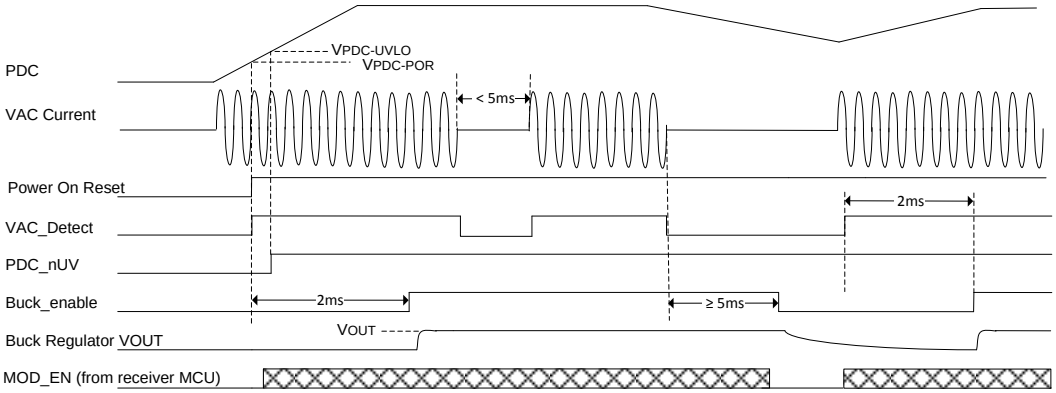


Figure 5: VAC Signal Loss & Buck Control

Detailed Ball Description

VAC1, VAC2 - AC Power input from resonant LC network
These terminals are connected to the wireless power supply receiver coil and resonant capacitor. It is recommended that the PCB traces are robust to handle high peak currents during power up maximum power transfer.

PDC - Rectified input signal
This terminal is the rectified output of the RX AC input voltage and serves as the DC supply for the device. It is recommended that a 10µF bypass capacitor rated for the maximum PDC voltage (> 2.2µF capacitance accounting for voltage derating, aging, and tolerance) be placed close to the device for best performance. Since this is the main power supply for the IC, good layout practices need to be followed for this connection.

BST - Bootstrap input
This terminal provides the bootstrap voltage required for the high-side NMOS switch of the buck regulator. An external ceramic capacitor placed between the BST and SW pins will provide the necessary gate drive voltage for the high-side switch. In normal operation, the capacitor is re-charged on every low-side synchronous switching action. For the case where the switch mode approaches 100% duty cycle for the high-side FET, the buck regulator will automatically reduce the duty cycle to a minimum off time on every 8th cycle to allow the BST capacitor to re-charge.

FB - Buck regulator output feedback
This is the input terminal for the buck regulator output voltage feedback. The external resistor divider network is configured according to the following equation if the external feedback mode is selected:

$$V_{OUT} = 0.9 \left(1 + \frac{R_{TOP}}{R_{BOT}}\right) \; ; \; V_{OUT} > \frac{V_{PDC}}{16}$$

FB is a high input impedance pin and input current is less than 100nA. Good layout practice is required for the feedback resistors and feedback traces; feedback trace should be kept as short as possible and minimum width/isolated to reduce stray capacitance and reduce noise injection. Also, the feedback connection point on the main V_{OUT} trace should be placed at the point where accurate V_{OUT} regulation is required to minimize load regulation across the PCB.

Detailed Ball Description (continued)

SW - Switching output
This is the switching node of the buck regulator. It should be connected directly to the output filter inductor L_{OUT} and bootstrap capacitor with a short, wide trace. SW pin switches between V_{PDC} and GND at the switching frequency, thus it is considered a noise source on the PCB. Route high impedance and quiet traces away from the SW trace.

GND - Ground
Ground reference. This pin will conduct both correlated and uncorrelated switching currents during power transfer mode from the COMM1/2 pins switching and the buck operating in PWM mode, as well as switching current from the internal oscillator and the integrated modulator. PCB layout must provide low resistance to the ground plane for stable operation.

COMM1, COMM2 - Modulation capacitor switches
COMM1 and COMM2 pins are momentarily grounded when the system or the device communicates to the wireless power transmitter. When the COMM1/2 switches close, this shifts the impedance seen by the RX coil L_{IN} and this shift is in turn reflected as a change in TX coil current that can be detected by the transmitter's demodulator. Depending on the MOD_CFG pin configuration and activity on the MOD_EN pin, the integrated modulator or the MOD_EN pin controls the COMM1/2 switches.

FREQ - Frequency detector output
This is an open drain output which outputs a clock reference running at the frequency of the input AC power signal divided by 8.

nALERT - MCU reset/interrupt
nALERT is an open drain output which is asserted low when the transmitter sends an ALERT command to the receiver to reset the MCU or to generate an interrupt. During the power up sequence, nALERT pin is pulled high by the external pull-up resistor, thus only the power transmitter ALERT command is allowed to assert this pin low.

MOD_EN - MCU modulation input
This is an active high CMOS input to drive the COMM1 and COMM2 pins to modulate the coil current to communicate with the wireless power transmitter. MOD_EN signal is generated by the external MCU and its output swing must conform to the input levels specified in the Electrical Characteristics section for the MOD_EN pin. Activity on the MOD_EN is also sampled by the control logic to transition between Stand-alone and Bypass modes as outlined in the MOD_CFG pin description.

Detailed Ball Description (continued)

MOD_CFG - Modulation configuration
PDC voltage and modulation control scheme for communication are configured by the MOD_CFG pin.

Bypass Mode
When the MOD_CFG pin is grounded (voltage < 250mV), the internal data modulator is bypassed and the external MCU is required to drive the MOD_EN pin to control the communication with the power transmitter. Thus, the MCU must be fully active prior to the device generating a stable output voltage V_{OUT}. The external MCU will set V_{PDC} by sending data packets to the transmitter.

Stand-alone Mode
If the MOD_CFG pin is grounded through an external precision resistor (voltage > 250mV), the voltage on the MOD_CFG pin determines the nominal rectified voltage on the PDC pin. In this mode, the integrated modulator generates the wireless power control packets and drives the COMM1/2 switches after power-on reset. This mode is referred to as the stand-alone mode as it does not require an external MCU to control the communication with the transmitter during receiver power up and for normal operation.

While in stand-alone mode, the device also monitors the MOD_EN pin to detect if the external MCU wants to take control of the communication with the power transmitter. If at least 8 pulses with a delay of less than 25ms between each pulse are detected on the MOD_EN pin, the device enters the (integrated modulator) bypass mode. Once in bypass mode and the MOD_EN pin activity stalls (less than 8 pulses in a 250 ms window), the device exits the bypass mode and returns to stand-alone mode and the integrated modulator resumes communication with the power transmitter.

MOD_CFG Pin Connection	RX Data Communication Modulator	COMM1/2 Pin Drive	V_{PDC}	Internal Modulator Bypass	Internal Modulator Fallback
Grounded	External MCU	MOD_EN	Set by External MCU's power control data packet	Integrated modulator always bypassed	Integrated modulator always bypassed
Resistor R_{MOD_CFG} to Ground	Integrated modulator	Integrated modulator	R_{MOD_CFG} / 5000	If MOD_EN pin pulses 8 times with delay < 25ms between pulses, COMM1/2 pins responsive to MOD_EN input	If MOD_EN pin pulses less than 8 times within 250ms window, COMM1/2 pins responsive to the integrated modulator

Table 2: PDC Voltage and Modulator Configuration

Regulator Internal Protection Details

Regulator Output Current Limit
The current through the high-side FET is sensed on a cycle by cycle basis and if current limit is reached, it will turn off the high-side FET in mid-cycle. In addition, the device senses the FB pin to identify hard short conditions and will direct the SW output to skip 4 cycles if current limit occurs when FB is low. This allows current built up in the inductor during the minimum on-time to decay sufficiently. Current limit is always active when the regulator is enabled and the soft start function ensures current limit does not prevent regulator startup.

Under extended over-current conditions (such as a short), the buck regulator switching will automatically be disabled. Once the over current condition is removed, the device automatically returns to normal operation.

Thermal Shutdown
If the die temperature exceeds T_{SD}, SW outputs will tri-state to protect the device and its load from damage. Once the device cools to $T_{SD} - T_{SD\_HYST}$, the buck regulator will attempt to start up again.

Reference Soft Start
Internal references are ramped to prevent the output from overshoot during initial startup. During the soft start ramp, current limit is still active, and protects the device in case of a shorted output.

Output Overvoltage
If the output of the regulator exceeds 3% of the set regulation voltage, the SW output tri-states to protect the device from damage. This check occurs at the start of each switching cycle. If overvoltage occurs mid-cycle, the switching for that cycle completes and the SW output tri-states on the next cycle.

PDC Under-Voltage Lockout
Buck regulator is off until PDC is over 4V with 300mV hysteresis.

Application Schematics

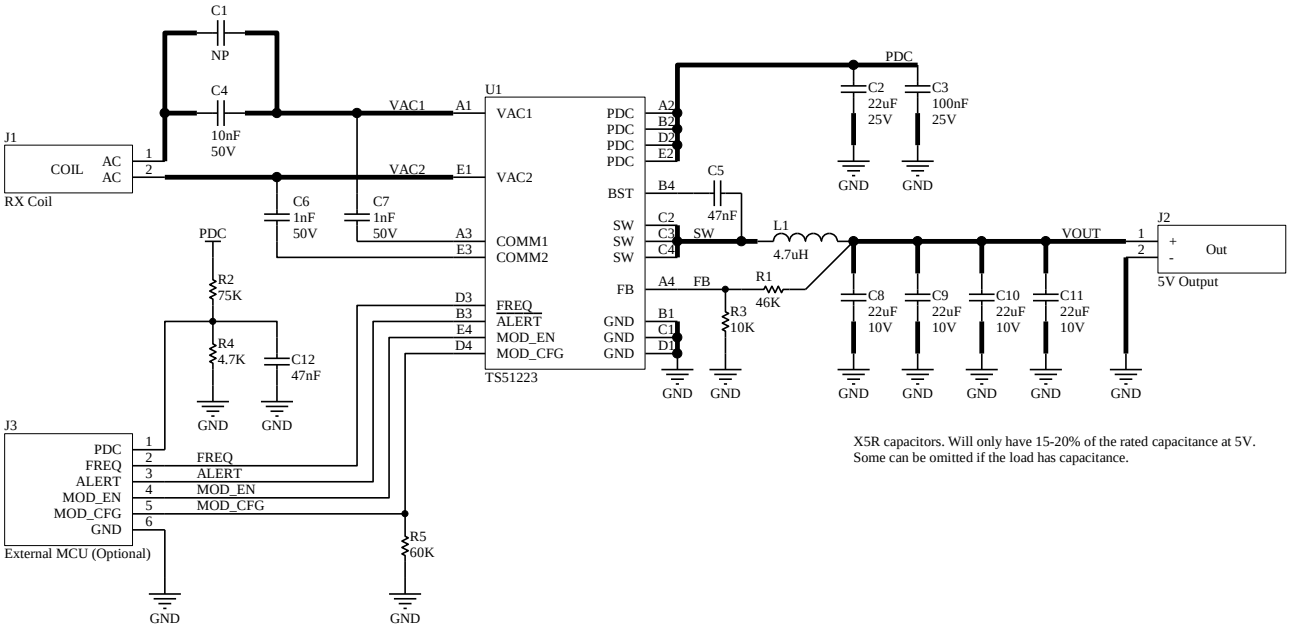
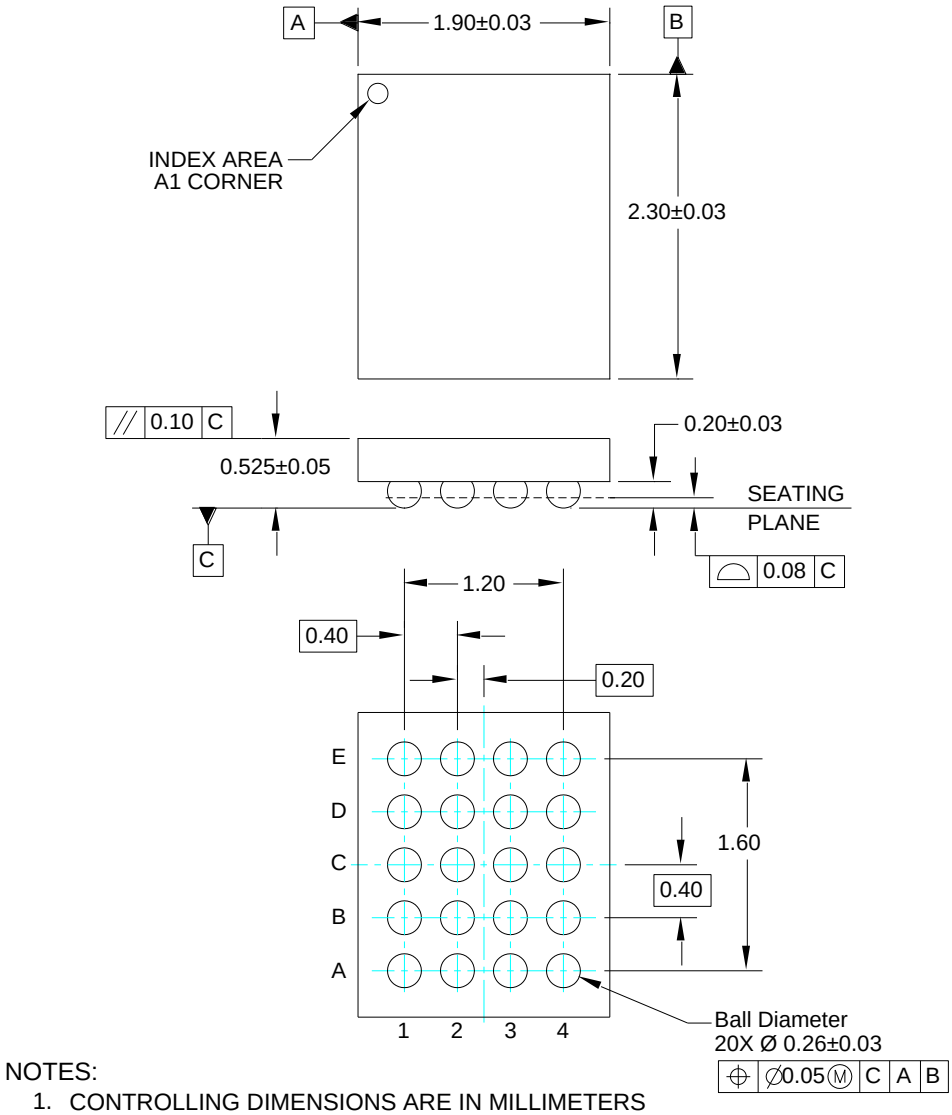


Figure 6: Standard Configuration
(V_{PDC}=12V, V_{OUT}=5V, I_{OUT}=100~400mA)



NOTES:
1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS

Figure 7: Package Outline Drawing

Package Information (continued)

BACK SIDE VIEW (BUMPS DOWN)

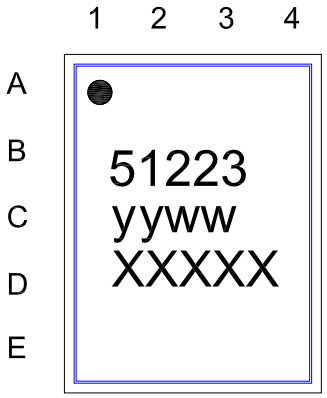
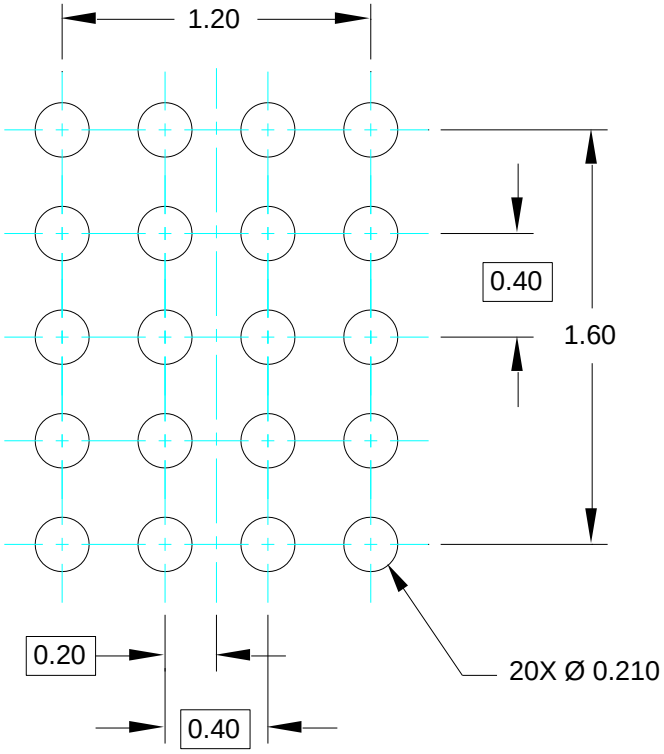


Figure 8: Device Symbolization



NOTES:

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2. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.

Figure 9: Recommended Board Layout Land Pattern

Ordering Information

Device Part Number	Description	20 Ball WCSP Package (4x5 ball array, 0.4mm ball pitch)
TS51223-M000WCSR	Wireless Power Receiver, external resistor feedback	Tape & Reel (3000 parts/reel)

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