## Thermal Characteristics

| Package | $I_D$ (continuous)† | $I_D$ (pulsed) | Power Dissipation @$T_A$ = 25°C | $I_{DR}$† | $I_{DRM}$ |
|---|---|---|---|---|---|
| TO-92 | -175mA | -800mA | 1.0W | -175mA | -800mA |

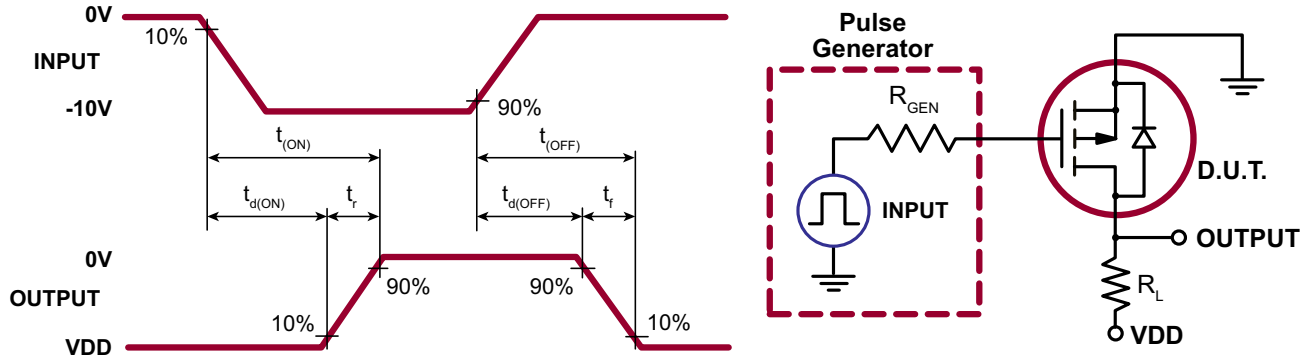
***Notes:***
*† $I_D$ (continuous) is limited by max rated $T_j$ .*

## Electrical Characteristics *($T_A$ = 25°C unless otherwise specified)*

| Sym | Parameter | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|---|
| $BV_{DSS}$ | Drain-to-source breakdown voltage | -200 | - | - | V | $V_{GS}$ = 0V, $I_D$ = -2.0mA |
| $V_{GS(th)}$ | Gate threshold voltage | -1.0 | - | -2.4 | V | $V_{GS}$ = $V_{DS}$, $I_D$= -1.0mA |
| $\Delta V_{GS(th)}$ | Change in $V_{GS(th)}$ with temperature | - | - | -4.5 | mV/°C | $V_{GS}$ = $V_{DS}$, $I_D$= -1.0mA |
| $I_{GSS}$ | Gate body leakage | - | - | -100 | nA | $V_{GS}$ = ± 20V, $V_{DS}$ = 0V |
| $I_{DSS}$ | Zero gate voltage drain current | - | - | -10 | µA | $V_{GS}$ = 0V, $V_{DS}$ = Max Rating |
| | | - | - | -1.0 | mA | $V_{DS}$ = 0.8 Max Rating, $V_{GS}$ = 0V, $T_A$ = 125°C |
| $I_{D(ON)}$ | ON-state drain current | -0.25 | - | - | A | $V_{GS}$ = -5.0V, $V_{DS}$ = -25V |
| | | -0.75 | - | - | | $V_{GS}$ = -10V, $V_{DS}$ = -25V |
| $R_{DS(ON)}$ | Static drain-to-source on-state resistance | - | 9.0 | 15 | Ω | $V_{GS}$ = -5.0V, $I_D$ = -100mA |
| | | - | 7.0 | 12 | | $V_{GS}$ = -10V, $I_D$ = -200mA |
| $\Delta R_{DS(ON)}$ | Change in $R_{DS(ON)}$ with temperature | - | - | 1.7 | %/°C | $V_{GS}$ = -10V, $I_D$ = -200mA |
| $G_{FS}$ | Forward transductance | 100 | 150 | - | mmho | $V_{DS}$ = -25V, $I_D$ = -400mA |
| $C_{ISS}$ | Input capacitance | - | 85 | 150 | pF | $V_{GS}$ = 0V, $V_{DS}$ = -25V, f = 1.0MHz |
| $C_{OSS}$ | Common source output capacitance | - | 30 | 85 | | |
| $C_{RSS}$ | Reverse transfer capacitance | - | 10 | 35 | | |
| $t_{d(ON)}$ | Turn-on delay time | - | - | 10 | ns | $V_{DD}$ = -25V, $I_D$ = -750mA, $R_{GEN}$ = 25Ω |
| $t_r$ | Rise time | - | - | 15 | | |
| $t_{d(OFF)}$ | Turn-off delay time | - | - | 20 | | |
| $t_f$ | Fall time | - | - | 16 | | |
| $V_{SD}$ | Diode forward voltage drop | - | - | -1.8 | V | $V_{GS}$ = 0V, $I_{SD}$ = -500mA |
| $t_{rr}$ | Reverse recovery time | - | 300 | - | ns | $V_{GS}$ = 0V, $I_{SD}$ = -500mA |

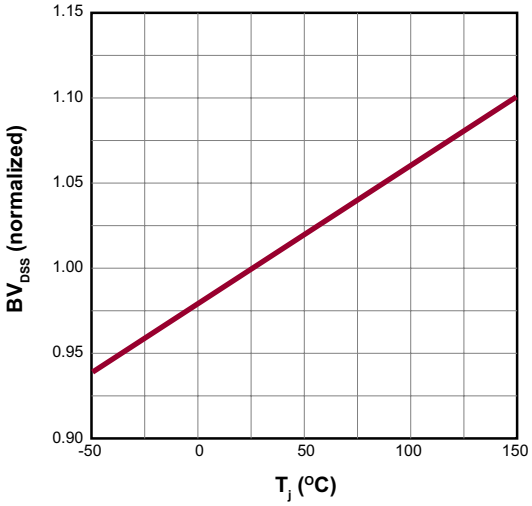
***Notes:***
1. *All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)*
2. *All A.C. parameters sample tested.*

## Switching Waveforms and Test Circuit

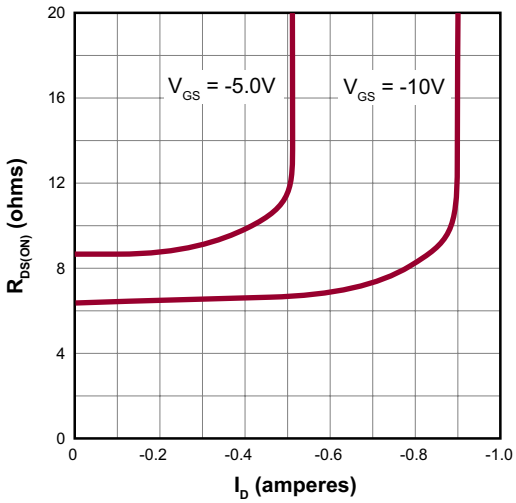


## Typical Performance Curves

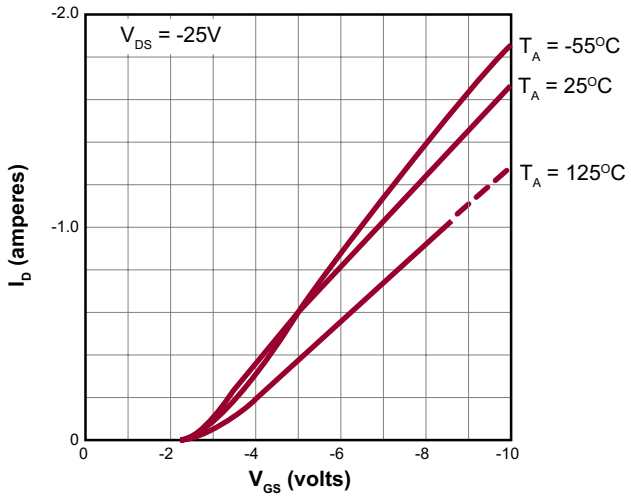
### $BV_{DSS}$ Variation with Temperature



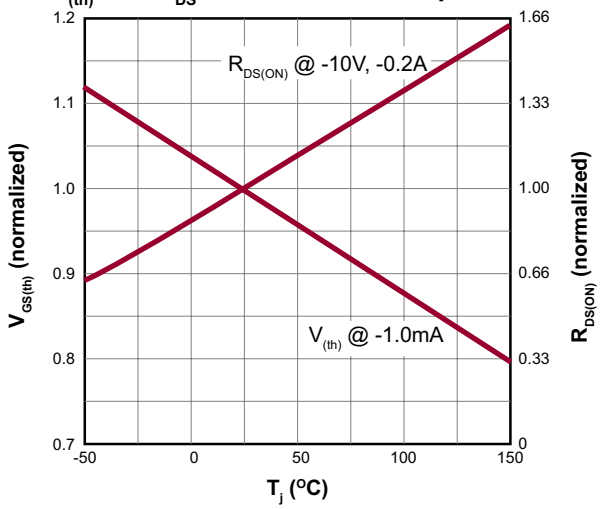

### On-Resistance vs. Drain Current



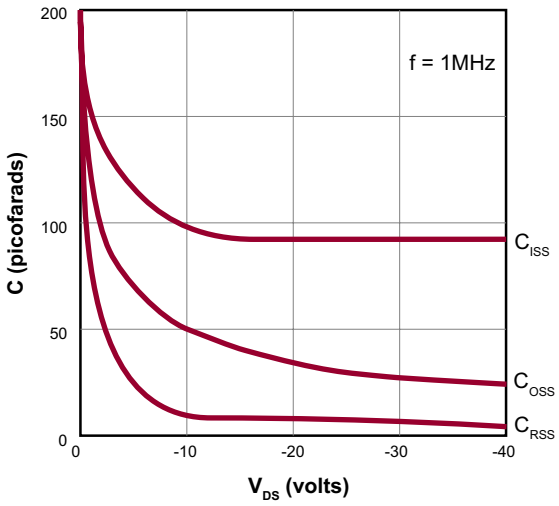

### Transfer Characteristics



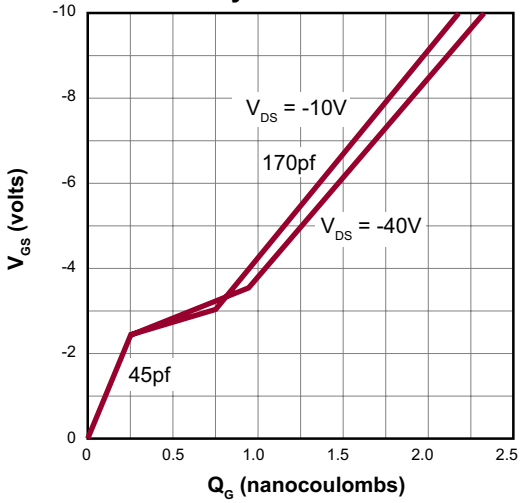

### $V_{(th)}$ and $R_{DS}$ Variation with Temperature




### Capacitance vs. Drain-to-Source Voltage

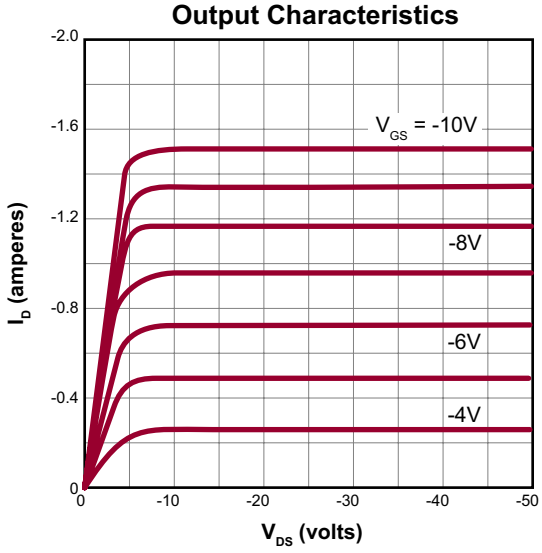



### Gate Drive Dynamic Characteristics

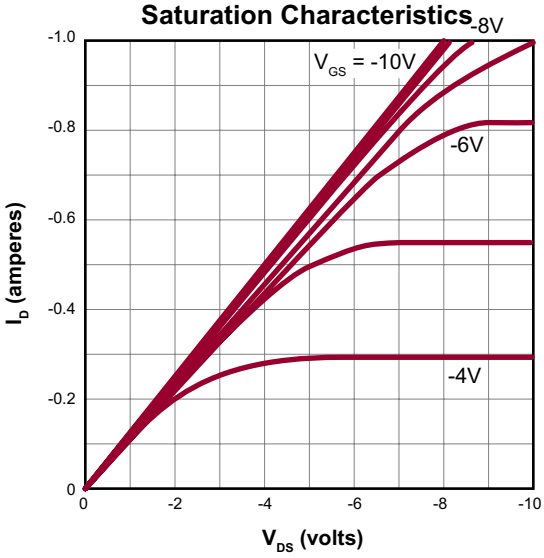


## Typical Performance Curves *(cont.)*

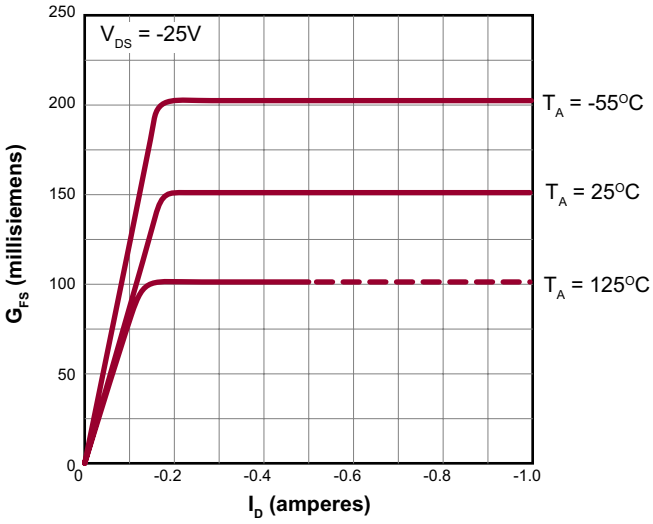
### Output Characteristics



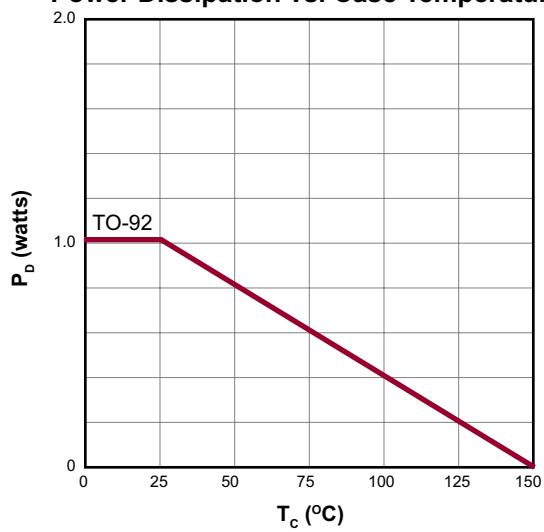

### Saturation Characteristics



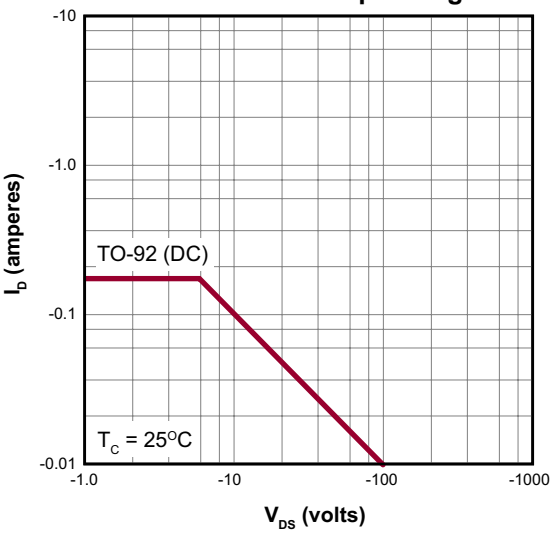

### Transconductance vs. Drain Current



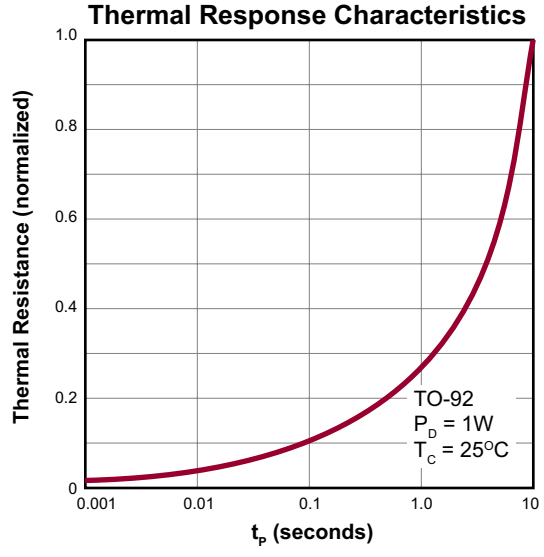

### Power Dissipation vs. Case Temperature



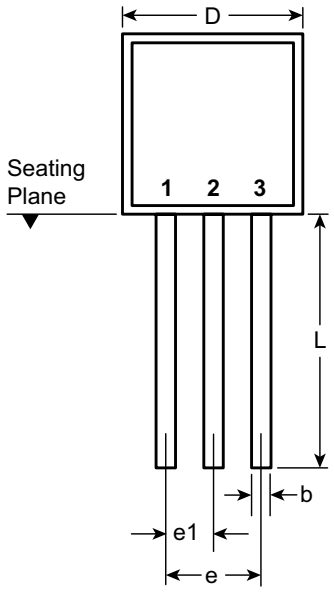

### Maximum Rated Safe Operating Area



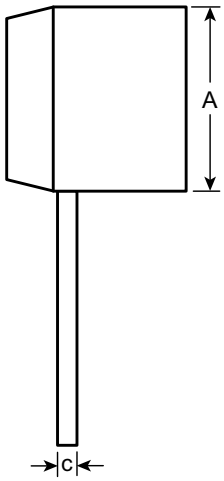

### Thermal Response Characteristics



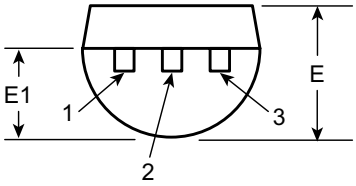
# 3-Lead TO-92 Package Outline (N3)




**Front View**




**Side View**




**Bottom View**

| Symbol | | A | b | c | D | E | E1 | e | e1 | L |
|---|---|---|---|---|---|---|---|---|---|---|
| Dimensions (inches) | MIN | .170 | .014† | .014† | .175 | .125 | .080 | .095 | .045 | .500 |
| | NOM | - | - | - | - | - | - | - | - | - |
| | MAX | .210 | .022† | .022† | .205 | .165 | .105 | .105 | .055 | .610* |

*JEDEC Registration TO-92.*
** This dimension is not specified in the JEDEC drawing.*
*† This dimension differs from the JEDEC drawing.*
***Drawings not to scale.***
***Supertex Doc.#:** DSPD-3TO92N3, Version E041009.*

*(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to http://www.supertex.com/packaging.html.)*



Supertex inc.
1235 Bordeaux Drive, Sunnyvale, CA 94089
Tel: 408-222-8888
**www.supertex.com**