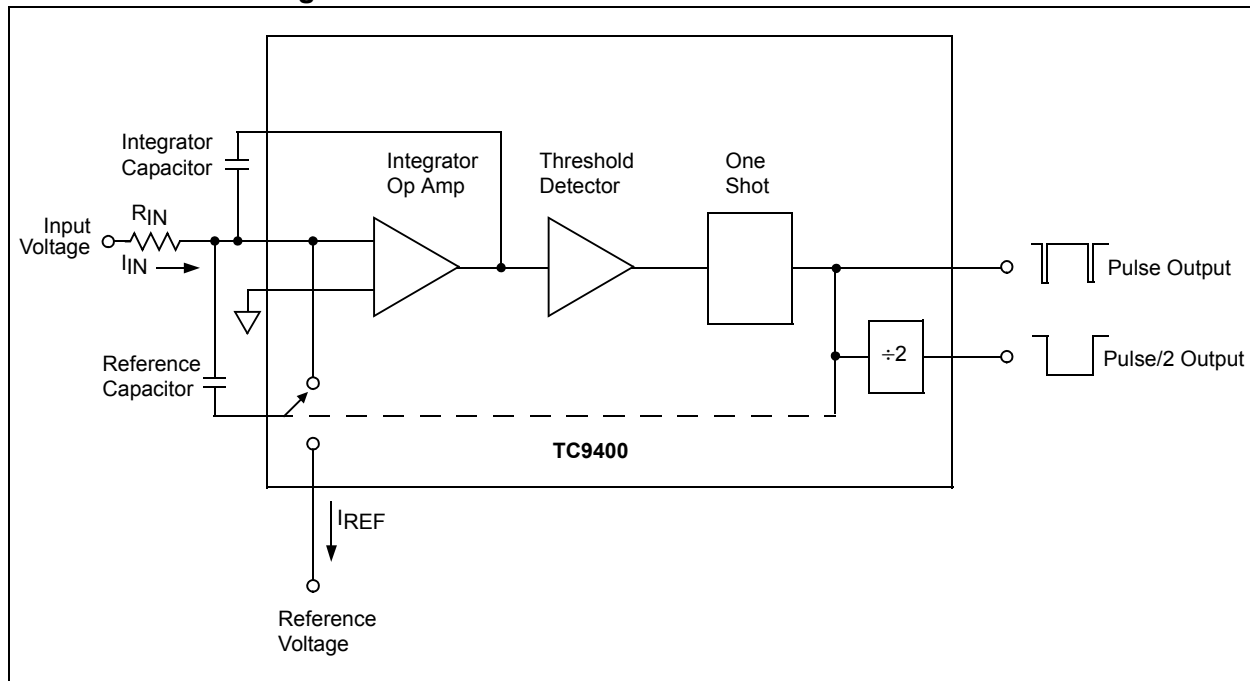


TC9400/9401/9402

Functional Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

$V_{DD} - V_{SS}$	+18V
I_{IN}	10 mA
$V_{OUTMAX} - V_{OUT}$ Common.....	23V
$V_{REF} - V_{SS}$	-1.5V
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range:	
C Device	0°C to +70°C
E Device.....	-40°C to +85°C
Package Dissipation ($T_A \leq 70^\circ\text{C}$):	
8-Pin CerDIP	800 mW
8-Pin Plastic DIP	730 mW
8-Pin SOIC.....	470 mW

† Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operation sections of the specifications is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

TC940X ELECTRICAL SPECIFICATIONS

Electrical Characteristics: unless otherwise specified, $V_{DD} = +5V$, $V_{SS} = -5V$, $V_{GND} = 0V$, $V_{REF} = -5V$, $R_{BIAS} = 100\text{ k}\Omega$, Full Scale = 10 kHz. $T_A = +25^\circ\text{C}$, unless temperature range is specified (-40°C to +85°C for E device, 0°C to +70°C for C device).

Parameter	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Units	Test Conditions
Voltage-to-Frequency											
Accuracy	TC9400			TC9401			TC9402				
Linearity 10 kHz	—	0.01	0.05	—	0.004	0.01	—	0.05	0.25	% Full Scale	Output Deviation from Straight Line Between Normalized Zero and Full Scale Input
Linearity 100 kHz	—	0.1	0.25	—	0.04	0.08	—	0.25	0.5	% Full Scale	Output Deviation from Straight Line Between Normalized Zero Reading and Full Scale Input
Gain Temperature Drift (Note 1)	—	± 25	± 40	—	± 25	± 40	—	± 50	± 100	ppm/°C Full Scale	Variation in Gain A due to Temperature Change
Gain Variance	—	± 10	—	—	± 10	—	—	± 10	—	% of Nominal	Variation from Ideal Accuracy
Zero Offset (Note 2)	—	± 10	± 50	—	± 10	± 50	—	± 20	± 100	mV	Correction at Zero Adjust for Zero Output when Input is Zero
Zero Temperature Drift (Note 1)	—	± 25	± 50	—	± 25	± 50	—	± 50	± 100	$\mu\text{V}/^\circ\text{C}$	Variation in Zero Offset Due to Temperature Change

- Note**
- 1: Full temperature range; not tested.
 - 2: $I_{IN} = 0$.
 - 3: Full temperature range, $I_{OUT} = 10\text{ mA}$.
 - 4: $I_{OUT} = 10\text{ }\mu\text{A}$.
 - 5: Threshold Detect = 5V, Amp Out = 0V, full temperature range.
 - 6: 10 Hz to 100 kHz; not tested.
 - 7: 5 μs minimum positive pulse width and 0.5 μs minimum negative pulse width.
 - 8: $t_R = t_F = 20\text{ ns}$.
 - 9: $R_L \geq 2\text{ k}\Omega$, tested @ 10 k Ω .
 - 10: Full temperature range, $V_{IN} = -0.1V$.

TC9400/9401/9402

TC940X ELECTRICAL SPECIFICATIONS (CONTINUED)

Electrical Characteristics: unless otherwise specified, $V_{DD} = +5V$, $V_{SS} = -5V$, $V_{GND} = 0V$, $V_{REF} = -5V$, $R_{BIAS} = 100\text{ k}\Omega$, Full Scale = 10 kHz. $T_A = +25^\circ\text{C}$, unless temperature range is specified (-40°C to $+85^\circ\text{C}$ for E device, 0°C to $+70^\circ\text{C}$ for C device).

Parameter	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Units	Test Conditions
Analog Input											
I_{IN} Full Scale	—	10	—	—	10	—	—	10	—	μA	Full Scale Analog Input Current to achieve Specified Accuracy
I_{IN} Over Range	—	—	50	—	—	50	—	—	50	μA	Over Range Current
Response Time	—	2	—	—	2	—	—	2	—	Cycle	Settling Time to 0.1% Full Scale
Digital Section	TC9400			TC9401			TC9402				
$V_{SAT} @ I_{OL} = 10\text{mA}$	—	0.2	0.4	—	0.2	0.4	—	0.2	0.4	V	Logic "0" Output Voltage (Note 3)
$V_{OUTMAX} - V_{OUT}$ Common (Note 4)	—	—	18	—	—	18	—	—	18	V	Voltage Range Between Output and Common
Pulse Frequency Output Width	—	3	—	—	3	—	—	3	—	μs	
Frequency-to-Voltage											
Supply Current											
I_{DD} Quiescent (Note 5)	—	1.5	6	—	1.5	6	—	3	10	mA	Current Required from Positive Supply during Operation
I_{SS} Quiescent (Note 5)	—	-1.5	-6	—	-1.5	-6	—	-3	-10	mA	Current Required from Negative Supply during Operation
V_{DD} Supply	4	—	7.5	4	—	7.5	4	—	7.5	V	Operating Range of Positive Supply
V_{SS} Supply	-4	—	-7.5	-4	—	-7.5	-4	—	-7.5	V	Operating Range of Negative Supply
Reference Voltage											
$V_{REF} - V_{SS}$	-2.5	—	—	-2.5	—	—	-2.5	—	—	V	Range of Voltage Reference Input
Accuracy											
Non-Linearity (Note 10)	—	0.02	0.05	—	0.01	0.02	—	0.05	0.25	% Full Scale	Deviation from ideal Transfer Function as a Percentage Full Scale Voltage
Input Frequency Range (Notes 7 and 8)	10	—	100k	10	—	100k	10	—	100k	Hz	Frequency Range for Specified Non-Linearity

Note 1: Full temperature range; not tested.

2: $I_{IN} = 0$.

3: Full temperature range, $I_{OUT} = 10\text{ mA}$.

4: $I_{OUT} = 10\text{ }\mu\text{A}$.

5: Threshold Detect = 5V, Amp Out = 0V, full temperature range.

6: 10 Hz to 100 kHz; not tested.

7: 5 μs minimum positive pulse width and 0.5 μs minimum negative pulse width.

8: $t_R = t_F = 20\text{ ns}$.

9: $R_L \geq 2\text{ k}\Omega$, tested @ 10 k Ω .

10: Full temperature range, $V_{IN} = -0.1V$.

TC940X ELECTRICAL SPECIFICATIONS (CONTINUED)

Electrical Characteristics: unless otherwise specified, $V_{DD} = +5V$, $V_{SS} = -5V$, $V_{GND} = 0V$, $V_{REF} = -5V$, $R_{BIAS} = 100\text{ k}\Omega$, Full Scale = 10 kHz. $T_A = +25^\circ\text{C}$, unless temperature range is specified (-40°C to $+85^\circ\text{C}$ for E device, 0°C to $+70^\circ\text{C}$ for C device).

Parameter	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Units	Test Conditions
Frequency Input											
Positive Excursion	0.4	—	V_{DD}	0.4	—	V_{DD}	0.4	—	V_{DD}	V	Voltage Required to Turn Threshold Detector On
Negative Excursion	-0.4	—	-2	-0.4	—	-2	-0.4	—	-2	V	Voltage Required to Turn Threshold Detector Off
Minimum Positive Pulse Width (Note 8)	—	5	—	—	5	—	—	5	—	μs	Time between Threshold Crossings
Minimum Negative Pulse Width (Note 8)	—	0.5	—	—	0.5	—	—	0.5	—	μs	Time Between Threshold Crossings
Input Impedance	—	10	—	—	10	—	—	—	10	$\text{M}\Omega$	
Analog Outputs											
	TC9400			TC9401			TC9402				
Output Voltage (Note 9)	—	$V_{DD} - 1$	—	—	$V_{DD} - 1$	—	—	$V_{DD} - 1$	—	V	Voltage Range of Op Amp Output for Specified Non-Linearity
Output Loading	2	—	—	2	—	—	2	—	—	$\text{k}\Omega$	Resistive Loading at Output of Op Amp
Supply Current											
	TC9400			TC9401			TC9402				
I_{DD} Quiescent (Note 10)	—	1.5	6	—	1.5	6	—	3	10	mA	Current Required from Positive Supply During Operation
I_{SS} Quiescent (Note 10)	—	-1.5	-6	—	-1.5	-6	—	-3	-10	mA	Current Required from Negative Supply During Operation
V_{DD} Supply	4	—	7.5	4	—	7.5	4	—	7.5	V	Operating Range of Positive Supply
V_{SS} Supply	-4	—	-7.5	-4	—	-7.5	-4	—	-7.5	V	Operating Range of Negative Supply
Reference Voltage											
$V_{REF} - V_{SS}$	-2.5	—	—	-2.5	—	—	-2.5	—	—	V	Range of Voltage Reference Input

- Note** 1: Full temperature range; not tested.
 2: $I_{IN} = 0$.
 3: Full temperature range, $I_{OUT} = 10\text{ mA}$.
 4: $I_{OUT} = 10\text{ }\mu\text{A}$.
 5: Threshold Detect = 5V, Amp Out = 0V, full temperature range.
 6: 10 Hz to 100 kHz; not tested.
 7: 5 μs minimum positive pulse width and 0.5 μs minimum negative pulse width.
 8: $t_R = t_F = 20\text{ ns}$.
 9: $R_L \geq 2\text{ k}\Omega$, tested @ 10 $\text{k}\Omega$.
 10: Full temperature range, $V_{IN} = -0.1V$.

TC9400/9401/9402

2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in [Table 2-1](#).

TABLE 2-1: PIN FUNCTION TABLE

Pin No.	Symbol	Description
1	I_{BIAS}	This pin sets bias current in the TC9400. Connect to V_{SS} through a 100 k Ω resistor.
2	ZERO ADJ	Low frequency adjustment input.
3	I_{IN}	Input current connection for the V/F converter.
4	V_{SS}	Negative power supply voltage connection, typically -5V.
5	V_{REF} OUT	Reference capacitor connection.
6	GND	Analog ground.
7	V_{REF}	Voltage reference input, typically -5V.
8	PULSE FREQ OUT	Frequency output. This open drain output will pulse LOW each time the Freq. Threshold Detector limit is reached. The pulse rate is proportional to input voltage.
9	OUTPUT COMMON	Source connection for the open drain output FETs.
10	FREQ/2 OUT	This open drain output is a square wave at one-half the frequency of the pulse output (Pin 8). Output transitions of this pin occur on the rising edge of Pin 8.
11	THRESHOLD DETECTOR	Input to the Threshold Detector. This pin is the frequency input during F/V operation.
12	AMPLIFIER OUT	Output of the integrator amplifier.
13	NC	No internal connection.
14	V_{DD}	Positive power supply connection, typically +5V.

2.1 Bias Current (I_{BIAS})

An external resistor, connected to V_{SS} , sets the bias point for the TC9400. Specifications for the TC9400 are based on $R_{BIAS} = 100 \text{ k}\Omega \pm 10\%$, unless otherwise noted.

Increasing the maximum frequency of the TC9400 beyond 100 kHz is limited by the pulse width of the pulse output (typically 3 μs). Reducing R_{BIAS} will decrease the pulse width and increase the maximum operating frequency, but linearity errors will also increase. R_{BIAS} can be reduced to 20 k Ω , which will typically produce a maximum full scale frequency of 500 kHz.

2.2 Zero Adjust

This pin is the non-inverting input of the operational amplifier. The low frequency set point is determined by adjusting the voltage at this pin.

2.3 Input Current (I_{IN})

The inverting input of the operational amplifier and the summing junction when connected in the V/F mode. An input current of 10 μA is specified, but an over range current up to 50 μA can be used without detrimental effect to the circuit operation. I_{IN} connects the summing junction of an operational amplifier. Voltage sources cannot be attached directly, but must be buffered by external resistors.

2.4 Voltage Capacitor (V_{REF} Out)

The charging current for C_{REF} is supplied through this pin. When the op amp output reaches the threshold level, this pin is internally connected to the reference voltage and a charge, equal to $V_{REF} \times C_{REF}$, is removed from the integrator capacitor. After about 3 μsec , this pin is internally connected to the summing junction of the op amp to discharge C_{REF} . Break-before-make switching ensures that the reference voltage is not directly applied to the summing junction.

2.5 Voltage Reference (V_{REF})

A reference voltage from either a precision source, or the V_{SS} supply is applied to this pin. Accuracy of the TC9400 is dependent on the voltage regulation and temperature characteristics of the reference circuitry.

Since the TC9400 is a charge balancing V/F converter, the reference current will be equal to the input current. For this reason, the DC impedance of the reference voltage source must be kept low enough to prevent linearity errors. For linearity of 0.01%, a reference impedance of 200 Ω or less is recommended. A 0.1 μF bypass capacitor should be connected from V_{REF} to ground.

2.6 Pulse Freq Out

This output is an open-drain N-channel FET, which provides a pulse waveform whose frequency is proportional to the input voltage. This output requires a pull-up resistor and interfaces directly with MOS, CMOS, and TTL logic (see [Figure 2-1](#)).

2.7 Output Common

The sources of both the FREQ/2 OUT and the PULSE FREQ OUT are connected to this pin. An output level swing from the drain voltage to ground, or to the V_{SS} supply, may be obtained by connecting this pin to the appropriate point.

2.8 Freq/2 Out

This output is an open-drain N-channel FET, which provides a square-wave one-half the frequency of the pulse frequency output. The FREQ/2 OUT output will change state on the rising edge of PULSE FREQ OUT. This output requires a pull-up resistor and interfaces directly with MOS, CMOS, and TTL logic.

2.9 Threshold Detector Input

In the V/F mode, this input is connected to the AMPLIFIER OUT output (Pin 12) and triggers a 3 μ s pulse when the input voltage passes through its threshold. In the F/V mode, the input frequency is applied to this input.

The nominal threshold of the detector is half way between the power supplies, or $(V_{DD} + V_{SS})/2 \pm 400$ mV. The TC9400's charge balancing V/F technique is not dependent on a precision comparator threshold, because the threshold only sets the lower limit of the op amp output. The op amp's peak-to-peak output swing, which determines the frequency, is only influenced by external capacitors and by V_{REF} .

2.10 Amplifier Out

This pin is the output stage of the operational amplifier. During V/F operation, a negative going ramp signal is available at this pin. In the F/V mode, a voltage proportional to the frequency input is generated.

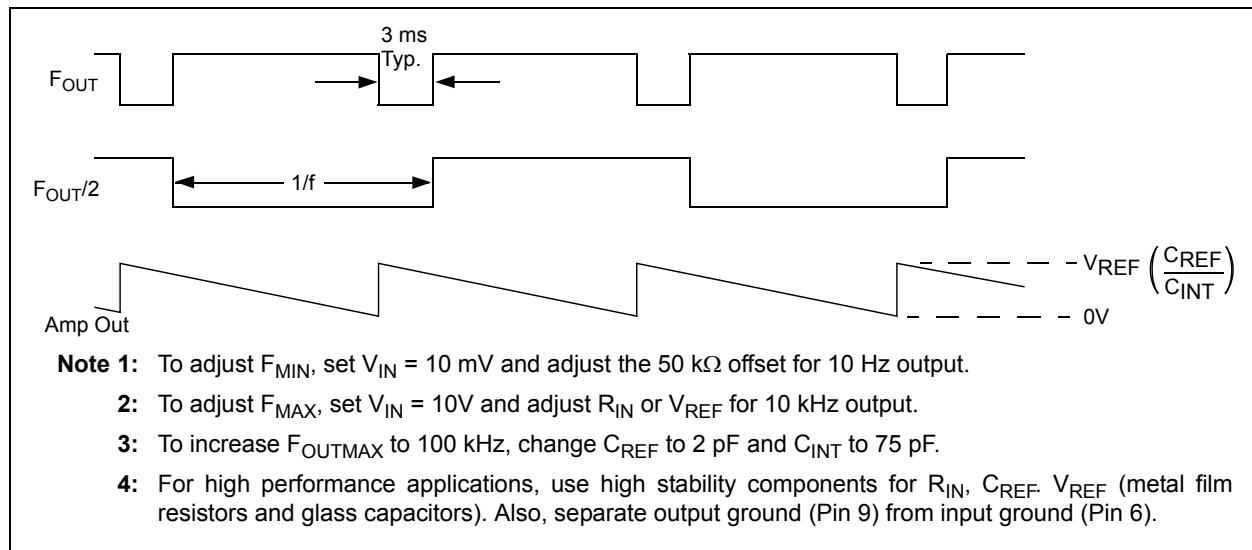


FIGURE 2-1: Output Waveforms.

TC9400/9401/9402

3.0 DETAILED DESCRIPTION

3.1 Voltage-to-Frequency (V/F) Circuit Description

The TC9400 V/F converter operates on the principal of charge balancing. The operation of the TC9400 is easily understood by referring to Figure 3-1. The input voltage (V_{IN}) is converted to a current (I_{IN}) by the input resistor. This current is then converted to a charge on the integrating capacitor and shows up as a linearly decreasing voltage at the output of the op amp. The lower limit of the output swing is set by the threshold detector, which causes the reference voltage to be applied to the reference capacitor for a time period long enough to charge the capacitor to the reference voltage. This action reduces the charge on the integrating capacitor by a fixed amount ($q = C_{REF} \times V_{REF}$), causing the op amp output to step up a finite amount.

At the end of the charging period, C_{REF} is shorted out. This dissipates the charge stored on the reference capacitor, so that when the output again crosses zero, the system is ready to recycle. In this manner, the continued discharging of the integrating capacitor by the input is balanced out by fixed charges from the refer-

ence voltage. As the input voltage is increased, the number of reference pulses required to maintain balance increases, which causes the output frequency to also increase. Since each charge increment is fixed, the increase in frequency with voltage is linear. In addition, the accuracy of the output pulse width does not directly affect the linearity of the V/F. The pulse must simply be long enough for full charge transfer to take place.

The TC9400 contains a "self-start" circuit to ensure the V/F converter always operates properly when power is first applied. In the event that, during power-on, the op amp output is below the threshold and C_{REF} is already charged, a positive voltage step will not occur. The op amp output will continue to decrease until it crosses the -3.0V threshold of the "self-start" comparator. When this happens, an internal resistor is connected to the op amp input, which forces the output to go positive until the TC9400 is in its normal Operating mode.

The TC9400 utilizes low-power CMOS processing for low input bias and offset currents, with very low power dissipation. The open drain N-channel output FETs provide high voltage and high current sink capability.

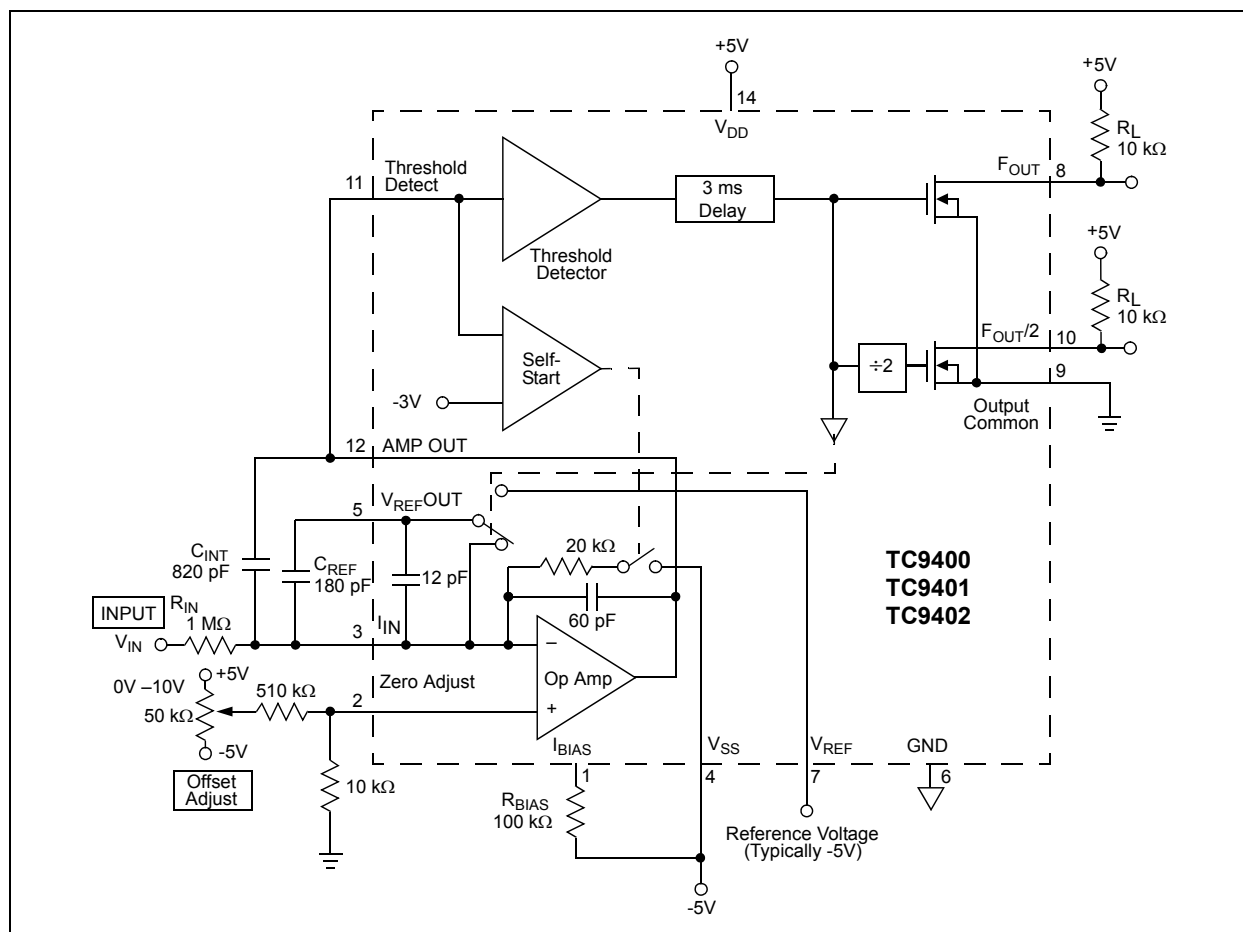


FIGURE 3-1: 10 Hz to 10 kHz V/F Converter.

3.2 Voltage-to-Time Measurements

The TC9400 output can be measured in the time domain as well as the frequency domain. Some microcomputers, for example, have extensive timing capability, but limited counter capability. Also, the response time of a time domain measurement is only the period between two output pulses, while the frequency measurement must accumulate pulses during the entire counter time-base period.

Time measurements can be made from either the TC9400's PULSE FREQ OUT output, or from the FREQ/2 OUT output. The FREQ/2 OUT output changes state on the rising edge of PULSE FREQ OUT, so FREQ/2 OUT is a symmetrical square wave at one-half the pulse output frequency. Timing measurements can, therefore, be made between successive PULSE FREQ OUT pulses, or while FREQ/2 OUT is high (or low).

TC9400/9401/9402

4.0 VOLTAGE-TO-FREQUENCY (V/F) CONVERTER DESIGN INFORMATION

4.1 Input/Output Relationships

The output frequency (F_{OUT}) is related to the analog input voltage (V_{IN}) by the transfer equation:

EQUATION 4-1:

$$\text{Frequency Out} = \frac{V_{IN}}{R_{IN}} \cdot \frac{1}{(V_{REF})(C_{REF})}$$

4.2 External Component Selection

4.2.1 R_{IN}

The value of this component is chosen to give a full scale input current of approximately 10 μA :

EQUATION 4-2:

$$R_{IN} \cong \frac{V_{IN}^{FULL SCALE}}{10 \mu\text{A}}$$

EQUATION 4-3:

$$R_{IN} \cong \frac{10V}{10 \mu\text{A}} = 1 M\Omega$$

Note that the value is an approximation and the exact relationship is defined by the transfer equation. In practice, the value of R_{IN} typically would be trimmed to obtain full scale frequency at V_{IN} full scale (see **Section 4.3 "Adjustment Procedure"**, Adjustment Procedure). Metal film resistors with 1% tolerance or better are recommended for high accuracy applications because of their thermal stability and low noise generation.

4.2.2 C_{INT}

The exact value is not critical but is related to C_{REF} by the relationship:

$$3C_{REF} \leq C_{INT} \leq 10C_{REF}$$

Improved stability and linearity are obtained when $C_{INT} \leq 4C_{REF}$. Low leakage types are recommended, although mica and ceramic devices can be used in applications where their temperature limits are not exceeded. Locate as close as possible to Pins 12 and 13.

4.2.3 C_{REF}

The exact value is not critical and may be used to trim the full scale frequency (see **Section 6.1 "Input/Output Relationships"**, Input/Output Relationships). Glass film or air trimmer capacitors are recommended because of their stability and low leakage. Locate as close as possible to Pins 5 and 3 (see **Figure 4-1**).

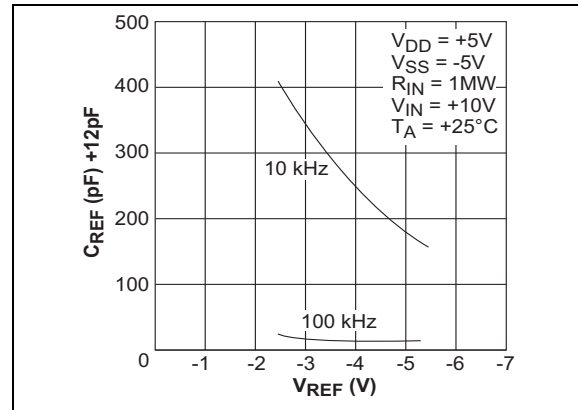


FIGURE 4-1: Recommended C_{REF} vs. V_{REF} .

4.2.4 V_{DD} , V_{SS}

Power supplies of $\pm 5V$ are recommended. For high accuracy requirements, 0.05% line and load regulation and 0.1 μF disc decoupling capacitors, located near the pins, are recommended.

4.3 Adjustment Procedure

Figure 3-1 shows a circuit for trimming the zero location. Full scale may be trimmed by adjusting R_{IN} , V_{REF} , or C_{REF} . Recommended procedure for a 10 kHz full scale frequency is as follows:

1. Set V_{IN} to 10 mV and trim the zero adjust circuit to obtain a 10 Hz output frequency.
2. Set V_{IN} to 10V and trim either R_{IN} , V_{REF} , or C_{REF} to obtain a 10 kHz output frequency.

If adjustments are performed in this order, there should be no interaction and they should not have to be repeated.

4.4 Improved Single Supply V/F Converter Operation

A TC9400, which operates from a single 12 to 15V variable power source, is shown in **Figure 4-2**. This circuit uses two Zener diodes to set stable biasing levels for the TC9400. The Zener diodes also provide the reference voltage, so the output impedance and temperature coefficient of the Zeners will directly affect power supply rejection and temperature performance. Full scale adjustment is accomplished by trimming the input current.

Trimming the reference voltage is not recommended for high accuracy applications unless an op amp is used as a buffer, because the TC9400 requires a low-impedance reference (see **Section 2.5 “Voltage Reference (VREF)”**, V_{REF} pin description, for more information).

The circuit of [Figure 4-2](#) will directly interface with CMOS logic operating at 12V to 15V. TTL or 5V CMOS logic can be accommodated by connecting the output pull-up resistors to the +5V supply. An optoisolator can also be used if an isolated output is required; also, see [Figure 4-3](#).

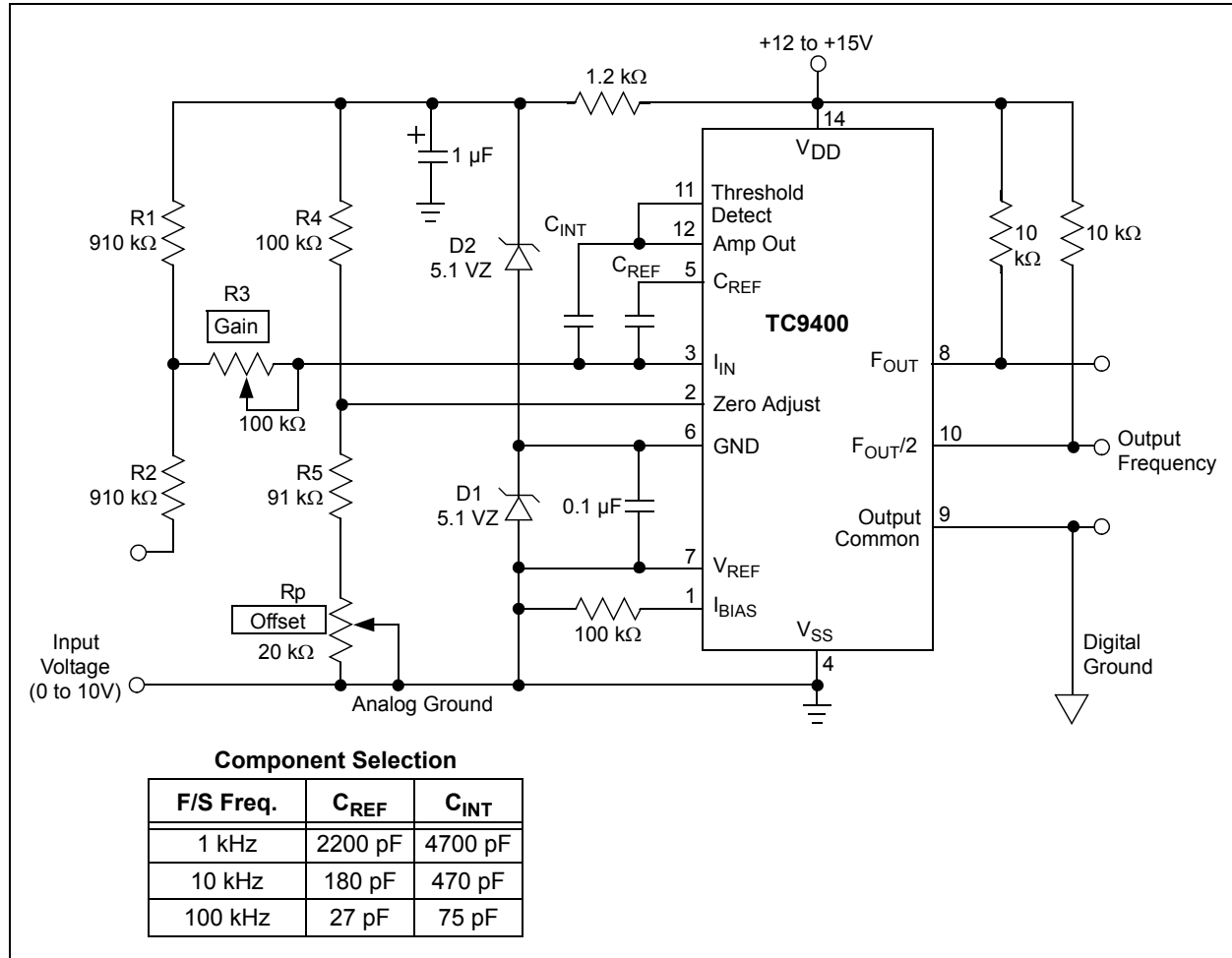


FIGURE 4-2: Voltage-to-Frequency.

TC9400/9401/9402

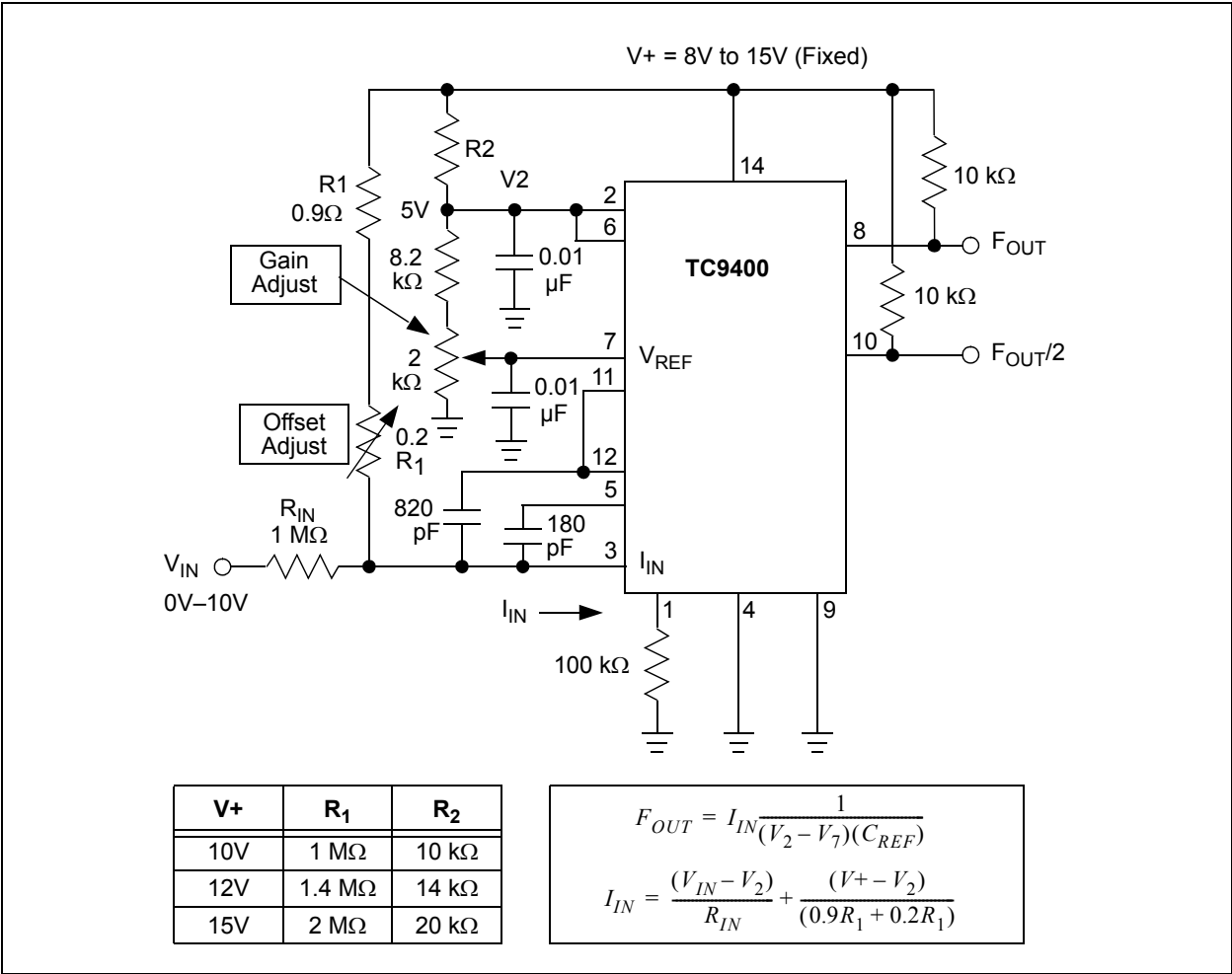


FIGURE 4-3: Fixed Voltage – Single Supply Operation.

5.0 FREQUENCY-TO-VOLTAGE (F/V) CIRCUIT DESCRIPTION

When used as an F/V converter, the TC9400 generates an output voltage linearly proportional to the input frequency waveform.

Each zero crossing at the threshold detector's input causes a precise amount of charge ($q = C_{REF} \times V_{REF}$) to be dispensed into the op amp's summing junction. This charge, in turn, flows through the feedback resistor, generating voltage pulses at the output of the op amp. A capacitor (C_{INT}) across R_{INT} averages these pulses into a DC voltage, which is linearly proportional to the input frequency.

TC9400/9401/9402

6.0 F/V CONVERTER DESIGN INFORMATION

6.1 Input/Output Relationships

The output voltage is related to the input frequency (F_{IN}) by the transfer equation:

EQUATION 6-1:

$$V_{OUT} = [V_{REF} C_{REF} R_{INT}] F_{IN}$$

The response time to a change in F_{IN} is equal to $(R_{INT} C_{INT})$. The amount of ripple on V_{OUT} is inversely proportional to C_{INT} and the input frequency.

C_{INT} can be increased to lower the ripple. Values of 1 μF to 100 μF are perfectly acceptable for low frequencies.

When the TC9400 is used in the Single Supply mode, V_{REF} is defined as the voltage difference between Pin 7 and Pin 2.

6.2 Input Voltage Levels

The input frequency is applied to the Threshold Detector input (Pin 11). As discussed in the V/F circuit section of this data sheet, the threshold of Pin 11 is approximately $(V_{DD} + V_{SS})/2 \pm 400$ mV. Pin 11's input voltage range extends from V_{DD} to about 2.5V below the threshold. If the voltage on Pin 11 goes more than 2.5 volts below the threshold, the V/F mode start-up comparator will turn on and corrupt the output voltage. The Threshold Detector input has about 200 mV of hysteresis.

In $\pm 5V$ applications, the input voltage levels for the TC9400 are ± 400 mV, minimum. If the frequency source being measured is unipolar, such as TTL or CMOS operating from a +5V source, then an AC coupled level shifter should be used. One such circuit is shown in Figure 6-1(a).

The level shifter circuit in Figure 6-1(b) can be used in single supply F/V applications. The resistor divider ensures that the input threshold will track the supply voltages. The diode clamp prevents the input from going far enough in the negative direction to turn on the start-up comparator. The diode's forward voltage decreases by 2.1 mV/ $^{\circ}C$, so for high ambient temperature operation, two diodes in series are recommended.

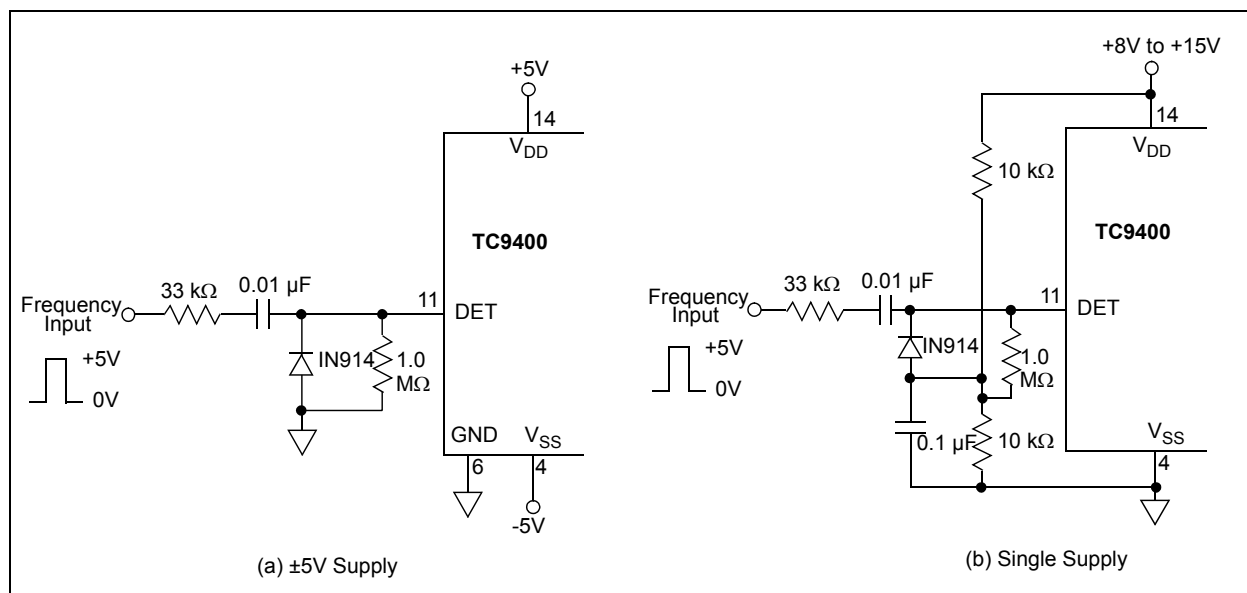


FIGURE 6-1: Frequency Input Level Shifter.

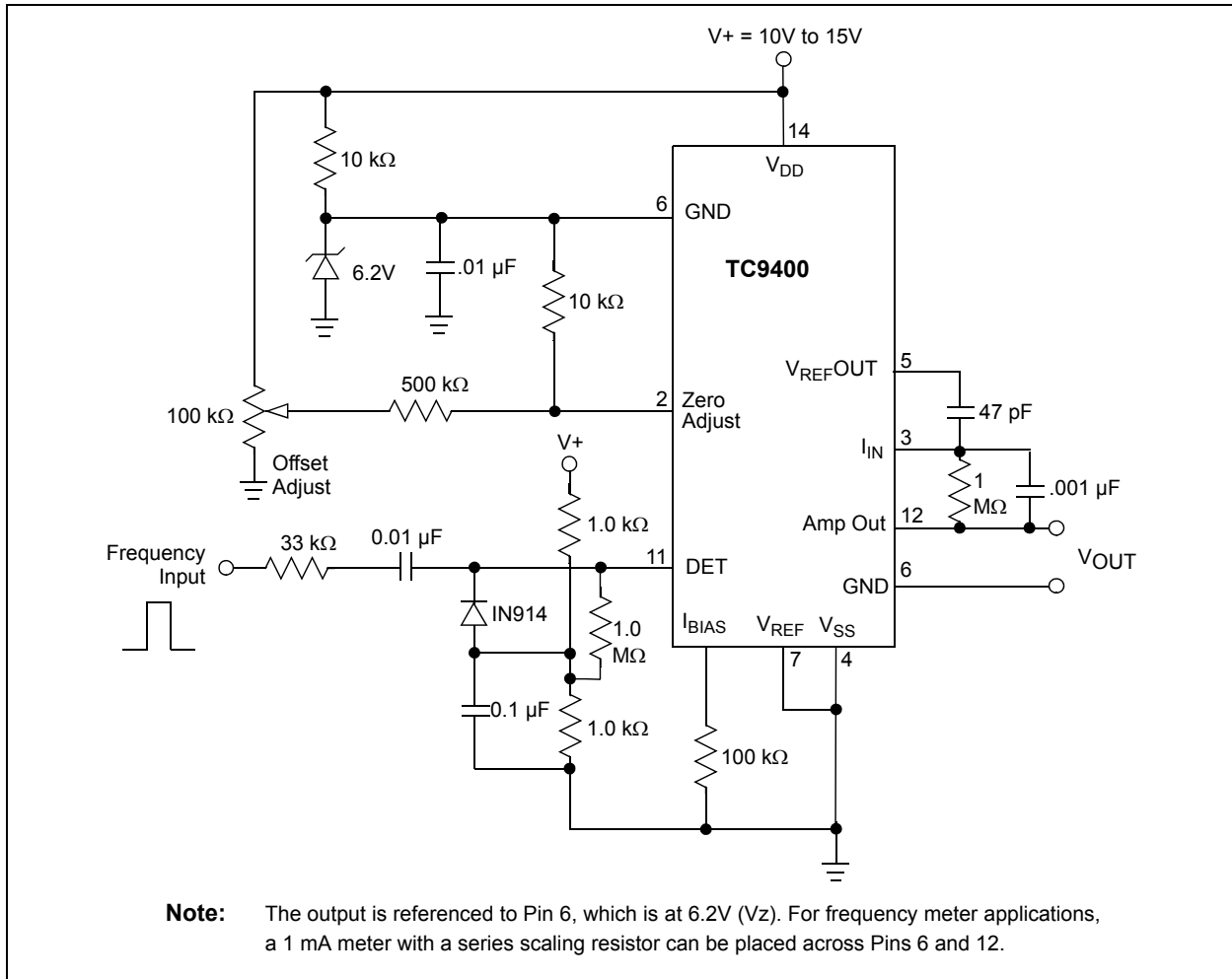


FIGURE 6-2: F/V Single Supply F/V Converter.

6.3 Input Buffer

F_{OUT} and $F_{OUT}/2$ are not used in the F/V mode. However, these outputs may be useful for some applications, such as a buffer to feed additional circuitry. Then, F_{OUT} will follow the input frequency waveform, except that F_{OUT} will go high 3 μs after F_{IN} goes high; $F_{OUT}/2$ will be square wave with a frequency of one-half F_{OUT} .

If these outputs are not used, Pins 8, 9 and 10 should be connected to ground (see Figure 6-3 and Figure 6-4).

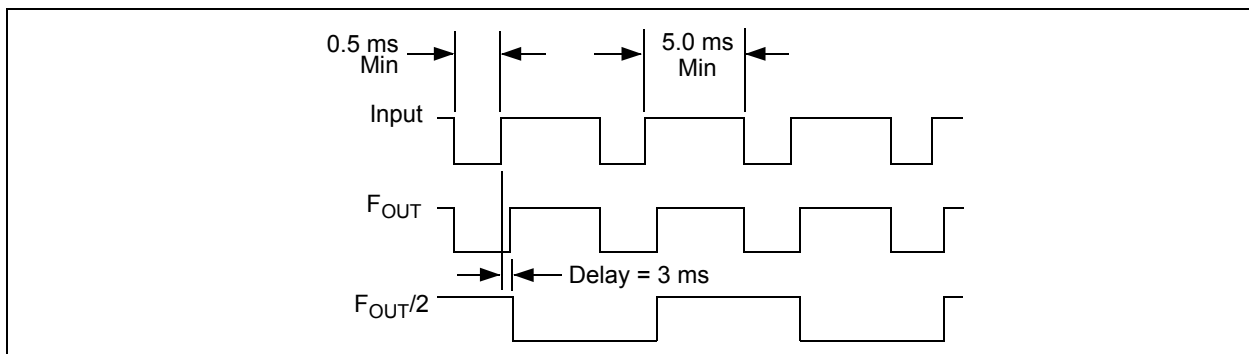
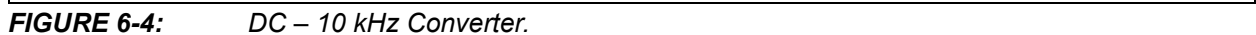


FIGURE 6-3: F/V Digital Outputs.

[illegible]

7.0 F/V POWER-ON RESET

In F/V mode, the TC9400 output voltage will occasionally be at its maximum value when power is first applied. This condition remains until the first pulse is applied to F_{IN} . In most frequency measurement applications, this is not a problem because proper operation begins as soon as the frequency input is applied.

In some cases, however, the TC9400 output must be zero at power-on without a frequency input. In such cases, a capacitor connected from Pin 11 to V_{DD} will usually be sufficient to pulse the TC9400 and provide a Power-on Reset (see Figure 7-1 (a) and (b)). Where predictable power-on operation is critical, a more complicated circuit, such as Figure 7-1 (b), may be required.

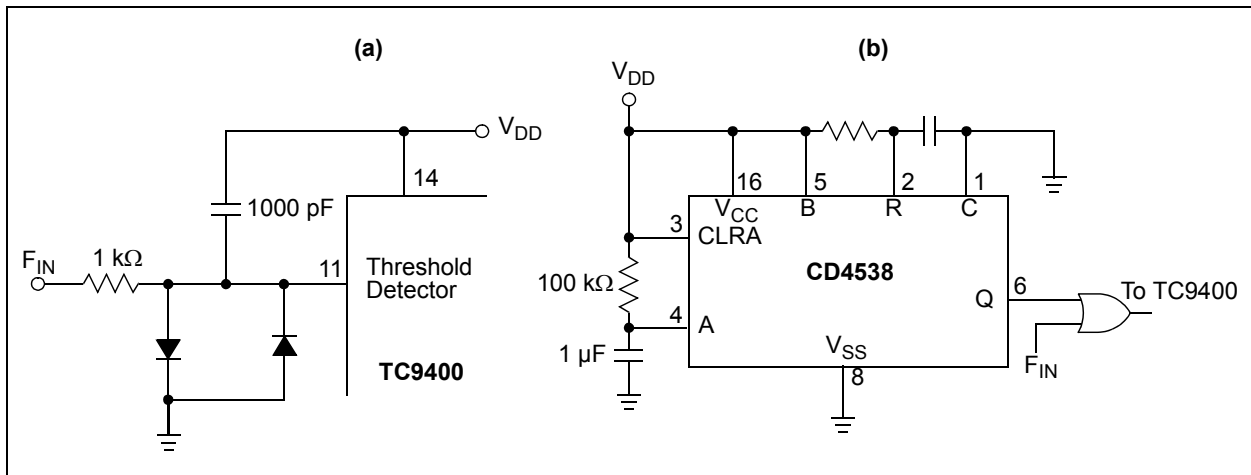
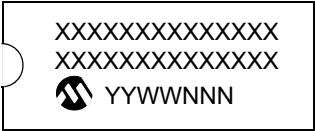


FIGURE 7-1: Power-On Operation/Reset.

8.0 PACKAGE INFORMATION

8.1 Package Marking Information

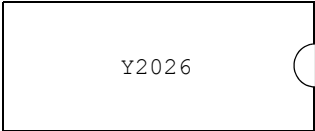
14-Lead CERDIP



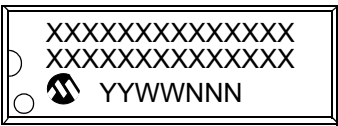
Example: (Front View)



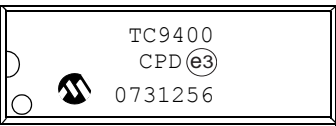
Example: (Back View)



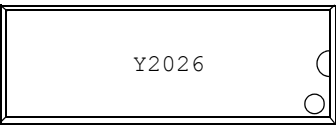
14-Lead PDIP



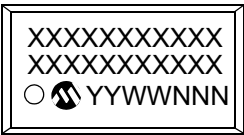
Example: (Front View)



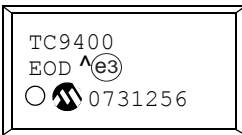
Example: (Back View)



14-Lead SOIC (.150")



Example: (Front View)



Example: (Back View)

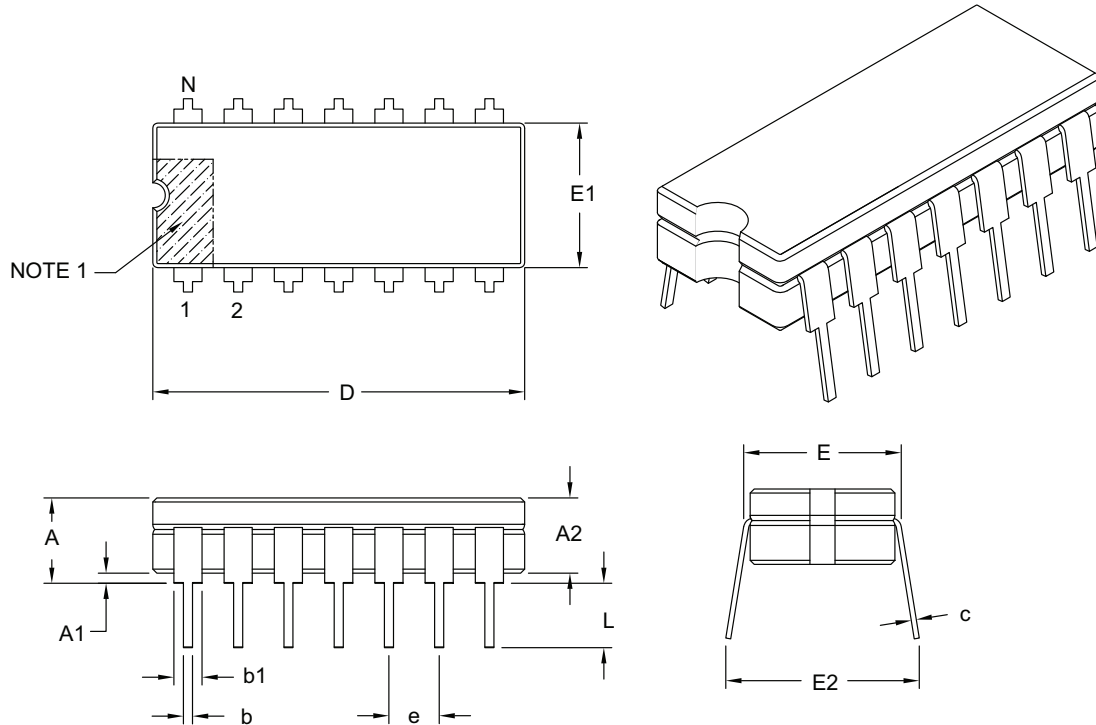


Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

14-Lead Ceramic Dual In-Line (JD) – .300" Body [CERDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Dimension Limits	Units	INCHES		
		MIN	NOM	MAX
Number of Pins	N	14		
Pitch	e	.100 BSC		
Top to Seating Plane	A	–	–	.200
Standoff §	A1	.015	–	–
Ceramic Package Height	A2	.140	–	.175
Shoulder to Shoulder Width	E	.290	–	.325
Ceramic Package Width	E1	.230	.288	.300
Overall Length	D	.740	.760	.780
Tip to Seating Plane	L	.125	–	.200
Lead Thickness	c	.008	–	.015
Upper Lead Width	b1	.045	–	.065
Lower Lead Width	b	.015	–	.023
Overall Row Spacing	E2	.320	–	.410

Notes:

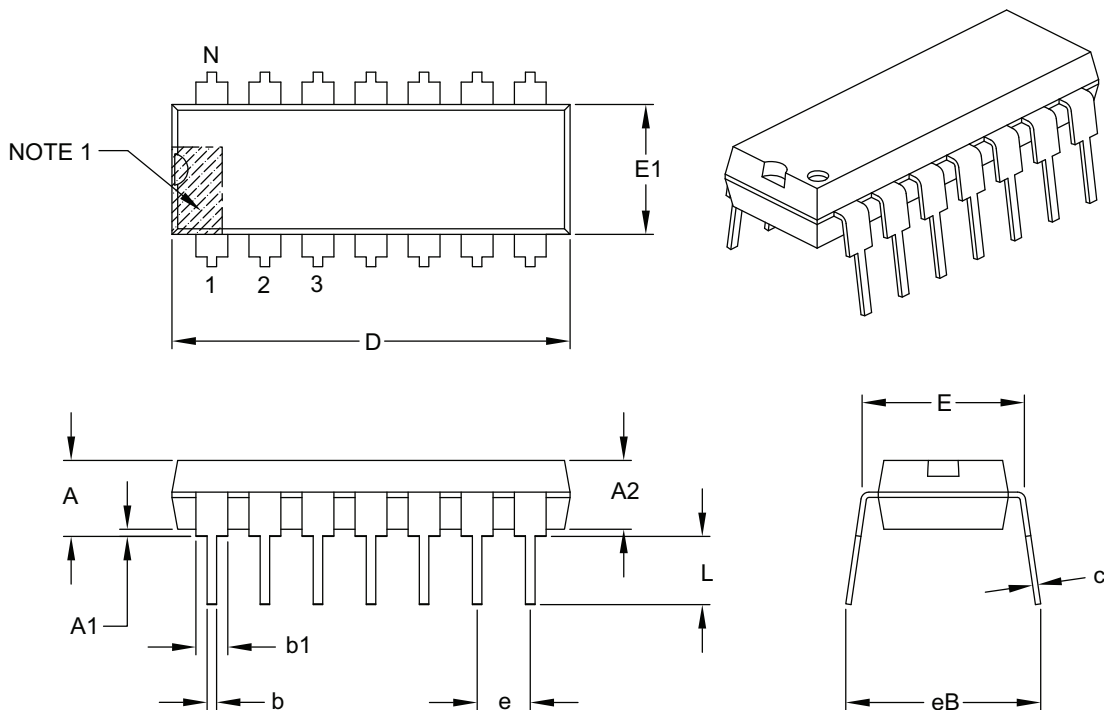
- Pin 1 visual index feature may vary, but must be located within the hatched area.
- § Significant Characteristic.
- Dimensioning and tolerancing per ASME Y14.5M.
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-002B

TC9400/9401/9402

14-Lead Plastic Dual In-Line (PD) – 300 mil Body [PDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Dimension Limits	Units	INCHES		
		MIN	NOM	MAX
Number of Pins	N	14		
Pitch	e	.100 BSC		
Top to Seating Plane	A	–	–	.210
Molded Package Thickness	A2	.115	.130	.195
Base to Seating Plane	A1	.015	–	–
Shoulder to Shoulder Width	E	.290	.310	.325
Molded Package Width	E1	.240	.250	.280
Overall Length	D	.735	.750	.775
Tip to Seating Plane	L	.115	.130	.150
Lead Thickness	c	.008	.010	.015
Upper Lead Width	b1	.045	.060	.070
Lower Lead Width	b	.014	.018	.022
Overall Row Spacing §	eB	–	–	.430

Notes:

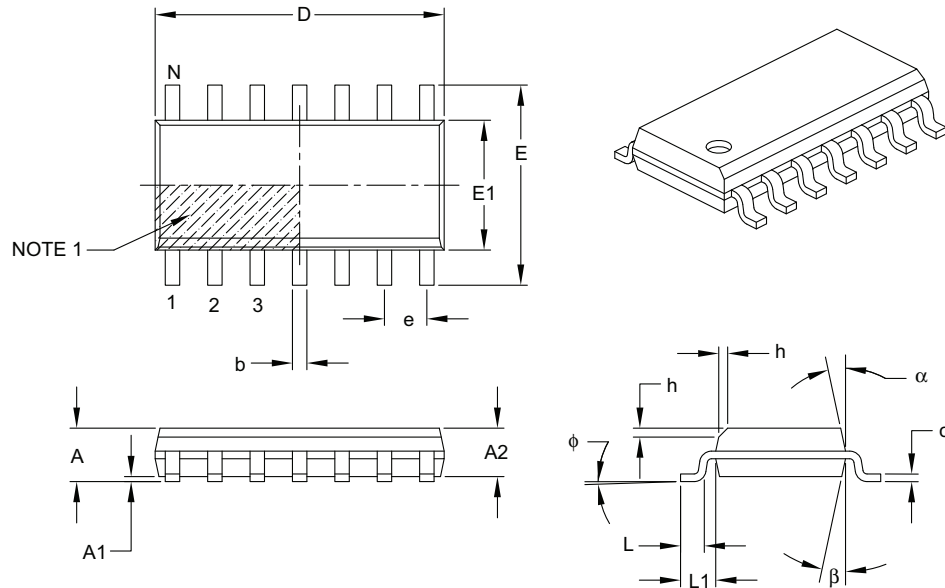
- Pin 1 visual index feature may vary, but must be located with the hatched area.
- § Significant Characteristic.
- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
- Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-005B

14-Lead Plastic Small Outline (OD) – Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	14		
Pitch	e	1.27 BSC		
Overall Height	A	–	–	1.75
Molded Package Thickness	A2	1.25	–	–
Standoff §	A1	0.10	–	0.25
Overall Width	E	6.00 BSC		
Molded Package Width	E1	3.90 BSC		
Overall Length	D	8.65 BSC		
Chamfer (optional)	h	0.25	–	0.50
Foot Length	L	0.40	–	1.27
Footprint	L1	1.04 REF		
Foot Angle	φ	0°	–	8°
Lead Thickness	c	0.17	–	0.25
Lead Width	b	0.31	–	0.51
Mold Draft Angle Top	α	5°	–	15°
Mold Draft Angle Bottom	β	5°	–	15°

Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- § Significant Characteristic.
- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
- Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-065B

TC9400/9401/9402

NOTES:

APPENDIX A: REVISION HISTORY

Revision D (September 2007)

The following is the list of modifications:

1. Corrected Figure 6-1.
2. Added History section.
3. Updated package marking information and package outline drawings
4. Added Product identification System section.

Revision C (May 2006)

Revision B (May 2002)

Revision A (April 2002)

- Original Release of this Document.

TC9400/9401/9402

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.		X	XX
Device	Temperature Range		Package
Device TC9400: Voltage-to-Frequency Converter TC9401: Voltage-to-Frequency Converter TC9402: Voltage-to-Frequency Converter			
Temperature Range E = -40°C to +85°C (Extended) C = 0°C to +70°C (Commercial)			
Package JD = Ceramic Dual-Inline (.300" Body), 14-lead PD = Plastic Dual-Inline (300 mil Body), 14-lead OD = Plastic Small Outline (3.90 MM Body), 14-lead OD713 = Plastic Small Outline (3.90 MM Body), 14-lead Tape and Reel.			
		Examples: a) TC9400COD: 0°C to +70°C, 14LD SOIC package. b) TC9400COD713: 0°C to +70°C, 14LD SOIC package, Tape and Reel c) TC9400CPD: 0°C to +70°C, 14LD PDIP package. d) TC9400EJD: -40°C to +85°C, 14LD PDIP package. a) TC9401CPD: 0°C to +70°C, 14LD PDIP package. b) TC9401EJD: -40°C to +85°C, 14LD Cerdip package. a) TC9402CPD: 0°C to +70°C, 14LD PDIP package. b) TC9402EJD: -40°C to +85°C, 14LD Cerdip package.	

TC9400/9401/9402

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

Information contained in this publication regarding device applications and the like is provided only for your convenience and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. MICROCHIP MAKES NO REPRESENTATIONS OR WARRANTIES OF ANY KIND WHETHER EXPRESS OR IMPLIED, WRITTEN OR ORAL, STATUTORY OR OTHERWISE, RELATED TO THE INFORMATION, INCLUDING BUT NOT LIMITED TO ITS CONDITION, QUALITY, PERFORMANCE, MERCHANTABILITY OR FITNESS FOR PURPOSE. Microchip disclaims all liability arising from this information and its use. Use of Microchip devices in life support and/or safety applications is entirely at the buyer's risk, and the buyer agrees to defend, indemnify and hold harmless Microchip from any and all damages, claims, suits, or expenses resulting from such use. No licenses are conveyed, implicitly or otherwise, under any Microchip intellectual property rights.

Trademarks

The Microchip name and logo, the Microchip logo, Accuron, dsPIC, KEELOQ, KEELOQ logo, microID, MPLAB, PIC, PICmicro, PICSTART, PRO MATE, rPIC and SmartShunt are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.


AmpLab, FilterLab, Linear Active Thermistor, Migratable Memory, MXDEV, MXLAB, SEEVAL, SmartSensor and The Embedded Control Solutions Company are registered trademarks of Microchip Technology Incorporated in the U.S.A.

Analog-for-the-Digital Age, Application Maestro, CodeGuard, dsPICDEM, dsPICDEM.net, dsPICworks, dsSPEAK, ECAN, ECONOMONITOR, FanSense, FlexROM, fuzzyLAB, In-Circuit Serial Programming, ICSP, ICEPIC, Mindi, MiWi, MPASM, MPLAB Certified logo, MPLIB, MPLINK, PICkit, PICDEM, PICDEM.net, PICLAB, PICtail, PowerCal, PowerInfo, PowerMate, PowerTool, REAL ICE, rLAB, Select Mode, Smart Serial, SmartTel, Total Endurance, UNI/O, WiperLock and ZENA are trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

SQTP is a service mark of Microchip Technology Incorporated in the U.S.A.

All other trademarks mentioned herein are property of their respective companies.

© 2007, Microchip Technology Incorporated, Printed in the U.S.A., All Rights Reserved.

 Printed on recycled paper.

QUALITY MANAGEMENT SYSTEM
CERTIFIED BY DNV
== ISO/TS 16949:2002 ==

Microchip received ISO/TS-16949:2002 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona; Gresham, Oregon and design centers in California and India. The Company's quality system processes and procedures are for its PIC® MCUs and dsPIC® DSCs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.



WORLDWIDE SALES AND SERVICE

AMERICAS

Corporate Office

2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7200
Fax: 480-792-7277
Technical Support:
<http://support.microchip.com>
Web Address:
www.microchip.com

Atlanta

Duluth, GA
Tel: 678-957-9614
Fax: 678-957-1455

Boston

Westborough, MA
Tel: 774-760-0087
Fax: 774-760-0088

Chicago

Itasca, IL
Tel: 630-285-0071
Fax: 630-285-0075

Dallas

Addison, TX
Tel: 972-818-7423
Fax: 972-818-2924

Detroit

Farmington Hills, MI
Tel: 248-538-2250
Fax: 248-538-2260

Kokomo

Kokomo, IN
Tel: 765-864-8360
Fax: 765-864-8387

Los Angeles

Mission Viejo, CA
Tel: 949-462-9523
Fax: 949-462-9608

Santa Clara

Santa Clara, CA
Tel: 408-961-6444
Fax: 408-961-6445

Toronto

Mississauga, Ontario,
Canada
Tel: 905-673-0699
Fax: 905-673-6509

ASIA/PACIFIC

Asia Pacific Office

Suites 3707-14, 37th Floor
Tower 6, The Gateway
Harbour City, Kowloon
Hong Kong
Tel: 852-2401-1200
Fax: 852-2401-3431

Australia - Sydney

Tel: 61-2-9868-6733
Fax: 61-2-9868-6755

China - Beijing

Tel: 86-10-8528-2100
Fax: 86-10-8528-2104

China - Chengdu

Tel: 86-28-8665-5511
Fax: 86-28-8665-7889

China - Fuzhou

Tel: 86-591-8750-3506
Fax: 86-591-8750-3521

China - Hong Kong SAR

Tel: 852-2401-1200
Fax: 852-2401-3431

China - Qingdao

Tel: 86-532-8502-7355
Fax: 86-532-8502-7205

China - Shanghai

Tel: 86-21-5407-5533
Fax: 86-21-5407-5066

China - Shenyang

Tel: 86-24-2334-2829
Fax: 86-24-2334-2393

China - Shenzhen

Tel: 86-755-8203-2660
Fax: 86-755-8203-1760

China - Shunde

Tel: 86-757-2839-5507
Fax: 86-757-2839-5571

China - Wuhan

Tel: 86-27-5980-5300
Fax: 86-27-5980-5118

China - Xian

Tel: 86-29-8833-7252
Fax: 86-29-8833-7256

ASIA/PACIFIC

India - Bangalore

Tel: 91-80-4182-8400
Fax: 91-80-4182-8422

India - New Delhi

Tel: 91-11-4160-8631
Fax: 91-11-4160-8632

India - Pune

Tel: 91-20-2566-1512
Fax: 91-20-2566-1513

Japan - Yokohama

Tel: 81-45-471- 6166
Fax: 81-45-471-6122

Korea - Daegu

Tel: 82-53-744-4301
Fax: 82-53-744-4302

Korea - Seoul

Tel: 82-2-554-7200
Fax: 82-2-558-5932 or
82-2-558-5934

Malaysia - Penang

Tel: 60-4-646-8870
Fax: 60-4-646-5086

Philippines - Manila

Tel: 63-2-634-9065
Fax: 63-2-634-9069

Singapore

Tel: 65-6334-8870
Fax: 65-6334-8850

Taiwan - Hsin Chu

Tel: 886-3-572-9526
Fax: 886-3-572-6459

Taiwan - Kaohsiung

Tel: 886-7-536-4818
Fax: 886-7-536-4803

Taiwan - Taipei

Tel: 886-2-2500-6610
Fax: 886-2-2508-0102

Thailand - Bangkok

Tel: 66-2-694-1351
Fax: 66-2-694-1350

EUROPE

Austria - Wels

Tel: 43-7242-2244-39
Fax: 43-7242-2244-393

Denmark - Copenhagen

Tel: 45-4450-2828
Fax: 45-4485-2829

France - Paris

Tel: 33-1-69-53-63-20
Fax: 33-1-69-30-90-79

Germany - Munich

Tel: 49-89-627-144-0
Fax: 49-89-627-144-44

Italy - Milan

Tel: 39-0331-742611
Fax: 39-0331-466781

Netherlands - Drunen

Tel: 31-416-690399
Fax: 31-416-690340

Spain - Madrid

Tel: 34-91-708-08-90
Fax: 34-91-708-08-91

UK - Wokingham

Tel: 44-118-921-5869
Fax: 44-118-921-5820

06/25/07