

Ordering Information

Part Number	Package Option	Packing
TC6320K6-G	8-Lead DFN (4x4)	3000/Reel
TC6320TG-G	8-Lead SOIC	2000/Reel

-G indicates package is RoHS compliant ('Green')



Absolute Maximum Ratings

Parameter	Value
DRAIN-to-SOURCE voltage	BV_{DSS}
DRAIN-to-GATE voltage	BV_{DGS}
Operating and storage temperature	-55°C to +150°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

Typical Thermal Resistance

Package	θ_{ja}
8-Lead DFN	44°C/W
8-Lead SOIC	101°C/W

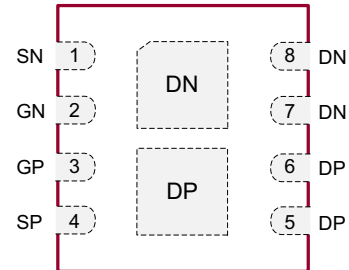
Note:

1.0oz, 4-layer, 3"x4" PCB

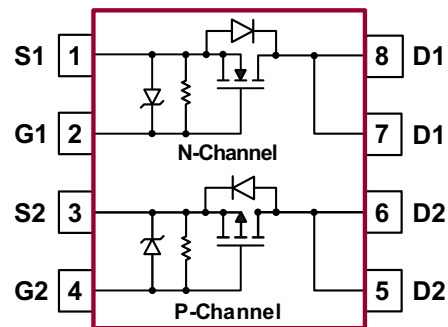
Product Summary

BV_{DSS}/BV_{DGS} (V)		$R_{DS(ON)}$ (max) (Ω)	
N-Channel	P-Channel	N-Channel	P-Channel
200	-200	7.0	8.0

Pin Configurations



8-Lead DFN
(top view)



8-Lead SOIC
(top view)

Package Marking



Y = Last Digit of Year Sealed
W = Code for Week Sealed
L = Lot Number
— = "Green" Packaging

Package may or may not include the following marks: Si or

8-Lead DFN



YY = Year Sealed
WW = Week Sealed
L = Lot Number
— = "Green" Packaging

Package may or may not include the following marks: Si or

8-Lead SOIC

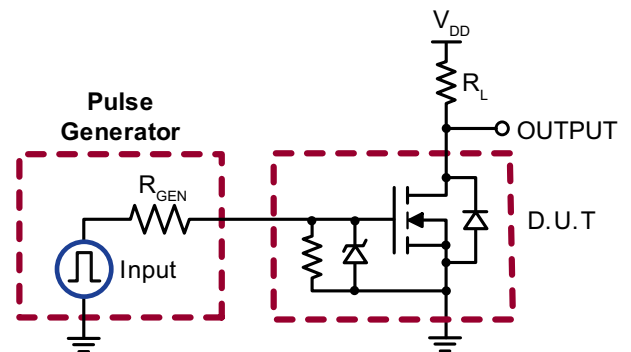
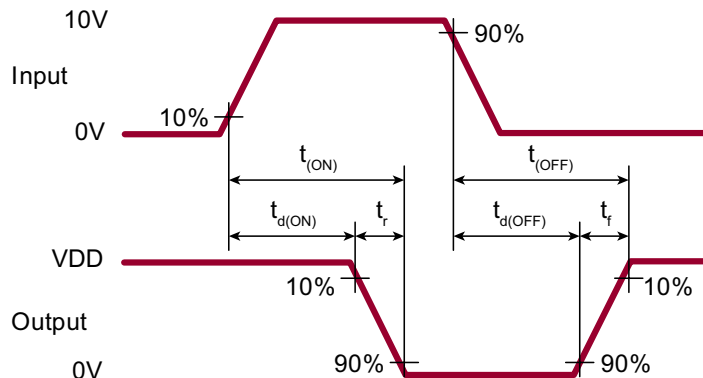
N-Channel Electrical Characteristics ($T_C = 25^\circ\text{C}$ unless otherwise specified)

Sym	Parameter	Min	Typ	Max	Units	Conditions
BV_{DSS}	DRAIN-to-SOURCE breakdown voltage	200	-	-	V	$V_{GS} = 0V, I_D = 2.0mA$
$V_{GS(th)}$	GATE threshold voltage	1.0	-	2.0	V	$V_{GS} = V_{DS}, I_D = 1.0mA$
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with temperature	-	-	-4.5	mV/ $^\circ\text{C}$	$V_{GS} = V_{DS}, I_D = 1.0mA$
R_{GS}	GATE-to-SOURCE shunt resistor	10	-	50	k Ω	$I_{GS} = 100\mu A$
VZ_{GS}	GATE-to-SOURCE Zener voltage	13.2	-	25	V	$I_{GS} = 2.0mA$
I_{DSS}	Zero GATE voltage DRAIN current	-	-	10.0	μA	$V_{DS} = \text{Max rating}, V_{GS} = 0V$
		-	-	1.0	mA	$V_{DS} = 0.8 \text{ Max Rating}, V_{GS} = 0V, T_A = 125^\circ\text{C}$
$I_{D(ON)}$	On-state DRAIN current	1.0	-	-	A	$V_{GS} = 4.5V, V_{DS} = 25V$
		2.0	-	-		$V_{GS} = 10V, V_{DS} = 25V$
$R_{DS(ON)}$	Static DRAIN-to-SOURCE on-state resistance	-	-	8.0	Ω	$V_{GS} = 4.5V, I_D = 150mA$
		-	-	7.0		$V_{GS} = 10V, I_D = 1.0A$
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with temperature	-	-	1.0	%/ $^\circ\text{C}$	$V_{GS} = 4.5V, I_D = 150mA$
G_{FS}	Forward transconductance	400	-	-	mmho	$V_{DS} = 25V, I_D = 500mA$
C_{ISS}	Input capacitance	-	-	110	pF	$V_{GS} = 0V,$ $V_{DS} = 25V,$ $f = 1.0MHz$
C_{OSS}	Common SOURCE output capacitance	-	-	60		
C_{RSS}	Reverse transfer capacitance	-	-	23		
$t_{d(ON)}$	Turn-on delay time	-	-	10	ns	$V_{DD} = 25V,$ $I_D = 1.0A,$ $R_{GEN} = 25\Omega$
t_r	Rise time	-	-	15		
$t_{d(OFF)}$	Turn-off delay time	-	-	20		
t_f	Fall time	-	-	15		
V_{SD}	Diode forward voltage drop	-	-	1.8	V	$V_{GS} = 0V, I_{SD} = 500mA$
t_{rr}	Reverse recovery time	-	300	-	ns	$V_{GS} = 0V, I_{SD} = 500mA$

Notes:

1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300 μs pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.

N-Channel Switching Waveforms and Test Circuit



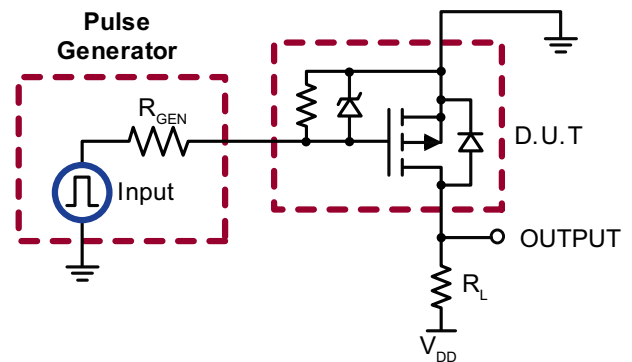
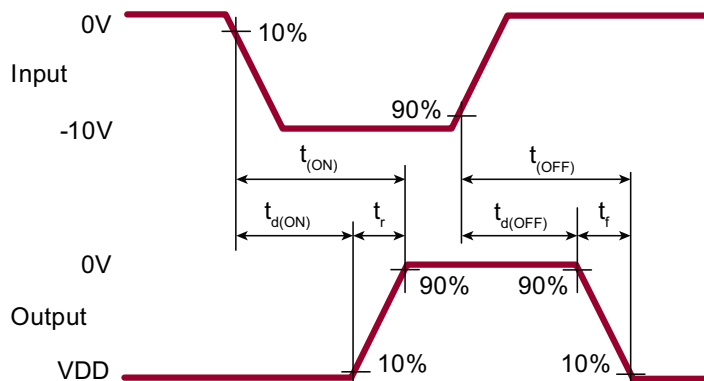
P-Channel Electrical Characteristics ($T_c = 25^\circ\text{C}$ unless otherwise specified)

Sym	Parameter	Min	Typ	Max	Units	Conditions
BV_{DSS}	DRAIN-to-SOURCE breakdown voltage	-200	-	-	V	$V_{GS} = 0V, I_D = -2.0mA$
$V_{GS(th)}$	GATE threshold voltage	-1.0	-	-2.4	V	$V_{GS} = V_{DS}, I_D = -1.0mA$
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with temperature	-	-	4.5	mV/ $^\circ\text{C}$	$V_{GS} = V_{DS}, I_D = -1.0mA$
R_{GS}	GATE-to-SOURCE shunt resistor	10	-	50	k Ω	$I_{GS} = 100\mu A$
VZ_{GS}	GATE-to-SOURCE Zener voltage	13.2	-	25	V	$I_{GS} = -2mA$
I_{DSS}	Zero GATE voltage DRAIN current	-	-	-10	μA	$V_{DS} = \text{Max rating}, V_{GS} = 0V$
		-	-	-1.0	mA	$V_{DS} = 0.8 \text{ Max Rating}, V_{GS} = 0V, T_A = 125^\circ\text{C}$
$I_{D(ON)}$	On-state DRAIN current	-1.0	-	-	A	$V_{GS} = -4.5V, V_{DS} = -25V$
		-2.0	-	-		$V_{GS} = -10V, V_{DS} = -25V$
$R_{DS(ON)}$	Static DRAIN-to-SOURCE on-state resistance	-	-	10	Ω	$V_{GS} = -4.5V, I_D = -150mA$
		-	-	8.0		$V_{GS} = -10V, I_D = -1.0A$
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with temperature	-	-	1.0	%/ $^\circ\text{C}$	$V_{GS} = -10V, I_D = -200mA$
G_{FS}	Forward transconductance	400	-	-	mmho	$V_{DS} = -25V, I_D = -500mA$
C_{ISS}	Input capacitance	-	-	200	pF	$V_{GS} = 0V,$ $V_{DS} = -25V,$ $f = 1.0MHz$
C_{OSS}	Common SOURCE output capacitance	-	-	55		
C_{RSS}	Reverse transfer capacitance	-	-	30		
$t_{d(ON)}$	Turn-on delay time	-	-	10	ns	$V_{DD} = -25V,$ $I_D = -1.0A,$ $R_{GEN} = 25\Omega$
t_r	Rise time	-	-	15		
$t_{d(OFF)}$	Turn-off delay time	-	-	20		
t_f	Fall time	-	-	15		
V_{SD}	Diode forward voltage drop	-	-	-1.8	V	$V_{GS} = 0V, I_{SD} = -500mA$
t_{rr}	Reverse recovery time	-	300	-	ns	$V_{GS} = 0V, I_{SD} = -500mA$

Notes:

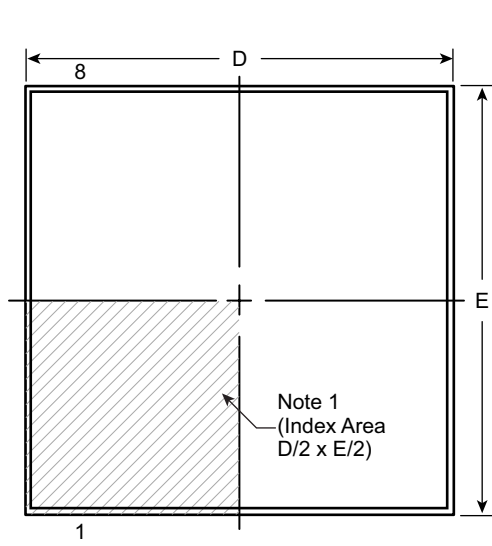
1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: $300\mu s$ pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.

P-Channel Switching Waveforms and Test Circuit

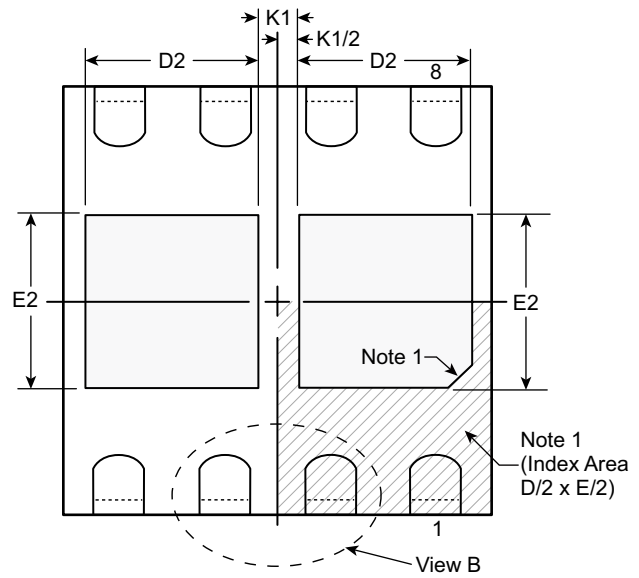


8-Lead DFN Package Outline (K6)

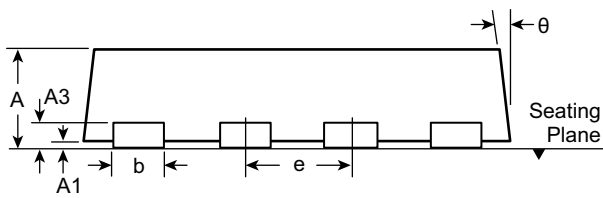
4.00x4.00mm body, 1.00mm height (max), 1.00mm pitch (dual pad)



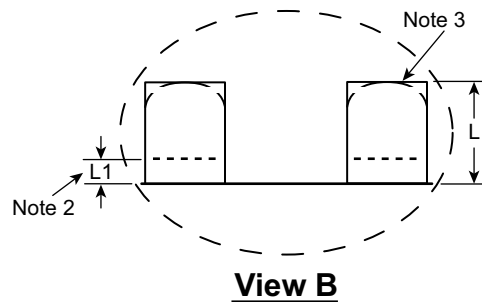
Top View



Bottom View



Side View



View B

Notes:

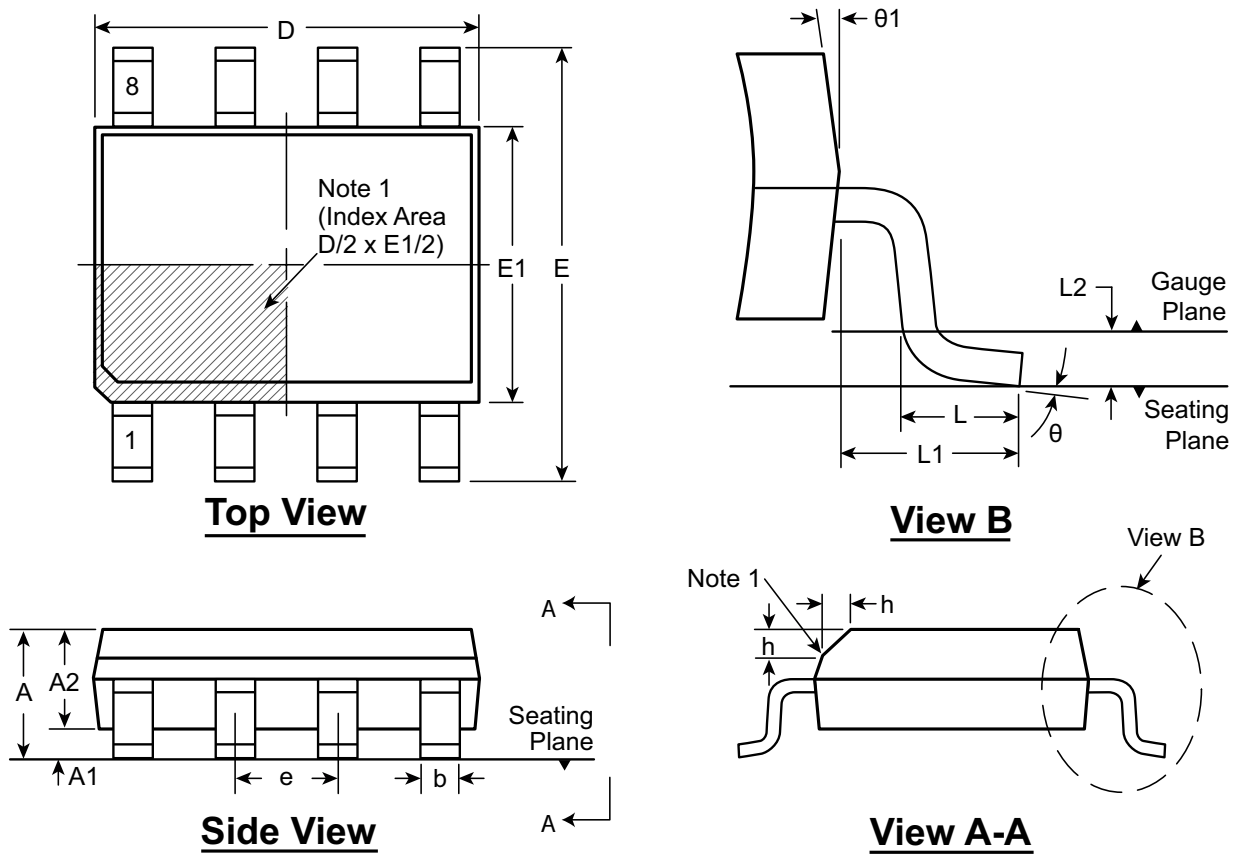
1. A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.
2. Depending on the method of manufacturing, a maximum of 0.15mm pullback (L1) may be present.
3. The inner tip of the lead may be either rounded or square.

Symbol		A	A1	A3	b	D	D2	E	E2	e	K1	L	L1	θ
Dimension (mm)	MIN	0.80	0.00	0.20 REF	0.25	3.90	1.35	3.90	1.35	1.00 BSC	0.50 REF	0.40	0.00	0°
	NOM	0.90	-		0.30	4.00	1.45	4.00	1.45			0.50	-	-
	MAX	1.00	0.05		0.35	4.10	1.55	4.10	1.55			0.60	0.15	14°

Drawings not to scale

Supertex Doc. #: DSPD-8DFNK64x4P100, Version C010813

8-Lead SOIC (Narrow Body) Package Outline (TG)
4.90x3.90mm body, 1.75mm height (max), 1.27mm pitch



Note:
1. This chamfer feature is optional. A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.

Symbol		A	A1	A2	b	D	E	E1	e	h	L	L1	L2	θ	θ1
Dimension (mm)	MIN	1.35*	0.10	1.25	0.31	4.80*	5.80*	3.80*	1.27 BSC	0.25	0.40	1.04 REF	0.25 BSC	0°	5°
	NOM	-	-	-	-	4.90	6.00	3.90		-	-			-	-
	MAX	1.75	0.25	1.65*	0.51	5.00*	6.20*	4.00*		0.50	1.27			8°	15°

JEDEC Registration MS-012, Variation AA, Issue E, Sept. 2005.
* This dimension is not specified in the JEDEC drawing.
Drawings are not to scale.
Supertex Doc. #: DSPD-8SOLGTG, Version I041309.

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to <http://www.supertex.com/packaging.html>.)

Supertex inc. does not recommend the use of its products in life support applications, and will not knowingly sell them for use in such applications unless it receives an adequate "product liability indemnification insurance agreement." **Supertex inc.** does not assume responsibility for use of devices described, and limits its liability to the replacement of the devices determined defective due to workmanship. No responsibility is assumed for possible omissions and inaccuracies. Circuitry and specifications are subject to change without notice. For the latest product specifications refer to the **Supertex inc.** (website: <http://www.supertex.com>)