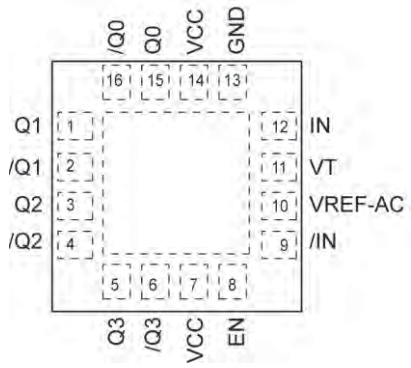
Ordering Information[1]

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY89833ALMG[2]	QFN-16	Industrial	833A with Pb-Free bar-line indicator	NiPdAu Pb-Free
SY89833ALMGTR[1 2]	QFN-16	Industrial	833A with Pb-Free bar-line indicator	NiPdAu Pb-Free

Notes:

1. Tape and Reel.
2. Pb-Free package is recommended for new designs.

Pin Configuration



16-Pin

Truth Table

IN	/IN	EN	Q	/Q
0	1	1	0	1
1	0	1	1	0
X	X	0	0[1]	1[1]

Note:

1. On next negative transition of the input signal (IN).

Pin Description

Pin Number	Pin Name	Pin Function
15, 16 1, 2 3, 4 5, 6	Q0, /Q0 Q1, /Q1 Q2, /Q2 Q3, /Q3	LVDS Differential Outputs: Normally terminated with 100Ω across the pair (Q, /Q). See “LVDS Outputs” section, Figure 2a. Unused outputs should be terminated with a 100Ω resistor across each pair.
8	EN	This single-ended TTL/CMOS-compatible input functions as a synchronous output enable. The synchronous enable ensures that enable/disable will only occur when the outputs are in a logic LOW state. Note that this input is internally connected to a 25kΩ pull-up resistor and will default to logic HIGH state (enabled) if left open.
9, 12	/IN, IN	Differential Input: This input pair is the differential signal input to the device. Input accepts AC- or DC-Coupled differential signals as small as 100mV. Each pin of the pair internally terminates to a VT pin through 50Ω. Note that this input will default to an intermediate state if left open. Please refer to the “Input Interface Applications” section for more details.
10	VREF-AC	Reference Voltage: This output biases to V_{CC}–1.4V. It is used when AC-Coupling the input (IN, /IN). For AC-Coupled applications, connect VREF-AC to VT pin and bypass with 0.1µF low ESR capacitor to V_{CC}. See “Input Interface Applications” section for more details. Maximum sink/source current is ±1.5mA. Due to the limited drive capability, each VREF-AC pin is only intended to drive its respective VT pin.
11	VT	Input Termination Center-Tap: Each side of the differential input pair terminates to the VT pin. The VT pin provides a center-tap to a termination network for maximum interface flexibility. See “Input Interface Applications” section for more details.
13	GND	Ground. GND pin and exposed pad must be connected to the most negative potential of the device ground.
7, 14	VCC	Positive Power Supply: Bypass with 0.1µF//0.01µF low ESR capacitors and place as close to each VCC pin as possible.

Absolute Maximum Ratings[1]

Supply Voltage (V_{CC}) ..... –0.5V to +4.0V
Input Voltage (V_{IN}) ..... –0.5V to V_{CC} +0.3V
LVDS Output Current (I_{OUT}) ..... ±10mA
Input Current
  Source or Sink Current on (IN, /IN) ..... ±50mA
V_T Current
  Source or Sink Current on (V_T) ..... ±100mA
V_{REF-AC} Current
  Source or Sink Current on (V_{REF-AC}) ..... ±2mA
Maximum Operating Junction Temperature ..... 125°C
Lead Temperature (soldering, 20sec.) ..... 260°C
Storage Temperature (T_s) ..... –65°C to +150°C

Operating Ratings[2]

Supply Voltage (V_{CC}) ..... +3.0V to +3.60V
Ambient Temperature (T_A) ..... –40°C to +85°C
Junction Thermal Resistance [3]
  QFN (θ_{JA})
    Still-Air ..... 75°C/W
  QFN (ψ_{JB}) ..... 33°C/W

Electrical Characteristics[4]

T_A = –40°C to +85°C, unless otherwise noted.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{CC}	Power Supply Voltage Range		3.0	3.3	3.6	V
I_{CC}	Power Supply Current	No load, max. V_{CC}.		75	100	mA
R_{IN}	Input Resistance (IN-to-VT)		45	50	55	Ω
$R_{DIFF-IN}$	Differential Input Resistance (IN-to-/IN)		90	100	110	Ω
V_{IH}	Input HIGH Voltage (IN-to-/IN)		1.2		V_{CC}	V
V_{IL}	Input LOW Voltage (IN-to-/IN)		0		V_{IH}–0.1	V
V_{IN}	Input Voltage Swing (IN-to-/IN)	See Figure 2c.	0.1		1.7	V
V_{DIFF_IN}	Differential Input Voltage	See Figure 2d.	0.2			V
|IIN|	Input Current (IN, /IN)	Note 5			45	mA
V_{REF-AC}	Reference Voltage		V_{CC}–1.525	V_{CC}–1.425	V_{CC}–1.325	V

Notes:

1. Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
3. Package thermal resistance assumes exposed pad is soldered (or equivalent) to the device's most negative potential on the PCB. ψ_{JB} and θ_{JA} values are determined for a 4-layer board in still-air number, unless otherwise stated.
4. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.
5. Due to the internal termination (see "Input Stage" section) the input current depends on the applied voltages at IN, /IN and VT inputs. Do not apply a combination of voltages that causes the input current to exceed the maximum limit!

LVDS Outputs DC Electrical Characteristics[6]

V_{CC} = 3.3V ±10%, R_L = 100Ω across the output, T_A = –40°C to +85°C, unless otherwise noted.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{OUT}	Output Voltage Swing	See Figure 2c.	250	325		mV
V_{DIFF_OUT}	Differential Output Voltage Swing	See Figure 2d.	500	650		mV
V_{OCM}	Output Common Mode Voltage		1.125		1.275	V
ΔV_{OCM}	Change in Common Mode Voltage		–50		50	mV

LVTTL/CMOS DC Electrical Characteristics[6]

V_{CC} = 3.3V ±10%, T_A = –40°C to +85°C, unless otherwise noted.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IH}	Input HIGH Voltage		2.0		V_{CC}	V
V_{IL}	Input LOW Voltage		0		0.8	V
I_{IH}	Input HIGH Current		–125		30	µA
I_{IL}	Input LOW Current		–300			µA

Notes:

6. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

AC Electrical Characteristics[7]

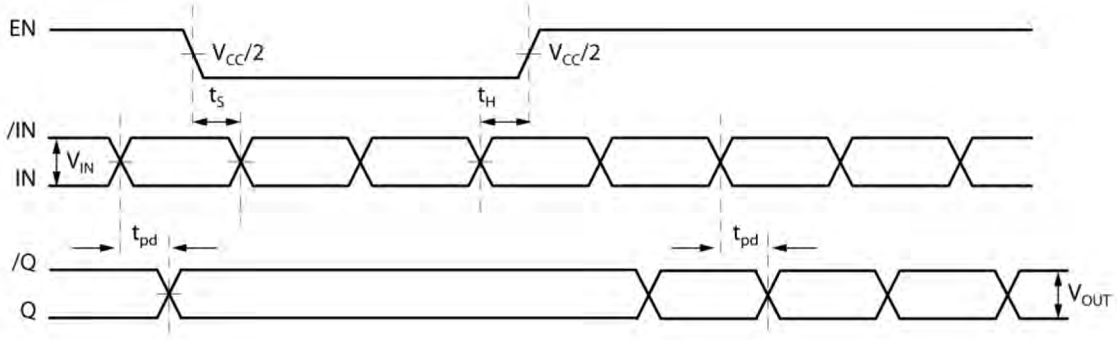
V_{CC} = 3.3V ±10%, R_L = 100Ω across the output, T_A = –40°C to +85°C, unless otherwise noted.

Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{MAX}	Maximum Frequency	V_{OUT} ≥ 200mV	2.0			GHz
t_{PD}	Propagation Delay		250		470	ps
t_{SKEW}	Within-Device Skew	Note 8		5	20	ps
	Part-to-Part Skew	Note 9			200	ps
t_S	Set-Up Time	Note 10	400			ps
t_H	Hold Time	Note 10	400			ps
t_{jitter}	RMS Phase Jitter	Output = 622MHz Integration Range 12kHz – 20MHz		125		fs
t_r, t_f	Output Rise/Fall Times (20% to 80%)	At full output swing.	60	110	190	ps
	Duty Cycle	Differential I/O	47		53	%

Notes:

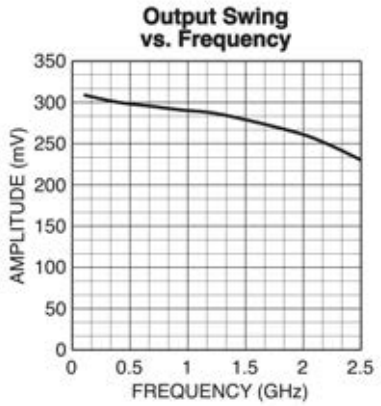
7. High-frequency AC parameters are guaranteed by design and characterization.
8. Within device skew is measured between two different outputs under identical input transitions.
9. Part-to-part skew is defined for two parts with identical power supply voltages at the same temperature and no skew at the edges at the respective inputs.
10. Set-up and hold times apply to synchronous applications that intend to enable/disable before the next clock cycle. For asynchronous applications, set-up and hold times do not apply.

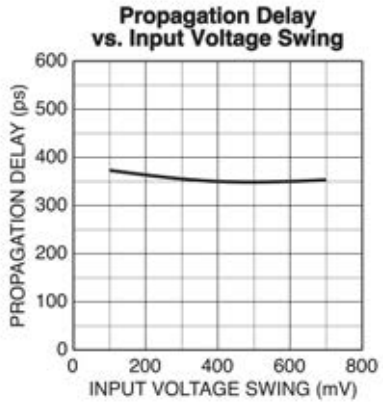
Timing Diagrams



Typical Characteristics

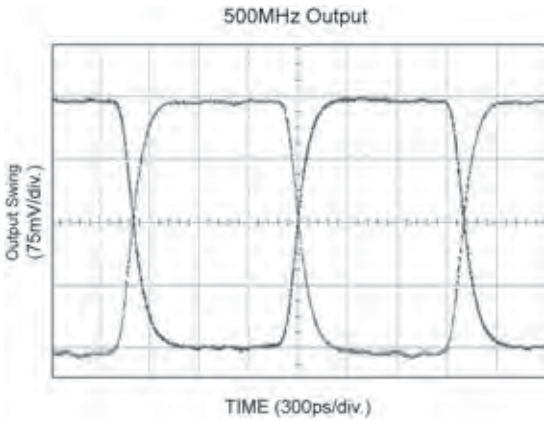
V_{CC} = 3.3V, GND = 0V, V_{IN} = 400mV, R_L = 100Ω across the outputs, T_A = 25ºC, unless otherwise stated.

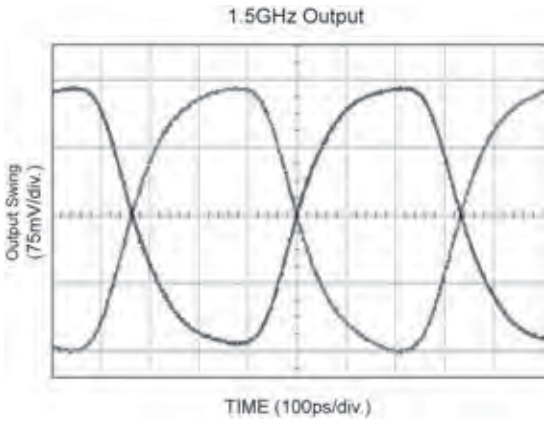


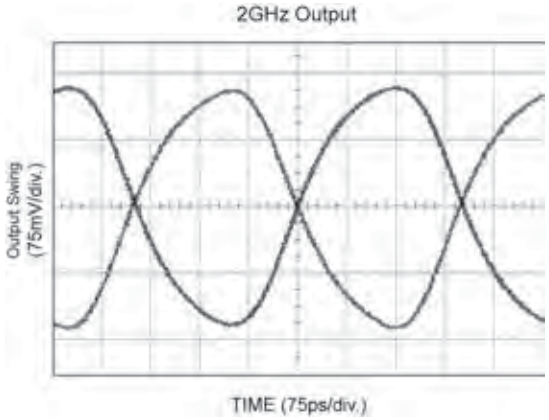


Functional Characteristics

V_{CC} = 3.3V, GND = 0V, V_{IN} = 400mV, R_L = 100Ω across the outputs, T_A = 25ºC, unless otherwise stated.







Input Stage

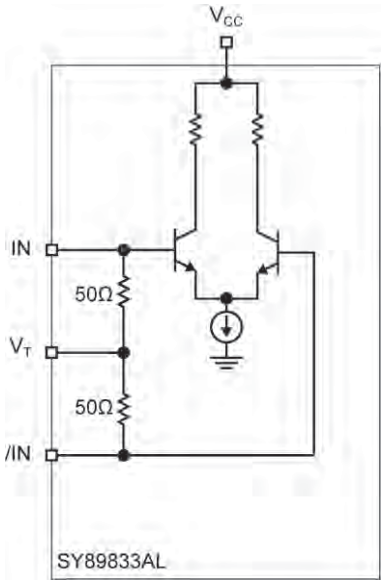


Figure 1. Simplified Differential Input Buffer

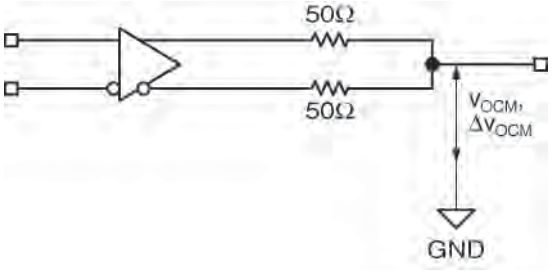


Figure 2b. LVDS Common Mode Measurement

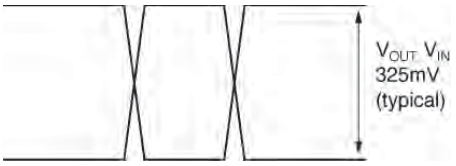


Figure 2c. Single-Ended Swing

LVDS Outputs

LVDS specifies a small swing of 325mV typical, on a nominal 1.20V common mode above ground. The common mode voltage has tight limits to permit large variations in ground noise between an LVDS driver and receiver.

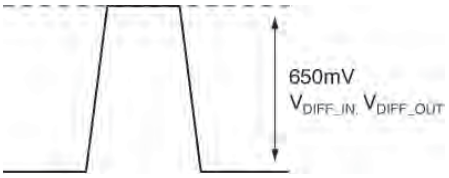


Figure 2d. Differential Swing

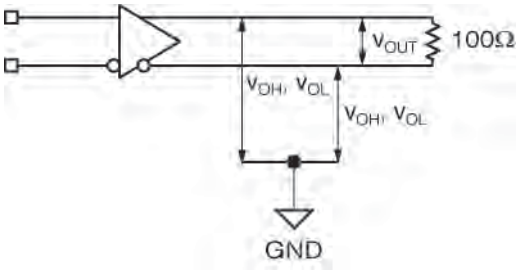


Figure 2a. LVDS Differential Measurement

Input Interface Applications

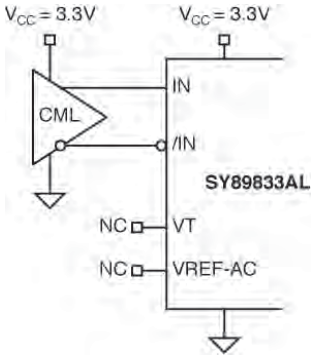


Figure 3a. DC-Coupled CML Input Interface
Option: May connect V_T to V_{CC}

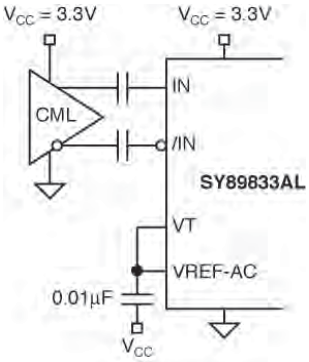


Figure 3b. AC-Coupled CML Input Interface

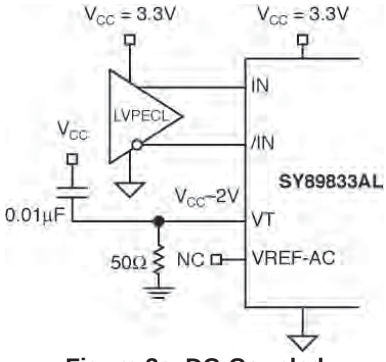


Figure 3c. DC-Coupled LVPECL Input Interface

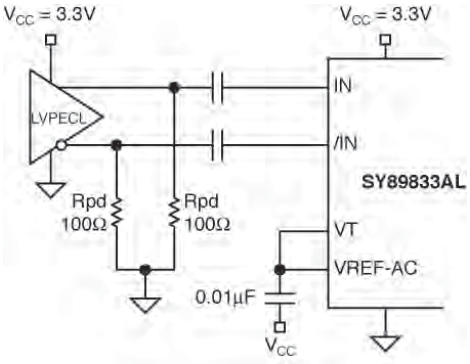


Figure 3d. AC-Coupled LVPECL Input Interface

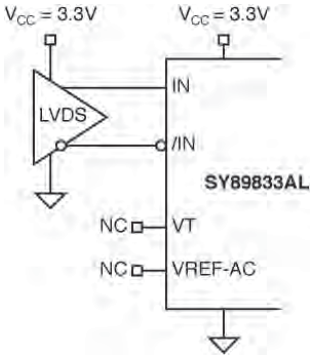
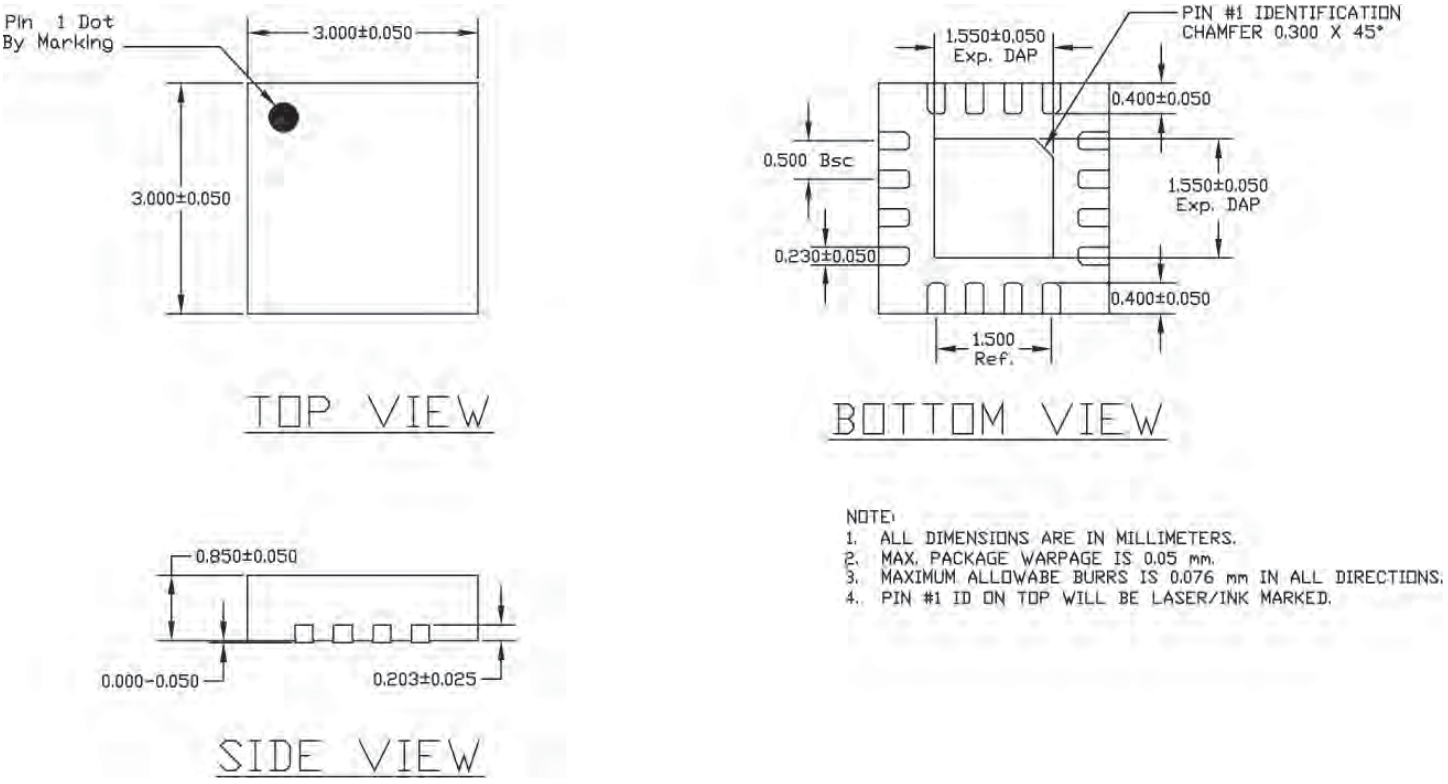


Figure 3e. LVDS Input Interface

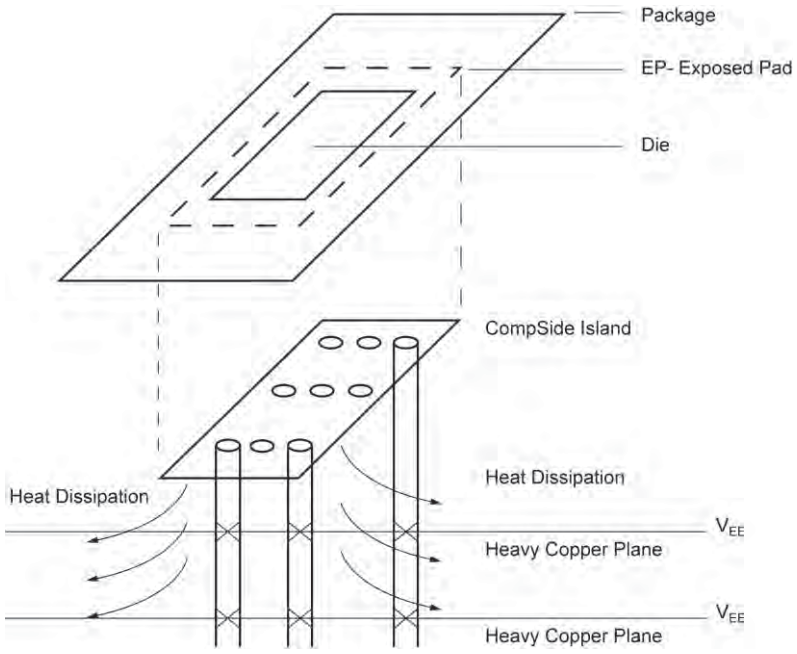
Related Product and Support Documentation

Part Number	Function	Datasheet Link
SY89830U	2.5V/3.3V/5V 2.5GHz 1:4 PECL/ECL Clock Driver with 2:1 Differential Input MUX	http://www.micrel.com/product-info/products/sy89830u.shtml
SY89831U	Ultra-Precision 1:4 LVPECL Fanout Buffer/Translator with Internal Termination	http://www.micrel.com/product-info/products/sy89831u.shtml
SY89832U	2.5V Ultra-Precision 1:4 LVDS Fanout Buffer/Translator with Internal Termination	http://www.micrel.com/product-info/products/sy89832u.shtml
SY89834U	2.5/3.3V Two Input, 1GHz LVTTL/CMOS-to-LVPECL 1:4 Fanout Buffer/Translator	http://www.micrel.com/product-info/products/sy89834u.shtml
SY89833L	3.3V Ultra-Precision 1:4 LVDS Fanout Buffer/Translator with Internal Termination	http://www.micrel.com/page.do?page=/product-info/products/sy89833l.shtml
HBW Solutions	New Products and Termination App. Note	http://www.micrel.com/product-info/as/solutions.shtml

Package Information



16-Pin QFN



PCB Thermal Consideration for 16-Pin QFN Package
(Always solder, or equivalent, the exposed pad to the PCB)

Package Notes:

1. Package meets Level 2 moisture sensitivity classification, and are shipped in dry-pack form.
2. Exposed pads must be soldered to a ground for proper thermal management.

MICREL, INC. 2180 FORTUNE DRIVE SAN JOSE, CA 95131 USA
TEL +1 (408) 944-0800 FAX +1 (408) 474-1000 WEB http://www.micrel.com