1. Ordering Guide

Industrial and Automotive Grade OPNs

Industrial-grade devices (part numbers having an “-I” in their suffix) are built using well-controlled, high-quality manufacturing flows to ensure robustness and reliability. Qualifications are compliant with JEDEC, and defect reduction methodologies are used throughout definition, design, evaluation, qualification, and mass production steps.

Automotive-grade devices (part numbers having an “-A” in their suffix) are built using automotive-specific flows at all steps in the manufacturing process to ensure robustness and low defectivity. These devices are supported with AIAG-compliant Production Part Approval Process (PPAP) documentation, and feature International Material Data System (IMDS) and China Automotive Material Data System (CAMDS) listing. Qualifications are compliant with AEC-Q100, and a zero-defect methodology is maintained throughout definition, design, evaluation, qualification, and mass production steps.

Table 1.1. Ordering Guide for Valid OPNs[1, 2, 4]

See the Top Marking section of this data sheet for the part number decoder.

Ordering Part Number (OPN)	Automotive OPNs[5, 6]	Number of Inputs VDD1 Side	Number of Inputs VDD2 Side	Max Data Rate (Mbps)	Default Output State	Isolation Rating (kV)	Package
Si8610BB-B-IS	Si8610BB-AS	1	0	150	Low	2.5	SOIC-8
Si8610BC-B-IS	Si8610BC-AS	1	0	150	Low	3.75	SOIC-8
Si8610EC-B-IS	Si8610EC-AS	1	0	150	High	3.75	SOIC-8
Si8610BD-B-IS	Si8610BD-AS	1	0	150	Low	5.0	WB SOIC-16
Si8610ED-B-IS	Si8610ED-AS	1	0	150	High	5.0	WB SOIC-16
Si8620BB-B-IS	Si8620BB-AS	2	0	150	Low	2.5	SOIC-8
Si8620EB-B-IS	Si8620EB-AS	2	0	150	High	2.5	SOIC-8
Si8620BC-B-IS	Si8620BC-AS	2	0	150	Low	3.75	SOIC-8
Si8620EC-B-IS	Si8620EC-AS	2	0	150	High	3.75	SOIC-8
Si8620BD-B-IS	Si8620BD-AS	2	0	150	Low	5.0	WB SOIC-16
Si8620ED-B-IS	Si8620ED-AS	2	0	150	High	5.0	WB SOIC-16
Si8621BB-B-IS	Si8621BB-AS	1	1	150	Low	2.5	SOIC-8
Si8621BC-B-IS	Si8621BC-AS	1	1	150	Low	3.75	SOIC-8
Si8621EC-B-IS	Si8621EC-AS	1	1	150	High	3.75	SOIC-8
Si8621BD-B-IS	Si8621BD-AS	1	1	150	Low	5.0	WB SOIC-16
Si8621ED-B-IS	Si8621ED-AS	1	1	150	High	5.0	WB SOIC-16
Si8622BB-B-IS	Si8622BB-AS	1	1	150	Low	2.5	SOIC-8
Si8622EB-B-IS	Si8622EB-AS	1	1	150	High	2.5	SOIC-8
Si8622BC-B-IS	Si8622BC-AS	1	1	150	Low	3.75	SOIC-8
Si8622EC-B-IS	Si8622EC-AS	1	1	150	High	3.75	SOIC-8
Si8622BD-B-IS	Si8622BD-AS	1	1	150	Low	5.0	WB SOIC-16
Si8622ED-B-IS	Si8622ED-AS	1	1	150	High	5.0	WB SOIC-16
SI8610BB-B-IM1	SI8610BB-AM1	1	0	150	Low	2.5	DFN-8
SI8610EB-B-IM1	SI8610EB-AM1	1	0	150	High	2.5	DFN-8

Ordering Part Number (OPN)	Automotive OPNs[5, 6]	Number of Inputs VDD1 Side	Number of Inputs VDD2 Side	Max Data Rate (Mbps)	Default Output State	Isolation Rating (kV)	Package
SI8620BB-B-IM1	SI8620BB-AM1	2	0	150	Low	2.5	DFN-8
SI8620EB-B-IM1	SI8620EB-AM1	2	0	150	High	2.5	DFN-8
SI8621BB-B-IM1	SI8621BB-AM1	1	1	150	Low	2.5	DFN-8
SI8621EB-B-IM1	SI8621EB-AM1	1	1	150	High	2.5	DFN-8
SI8622BB-B-IM1	SI8622BB-AM1	1	1	150	Low	2.5	DFN-8
SI8622EB-B-IM1	SI8622EB-AM1	1	1	150	High	2.5	DFN-8
Product Options with Reinforced VDE 0884-10 Rating with 10 kV Surge Capability							
Si8620BT-IS	Si8620BT-AS	2	0	150	Low	5.0	WB SOIC-16
Si8620ET-IS	Si8620ET-AS	2	0	150	High	5.0	WB SOIC-16
Si8621BT-IS	Si8621BT-AS	1	1	150	Low	5.0	WB SOIC-16
Si8621ET-IS	Si8621ET-AS	1	1	150	High	5.0	WB SOIC-16
Si8622BT-IS	Si8622BT-AS	1	1	150	Low	5.0	WB SOIC-16
Si8622ET-IS	Si8622ET-AS	1	1	150	High	5.0	WB SOIC-16

Note:

1. All packages are RoHS-compliant with peak reflow temperatures of 260 °C according to the JEDEC industry standard classifications and peak solder temperatures.
2. “Si” and “SI” are used interchangeably.
3. An "R" at the end of the part number denotes tape and reel packaging option.
4. The temperature ranges is –40 to +125 °C.
5. Automotive-Grade devices (with an "–A" suffix) are identical in construction materials, topside marking, and electrical parameters to their Industrial-Grade (with an "–I" suffix) version counterparts. Automotive-Grade products are produced utilizing full automotive process flows and additional statistical process controls throughout the manufacturing flow. The Automotive-Grade part number is included on shipping labels.
6. In the top markings of each device, the Manufacturing Code represented by either “RTTTTT” or “TTTTTT” contains as its first character a letter in the range N through Z to indicate Automotive-Grade.

Table of Contents

2. System Overview

2.1 Theory of Operation

The operation of an Si861x/2x channel is analogous to that of an opto coupler, except an RF carrier is modulated instead of light. This simple architecture provides a robust isolated data path and requires no special considerations or initialization at start-up. A simplified block diagram for a single Si861x/2x channel is shown in the figure below.

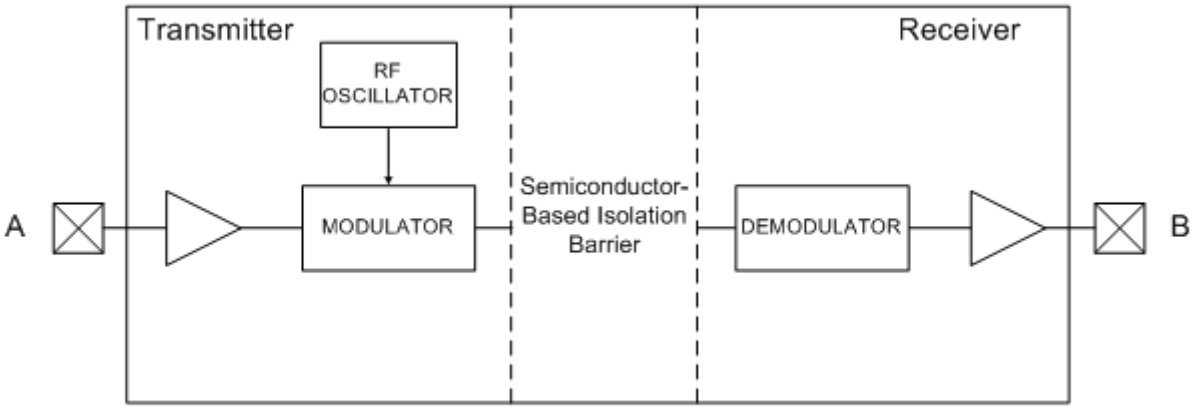


Figure 2.1. Simplified Channel Diagram

A channel consists of an RF Transmitter and RF Receiver separated by a semiconductor-based isolation barrier. Referring to the transmitter, input A modulates the carrier provided by an RF oscillator using on/off keying. The Receiver contains a demodulator that decodes the input state according to its RF energy content and applies the result to output B via the output driver. This RF on/off keying scheme is superior to pulse code schemes as it provides best-in-class noise immunity, low power consumption, and improved immunity to magnetic fields. See the following figure for more details.

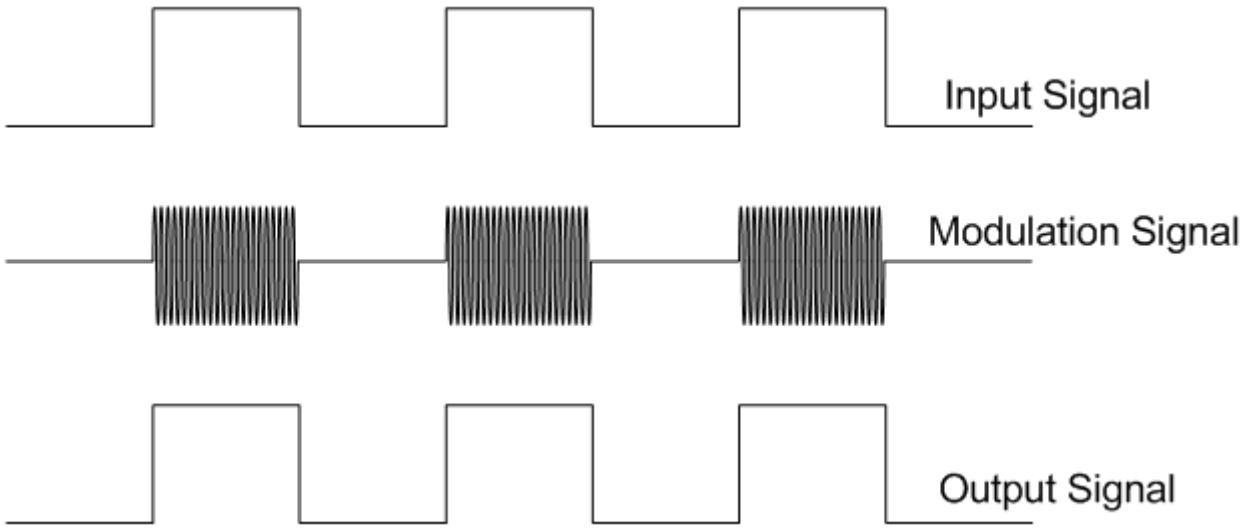


Figure 2.2. Modulation Scheme

2.2 Eye Diagram

The figure below illustrates an eye diagram taken on an Si8610. For the data source, the test used an Anritsu (MP1763C) Pulse Pattern Generator set to 1000 ns/div. The output of the generator's clock and data from an Si8610 were captured on an oscilloscope. The results illustrate that data integrity was maintained even at the high data rate of 150 Mbps. The results also show that 2 ns pulse width distortion and 350 ps peak jitter were exhibited.

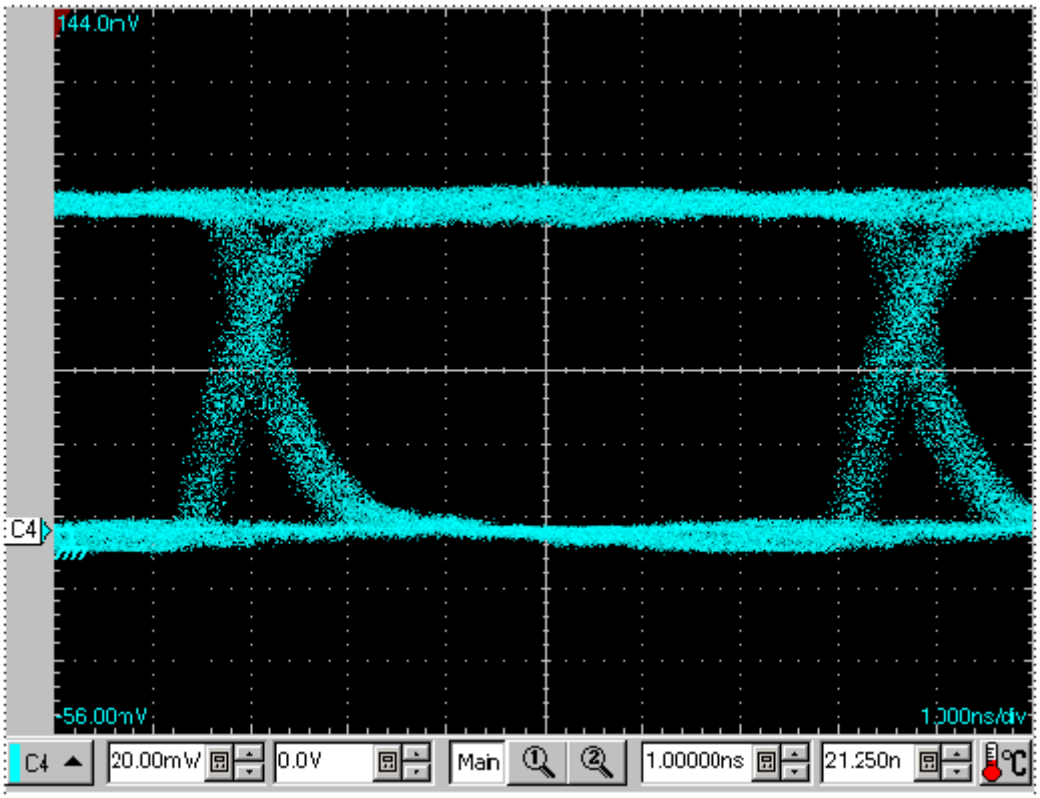


Figure 2.3. Eye Diagram

3. Device Operation

Device behavior during start-up, normal operation, and shutdown is shown in Figure 3.1 Device Behavior during Normal Operation on page 8, where UVLO+ and UVLO– are the respective positive-going and negative-going thresholds. Refer to the following table to determine outputs when power supply (VDD) is not present.

Table 3.1. Si86xx Logic Operation

V_I Input[1, 2]	VDDI State[1, 3, 4]	VDDO State[1, 3, 4]	V_O Output[1, 2]	Comments
H	P	P	H	Normal operation.
L	P	P	L	
X[5]	UP	P	L[6] H[6]	Upon transition of VDDI from unpowered to powered, V_O returns to the same state as V_I in less than 1 µs.
X[5]	P	UP	Undetermined	Upon transition of VDDO from unpowered to powered, V_O returns to the same state as V_I within 1 µs.

Note:

1. VDDI and VDDO are the input and output power supplies. VI and VO are the respective input and output terminals.
2. X = not applicable; H = Logic High; L = Logic Low; Hi-Z = High Impedance.
3. “Powered” state (P) is defined as 2.5 V < VDD < 5.5 V.
4. “Unpowered” state (UP) is defined as VDD = 0 V.
5. Note that an I/O can power the die for a given side through an internal diode if its source has adequate current.
6. See Ordering Guide for details. This is the selectable fail-safe operating mode (ordering option). Some devices have default output state = H, and some have default output state = L, depending on the ordering part number (OPN). For default high devices, the data channels have pull-ups on inputs/outputs. For default low devices, the data channels have pull-downs on inputs/outputs.

3.1 Device Startup

Outputs are held low during powerup until VDD is above the UVLO threshold for time period tSTART. Following this, the outputs follow the states of inputs.

3.2 Undervoltage Lockout

Undervoltage Lockout (UVLO) is provided to prevent erroneous operation during device startup and shutdown or when VDD is below its specified operating circuits range. Both Side A and Side B each have their own undervoltage lockout monitors. Each side can enter or exit UVLO independently. For example, Side A unconditionally enters UVLO when V_{DD1} falls below $V_{DD1(UVLO–)}$ and exits UVLO when V_{DD1} rises above $V_{DD1(UVLO+)}$. Side B operates the same as Side A with respect to its V_{DD2} supply.

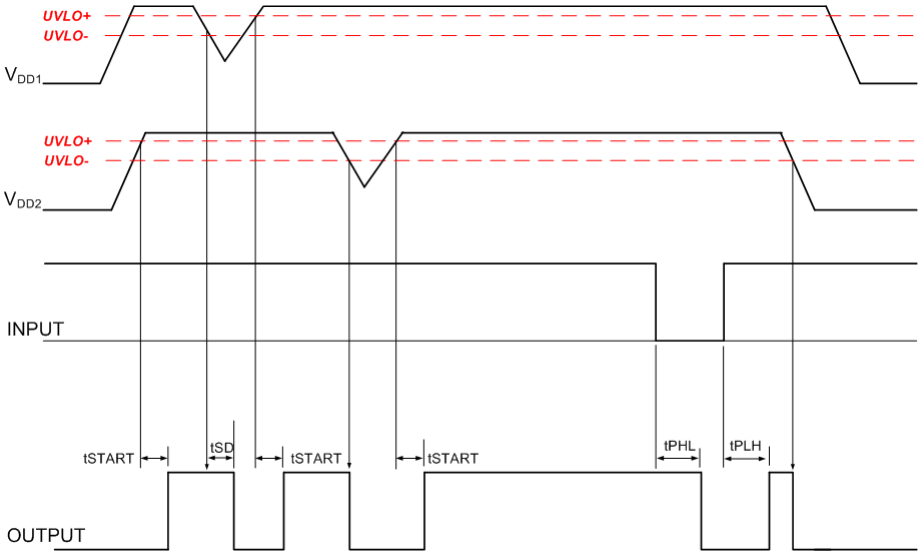


Figure 3.1. Device Behavior during Normal Operation

3.3 Layout Recommendations

To ensure safety in the end-user application, high-voltage circuits (i.e., circuits with >30 V_{AC}) must be physically separated from the safety extra-low-voltage circuits (SELV is a circuit with <30 V_{AC}) by a certain distance (creepage/clearance). If a component, such as a digital isolator, straddles this isolation barrier, it must meet those creepage/clearance requirements and also provide a sufficiently large high-voltage breakdown protection rating (commonly referred to as working voltage protection). Table 4.6 Insulation and Safety-Related Specifications on page 24 and Table 4.8 VDE 0884-10 Insulation Characteristics[1] on page 25 detail the working voltage and creepage/clearance capabilities of the Si86xx. These tables also detail the component standards (UL1577, IEC60747, CSA 5A), which are readily accepted by certification bodies to provide proof for end-system specifications requirements. Refer to the end-system specification (61010-1, 60950-1, 60601-1, etc.) requirements before starting any design that uses a digital isolator.

3.3.1 Supply Bypass

The Si861x/2x family requires a 0.1 µF bypass capacitor between V_{DD1} and GND1 and V_{DD2} and GND2. The capacitor should be placed as close as possible to the package. To enhance the robustness of a design, the user may also include resistors (50–300 Ω) in series with the inputs and outputs if the system is excessively noisy.

3.3.2 Output Pin Termination

The nominal output impedance of an isolator driver channel is approximately 50 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.

3.4 Fail-Safe Operating Mode

Si86xx devices feature a selectable (by ordering option) mode whereby the default output state (when the input supply is unpowered) can either be a logic high or logic low when the output supply is powered. See Table 3.1 Si86xx Logic Operation on page 7 and 1. Ordering Guide for more information.

3.5 Typical Performance Characteristis

The typical performance characteristics depicted in the following diagrams are for information purposes only. Refer to 4. Electrical Specifications for actual specification limits.

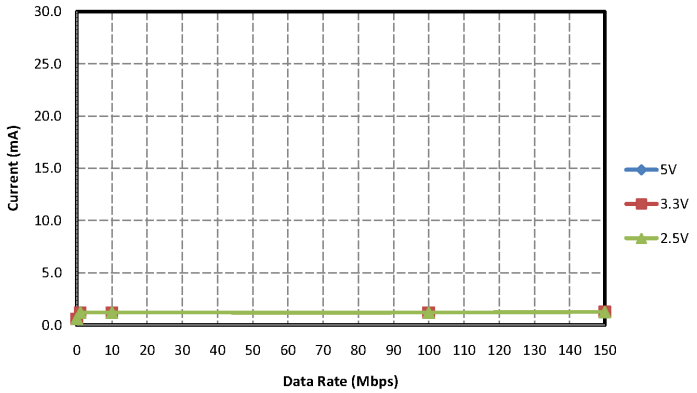


Figure 3.2. Si8610 Typical V_{DD1} Supply Current vs. Data Rate 5, 3.3, and 2.50 V Operation

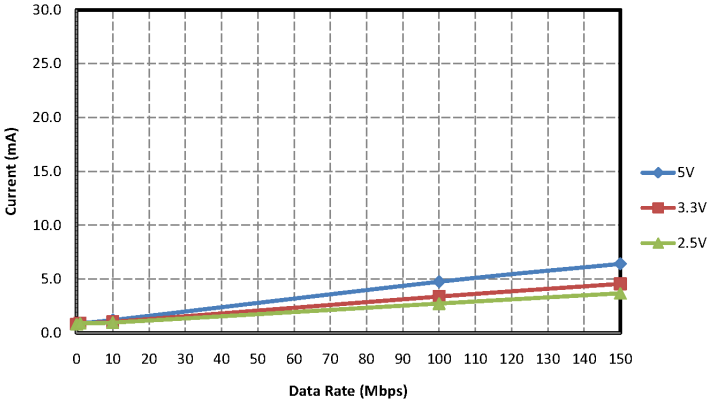


Figure 3.3. Si8610 Typical V_{DD2} Supply Current vs. Data Rate 5, 3.3, and 2.50 V Operation (15 pF Load)

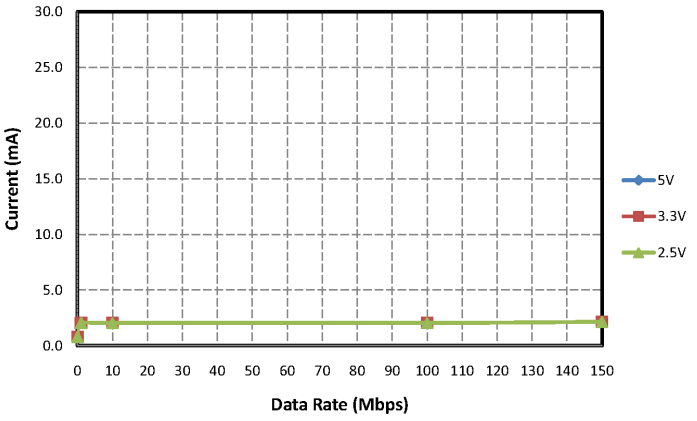


Figure 3.4. Si8620 Typical V_{DD1} Supply Current vs. Data Rate 5, 3.3, and 2.50 V Operation

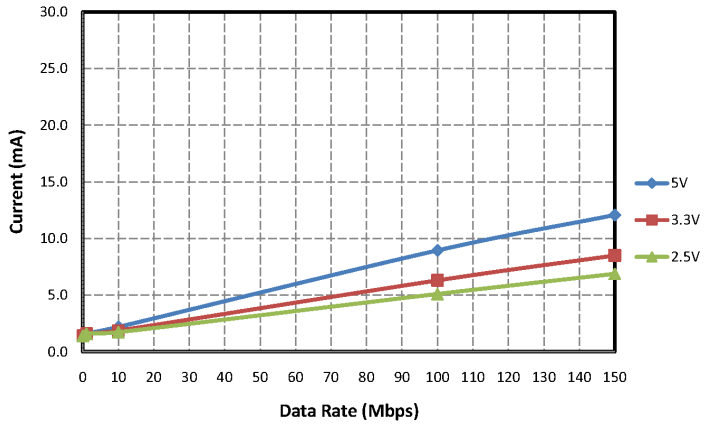


Figure 3.5. Si8620 Typical V_{DD2} Supply Current vs. Data Rate 5, 3.3, and 2.50 V Operation (15 pF Load)

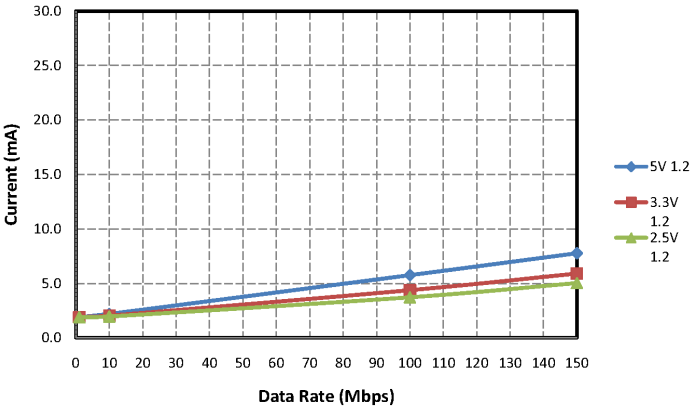


Figure 3.6. Si8621 Typical V_{DD1} or V_{DD2} Supply Current vs. Data Rate 5, 3.3, and 2.50 V Operation (15 pF Load)

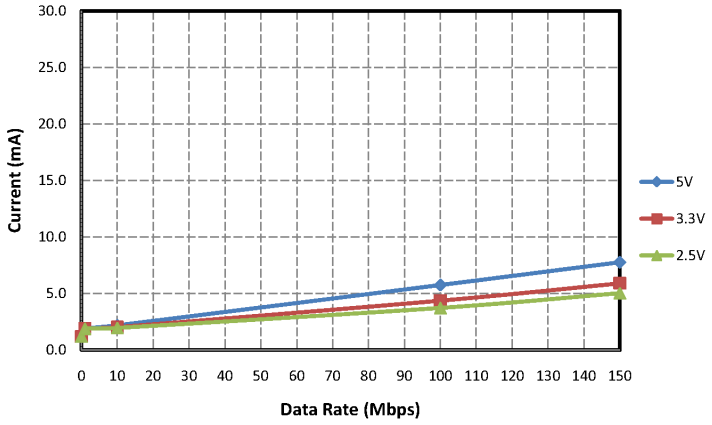


Figure 3.7. Si8622 Typical V_{DD1} or V_{DD2} Supply Current vs. Data Rate 5, 3.3, and 2.50 V Operation (15 pF Load)

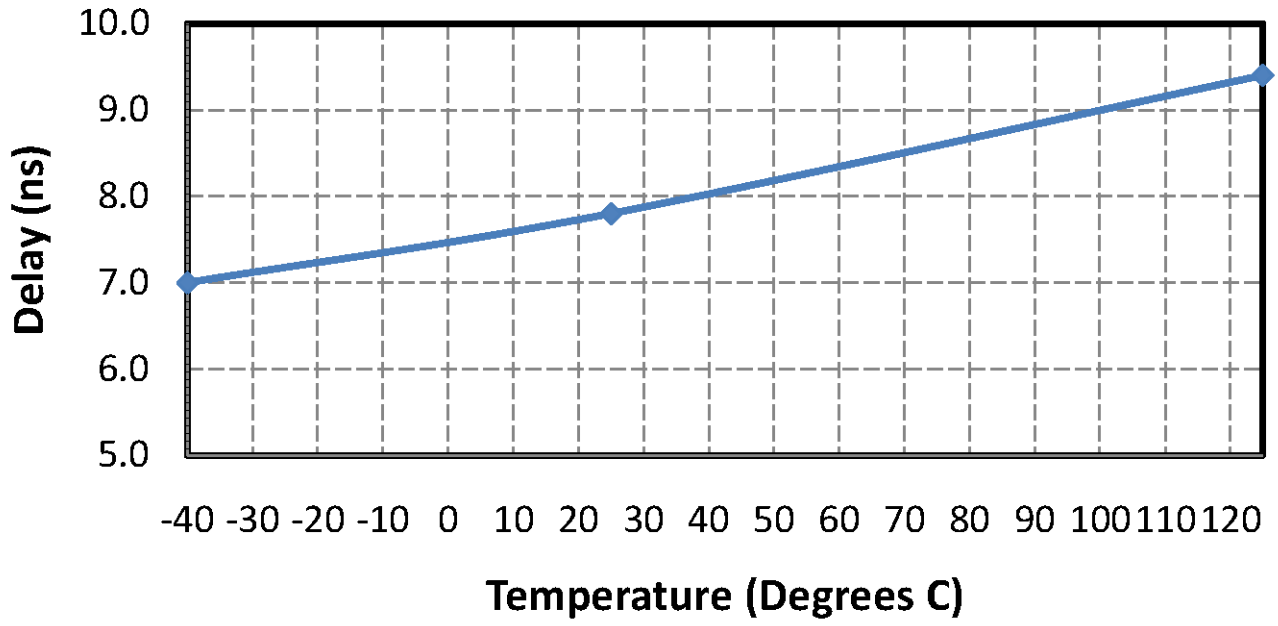


Figure 3.8. Propagation Delay vs. Temperature (5.0 V Data)

4. Electrical Specifications

Table 4.1. Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Ambient Operating Temperature[1]	TA	–40	25	125[1]	°C
Supply Voltage	VDD1	2.5	—	5.5	V
	VDD2	2.5	—	5.5	V

Note:
1. The maximum ambient temperature is dependent on data frequency, output loading, number of operating channels, and supply voltage.

Table 4.2. Electrical Characteristics[1]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
VDD Undervoltage Threshold	VDD_{UV+}	V_{DD1}, V_{DD2} rising	1.95	2.24	2.375	V
VDD Undervoltage Threshold	VDD_{UV-}	V_{DD1}, V_{DD2} falling	1.88	2.16	2.325	V
VDD Undervoltage Hysteresis	VDD_{HYS}		50	70	95	mV
Positive-Going Input Threshold	VT+	All inputs rising	1.4	1.67	1.9	V
Negative-Going Input Threshold	VT–	All inputs falling	1.0	1.23	1.4	V
Input Hysteresis	V_{HYS}		0.38	0.44	0.50	V
High Level Input Voltage	V_{IH}		2.0	—	—	V
Low Level Input Voltage	V_{IL}		—	—	0.8	V
High Level Output Voltage	V_{OH}	Ioh = –4 mA	V_{DD1}, V_{DD2} – 0.4	4.8	—	V
Low Level Output Voltage	V_{OL}	Iol = 4 mA	—	0.2	0.4	V
Input Leakage Current Si86xxxB/C/D Si86xxxT	I_L		— —	— —	±10 ±15	µA
Output Impedance[2]	Z_O		—	50	—	Ω
DC Supply Current (All Inputs 0 V or at Supply)						
Si8610Bx, Ex V_{DD1} V_{DD2} V_{DD1} V_{DD2}		 V_I = 0(Bx), 1(Ex) V_I = 0(Bx), 1(Ex) V_I = 1(Bx), 0(Ex) V_I = 1(Bx), 0(Ex)	 — — — —	 0.6 0.8 1.8 0.8	 1.2 1.5 2.9 1.5	mA

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Si8620Bx, Ex						
V_{DD1}		V_I = 0(Bx), 1(Ex)	—	0.8	1.4	
V_{DD2}		V_I = 0(Bx), 1(Ex)	—	1.4	2.2	mA
V_{DD1}		V_I = 1(Bx), 0(Ex)	—	3.3	5.3	
V_{DD2}		V_I = 1(Bx), 0(Ex)	—	1.4	2.2	
Si8621Bx, Ex						
V_{DD1}		V_I = 0(Bx), 1(Ex)	—	1.2	1.9	
V_{DD2}		V_I = 0(Bx), 1(Ex)	—	1.2	1.9	mA
V_{DD1}		V_I = 1(Bx), 0(Ex)	—	2.4	3.8	
V_{DD2}		V_I = 1(Bx), 0(Ex)	—	2.4	3.8	
Si8622Bx, Ex						
V_{DD1}		V_I = 0(Bx), 1(Ex)	—	2.6	4.2	
V_{DD2}		V_I = 0(Bx), 1(Ex)	—	3.3	5.3	mA
V_{DD1}		V_I = 1(Bx), 0(Ex)	—	4.0	6.4	
V_{DD2}		V_I = 1(Bx), 0(Ex)	—	4.8	7.7	
1 Mbps Supply Current (All Inputs = 500 kHz Square Wave, C_L = 15 pF on All Outputs)						
Si8610Bx, Ex						
V_{DD1}			—	1.2	2.0	mA
V_{DD2}			—	0.9	1.5	
Si8620Bx, Ex						
V_{DD1}			—	2.1	3.1	mA
V_{DD2}			—	1.6	2.4	
Si8621Bx, Ex						
V_{DD1}			—	1.9	2.9	mA
V_{DD2}			—	1.9	2.9	
Si8622Bx, Ex						
V_{DD1}			—	3.4	5.1	mA
V_{DD2}			—	4.2	6.2	
10 Mbps Supply Current (All Inputs = 5 MHz Square Wave, C_L = 15 pF on All Outputs)						
Si8610Bx, Ex						
V_{DD1}			—	1.2	2.0	mA
V_{DD2}			—	1.2	2.0	

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Si8620Bx, Ex						
V_{DD1}			—	2.1	3.1	mA
V_{DD2}			—	2.2	3.3	
Si8621Bx, Ex						
V_{DD1}			—	2.2	3.3	mA
V_{DD2}			—	2.2	3.3	
Si8622Bx, Ex						
V_{DD1}			—	3.7	5.5	mA
V_{DD2}			—	4.4	6.7	
100 Mbps Supply Current (All Inputs = 50 MHz Square Wave, C_L = 15 pF on All Outputs)						
Si8610Bx, Ex						
V_{DD1}			—	1.2	2.0	mA
V_{DD2}			—	4.8	6.7	
Si8620Bx, Ex						
V_{DD1}			—	2.1	3.1	mA
V_{DD2}			—	8.9	12.5	
Si8621Bx, Ex						
V_{DD1}			—	5.8	8.1	mA
V_{DD2}			—	5.8	8.1	
Si8622Bx, Ex						
V_{DD1}			—	7.6	10.6	mA
V_{DD2}			—	8.2	11.4	
Timing Characteristics						
Si861x/2x Bx, Ex						
Data Rate			0	—	150	Mbps
Minimum Pulse Width			—	—	5.0	ns
Propagation Delay	t_{PHL}, t_{PLH}	See Figure 4.1 Propagation Delay Timing on page 15	5.0	8.0	13	ns
Pulse Width Distortion |tPLH – tPHL|	PWD	See Figure 4.1 Propagation Delay Timing on page 15	—	0.2	4.5	ns
Propagation Delay Skew[3]	$t_{PSK(P-P)}$		—	2.0	4.5	ns
Channel-Channel Skew	t_{PSK}		—	0.4	2.5	ns
All Models						

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Rise Time	t_r	C_L = 15 pF See Figure 4.1 Propagation Delay Timing on page 15	—	2.5	4.0	ns
Output Fall Time	t_f	C_L = 15 pF See Figure 4.1 Propagation Delay Timing on page 15	—	2.5	4.0	ns
Peak Eye Diagram Jitter	$t_{JIT(PK)}$	See Figure 2.3 Eye Diagram on page 6	—	350	—	ps
Common Mode Transient Immunity	CMTI	V_I = V_{DD} or 0 V V_{CM} = 1500 V See Figure 4.2 Common-Mode Transient Immunity Test Circuit on page 15				kV/µs
Si86xxxB/C/D			35	50	—	
Si86xxxT			60	100	—	
Start-up Time[4]	t_{SU}		—	15	40	µs

Note:

1. V_{DD1} = 5 V ±10%; V_{DD2} = 5 V ±10%, T_A = –40 to 125 °C
2. The nominal output impedance of an isolator driver channel is approximately 50 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled-impedance PCB traces.
3. $t_{PSK(P-P)}$ is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.
4. Start-up time is the time period from the application of power to the appearance of valid data at the output.

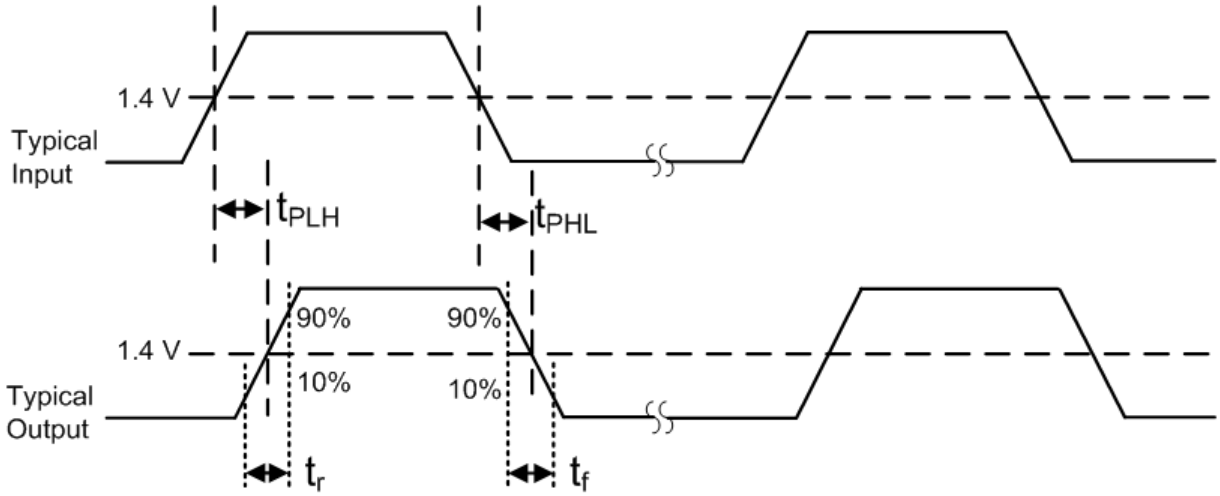


Figure 4.1. Propagation Delay Timing

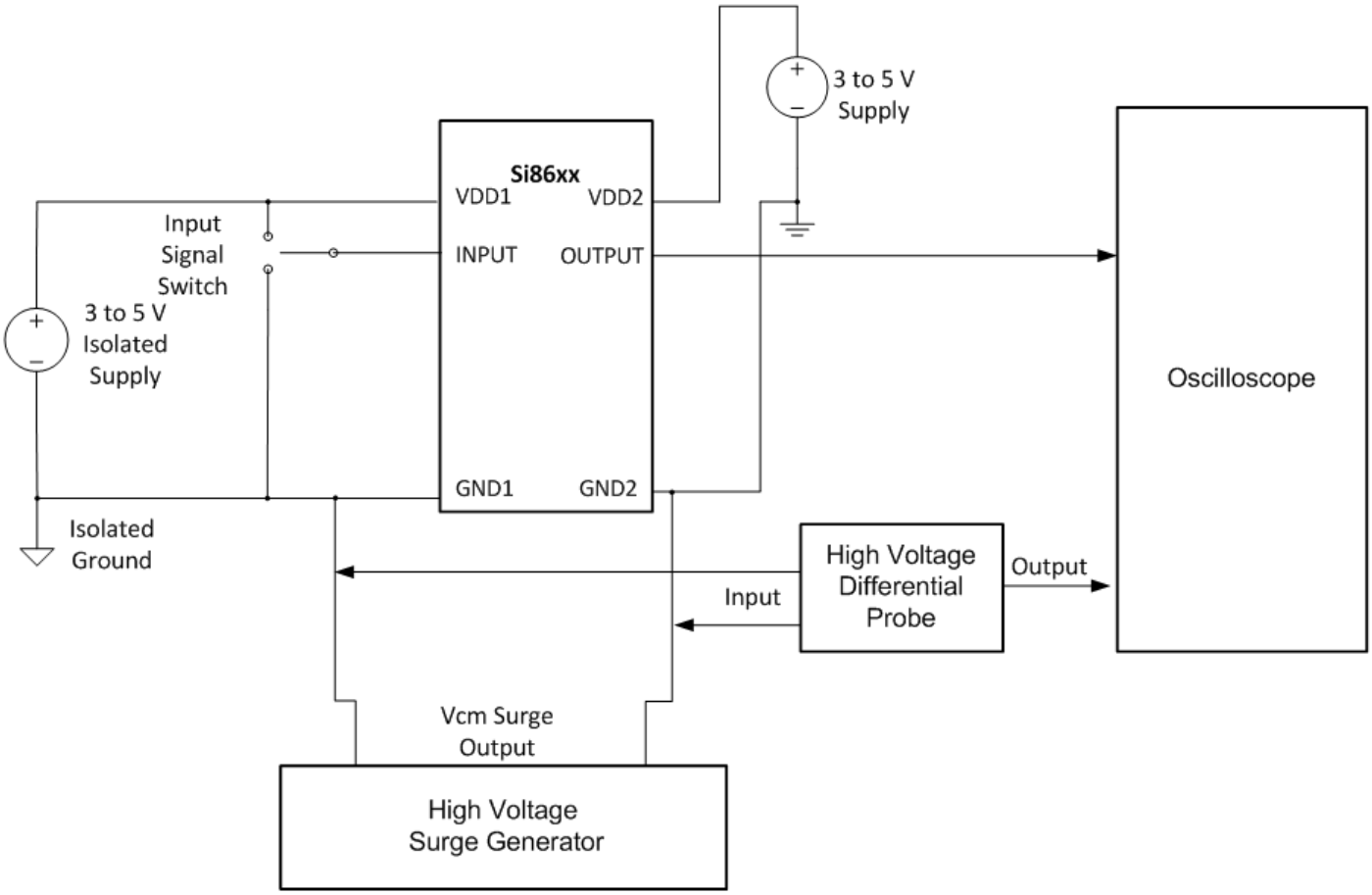


Figure 4.2. Common-Mode Transient Immunity Test Circuit

Table 4.3. Electrical Characteristics[1]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
VDD Undervoltage Threshold	VDD_{UV+}	V_{DD1}, V_{DD2} rising	1.95	2.24	2.375	V
VDD Undervoltage Threshold	VDD_{UV-}	V_{DD1}, V_{DD2} falling	1.88	2.16	2.325	V
VDD Undervoltage Hysteresis	VDD_{HYS}		50	70	95	mV
Positive-Going Input Threshold	VT+	All inputs rising	1.4	1.67	1.9	V
Negative-Going Input Threshold	VT–	All inputs falling	1.0	1.23	1.4	V
Input Hysteresis	V_{HYS}		0.38	0.44	0.50	V
High Level Input Voltage	V_{IH}		2.0	—	—	V
Low Level Input Voltage	V_{IL}		—	—	0.8	V
High Level Output Voltage	V_{OH}	Ioh = –4 mA	V_{DD1}, V_{DD2} – 0.4	3.1	—	V
Low Level Output Voltage	V_{OL}	Iol = 4 mA	—	0.2	0.4	V
Input Leakage Current						
Si86xxxB/C/D	I_L		—	—	±10	µA
Si86xxxT			—	—	±15	
Output Impedance[2]	Z_O		—	50	—	Ω
DC Supply Current (All Inputs 0 V or at Supply)						
Si8610Bx, Ex						
V_{DD1}		V_I = 0(Bx), 1(Ex)	—	0.6	1.2	
V_{DD2}		V_I = 0(Bx), 1(Ex)	—	0.8	1.5	mA
V_{DD1}		V_I = 1(Bx), 0(Ex)	—	1.8	2.9	
V_{DD2}		V_I = 1(Bx), 0(Ex)	—	0.8	1.5	
Si8620Bx, Ex						
V_{DD1}		V_I = 0(Bx), 1(Ex)	—	0.8	1.4	
V_{DD2}		V_I = 0(Bx), 1(Ex)	—	1.4	2.2	mA
V_{DD1}		V_I = 1(Bx), 0(Ex)	—	3.3	5.3	
V_{DD2}		V_I = 1(Bx), 0(Ex)	—	1.4	2.2	
Si8621Bx, Ex						
V_{DD1}		V_I = 0(Bx), 1(Ex)	—	1.2	1.9	
V_{DD2}		V_I = 0(Bx), 1(Ex)	—	1.2	1.9	mA
V_{DD1}		V_I = 1(Bx), 0(Ex)	—	2.4	3.8	
V_{DD2}		V_I = 1(Bx), 0(Ex)	—	2.4	3.8	

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Si8622Bx, Ex						
V_{DD1}		V_I = 0(Bx), 1(Ex)	—	2.6	4.2	mA
V_{DD2}		V_I = 0(Bx), 1(Ex)	—	3.3	5.3	
V_{DD1}		V_I = 1(Bx), 0(Ex)	—	4.0	6.4	
V_{DD2}		V_I = 1(Bx), 0(Ex)	—	4.8	7.7	
1 Mbps Supply Current (All Inputs = 500 kHz Square Wave, C_L = 15 pF on All Outputs)						
Si8610Bx, Ex						
V_{DD1}			—	1.2	2.0	mA
V_{DD2}			—	0.9	1.5	
Si8620Bx, Ex						
V_{DD1}			—	2.1	3.1	mA
V_{DD2}			—	1.6	2.4	
Si8621Bx, Ex						
V_{DD1}			—	1.9	2.9	mA
V_{DD2}			—	1.9	2.9	
Si8622Bx, Ex						
V_{DD1}			—	3.4	5.1	mA
V_{DD2}			—	4.2	6.2	
10 Mbps Supply Current (All Inputs = 5 MHz Square Wave, C_L = 15 pF on All Outputs)						
Si8610Bx, Ex						
V_{DD1}			—	1.2	2.0	mA
V_{DD2}			—	1.0	1.8	
Si8620Bx, Ex						
V_{DD1}			—	2.1	3.1	mA
V_{DD2}			—	1.9	2.8	
Si8621Bx, Ex						
V_{DD1}			—	2.0	3.0	mA
V_{DD2}			—	2.0	3.0	
Si8622Bx, Ex						
V_{DD1}			—	3.5	5.3	mA
V_{DD2}			—	4.3	6.4	
100 Mbps Supply Current (All Inputs = 50 MHz Square Wave, C_L = 15 pF on All Outputs)						
Si8610Bx, Ex						
V_{DD1}			—	1.2	2.0	mA
V_{DD2}			—	3.4	5.1	

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Si8620Bx, Ex						
V_{DD1}			—	2.1	3.1	mA
V_{DD2}			—	6.3	8.8	
Si8621Bx, Ex						
V_{DD1}			—	4.4	6.1	mA
V_{DD2}			—	4.4	6.1	
Si8622Bx, Ex						
V_{DD1}			—	5.9	8.2	mA
V_{DD2}			—	6.6	9.3	
Timing Characteristics						
Si861x/2x Bx, Ex						
Data Rate			0	—	150	Mbps
Minimum Pulse Width			—	—	5.0	ns
Propagation Delay	t_{PHL}, t_{PLH}	See Figure 4.1 Propagation Delay Timing on page 15	5.0	8.0	13	ns
Pulse Width Distortion |tPLH – tPHL|	PWD	See Figure 4.1 Propagation Delay Timing on page 15	—	0.2	4.5	ns
Propagation Delay Skew[3]	$t_{PSK(P-P)}$		—	2.0	4.5	ns
Channel-Channel Skew	t_{PSK}		—	0.4	2.5	ns
All Models						
Output Rise Time	t_r	C_L = 15 pF See Figure 4.1 Propagation Delay Timing on page 15	—	2.5	4.0	ns
Output Fall Time	t_f	C_L = 15 pF See Figure 4.1 Propagation Delay Timing on page 15	—	2.5	4.0	ns
Peak Eye Diagram Jitter	$t_{JIT(PK)}$	See Figure 2.3 Eye Diagram on page 6	—	350	—	ps
Common Mode Transient Immunity Si86xxxB/C/D Si86xxxT	CMTI	V_I = V_{DD} or 0 V VCM = 1500 V See Figure 4.2 Common-Mode Transient Immunity Test Circuit on page 15	 35 60	 50 100	 — —	kV/µs
Start-up Time[4]	t_{SU}		—	15	40	µs

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit

Note:

1. V_{DD1} = 3.3 V ±10%; V_{DD2} = 3.3 V ±10%, T_A = –40 to 125 °C
2. The nominal output impedance of an isolator driver channel is approximately 50 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled-impedance PCB traces.
3. $t_{PSK(P-P)}$ is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.
4. Start-up time is the time period from the application of power to the appearance of valid data at the output.

Table 4.4. Electrical Characteristics[1]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
VDD Undervoltage Threshold	VDD_{UV+}	V_{DD1}, V_{DD2} rising	1.95	2.24	2.375	V
VDD Undervoltage Threshold	$VDD_{UV–}$	V_{DD1}, V_{DD2} falling	1.88	2.16	2.325	V
VDD Undervoltage Hysteresis	VDD_{HYS}		50	70	95	mV
Positive-Going Input Threshold	VT+	All inputs rising	1.4	1.67	1.9	V
Negative-Going Input Threshold	VT–	All inputs falling	1.0	1.23	1.4	V
Input Hysteresis	V_{HYS}		0.38	0.44	0.50	V
High Level Input Voltage	V_{IH}		2.0	—	—	V
Low Level Input Voltage	V_{IL}		—	—	0.8	V
High Level Output Voltage	V_{OH}	Ioh = –4 mA	V_{DD1}, V_{DD2} – 0.4	2.3	—	V
Low Level Output Voltage	V_{OL}	Iol = 4 mA	—	0.2	0.4	V
Input Leakage Current						
Si86xxxB/C/D	I_L		—	—	±10	µA
Si86xxxT			—	—	±15	
Output Impedance[2]	Z_O		—	50	—	Ω
DC Supply Current (All Inputs 0 V or at Supply)						
Si8610Bx, Ex						
V_{DD1}		V_I = 0(Bx), 1(Ex)	—	0.6	1.2	
V_{DD2}		V_I = 0(Bx), 1(Ex)	—	0.8	1.5	mA
V_{DD1}		V_I = 1(Bx), 0(Ex)	—	1.8	2.9	
V_{DD2}		V_I = 1(Bx), 0(Ex)	—	0.8	1.5	
Si8620Bx, Ex						
V_{DD1}		V_I = 0(Bx), 1(Ex)	—	0.8	1.4	
V_{DD2}		V_I = 0(Bx), 1(Ex)	—	1.4	2.2	mA
V_{DD1}		V_I = 1(Bx), 0(Ex)	—	3.3	5.3	
V_{DD2}		V_I = 1(Bx), 0(Ex)	—	1.4	2.2	

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Si8621Bx, Ex						
V_{DD1}		V_I = 0(Bx), 1(Ex)	—	1.2	1.9	mA
V_{DD2}		V_I = 0(Bx), 1(Ex)	—	1.2	1.9	
V_{DD1}		V_I = 1(Bx), 0(Ex)	—	2.4	3.8	
V_{DD2}		V_I = 1(Bx), 0(Ex)	—	2.4	3.8	
Si8622Bx, Ex						
V_{DD1}		V_I = 0(Bx), 1(Ex)	—	2.6	4.2	mA
V_{DD2}		V_I = 0(Bx), 1(Ex)	—	3.3	5.3	
V_{DD1}		V_I = 1(Bx), 0(Ex)	—	4.0	6.4	
V_{DD2}		V_I = 1(Bx), 0(Ex)	—	4.8	7.7	
1 Mbps Supply Current (All Inputs = 500 kHz Square Wave, C_L = 15 pF on All Outputs)						
Si8610Bx, Ex						
V_{DD1}			—	1.2	2.0	mA
V_{DD2}			—	0.9	1.5	
Si8620Bx, Ex						
V_{DD1}			—	2.1	3.1	mA
V_{DD2}			—	1.6	2.4	
Si8621Bx, Ex						
V_{DD1}			—	1.9	2.9	mA
V_{DD2}			—	1.9	2.9	
Si8622Bx, Ex						
V_{DD1}			—	3.4	5.1	mA
V_{DD2}			—	4.2	6.2	
10 Mbps Supply Current (All Inputs = 5 MHz Square Wave, C_L = 15 pF on All Outputs)						
Si8610Bx, Ex						
V_{DD1}			—	1.2	2.0	mA
V_{DD2}			—	1.0	1.6	
Si8620Bx, Ex						
V_{DD1}			—	2.1	3.1	mA
V_{DD2}			—	1.7	2.6	
Si8621Bx, Ex						
V_{DD1}			—	2.0	2.9	mA
V_{DD2}			—	2.0	2.9	

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Si8622Bx, Ex						
V_{DD1}			—	3.5	5.2	mA
V_{DD2}			—	4.2	6.3	
100 Mbps Supply Current (All Inputs = 50 MHz Square Wave, C_L = 15 pF on All Outputs)						
Si8610Bx, Ex						
V_{DD1}			—	1.2	2.0	mA
V_{DD2}			—	2.7	4.4	
Si8620Bx, Ex						
V_{DD1}			—	2.1	3.1	mA
V_{DD2}			—	5.1	7.1	
Si8621Bx, Ex						
V_{DD1}			—	3.7	5.2	mA
V_{DD2}			—	3.7	5.2	
Si8622Bx, Ex						
V_{DD1}			—	5.2	7.3	mA
V_{DD2}			—	6.0	8.4	
Timing Characteristics						
Si861x/2x Bx, Ex						
Data Rate			0	—	150	Mbps
Minimum Pulse Width			—	—	5.0	ns
Propagation Delay	t_{PHL}, t_{PLH}	See Figure 4.1 Propagation Delay Timing on page 15	5.0	8.0	14	ns
Pulse Width Distortion |tPLH – tPHL|	PWD	See Figure 4.1 Propagation Delay Timing on page 15	—	0.2	5.0	ns
Propagation Delay Skew[3]	$t_{PSK(P-P)}$		—	2.0	5.0	ns
Channel-Channel Skew	t_{PSK}		—	0.4	2.5	ns
All Models						
Output Rise Time	t_r	C_L = 15 pF See Figure 4.1 Propagation Delay Timing on page 15	—	2.5	4.0	ns
Output Fall Time	t_f	C_L = 15 pF See Figure 4.1 Propagation Delay Timing on page 15	—	2.5	4.0	ns
Peak Eye Diagram Jitter	$t_{JIT(PK)}$	See Figure 2.3 Eye Diagram on page 6	—	350	—	ps

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Common Mode Transient Immunity Si86xxxB/C/D Si86xxxT	CMTI	$V_I = V_{DD}$ or 0 V VCM = 1500 V See Figure 4.2 Common-Mode Transient Immunity Test Circuit on page 15	 35 60	 50 100	 — —	kV/µs
Start-up Time[4]	t_{SU}		—	15	40	µs

Note:

1. V_{DD1} = 2.5 V ±5%; V_{DD2} = 2.5 V ±5%, T_A = –40 to 125 °C
2. The nominal output impedance of an isolator driver channel is approximately 50 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled-impedance PCB traces.
3. $t_{PSK(P-P)}$ is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.
4. Start-up time is the time period from the application of power to the appearance of valid data at the output.

Table 4.5. Regulatory Information[1, 2, 3, 4]

For All Product Options Except Si86xxxT
CSA
The Si861x/2x is certified under CSA. For more details, see Master Contract File 232873.
60950-1, 62368-1: Up to 600 V_{RMS} reinforced insulation working voltage; up to 1000 V_{RMS} basic insulation working voltage.
60601-1: Up to 125 V_{RMS} reinforced insulation working voltage; up to 380 V_{RMS} basic insulation working voltage.
VDE
The Si861x/2x is certified according to VDD 0884-10. For more details, see File 5006301-4880-0001.
VDD 0884-10: Up to 1200 Vpeak for basic insulation working voltage.
60950-1, 62368-1: Up to 600 V_{RMS} reinforced insulation working voltage; up to 1000 V_{RMS} basic insulation working voltage.
UL
The Si861x/2x is certified under UL1577 component recognition program. For more details, see File E257455.
Rated up to 5000 V_{RMS} isolation voltage for basic protection.
CQC
The Si861x/2x is certified under GB4943.1-2011. For more details, see certificates CQC13001096110 and CQC13001096239.
Rated up to 600 V_{RMS} reinforced insulation working voltage; up to 1000 V_{RMS} basic insulation working voltage.
For All Si86xxxT Product Options
CSA
Certified under CSA. For more details, see Master Contract File 232873.
60950-1, 62368-1: Up to 600 V_{RMS} reinforced insulation working voltage; up to 1000 V_{RMS} basic insulation working voltage.
VDE
Certified according to VDE 0884-10.
UL
Certified under UL1577 component recognition program. For more details, see File E257455.
Rated up to 5000 V_{RMS} isolation voltage for basic protection.
CQC
Certified under GB4943.1-2011.
Rated up to 600 V_{RMS} reinforced insulation working voltage; up to 1000 V_{RMS} basic insulation working voltage.
Note: 1. Regulatory Certifications apply to 2.5 kV_{RMS} rated devices, which are production tested to 3.0 kV_{RMS} for 1 s. 2. Regulatory Certifications apply to 3.75 kV_{RMS} rated devices, which are production tested to 4.5 kV_{RMS} for 1 s. 3. Regulatory Certifications apply to 5.0 kV_{RMS} rated devices, which are production tested to 6.0 kV_{RMS} for 1 s. 4. For more information, see 1. Ordering Guide.

Table 4.6. Insulation and Safety-Related Specifications

Parameter	Symbol	Test Condition	Value			Unit
			WB SOIC-16	SOIC-8	DFN-8	
Nominal External Air Gap (Clearance)[1]	CLR		8.0	4.9	3.4	mm
Nominal External Tracking (Creepage)[1]	CPG		8.0	4.01	3.4	mm
Minimum Internal Gap (Internal Clearance)	DTI		0.014	0.014	0.014	mm
Tracking Resistance	PTI or CTI	IEC60112	600	600	600	V_{RMS}
Erosion Depth	ED		0.019	0.019	0.051 0.087	mm
Resistance (Input-Output)[2]	R_{IO}		10^{12}	10^{12}	10^{12}	W
Capacitance (Input-Output)[2]	C_{IO}	f = 1 MHz	2.0	2.0	2.0	pF
Input Capacitance[3]	C_I		4.0	4.0	4.0	pF

Note:

1. The values in this table correspond to the nominal creepage and clearance values. VDE certifies the clearance and creepage limits as 4.7 mm minimum for the SOIC-8 package and 8.5 mm minimum for the WB SOIC-16 package. UL does not impose a clearance and creepage minimum for component-level certifications. CSA certifies the clearance and creepage limits as 3.9 mm minimum for the SOIC-8 and 7.6 mm minimum for the WB SOIC-16 package.
2. To determine resistance and capacitance, the Si86xx is converted into a 2-terminal device. All pins on the side 1 are shorted together to form the first terminal, the same is done with side 2 to form the second terminal. The parameters are then measured between these two terminals.
3. Measured from input pin to ground.

Table 4.7. IEC 60664-1 Ratings

Parameter	Test Conditions	Specification		
		WB SOIC-16	SOIC-8	DFN-8
Basic Isolation Group	Material Group	I	I	I
Installation Classification	Rated Mains Voltages ≤ 150 V_{RMS}	I-IV	I-IV	I-IV
	Rated Mains Voltages ≤ 300 V_{RMS}	I-IV	I-III	I-III
	Rated Mains Voltages ≤ 400 V_{RMS}	I-III	I-II	I-II
	Rated Mains Voltages ≤ 600 V_{RMS}	I-III	I-II	I-II

Table 4.8. VDE 0884-10 Insulation Characteristics[1]

Parameter	Symbol	Test Condition	Characteristic		Unit
			WB SOIC-16	SOIC-8	
Maximum Working Insulation Voltage	V_{IORM}		1200	630	Vpeak
Input to Output Test Voltage	V_{PR}	Method b1 (V_{IORM} x 1.875 = VPR, 100% Production Test, t_m = 1 sec, Partial Discharge < 5 pC)	2250	1182	Vpeak
Transient Overvoltage	V_{IOTM}	t = 60 sec	6000	6000	Vpeak
Surge Voltage	V_{IOSM}	Tested per IEC 60065 with surge voltage of 1.2 µs/50 µs Si86xxxT tested with magnitude 6250 V x 1.6 = 10 kV Si86xxxB/C/D tested with 4000 V	 6250 4000	 — 4000	Vpeak
Pollution Degree (DIN VDE 0110, Table 1)			2	2	
Insulation Resistance at T_S, V_{IO} = 500 V	R_S		$>10^9$	$>10^9$	Ω

Note:

1. Maintenance of the safety data is ensured by protective circuits. The Si86xxxx provides a climate classification of 40/125/21.
2. The DFN-8 package is not certified to VDE 0884-10 and hence cannot be listed under this table. Refer to Table 4.5, CSA section for working voltage specifications.

Table 4.9. IEC Safety Limiting Values[1]

Parameter	Symbol	Test Condition	Max		Unit
			WB SOIC-16	SOIC-8	
Safety Temperature	T_S		150	150	°C
Safety Input Current	I_S	θ_{JA} = 140 °C/W (SOIC-8) 100 °C/W (WB SOIC-16) V_I = 5.5 V, T_J = 150 °C, T_A = 25 °C	220	160	mA
Device Power Dissipation[2]	P_D		150	150	mW

Note:

1. Maximum value allowed in the event of a failure; also see the thermal derating curve in Figure 4.3 (WB SOIC-16) Thermal Derating Curve for Safety Limiting Current on page 26 and Figure 4.4 (SOIC-8) Thermal Derating Curve for Safety Limiting Current on page 26.
2. The Si86xx is tested with VDD1 = VDD2 = 5.5 V; T_J = 150 ºC; C_L = 15 pF, input a 150 Mbps 50% duty cycle square wave.

Table 4.10. Thermal Characteristics

Parameter	Symbol	WB SOIC-16	SOIC-8	DFN-8	Unit
IC Junction-to-Air Thermal Resistance	θ_{JA}	100	140	94	°C/W

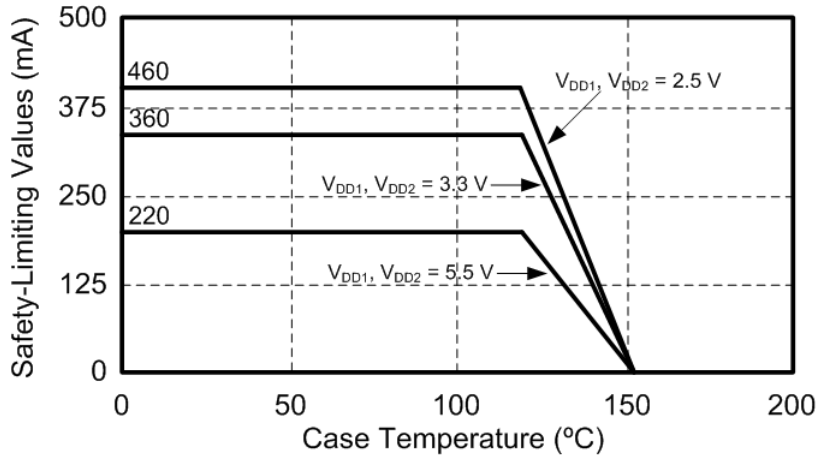


Figure 4.3. (WB SOIC-16) Thermal Derating Curve for Safety Limiting Current

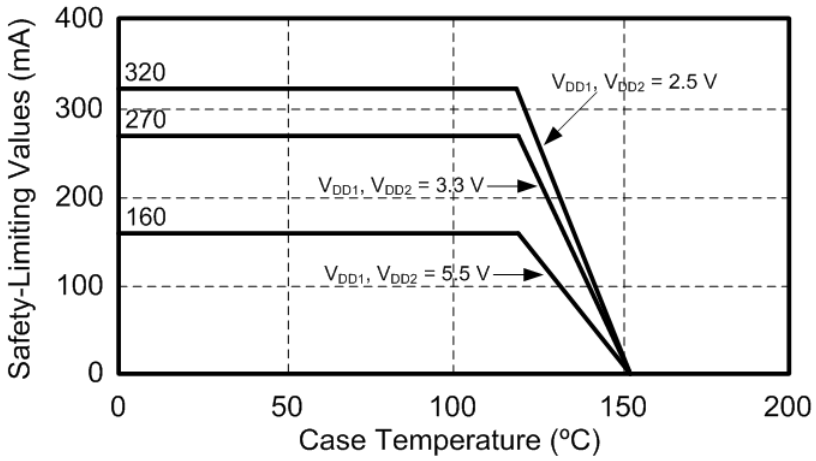


Figure 4.4. (SOIC-8) Thermal Derating Curve for Safety Limiting Current

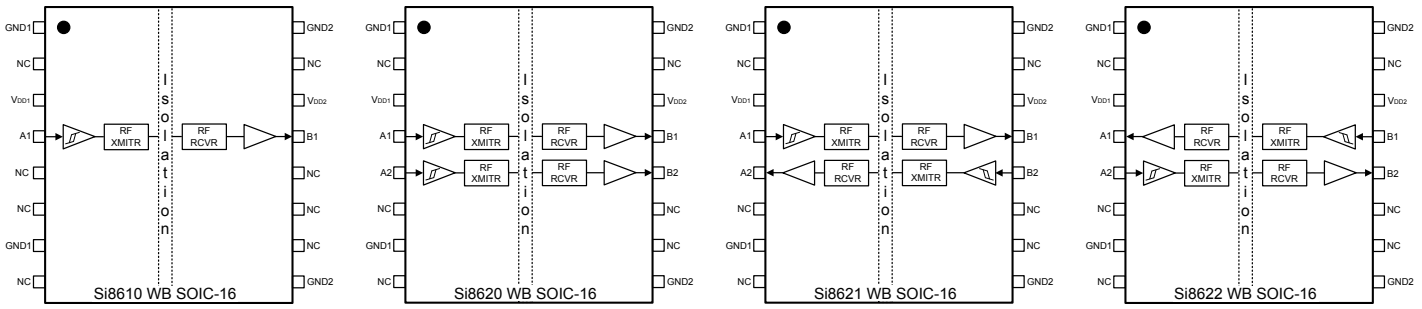
Table 4.11. Absolute Maximum Ratings[1]

Parameter	Symbol	Min	Max	Unit
Storage Temperature[2]	T_{STG}	–65	150	°C
Operating Temperature	T_A	–40	125	°C
Junction Temperature	T_J	—	150	°C
Supply Voltage	V_{DD1}, V_{DD2}	–0.5	7.0	V
Input Voltage	V_I	–0.5	V_{DD} + 0.5	V
Output Voltage	V_O	–0.5	V_{DD} + 0.5	V
Output Current Drive Channel	I_O	—	10	mA
Lead Solder Temperature (10 s)		—	260	°C
Maximum Isolation (Input to Output) (1 sec) SOIC-8 & DFN-8		—	4500	V_{RMS}
Maximum Isolation (Input to Output) (1 sec) WB SOIC-16		—	6500	V_{RMS}

Note:

1. Permanent device damage may occur if the absolute maximum ratings are exceeded. Functional operation should be restricted to conditions as specified in the operational sections of this data sheet. Exposure to absolute maximum ratings for exteneded periods may degrade performance.
2. VDE certifies storage temperature from –40 to 150 °C.

5. Pin Descriptions (WB SOIC-16)

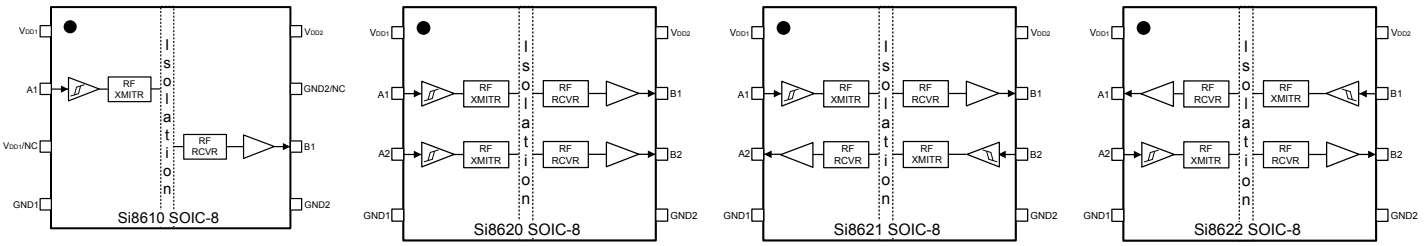


Name	WB SOIC-16 Pin# Si8610	WB SOIC-16 Pin# Si862x	Type	Description
GND1	1	1	Ground	Side 1 ground.
NC[1]	2, 5, 6, 8,10, 11, 12, 15	2, 6, 8,10, 11, 15	No Connect	NC
V_{DD1}	3	3	Supply	Side 1 power supply.
A1	4	4	Digital I/O	Side 1 digital input or output.
A2	NC	5	Digital I/O	Side 1 digital input or output.
GND1	7	7	Ground	Side 1 ground.
GND2	9	9	Ground	Side 2 ground.
B2	NC	12	Digital I/O	Side 2 digital input or output.
B1	13	13	Digital I/O	Side 2 digital input or output.
V_{DD2}	14	14	Supply	Side 2 power supply.
GND2	16	16	Ground	Side 2 ground.

Note:

1. No Connect. These pins are not internally connected. They can be left floating, tied to V_{DD}, or tied to GND.

6. Pin Descriptions (SOIC-8)

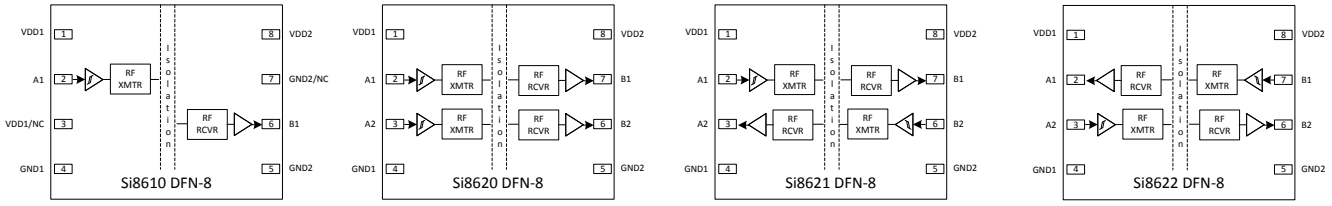


Name	SOIC-8 Pin# Si861x	SOIC-8 Pin# Si862x	Type	Description
V_{DD1}/NC[1]	1, 3	1	Supply	Side 1 power supply.
GND1	4	4	Ground	Side 1 ground.
A1	2	2	Digital I/O	Side 1 digital input or output.
A2	NA	3	Digital I/O	Side 1 digital input or output.
B1	6	7	Digital I/O	Side 2 digital input or output.
B2	NA	6	Digital I/O	Side 2 digital input or output.
V_{DD2}	8	8	Supply	Side 2 power supply.
GND2/NC[1]	5.7	5	Ground	Side 2 ground.

Note:

1. No connect. These pins are not internally connected. They can be left floating, tied to VDD, or tied to GND.

7. Pin Descriptions (DFN-8)



Name	DFN-8 Pin# Si861x	DFN-8 Pin# Si862x	Type	Description
V_{DD1}/NC[1]	1, 3	1	Supply	Side 1 power supply.
GND1	4	4	Ground	Side 1 ground.
A1	2	2	Digital I/O	Side 1 digital input or output.
A2	NA	3	Digital I/O	Side 1 digital input or output.
B1	6	7	Digital I/O	Side 2 digital input or output.
B2	NA	6	Digital I/O	Side 2 digital input or output.
V_{DD2}	8	8	Supply	Side 2 power supply.
GND2/NC[1]	5.7	5	Ground	Side 2 ground.

Note:

1. No connect. These pins are not internally connected. They can be left floating, tied to VDD, or tied to GND.

8. Package Outline: WB SOIC-16

The figure below illustrates the package details for the Triple-Channel Digital Isolator. The table lists the values for the dimensions shown in the illustration.

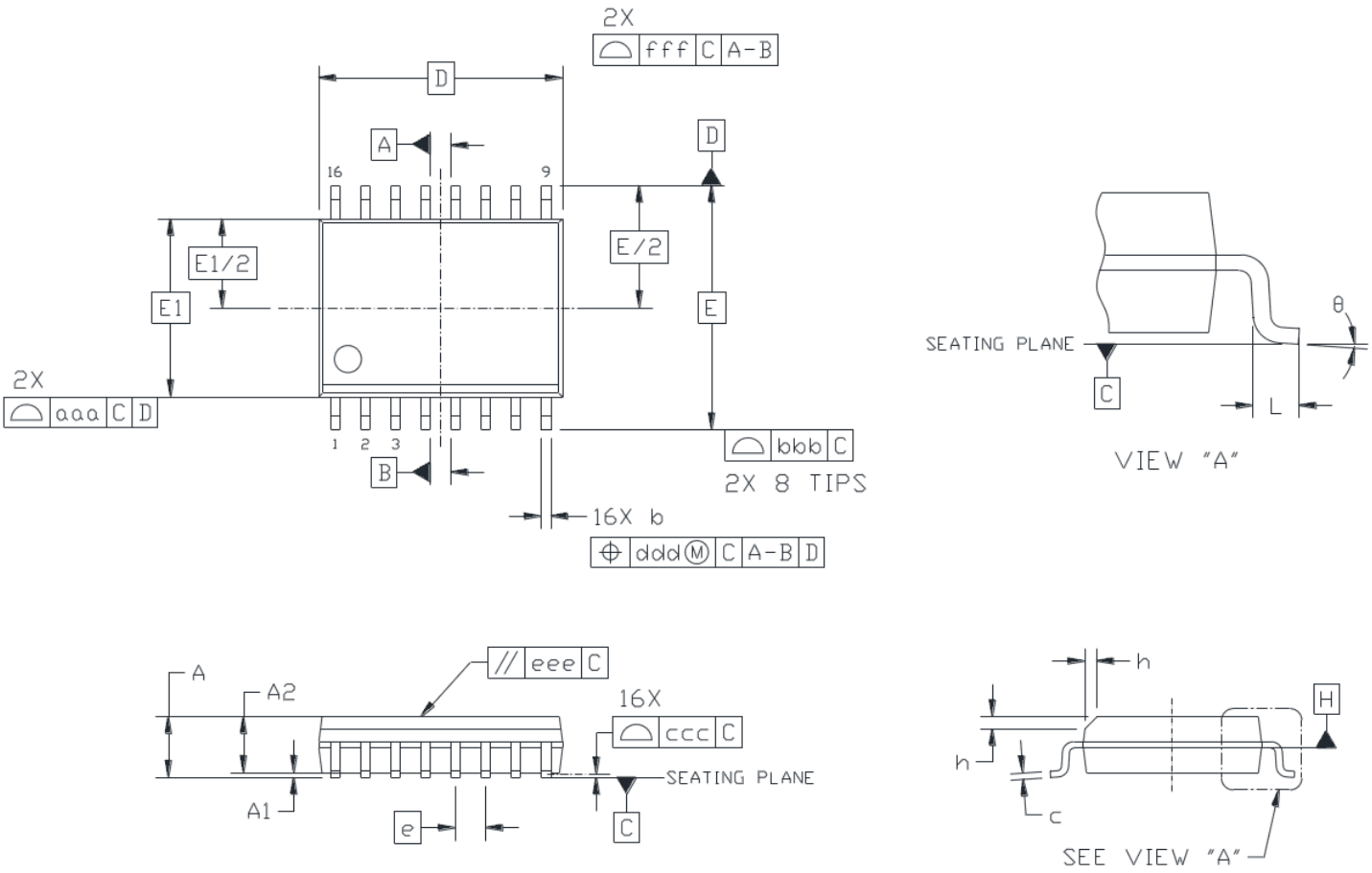


Figure 8.1. WB SOIC-16

Table 8.1. WB SOIC-16 Package Diagram Dimensions[1, 2, 3, 4]

Dimension	Min	Max
A	—	2.65
A1	0.10	0.30
A2	2.05	—
b	0.31	0.51
c	0.20	0.33
D	10.30 BSC	
E	10.30 BSC	
E1	7.50 BSC	
e	1.27 BSC	
L	0.40	1.27
h	0.25	0.75
θ	0°	8°
aaa	—	0.10
bbb	—	0.33
ccc	—	0.10
ddd	—	0.25
eee	—	0.10
fff	—	0.20

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC Outline MS-013, Variation AA.
4. Recommended reflow profile per JEDEC J-STD-020 specification for small body, lead-free components.

9. Land Pattern: WB SOIC-16

The figure below illustrates the recommended land pattern details for the Si861x/2x in a WB SOIC-16 package. The table lists the values for the dimensions shown in the illustration.

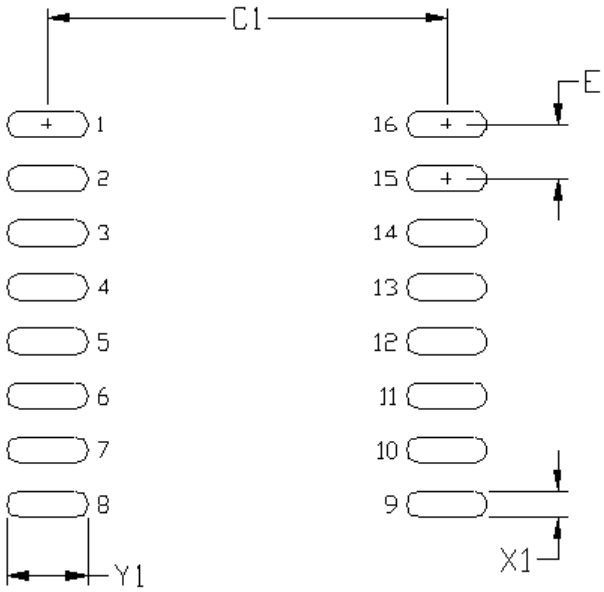


Figure 9.1. PCB Land Pattern: WB SOIC-16

Table 9.1. WB SOIC-16 Land Pattern Dimensions[1, 2]

Dimension	Feature	(mm)
C1	Pad Column Spacing	9.40
E	Pad Row Pitch	1.27
X1	Pad Width	0.60
Y1	Pad Length	1.90

Note:

1. This Land Pattern Design is based on IPC-7351 pattern SOIC127P1032X265-16AN for Density Level B (Median Land Protrusion).
2. All feature sizes shown are at Maximum Material Condition (MMC) and a card fabrication tolerance of 0.05 mm is assumed.

10. Package Outline: SOIC-8

The figure below illustrates the package details for the Si86xx. The table lists the values for the dimensions shown in the illustration.

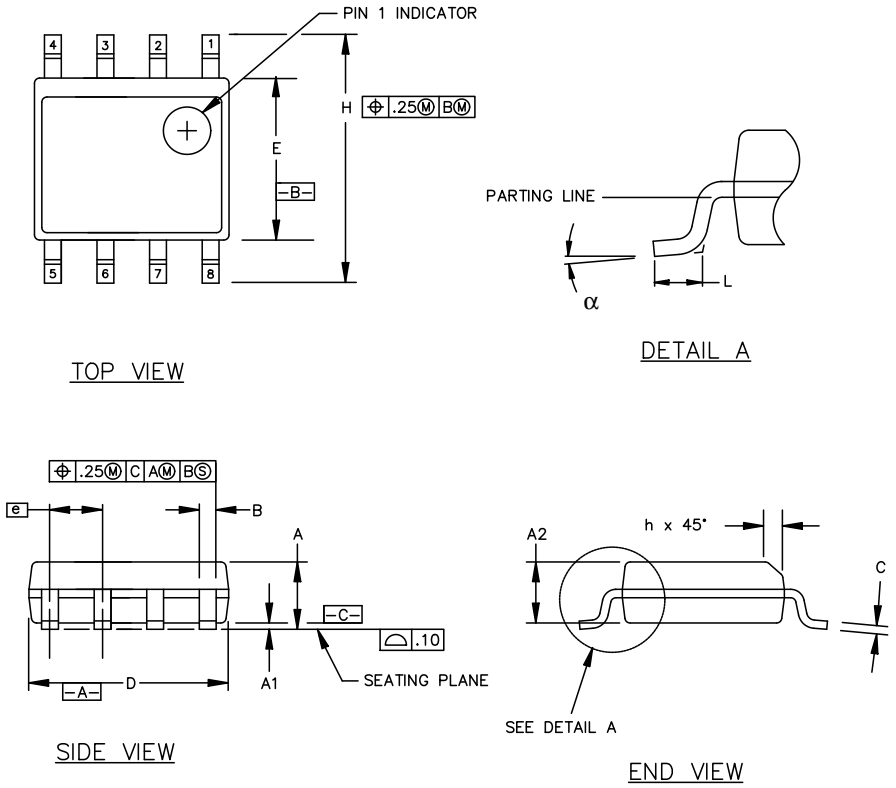


Figure 10.1. SOIC-8 Package

Table 10.1. SOIC-8 Package Diagram Dimensions

Symbol	Millimeters	
	Min	Max
A	1.35	1.75
A1	0.10	0.25
A2	1.40 REF	1.55 REF
B	0.33	0.51
C	0.19	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.27
m	0°	8°

11. Land Pattern: SOIC-8

The figure below illustrates the recommended land pattern details for the Si86xx in a SOIC-8. The table lists the values for the dimensions shown in the illustration.

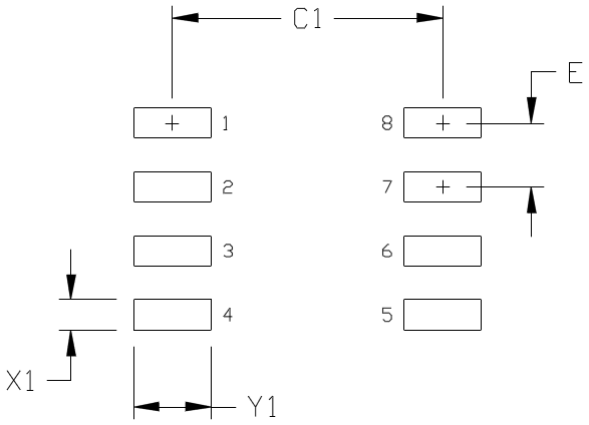


Figure 11.1. PCB Land Pattern: SOIC-8

Table 11.1. SOIC-8 Land Pattern Dimensions[1, 2]

Dimension	Feature	(mm)
C1	Pad Column Spacing	5.40
E	Pad Row Pitch	1.27
X1	Pad Width	0.60
Y1	Pad Length	1.55

Note:

1. This Land Pattern Design is based on IPC-7351 pattern SOIC127P600X173-8N for Density Level B (Median Land Protrusion).
2. All feature sizes shown are at Maximum Material Condition (MMC) and a card fabrication tolerance of 0.05 mm is assumed.

12. Package Outline: DFN-8

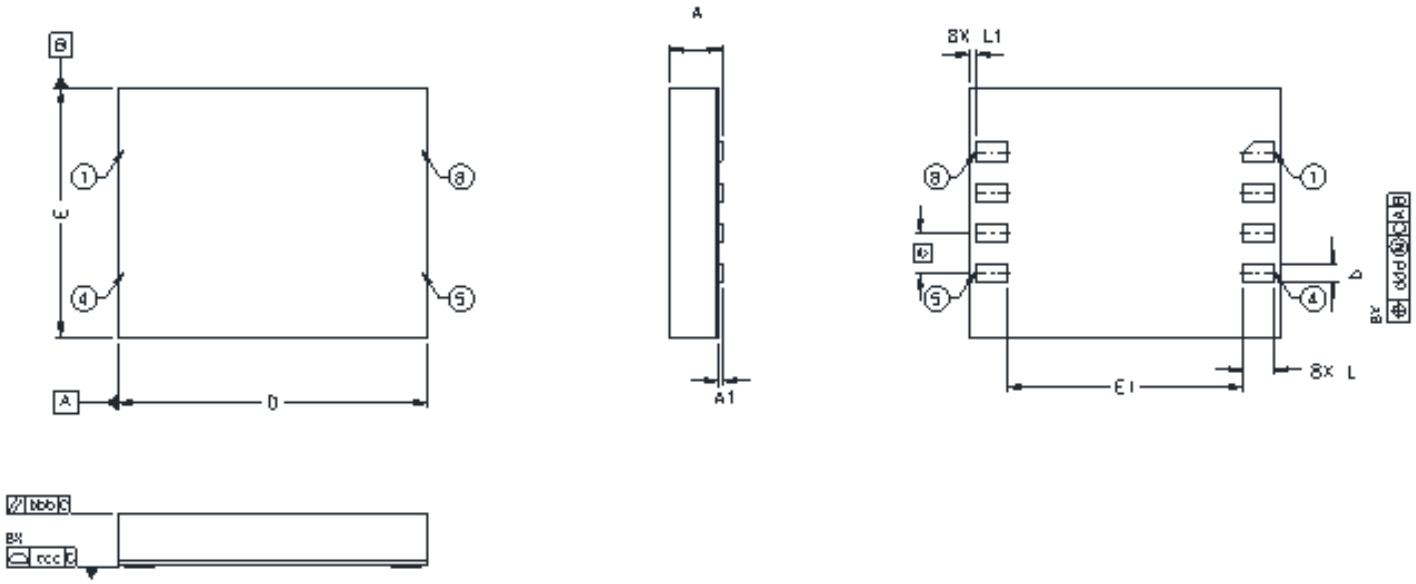


Figure 12.1. DFN-8 Package Outline

Dimension	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	0	--	0.05
b	0.25	0.30	0.35
D	4.90	5.00	5.10
e		0.65 BSC	
E	3.90	4.00	4.10
E1		3.80 REF	
L	0.45	0.50	0.55
L1	0.05	0.10	0.15
bbb	--	--	0.10
ccc	--	--	0.08
ddd	--	--	0.10

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.

13. Land Pattern: DFN-8

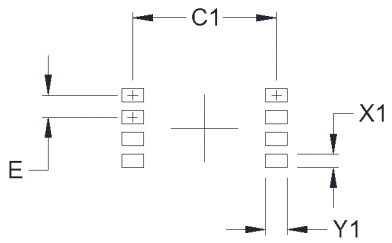


Figure 13.1. PCB Land Pattern: DFN-8

Table 13.1. DFN-8 Land Pattern Dimensions

Dimension	mm
C1	4.30
E	0.65
X1	0.65
Y1	0.40

Note:

General

1. All dimensions shown are in millimeters (mm).
2. This Land Pattern Design is based on the IPC-7351 guidelines.
3. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

Solder Mask Design

1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 mm minimum, all the way around the pad.

Stencil Design

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1.

Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020D specification for Small Body Components.

14. Top Marking: WB SOIC-16

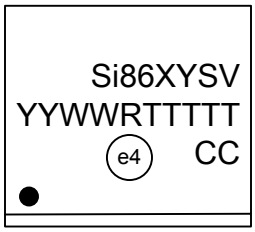


Figure 14.1. WB SOIC-16 Top Marking

Table 14.1. WB SOIC-16 Top Marking Explanation

Line 1 Marking:	Base Part Number Ordering Options (See Ordering Guide for more information.)	Si86 = Isolator product series X = # of data channels (2, 1) Y = # of reverse channels (2, 1, 0)[1] S = Speed Grade (max data rate) and operating mode: B = 150 Mbps (default output = low) E = 150 Mbps (default output = high) V = Insulation rating B = 2.5 kV; C = 3.75 kV; D = 5.0 kV; T = 5.0 kV with 10 kV surge capability.
Line 2 Marking:	YY = Year WW = Workweek	Assigned by assembly subcontractor. Corresponds to the year and workweek of the mold date.
	RTTTTT = Mfg Code	Manufacturing code from assembly house “R” indicates revision
Line 3 Marking:	Circle = 1.7 mm Diameter (Center-Justified)	“e4” Pb-Free Symbol
	Country of Origin ISO Code Abbreviation	CC = Country of Origin ISO Code Abbreviation • TW = Taiwan • TH = Thailand

Note:

1. The Si8622 has 1 forward and 1 reverse channel, but directionality is reversed compared to the Si8621, as shown in 5. Pin Descriptions (WB SOIC-16) and 6. Pin Descriptions (SOIC-8)

15. Top Marking: SOIC-8

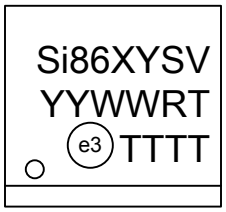


Figure 15.1. SOIC-8 Top Marking

Table 15.1. SOIC-8 Top Marking Explanation

Line 1 Marking:	Base Part Number Ordering Options (See Ordering Guide for more information).	Si86 = Isolator Product Series XY = Channel Configuration S = Speed Grade (max data rate) V = Insulation rating
Line 2 Marking:	YY = Year WW = Workweek	Assigned by assembly subcontractor. Corresponds to the year and workweek of the mold date.
	R = Product (OPN) Revision T = First character of the manufacturing code	First two characters of the manufacturing code from Assembly.
Line 3 Marking:	Circle = 1.1 mm Diameter	“e3” Pb-Free Symbol.
	TTTT = Last four characters of the manufacturing code	Last four characters of the manufacturing code.

Note:

1. The Si8622 has 1 forward and 1 reverse channel, but directionality is reversed compared to the Si8621, as shown in 5. Pin Descriptions (WB SOIC-16) and 6. Pin Descriptions (SOIC-8)

16. Top Marking: DFN-8

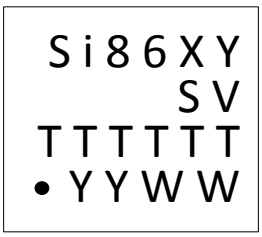


Figure 16.1. DFN-8 Top Marking

Line 1 Marking	Base Part Number Ordering Options (See Ordering Guide for more information).	Si86 = Isolator Product Series XY = Channel Configuration
Line 2 Marking	Ordering Options	S = Default High or Low Option V = Insulation Rating
Line 3 Marking	Manufacturing code	
Line 4 Marking	YY = Year WW = Workweek	Assigned by assembly subcontractor. Corresponds to the year and workweek of the mold date.
Note: The Si8622 has 1 forward and 1 reverse channel, but directionality is reversed as compared to Si8621, as shown in Pin Descriptions sections.		

17. Revision History

Revision 1.76

December 2020
- Added DFN-8 package option
- Corrected typos in VT+, VT- and VHYS (HYS is subscript) values in Table 4.4
- Standardized package designations across document

Revision 1.75

September 2019
- Updated the Ordering Guide.

Revision 1.74

October 2018
- Updated the Ordering Guide for Automotive-Grade OPN options.

Revision 1.73

May 2018
- Updated the Ordering Guide for Automotive-Grade OPN options.

Revision 1.72

April 2018
- Added Si8610ED-AS to Ordering Guide for Automotive-Grade OPN options.

Revision 1.71
- Added new table to Ordering Guide for Automotive-Grade OPN options.

Revision 1.7
- Added following note to 1. Ordering Guide: "An 'R' at the end of the part number denotes tape and reel packaging option."

Revision 1.6
- Added product options Si862xxT in 1. Ordering Guide.
- Added spec line items for Input Leakage Current pertaining to Si862xxT in 4. Electrical Specifications.
- Updated IEC 60747-5-2 to IEC 60747-5-5 in all instances in document.

Revision 1.5
- Updated Table 5 on page 17.
  - Added CQC certificate numbers.
- Updated "5. Ordering Guide" on page 11.
  - Removed references to moisture sensitivity levels.
  - Removed Note 2.

Revision 1.4
- Added Figure 2, “Common Mode Transient Immunity Test Circuit,” on page 8.
- Added references to CQC throughout.
- Added references to 2.5 kV_{RMS} devices throughout.
- Updated "5. Ordering Guide" on page 11.
- Updated "10.1. WB SOIC-16 Top Marking" on page 18.

Revision 1.3

- Updated Table 11 on page 21.
  - Added junction temperature spec.
- Updated "2.3.1. Supply Bypass" on page 6.
- Removed “3.3.2. Pin Connections” on page 22.
- Updated "5. Ordering Guide" on page 11.
  - Removed Rev A devices.
- Updated "6. Package Outline: WB SOIC-16" on page 13.
- Updated Top Marks.
  - Added revision description.

Revision 1.2

- Updated Table 1 on page 4.
  - Deleted reference to EN.
- Updated "5. Ordering Guide" on page 11 to include MSL2A.

Revision 1.1

- Updated High Level Output Voltage VOH to 3.1 V in Table 3, “Electrical Characteristics,” on page 9.
- Updated High Level Output Voltage VOH to 2.3 V in Table 4, “Electrical Characteristics,” on page 13.

Revision 1.0

- Updated “Table 3. Electrical Characteristics”.
- Reordered spec tables to conform to new convention.
- Removed “pending” throughout document.

Revision 0.3

- Added chip graphics on page 1.
- Updated Table 6, “Insulation and Safety-Related Specifications,” on page 18.
- Updated Table 8, “IEC 60747-5-5 Insulation Characteristics for Si86xxxx*,” on page 19.
- Updated "3. Pin Descriptions (WB SOIC-16)" on page 9.
- Updated "4. Pin Descriptions (SOIC-8)" on page 10.
- Updated "5. Ordering Guide" on page 11.

Revision 0.2

- Added chip graphics on page 1.
- Moved Tables 1 and 11 to page 21.
- Updated Table 6, “Insulation and Safety-Related Specifications,” on page 18.
- Updated Table 8, “IEC 60747-5-5 Insulation Characteristics for Si86xxxx*,” on page 19.
- Moved Table 1 to page 4.
- Moved “Typical Performance Characteristics” to page 7.
- Updated "3. Pin Descriptions (WB SOIC-16)" on page 9.
- Updated "4. Pin Descriptions (SOIC-8)" on page 10.
- Updated "5. Ordering Guide" on page 11.

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