System designers can add digital terrestrial radio capability in a simple and inexpensive way through the SAF3560. The SAF3560 decodes digital radio input to provide digital audio and also processes digital data. Multiple interfaces give flexibility while integrating the SAF3560 into the receiver system.

2. Features and benefits

2.1 HD Radio technology

- HD Radio signal decoding for AM and FM digital audio
- Dual HD Radio support for support of second station for background scanning and data service
- Front end to baseband interface support through serial baseband I^2S-bus type interface
- Secondary baseband interface for dual tuner applications
- Metadata support for HD Radio reception
- Data services support for HD Radio reception
- Advanced HD Radio feature support, such as[1]:
  - Conditional Access (CA)
  - Store and replay
  - Apple ID3 tag
  - Multicasting
  - Electronic Program Guide (EPG)

2.2 Digital audio

- Up to 6 channel (5.1) audio support through I^2S-bus serial audio interface
- Optional SRC (8 kHz to 48 kHz) for up to 6 channels of I^2S-bus audio output
- I^2S-bus serial audio input for auxiliary processing
- Optional SRC (8 kHz to 48 kHz) for I^2S-bus input
- Optional restricted support for 96 kHz input and output sample-rate conversion
- Optional digital audio output through S/PDIF (without SRC)
- Basic audio processing for external digital audio sources
- Advanced audio processing (contact NXP Semiconductors for a list of supported audio processing features: Section 14 “Contact information”)

2.3 Memory

- Supports SDR-SDRAM controller (up to 512 Mbit in 16-bit configuration)
- Supports serial NOR-Flash memory with various sizes depending on the actual application

1. Contact NXP Semiconductors for a detailed list of supported feature sets: Section 14 “Contact information”.

2.4 Other peripheral interfaces

- Two I^2C-bus interfaces
- Three Serial Peripheral Interfaces (SPI)
- One UART interface
- Five individual GPIO pins for applications and diagnostics
- One JTAG interface for diagnostics

2.5 Miscellaneous

- One internal clock oscillator and two internal Phase-Locked Loops (PLL)
- Can run on external crystal or reference clock from an external IC
- Powerful signal and audio processing core architecture
- Qualified in accordance with *AEC-Q100*

3. Quick reference data

Table 1. Power supply characteristics

After power-up the SAF3560 needs a reset pulse for at least 2 ms.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Supply voltages							
$V_{DDA(OSC)(1V2)}$	oscillator analog supply voltage (1.2 V)			1.14	1.2	1.32	V
$V_{DDA(PLL)(1V2)}$	PLL analog supply voltage (1.2 V)			1.14	1.2	1.32	V
$V_{DDD(C)(1V2)}$	core digital supply voltage (1.2 V)			1.14	1.2	1.32	V
$V_{DDD(GP)(3V3)}$	general purpose digital supply voltage (3.3 V)			3.0	3.3	3.6	V
$V_{DDD(DSP)(3V3)}$	DSP digital supply voltage (3.3 V)			3.0	3.3	3.6	V
$V_{DDD(JTAG)(3V3)}$	JTAG digital supply voltage (3.3 V)			3.0	3.3	3.6	V
$V_{DDD(MC)(3V3)}$	microcontroller digital supply voltage (3.3 V)			3.0	3.3	3.6	V
$V_{DDD(MEM)(1V2)}$	memory digital supply voltage (1.2 V)			1.14	1.2	1.32	V
$V_{DDD(SDRAM)(3V3)}$	SDRAM digital supply voltage (3.3 V)			3.0	3.3	3.6	V
Supply currents							
I_{DD}	supply current	all core related blocks	[1]	-	90	116	mA
		all I/O related blocks	[2]	-	28	37	mA
Power dissipation							
P_{tot}	total power dissipation			-	0.2	0.5	W

[1] Through pins $V_{DDA(OSC)(1V2)}$, $V_{DDA(PLL)(1V2)}$, $V_{DDD(C)(1V2)}$ and $V_{DDD(MEM)(1V2)}$.

[2] Through pins $V_{DDD(GP)(3V3)}$, $V_{DDD(DSP)(3V3)}$, $V_{DDD(JTAG)(3V3)}$, $V_{DDD(MC)(3V3)}$ and $V_{DDD(SDRAM)(3V3)}$.

4. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
SAF3560HV/V110x	HLQFP144	plastic thermal enhanced low profile quad flat package; 144 leads; body 20 × 20 × 1.4 mm; exposed die pad	SOT612-4
SAF3560EL/V110x	LFBGA170	plastic low profile fine pitch ball grid array package; 170 balls	SOT1315-1

Table 3. Subtypes and main applications

Type number	Main application	Option	HLQFP144	LFBGA170
SAF3560xx/V1100	HD Radio 1.0, supporting external clock from NXP radio/audio DSPs[1]	single tuner	yes	yes
SAF3560xx/V1101	HD Radio 1.0 + Conditional Access (CA)	single tuner	yes	no
SAF3560xx/V1102	HD Radio 1.5, supporting external clock from NXP radio/audio DSPs[1]	dual tuner	yes	yes
SAF3560xx/V1103	HD Radio 1.5 + Conditional Access (CA)	dual tuner	yes	no
SAF3560xx/V1104	HD Radio 1.0 + Conditional Access (CA), supporting external clock from NXP radio/audio DSPs[1]	single tuner	yes	yes
SAF3560xx/V1105	HD Radio 1.5 + Conditional Access (CA), supporting external clock from NXP radio/audio DSPs[1]	dual tuner	yes	yes

[1] Contact NXP Sales regarding supported radio/audio DSPs: Section 14 “Contact information”.

5. Block diagram

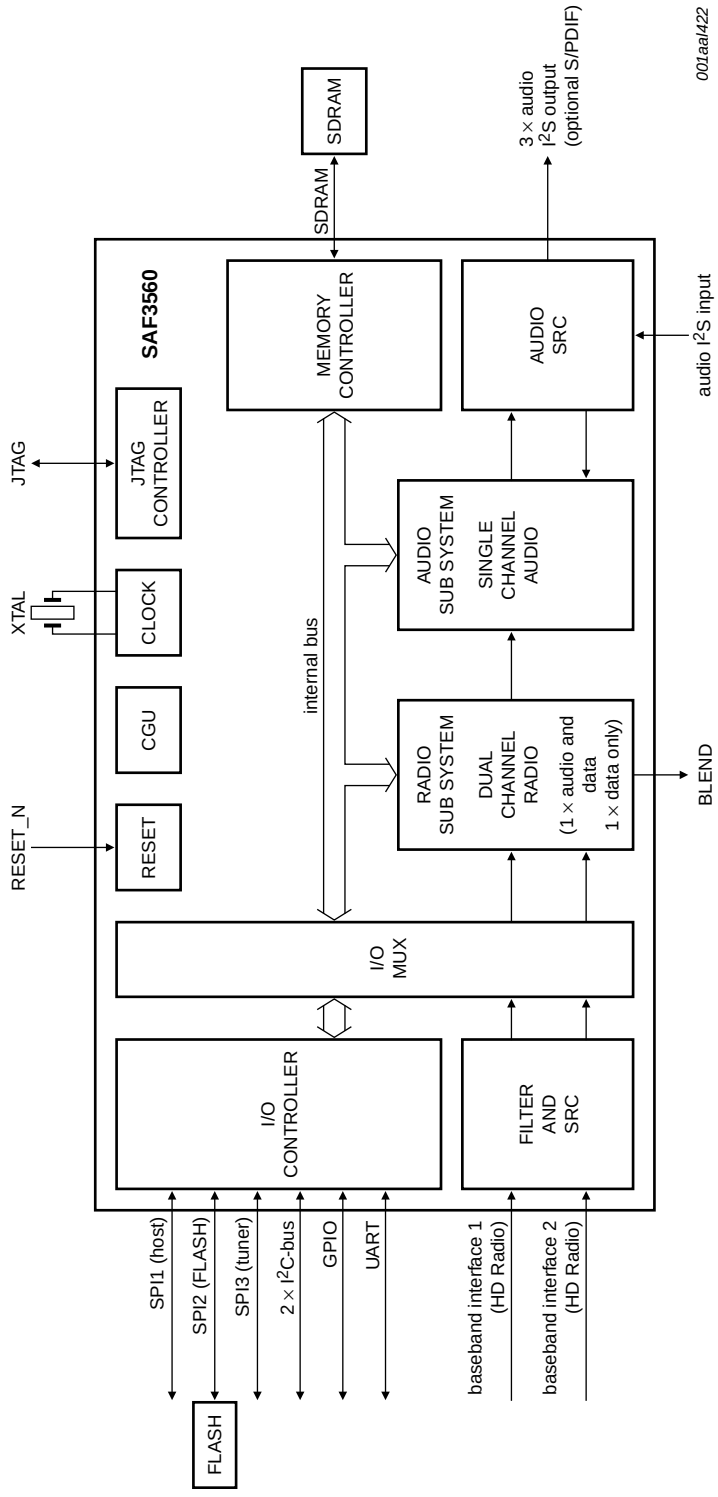


Fig 2. Block diagram of SAF3560

6. Pinning information

6.1 Pinning

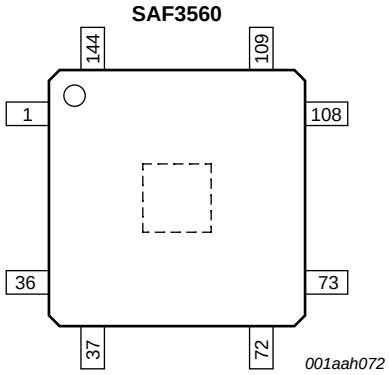


Fig 3. Pin configuration (HLQFP144)

Table 4. Pin allocation table (HLQFP144)

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	CLKOUT	2	RESET_N	3	I2C1_SCL	4	I2C1_SDA
5	I2C1_DA	6	$V_{DDD(MC)(3V3)}$	7	I2C2_SCL	8	I2C2_SDA
9	I2C2_DA	10	SPI1_SO	11	SPI1_SI	12	SPI1_SCLK
13	SPI1_SS_N	14	$V_{DDD(C)(1V2)}$	15	$V_{DDD(MC)(3V3)}$	16	SPI2_MI
17	SPI2_MO	18	SPI2_SCLK	19	SPI2_SS1_N	20	SPI2_SS2_N
21	$V_{DDD(MC)(3V3)}$	22	SPI2_SS3_N	23	SPI2_SS4_N	24	UART_TD
25	UART_RD	26	UART_RTS	27	$V_{DDD(C)(1V2)}$	28	$V_{DDD(MC)(3V3)}$
29	UART_CTS	30	SPI3_MISO	31	SPI3_MOSI	32	SPI3_SCLK
33	SPI3_SS1_N	34	$V_{DDD(GP)(3V3)}$	35	SPI3_SS2_N	36	GPIO0
37	GPIO1	38	GPIO2	39	GPIO3	40	GPIO4
41	-[1]	42	$V_{DDD(GP)(3V3)}$	43	-	44	-
45	-	46	-	47	-	48	-
49	-	50	-	51	-	52	-
53	-	54	-	55	BB1_I2S_BCK	56	BB1_I2S_WS
57	BB1_I2S_I	58	BB1_I2S_Q	59	BB2_I2S_BCK	60	BB2_I2S_WS
61	BB2_I2S_I	62	BB2_I2S_Q	63	$V_{DDD(C)(1V2)}$	64	$V_{DDD(DSP)(3V3)}$
65	HBCKOUT	66	I2S1_O_BCK	67	I2S1_O_WS	68	I2S1_O_SD
69	BLEND	70	$V_{DDD(MEM)(1V2)}$	71	$V_{DDD(DSP)(3V3)}$	72	I2S2_O_SD
73	I2S3_O_SD/ SPDIF_O	74	I2S_I_WS	75	I2S_I_BCK	76	I2S_I_SD
77	SDRAM_DIO0	78	SDRAM_DIO1	79	SDRAM_DIO2	80	$V_{DDD(SDRAM)(3V3)}$
81	SDRAM_DIO3	82	SDRAM_DIO4	83	SDRAM_DIO5	84	SDRAM_DIO6
85	$V_{DDD(SDRAM)(3V3)}$	86	SDRAM_DIO7	87	SDRAM_DIO8	88	SDRAM_DIO9
89	SDRAM_DIO10	90	$V_{DDD(SDRAM)(3V3)}$	91	$V_{DDD(C)(1V2)}$	92	SDRAM_DIO11

Table 4. Pin allocation table (HLQFP144) *...continued*

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
93	SDRAM_DIO12	94	SDRAM_DIO13	95	SDRAM_DIO14	96	$V_{DDD(SDRAM)(3V3)}$
97	SDRAM_DIO15	98	SDRAM_WE_N	99	SDRAM_DQM0	100	SDRAM_DQM1
101	$V_{DDD(SDRAM)(3V3)}$	102	$V_{DDD(MEM)(1V2)}$	103	SDRAM_BA0	104	SDRAM_BA1
105	SDRAM_CS_N	106	SDRAM_RAS_N	107	$V_{DDD(SDRAM)(3V3)}$	108	SDRAM_CAS_N
109	SDRAM_CLKE	110	SDRAM_AO0	111	SDRAM_AO1	112	$V_{DDD(SDRAM)(3V3)}$
113	SDRAM_AO2	114	SDRAM_AO3	115	SDRAM_AO4	116	$V_{DDD(SDRAM)(3V3)}$
117	SDRAM_AO5	118	SDRAM_AO6	119	SDRAM_AO7	120	SDRAM_AO8
121	SDRAM_AO9	122	$V_{DDD(SDRAM)(3V3)}$	123	SDRAM_AO10	124	$V_{DDD(C)(1V2)}$
125	SDRAM_AO11	126	SDRAM_AO12	127	SDRAM_CLK	128	SDRAM_CLKIN
129	$V_{DDD(SDRAM)(3V3)}$	130	V_{SS}[2]	131	TRST_N	132	TCK
133	TMS	134	$V_{DDD(C)(1V2)}$	135	TDI	136	TDO
137	V_{SS}[2]	138	$V_{DDD(JTAG)(3V3)}$	139	$V_{DDA(PLL)(1V2)}$	140	$V_{DDA(OSC)(1V2)}$
141	XTALI	142	XTALO	143	$V_{DDD(MEM)(1V2)}$	144	V_{SS}[2]

[1] See Table 15 for unused pins.

[2] Global V_{SS} pin at backside contact.

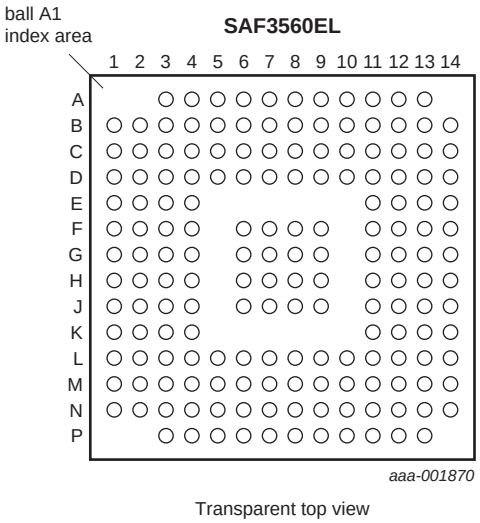


Fig 4. Pin configuration (LFBGA170)

Table 5. Pin allocation table (LFBGA170)

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
Row A							
A3	XTALI	A4	XTALO	A5	$V_{DDA(PLL)(1V2)}$	A6	TDI
A7	SDRAM_CLKIN	A8	SDRAM_CLK	A9	$V_{DDD(C)(1V2)}$	A10	SDRAM_AO8
A11	SDRAM_AO5	A12	$V_{DDD(SDRAM)(3V3)}$	A13	SDRAM_AO4		

Table 5. Pin allocation table (LFBGA170)

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
Row B							
B1	RESET_N	B2	CLKOUT	B3	$V_{DDD(MEM)(1V2)}$	B4	V_{SS}
B5	$V_{DDD(JTAG)(3V3)}$	B6	$V_{DDD(C)(1V2)}$	B7	TRST_N	B8	V_{SS}
B9	SDRAM_AO10	B10	SDRAM_AO7	B11	V_{SS}	B12	SDRAM_AO3
B13	SDRAM_AO2	B14	$V_{DDD(SDRAM)(3V3)}$				
Row C							
C1	I2C1_DA	C2	I2C1_SDA	C3	I2C1_SCL	C4	$V_{DDA(OSC)(1V2)}$
C5	V_{SS}	C6	TMS	C7	V_{SS}	C8	SDRAM_AO12
C9	$V_{DDD(SDRAM)(3V3)}$	C10	V_{SS}	C11	SDRAM_AO1	C12	SDRAM_AO0
C13	V_{SS}	C14	SDRAM_CLKE				
Row D							
D1	I2C2_DA	D2	I2C2_SDA	D3	I2C2_SCL	D4	$V_{DDD(MC)(3V3)}$
D5	TDO	D6	TCK	D7	$V_{DDD(SDRAM)(3V3)}$	D8	SDRAM_AO11
D9	SDRAM_AO9	D10	SDRAM_AO6	D11	SDRAM_CS_N	D12	SDRAM_RAS_N
D13	$V_{DDD(SDRAM)(3V3)}$	D14	SDRAM_CAS_N				
Row E							
E1	SPI1_SS_N	E2	SPI1_SCLK	E3	SPI1_SI	E4	SPI1_SO
E11	$V_{DDD(MEM)(1V2)}$	E12	SDRAM_BA0	E13	SDRAM_BA1	E14	V_{SS}
Row F							
F1	SPI2_SCLK	F2	SPI2_MO	F3	SPI2_MI	F4	$V_{DDD(C)(1V2)}$
F6	V_{SS}	F7	V_{SS}	F8	V_{SS}	F9	V_{SS}
F11	V_{SS}	F12	SDRAM_DIO14	F13	SDRAM_DQM1	F14	$V_{DDD(SDRAM)(3V3)}$
Row G							
G1	SPI2_SS4_N	G2	SPI2_SS3_N	G3	SPI2_SS2_N	G4	SPI2_SS1_N
G6	V_{SS}	G7	V_{SS}	G8	V_{SS}	G9	V_{SS}
G11	SDRAM_DQM0	G12	$V_{DDD(SDRAM)(3V3)}$	G13	SDRAM_DIO15	G14	SDRAM_DIO11
Row H							
H1	UART_CTS	H2	UART_RTS	H3	UART_RD	H4	UART_TD
H6	V_{SS}	H7	V_{SS}	H8	V_{SS}	H9	V_{SS}
H11	SDRAM_WE_N	H12	SDRAM_DIO12	H13	V_{SS}	H14	SDRAM_DIO13
Row J							
J1	$V_{DDD(C)(1V2)}$	J2	$V_{DDD(MC)(3V3)}$	J3	$V_{DDD(MC)(3V3)}$	J4	$V_{DDD(MC)(3V3)}$
J6	V_{SS}	J7	V_{SS}	J8	V_{SS}	J9	V_{SS}
J11	V_{SS}	J12	SDRAM_DIO10	J13	$V_{DDD(SDRAM)(3V3)}$	J14	$V_{DDD(C)(1V2)}$
Row K							
K1	SPI3_SS1_N	K2	SPI3_SCLK	K3	SPI3_MOSI	K4	SPI3_MISO
K11	I2S_I_SD	K12	$V_{DDD(SDRAM)(3V3)}$	K13	SDRAM_DIO6	K14	SDRAM_DIO9

Table 5. Pin allocation table (LFBGA170)

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
Row L							
L1	GPIO0	L2	GPIO1	L3	$V_{DDD(GP)(3V3)}$	L4	SPI3_SS2_N
L5	-[1]	L6	-	L7	BB1_I2S_BCK	L8	BB2_I2S_BCK
L9	BLEND	L10	$V_{DDD(DSP)(3V3)}$	L11	I2S_I_BCK	L12	SDRAM_DIO2
L13	SDRAM_DIO5	L14	SDRAM_DIO8				
Row M							
M1	$V_{DDD(GP)(3V3)}$	M2	GPIO2	M3	GPIO3	M4	GPIO4
M5	-	M6	-	M7	BB1_I2S_WS	M8	BB2_I2S_WS
M9	I2S1_O_WS	M10	HBCKOUT	M11	I2S_I_WS	M12	SDRAM_DIO1
M13	V_{SS}	M14	SDRAM_DIO7				
Row N							
N1	-	N2	-	N3	-	N4	-
N5	-	N6	-	N7	BB1_I2S_I	N8	BB2_I2S_I
N9	I2S1_O_SD	N10	$V_{DDD(MEM)(1V2)}$	N11	I2S3_O_SD/ SPDIF_O	N12	V_{SS}
N13	SDRAM_DIO4	N14	$V_{DDD(SDRAM)(3V3)}$				
Row P							
P3	-	P4	-	P5	-	P6	$V_{DDD(C)(1V2)}$
P7	BB1_I2S_Q	P8	BB2_I2S_Q	P9	I2S1_O_BCK	P10	$V_{DDD(DSP)(3V3)}$
P11	I2S2_O_SD	P12	SDRAM_DIO0	P13	SDRAM_DIO3		

[1] See Table 15 for unused pins.

6.2 Pin description

Table 6. Pin description overview

Pin category	Details	Table number
Power supply pins	analog and digital supply pins	Table 7
Baseband interface pins	baseband and audio pins (I^2S-bus)	Table 8
Generic interface pins	GPIO and SPI3 pins	Table 9
SDRAM interface pins	data, address and control pins	Table 10
Serial NOR-Flash interface pins	SPI2 pins	Table 11
External host microcontroller interface pins	SPI1, I2C1, I2C2, UART, CLKOUT and RESET_N pins	Table 12
JTAG interface pins	JTAG pins	Table 13
Crystal oscillator pins	XTALI and XTALO pins	Table 14

Table 7. Pin description (power supplies)

Symbol	Pin		Type[1]	Description
	HLQFP144	LFBGA170		
Global ground supply				
V_{SS}	130, 137, 144 and backside contact	B4, B8, B11, C5, C7, C10, C13, E14, F6 to F9, F11, G6 to G9, H6 to H9, H13, J6 to J9, J11, N12 and M13	G	analog and digital global ground supply
Analog supplies				
$V_{DDA(OSC)(1V2)}$	140	C4	P	oscillator analog supply voltage (1.2 V)
$V_{DDA(PLL)(1V2)}$	139	A5	P	PLL analog supply voltage (1.2 V)
Digital supplies				
$V_{DDD(C)(1V2)}$	14, 27, 63, 91, 124 and 134	A9, B6, F4, J1, J14 and P6	P	core digital supply voltage (1.2 V)
$V_{DDD(GP)(3V3)}$	34 and 42	L3 and M1	P	general purpose digital supply voltage (3.3 V)
$V_{DDD(DSP)(3V3)}$	64 and 71	L10 and P10	P	DSP digital supply voltage (3.3 V)
$V_{DDD(JTAG)(3V3)}$	138	B5	P	JTAG digital supply voltage (3.3 V)
$V_{DDD(MC)(3V3)}$	6, 15, 21 and 28	D4, J2, J3 and J4,	P	microcontroller digital supply voltage (3.3 V)
$V_{DDD(SDRAM)(3V3)}$	80, 85, 90, 96, 101, 107, 112, 116, 122 and 129	A12, B14, C9, D7, D13, F14, G12, J13, K12 and N14,	P	SDRAM digital supply voltage (3.3 V)
$V_{DDD(MEM)(1V2)}$	70, 102 and 143	B3, E11 and N10	P	memory digital supply voltage (1.2 V)

[1] Table 16 defines the pin type.

Table 8. Pin description (baseband interface)

Symbol	Pin		Type[1]	Description
	HLQFP144	LFBGA170		
Baseband interface				
BB1_I2S_BCK	55	L7	IOZU-H	bit clock input and output of first baseband interface
BB1_I2S_I	57	N7	IZU-H	I data input line of first baseband interface
BB1_I2S_Q	58	P7	IZU-H	Q data input line of first baseband interface
BB1_I2S_WS	56	M7	IOZU-H	word select input and output line of first baseband interface
BLEND	69	L9	OL	blend indicator output, HIGH = digital audio / LOW = analog radio[2]
BB2_I2S_BCK	59	L8	IOZU-H	bit clock input and output of second baseband interface
BB2_I2S_I	61	N8	IZU-H	I data input line of second baseband interface
BB2_I2S_Q	62	P8	IZU-H	Q data input line of second baseband interface
BB2_I2S_WS	60	M8	IOZU-H	word select input and output line of second baseband interface
Audio interface				
HBCKOUT	65	M10	IOZU	high-speed bit clock output[3]
I2S_I_BCK	75	L11	IOZU-H	bit clock input and output line of I^2S-bus input interface
I2S_I_SD	76	K11	IZU-H	serial data input line of I^2S-bus input interface
I2S_I_WS	74	M11	IOZU-H	word select input and output line of I^2S-bus input interface
I2S3_O_SD/ SPDIF_O	73	N11	OL	serial data output line of third I^2S-bus output interface; in alternative Sony/Philips digital output interface

Table 8. Pin description (baseband interface) *…continued*

Symbol	Pin		Type[1]	Description
	HLQFP144	LFBGA170		
I2S2_O_SD	72	P11	OL	serial data output line of second I^2S-bus output interface
I2S1_O_BCK	66	P9	IOZU-H	bit clock input and output line of first I^2S-bus output interface
I2S1_O_SD	68	N9	OL	serial data output line of first I^2S-bus output interface
I2S1_O_WS	67	M9	IOZU-H	word select input and output line of first I^2S-bus output interface

[1] Table 16 defines the pin type.

[2] Required for seamless switching between digital and analog AM/FM modes in HD Radio applications under bad reception conditions.

[3] $256 \times f_S$ output, required by some external DACs.

Table 9. Pin description (generic tuner interface)

Symbol	Pin		Type[1]	Description
	HLQFP144	LFBGA170		
GPIO interface				
GPIO4	40	M4	IOZU	general-purpose input and output port 4
GPIO3	39	M3	IOZU	general-purpose input and output port 3
GPIO2	38	M2	IOZU	general-purpose input and output port 2
GPIO1	37	L2	IOZU	general-purpose input and output port 1
GPIO0	36	L1	IOZU	general-purpose input and output port 0
SPI3 interface				
SPI3_MISO	30	K4	IOZU-H	master input, slave output of third SPI interface
SPI3_MOSI	31	K3	IOZU-H	master output, slave input of third SPI interface
SPI3_SCLK	32	K2	IOZU-H	serial clock input and output of third SPI interface
SPI3_SS1_N	33	K1	IOZU-H	slave select 1 input and output of third SPI interface (active LOW)
SPI3_SS2_N	35	L4	OZU	slave select 2 output of third SPI interface (active LOW)

[1] Table 16 defines the pin type.

Table 10. Pin description (SDRAM interface)

Symbol	Pin		Type[1]	Description
	HLQFP144	LFBGA170		
Data input and output interface				
SDRAM_DIO15	97	G13	IOL	data input and output bit 15
SDRAM_DIO14	95	F12	IOL	data input and output bit 14
SDRAM_DIO13	94	H14	IOL	data input and output bit 13
SDRAM_DIO12	93	H12	IOL	data input and output bit 12
SDRAM_DIO11	92	G14	IOL	data input and output bit 11
SDRAM_DIO10	89	J12	IOL	data input and output bit 10
SDRAM_DIO9	88	K14	IOL	data input and output bit 9
SDRAM_DIO8	87	L14	IOL	data input and output bit 8
SDRAM_DIO7	86	M14	IOL	data input and output bit 7

Table 10. Pin description (SDRAM interface) *…continued*

Symbol	Pin		Type[1]	Description
	HLQFP144	LFBGA170		
SDRAM_DIO6	84	K13	IOL	data input and output bit 6
SDRAM_DIO5	83	L13	IOL	data input and output bit 5
SDRAM_DIO4	82	N13	IOL	data input and output bit 4
SDRAM_DIO3	81	P13	IOL	data input and output bit 3
SDRAM_DIO2	79	L12	IOL	data input and output bit 2
SDRAM_DIO1	78	M12	IOL	data input and output bit 1
SDRAM_DIO0	77	P12	IOL	data input and output bit 0
Address output interface				
SDRAM_AO12	126	C8	OZU	address output bit 12
SDRAM_AO11	125	D8	OZU	address output bit 11
SDRAM_AO10	123	B9	OZU	address output bit 10
SDRAM_AO9	121	D9	OZU	address output bit 9
SDRAM_AO8	120	A10	OZU	address output bit 8
SDRAM_AO7	119	B10	OZU	address output bit 7
SDRAM_AO6	118	D10	OZU	address output bit 6
SDRAM_AO5	117	A11	OZU	address output bit 5
SDRAM_AO4	115	A13	OZU	address output bit 4
SDRAM_AO3	114	B12	OZU	address output bit 3
SDRAM_AO2	113	B13	OZU	address output bit 2
SDRAM_AO1	111	C11	OZU	address output bit 1
SDRAM_AO0	110	C12	OZU	address output bit 0
Control interface				
SDRAM_BA1	104	E13	OZU	bit 1 of bank address output
SDRAM_BA0	103	E12	OZU	bit 0 of bank address output
SDRAM_CAS_N	108	D14	OZU	column address selector output (active LOW)
SDRAM_CLK	127	A8	OZU	clock output
SDRAM_CLKE	109	C14	OZU	clock enable output
SDRAM_CLKIN	128	A7	IZU	clock input for resynchronization
SDRAM_CS_N	105	D11	OZU	chip select output (active LOW)
SDRAM_DQM1	100	F13	OL	MSByte of data qualifier mask output
SDRAM_DQM0	99	G11	OL	LSByte of data qualifier mask output
SDRAM_RAS_N	106	D12	OZU	row address selector output (active LOW)
SDRAM_WE_N	98	H11	OZU	write enable output (active LOW)

[1] Table 16 defines the pin type.

Table 11. Pin description (serial NOR-Flash interface)

Symbol	Pin		Type[1]	Description
	HLQFP144	LFBGA170		
SPI2 interface				
SPI2_MI	16	F3	IZU	master input of second SPI interface
SPI2_MO	17	F2	OZD	master output of second SPI interface
SPI2_SCLK	18	F1	OZU	serial clock output of second SPI interface
SPI2_SS1_N	19	G4	OZU	slave select 1 output of second SPI interface (active LOW)
SPI2_SS2_N	20	G3	OZU	slave select 2 output of second SPI interface (active LOW)
SPI2_SS3_N	22	G2	OZU	slave select 3 output of second SPI interface (active LOW)
SPI2_SS4_N	23	G1	OZU	slave select 4 output of second SPI interface (active LOW)

[1] Table 16 defines the pin type.

Table 12. Pin description (external host microcontroller interface)

Symbol	Pin		Type[1]	Description
	HLQFP144	LFBGA170		
CLKOUT	1	B2	OL	clock output; clock source and clock frequency are programmable through software
RESET_N	2	B1	IZU-H	master reset input from host microcontroller (active LOW)
I^2C-bus interface (master and slave)				
I2C2_DA	9	D1	IOZD-H	data acknowledge input and output of the I^2C-bus interface 2
I2C2_SCL	7	D3	IOZU	serial clock input and output of the I^2C-bus interface 2
I2C2_SDA	8	D2	IOZU	serial data input and output of the I^2C-bus interface 2
I2C1_DA	5	C1	IOZD-H	data acknowledge input and output of the I^2C-bus interface 1
I2C1_SCL	3	C3	IOZU	serial clock input and output of the I^2C-bus interface 1
I2C1_SDA	4	C2	IOZU-H	serial data input and output of the I^2C-bus interface 1
SPI1 interface				
SPI1_SCLK	12	E2	IZU-H	serial clock input of first SPI interface
SPI1_SI	11	E3	IZU-H	slave input of first SPI interface
SPI1_SO	10	E4	OL	slave output of first SPI interface
SPI1_SS_N	13	E1	IZU-H	slave select input of first SPI interface (active LOW)
UART interface				
UART_CTS	29	H1	IZU	UART clear-to-send signal input
UART_RD	25	H3	IZU	UART receive data input
UART_RTS	26	H2	OH	UART ready-to-send signal output
UART_TD	24	H4	OH	UART transmit data output

[1] Table 16 defines the pin type.

Table 13. Pin description (JTAG interface)

Symbol	Pin		Type[1]	Description
	HLQFP144	LFBGA170		
TCK	132	D6	IZU	test clock input
TDI	135	A6	IZU	test serial data input
TDO	136	D5	OL	test serial data output
TMS	133	C6	IZU	test mode select input
TRST_N	131	B7	IZU	test reset input; drive LOW for normal operating

[1] Table 16 defines the pin type.

Table 14. Pin description (crystal oscillator)

Symbol	Pin		Type[1]	Description
	HLQFP144	LFBGA170		
XTALI	141	A3	AI	crystal oscillator analog input
XTALO	142	A4	AO	crystal oscillator analog output

[1] Table 16 defines the pin type.

Table 15. Pin description (internally connected pins)

Symbol	Pin		Type	Description
	HLQFP144	LFBGA170		
i.c.	41, 43 to 54	L5, L6, M5, M6, N1 to N6, P3 to P5	-	internally connected; leave open

Table 16. Pin type description

Type	Description	Unused pins[1]
Generic pin types		
AI	analog input pin	always connect to quartz crystal
AO	analog output pin	always connect to quartz crystal
G	ground pin	use all ground pins
IOL	digital input and output; drives LOW after reset	can be left open
IOZD	digital input and output pin with weak pull-down	can be left open
IOZU	digital input and output pin with weak pull-up	can be left open
IZU	digital input pin with weak pull-up	can be left open
OH	digital output; drives HIGH after reset	can be left open
OL	digital output; drives LOW after reset	can be left open
OZD	digital output pin with weak pull-down	can be left open
OZU	digital output pin with weak pull-up	can be left open
P	power supply pin	use all power supply pins
Specific pin types		
-H	pins with hysteresis	see generic types

[1] Applications, which do not need all pins from SAF3560, can treat unused pins as indicated without damage or malfunction of the device.

7. Limiting values

Table 17. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
$V_{DDA(OSC)(1V2)}$	oscillator analog supply voltage (1.2 V)			−0.5	+1.7	V
$V_{DDA(PLL)(1V2)}$	PLL analog supply voltage (1.2 V)			−0.5	+1.7	V
$V_{DDD(C)(1V2)}$	core digital supply voltage (1.2 V)			−0.5	+1.7	V
$V_{DDD(GP)(3V3)}$	general purpose digital supply voltage (3.3 V)			−0.5	+3.9	V
$V_{DDD(DSP)(3V3)}$	DSP digital supply voltage (3.3 V)			−0.5	+3.9	V
$V_{DDD(JTAG)(3V3)}$	JTAG digital supply voltage (3.3 V)			−0.5	+3.9	V
$V_{DDD(MC)(3V3)}$	microcontroller digital supply voltage (3.3 V)			−0.5	+3.9	V
$V_{DDD(SDRAM)(3V3)}$	SDRAM digital supply voltage (3.3 V)			−0.5	+3.9	V
$V_{DDD(MEM)(1V2)}$	memory digital supply voltage (1.2 V)			−0.5	+1.7	V
T_{amb}	ambient temperature			−40	+85	°C
T_{stg}	storage temperature			−65	+150	°C
V_{ESD}	electrostatic discharge voltage	human body model	[1]	-	±2000	V
		charged device model	[2]			
		corner pins		-	±750	V
		other pins		-	±500	V
I_{lu}	latch-up current	all supply voltages below the maximum values listed in this table	[2]	−100	+100	mA

[1] Class 2 according to *JEDEC JESD22-A114*.

[2] According to *AEC-Q100-G*.

8. Thermal characteristics

The SAF3560 has no special thermal requirements. The backside contact of the HLQFP144 package is needed for electrical reasons. For soldering considerations, see Section 10.

Table 18. Thermal characteristics

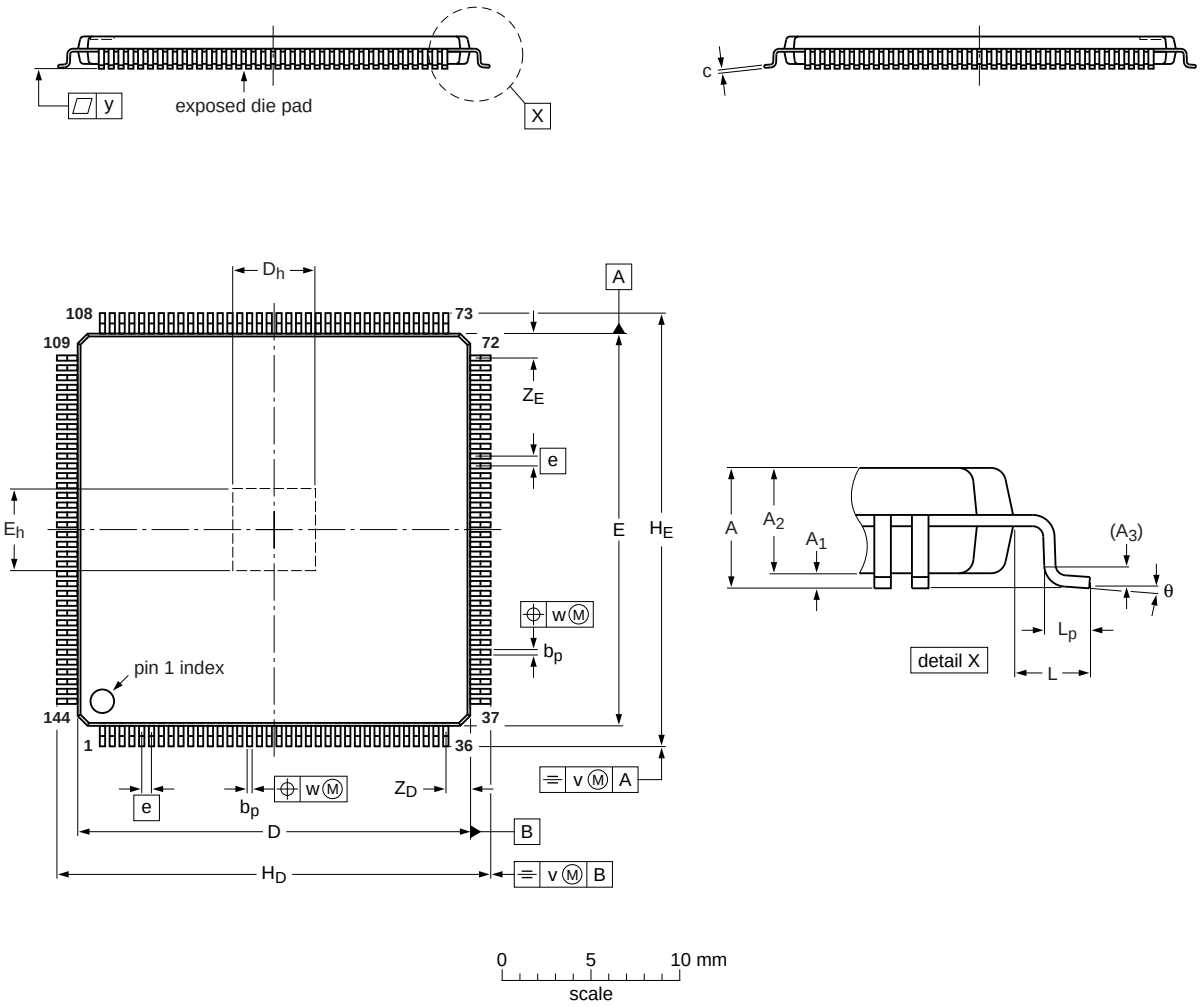
Symbol	Parameter	Conditions		Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air			
		HLQFP144	[1][2]	26.3	K/W
		LBGA170 four-layer board	[1]	30	K/W

[1] The overall $R_{th(j-a)}$ is based on JEDEC conditions and can vary depending on the board layout. To minimize the effective $R_{th(j-a)}$, all power and ground pins must be connected to the power and ground layers directly. An ample amount of copper area directly under the SAF3560 with a number of through-hole plating, which connect to the ground layer (four-layer board: second layer), can also reduce the effective $R_{th(j-a)}$. In addition, the use of soldering glue with a high thermal conductance after curing is recommended.

[2] Do not use any solder-stop varnish under the chip.

9. Package outline

HLQFP144: plastic thermal enhanced low profile quad flat package; 144 leads; body 20 x 20 x 1.4 mm; exposed die pad **SOT612-4**



DIMENSIONS (mm are the original dimensions)

UNIT	A max	A_1	A_2	A_3	b_p	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.12 0.05	1.45 1.35	0.25	0.27 0.17	0.20 0.09	20.1 19.9	4.3 4.1	20.1 19.9	4.3 4.1	0.5	22.15 21.85	22.15 21.85	1	0.75 0.45	0.2	0.08	0.08	1.4 1.1	1.4 1.1	7° 0°

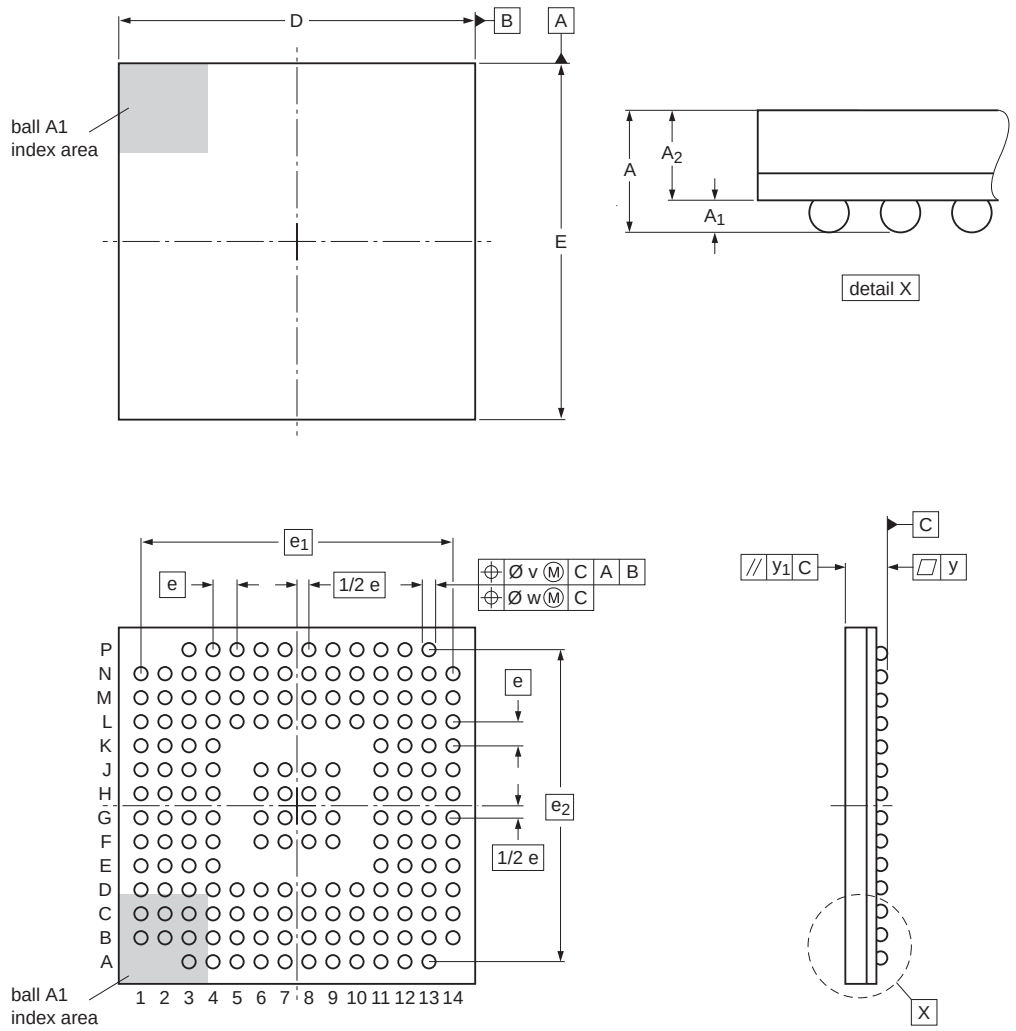
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT612-4		MS-026				~~07-12-11~~ 08-01-18

Fig 5. Package outline SOT612-4 (HLQFP144)

LFBGA170: plastic low profile fine-pitch ball grid array package; 170 balls **SOT1315-1**



Dimensions (mm are the original dimensions)

Unit		A	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y	y_1
mm	max	1.50	0.40	1.10	0.50	12.1	12.1							
	nom	1.35	0.35	1.00	0.45	12.0	12.0	0.80	10.4	10.4	0.15	0.08	0.12	0.10
	min	1.25	0.30	0.95	0.40	11.9	11.9							

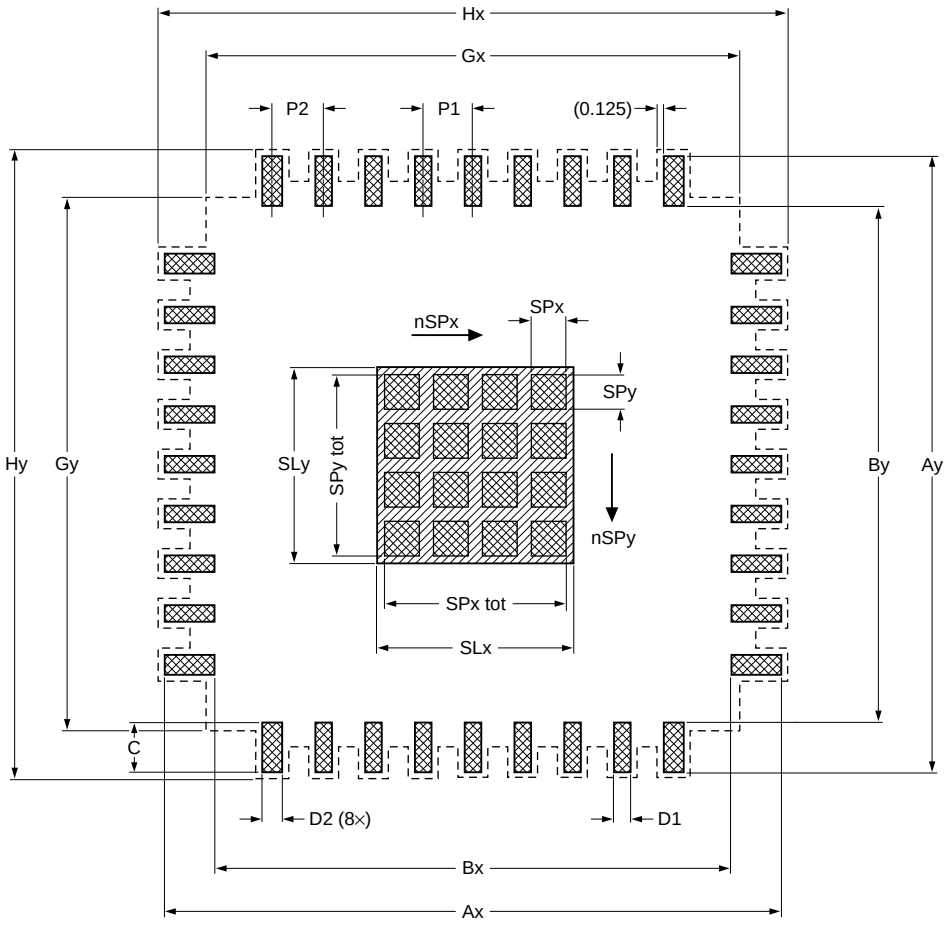
sot1315-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1315-1		MO-205				~~11-09-05~~ 11-11-01

Fig 6. Package outline SOT1315-1 (LFBGA170)

10. Soldering

Footprint information for reflow soldering of HLQFP144 package **SOT612-4**



Generic footprint pattern

Refer to the package outline drawing for actual layout

solder land

solder paste

occupied area

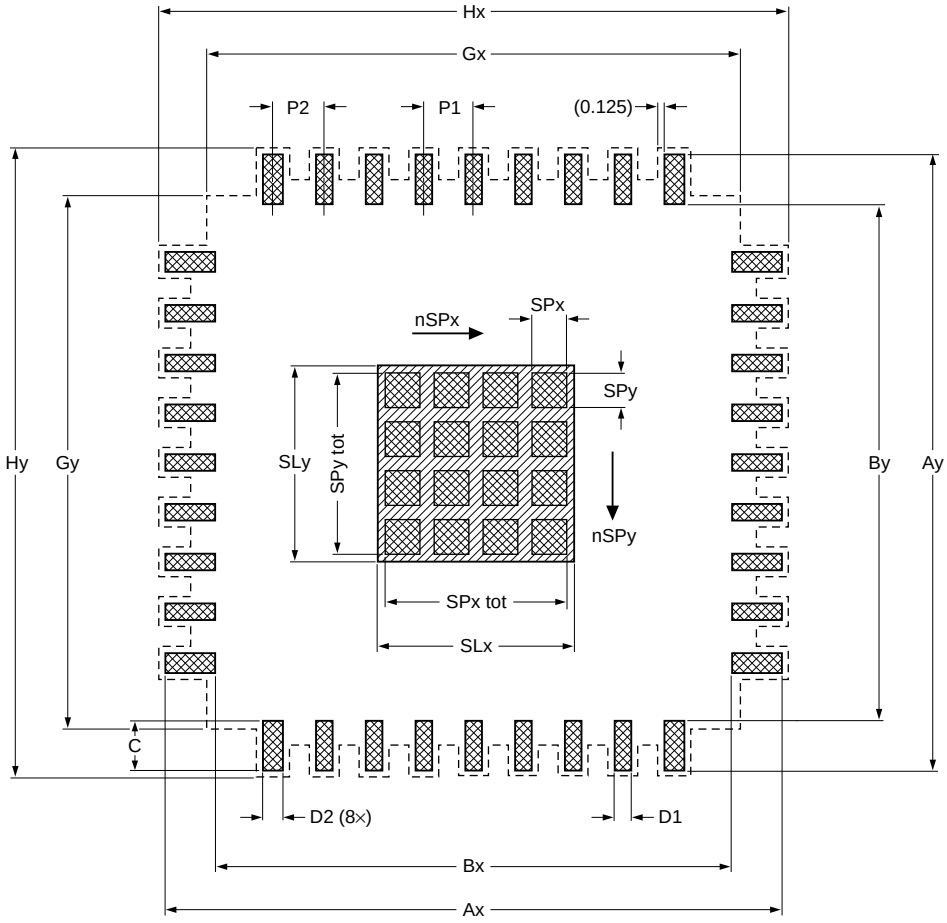
nSPx	nSPy
4	4

DIMENSIONS in mm

P1	P2	Ax	Ay	Bx	By	C	D1	D2	Gx	Gy	Hx	Hy	SLx	SLy	SPx tot	SPy tot	SPx	SPy
0.500	0.560	23.300	23.300	20.300	20.300	1.500	0.280	0.400	20.500	20.500	23.550	23.550	4.500	4.500	4.400	4.400	0.750	0.750

Fig 7. Soldering footprint SOT612-4 (HLQFP144)

Footprint information for reflow soldering of HLQFP144 package **SOT612-4**



Generic footprint pattern

Refer to the package outline drawing for actual layout

solder land

solder paste

occupied area

nSPx	nSPy
4	4

DIMENSIONS in mm

P1	P2	Ax	Ay	Bx	By	C	D1	D2	Gx	Gy	Hx	Hy	SLx	SLy	SPx tot	SPy tot	SPx	SPy
0.500	0.560	23.300	23.300	20.300	20.300	1.500	0.280	0.400	20.500	20.500	23.550	23.550	4.500	4.500	4.400	4.400	0.750	0.750

Fig 8. Soldering footprint SOT1315-1 (LFBGA170)

11. Abbreviations

Table 19. Abbreviations

Acronym	Description
AEC	Automotive Electronics Council
AM	Amplitude Modulation
BBI	BaseBand Interface
BCK	Bit Clock
CA	Conditional Access
CD	Compact Disc
CGU	Clock Generation Unit
CTS	Clear To Send
DAC	Digital-to-Analog Converter
DSP	Digital Signal Processor
EPG	Electronic Program Guide
FM	Frequency Modulation
GP	General Purpose
GPIO	General-Purpose Input and Output
HPPI	Host Processor Primary Interface
HPSI	Host Processor Secondary Interface
IC	Integrated Circuit
IF	Intermediate Frequency
I^2C-bus	Inter-IC bus
I^2S	Inter-IC Sound
I/O	Input/Output
JEDEC	Joint Electronic Device Engineering Council
JTAG	Joint Test Action Group
MUX	MUltipleXer
PCB	Printed-Circuit Board
PLL	Phase-Locked Loop
PROM	Programmable ROM
RAM	Random Access Memory
ROM	Read-Only Memory
RS232	Recommended Standard 232[1]
RTS	Ready To Send
RXD	Receive Data[2]
SD	Secure Digital memory card
SDR	Single Data Rate
SDRAM	Synchronous Dynamic RAM
SPI	Serial Peripheral Interface
S/PDIF	Sony/Philips Digital InterFace
SRC	Sample-Rate Converter

Table 19. Abbreviations *...continued*

Acronym	Description
TXD	Transmit Data[2]
UART	Universal Asynchronous Receiver Transmitter
WS	Word Select

[1] A serial interface.

[2] In this context, the X has no specific meaning.

12. Revision history

Table 20. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
SAF3560_SDS v.5	20130208	Product short data sheet	-	SAF3560_SDS v.4
Modifications:	• New package added (SOT1315-AA1) • Order pin list SAF3560EL			
SAF3560_SDS v.4	20111129	Product short data sheet	-	SAF3560_SDS v.3
Modifications:	• Two new types added (V1104/V1105) • Minor text changes			
SAF3560_SDS v.3	20100915	Product short data sheet	-	SAF3560_SDS v.2
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted where appropriate. • Minor text changes			
SAF3560_SDS v.2	20100503	Product short data sheet	-	-

13. Legal information

13.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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15. Contents

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