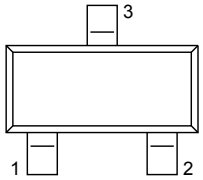
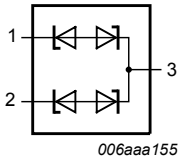
5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	K1	cathode (diode 1)	 TO-236AB (SOT23)	
2	K2	cathode (diode 2)		
3	K	common cathode		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PESD2IVN24-T	TO-236AB	plastic, surface-mounted package; 3 terminals; 1.9 mm pitch; 2.9 mm x 1.3 mm x 1 mm body	SOT23

7. Marking

Table 4. Marking codes

Type number	Marking code[1]
PESD2IVN24-T	BV%

[1] % = placeholder for manufacturing site code

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
I_{PPM}	rated peak pulse current	t_p = 8/20 µs	[1] [2]	-	3.5	A
T_j	junction temperature			-	150	°C
T_{amb}	ambient temperature			-55	150	°C
T_{stg}	storage temperature			-65	150	°C
ESD maximum ratings						
V_{ESD}	electrostatic discharge voltage	IEC 61000-4-2; contact discharge	[2] [3]	-	30	kV
		ISO 10605; contact discharge; C = 330 pF, R = 330 Ω	[2] [3]	-	30	kV
		ISO 10605; contact discharge; C = 150 pF, R = 330 Ω	[2] [3]	-	30	kV

[1] According to IEC 61000-4-5.
[2] Measured from pin 1 or 2 to pin 3.
[3] Device stressed with ten non-repetitive ESD pulses.

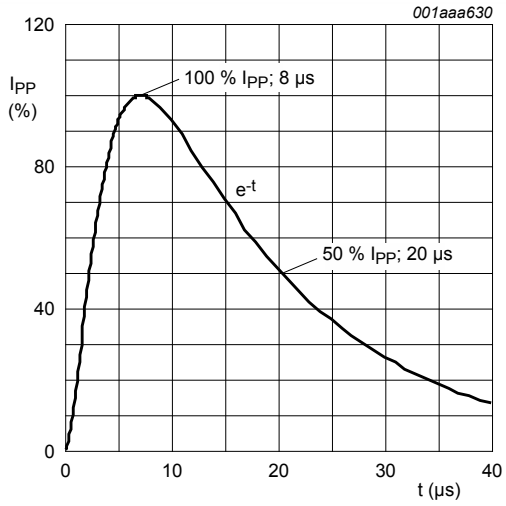


Fig. 1. 8/20 µs pulse waveform according to IEC 61000-4-5

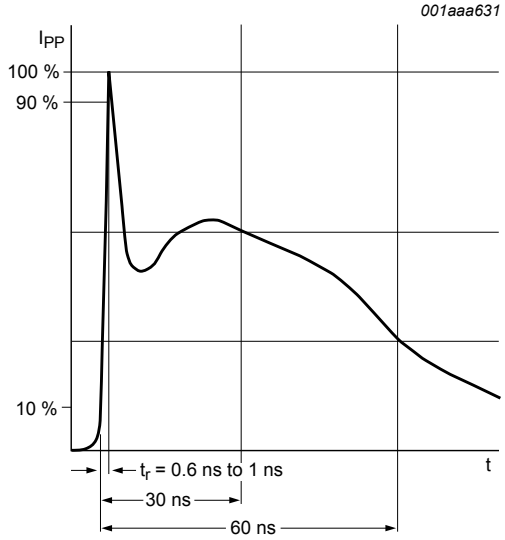


Fig. 2. ESD pulse waveform according to IEC 61000-4-2

9. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{RWM}	reverse standoff voltage	T_{amb} = 25 °C		-	-	24	V
V_{BR}	breakdown voltage	I_R = 10 mA; T_{amb} = 25 °C	[1]	25.5	30.5	35.5	V
I_{RM}	reverse leakage current	V_{RWM} = 24 V; T_{amb} = 25 °C	[1]	-	1	50	nA
C_d	diode capacitance	f = 1 MHz; V_R = 0 V; T_{amb} = 25 °C	[1]	-	14	17	pF
$\Delta C_d/C_d$	diode capacitance matching		[2]	-	0.1	-	%
		f = 1 MHz; V_R = 2.5 V; T_{amb} = 25 °C	[2]	-	0.1	-	%
V_{CL}	clamping voltage	I_{PPM} = 1 A; t_p = 8/20 µs; T_{amb} = 25 °C	[3] [1]	-	31	40	V
		I_{PPM} = 3.5 A; t_p = 8/20 µs; T_{amb} = 25 °C	[3] [1]	-	33	42	V
		I_{PP} = 16 A; t_p = TLP; T_{amb} = 25 °C	[4] [1]	-	32	-	V
R_{dyn}	dynamic resistance	I_R = 10 A; T_{amb} = 25 °C	[4] [1]	-	0.2	-	Ω

[1] Measured from pin 1 or 2 to pin 3.
[2] ΔC_d is the difference of the capacitance measured between pin 1 and pin 3 and the capacitance measured between pin 2 and pin 3.
[3] Device stressed with 8/20 µs exponential decay waveform according to IEC 61000-4-5.
[4] Non-repetitive current pulse, Transmission Line Pulse (TLP); square pulse; ANSI / ESD STM5.5.1-2008

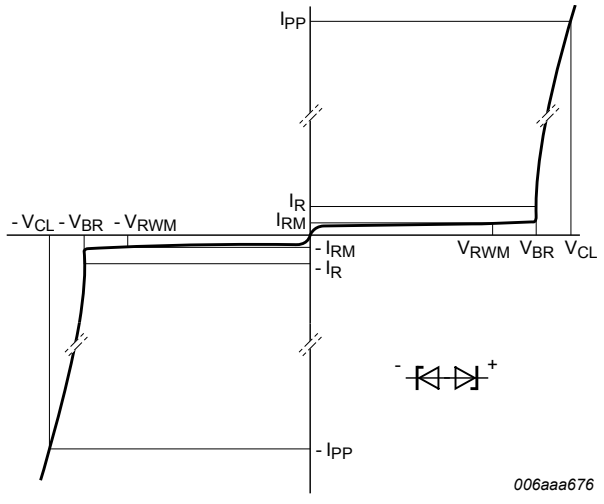


Fig. 3. V-I characteristics for a bidirectional ESD protection diode

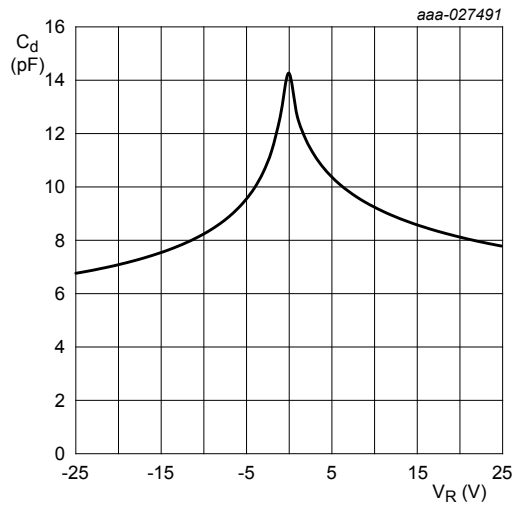
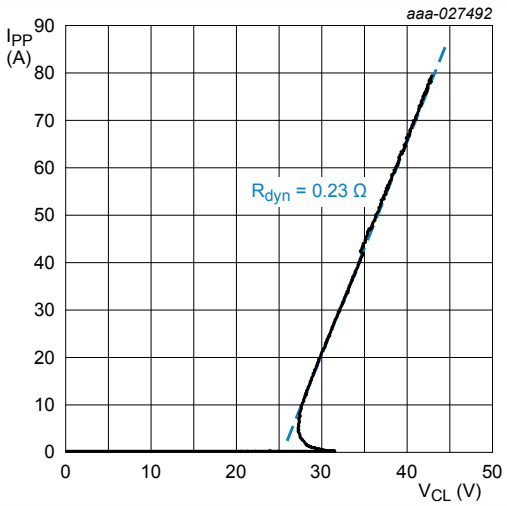
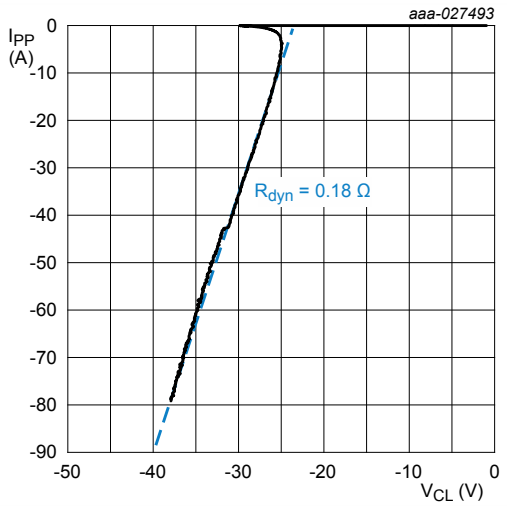


Fig. 4. Diode capacitance as a function of reverse voltage; typical values



t_p = 100 ns; Transmission Line Pulse (TLP)

Fig. 5. Positive clamping voltage (TLP); typical values



t_p = 100 ns; Transmission Line Pulse (TLP)

Fig. 6. Negative clamping voltage (TLP); typical values

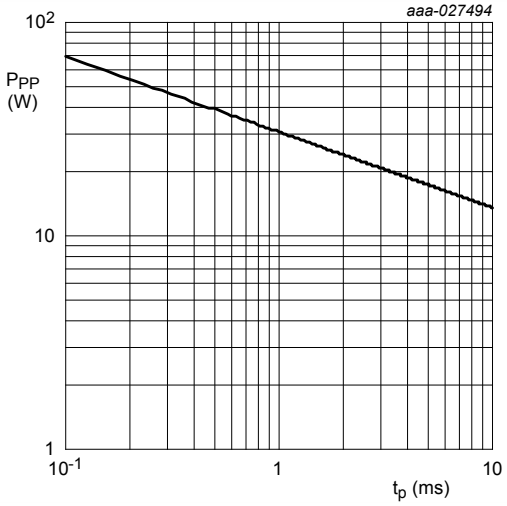


Fig. 7. Peak pulse power as a function of exponential pulse duration; typical values

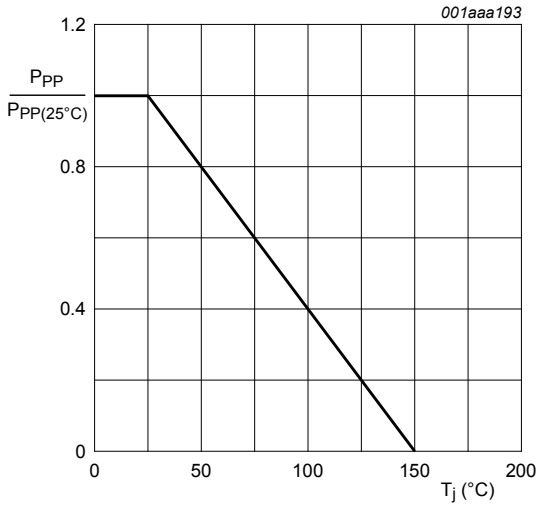


Fig. 8. Relative variation of peak pulse power as a function of junction temperature; typical values

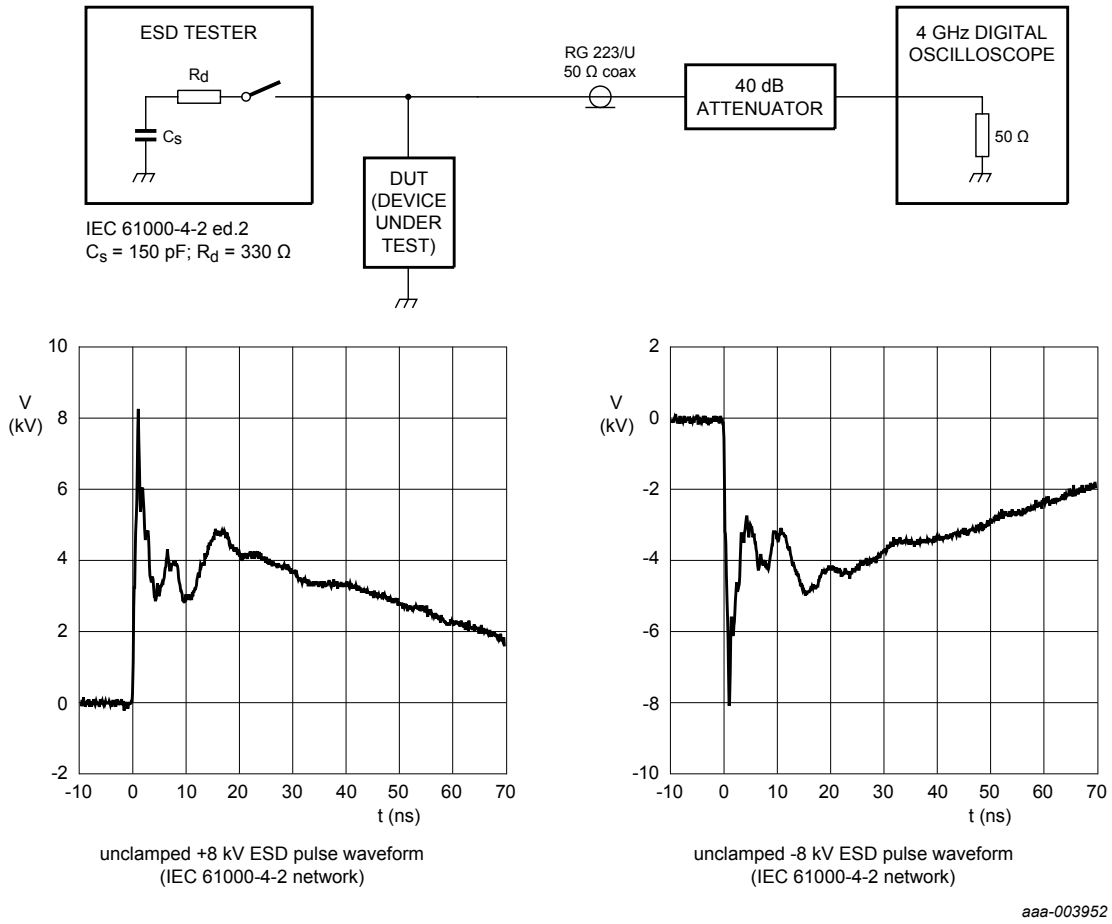


Fig. 9. ESD clamping test setup and waveforms

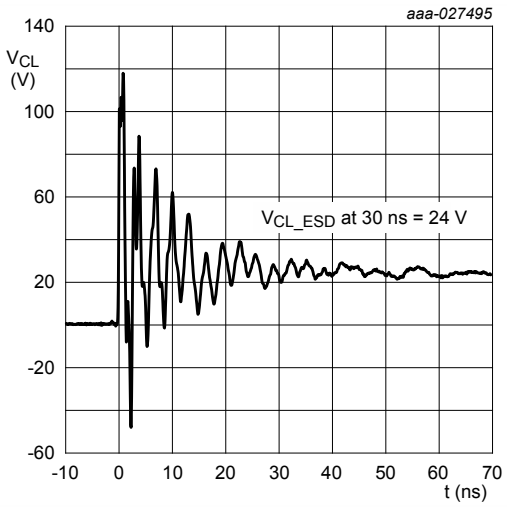


Fig. 10. Clamped +8 kV pulse waveform (IEC 61000-4-2 network)

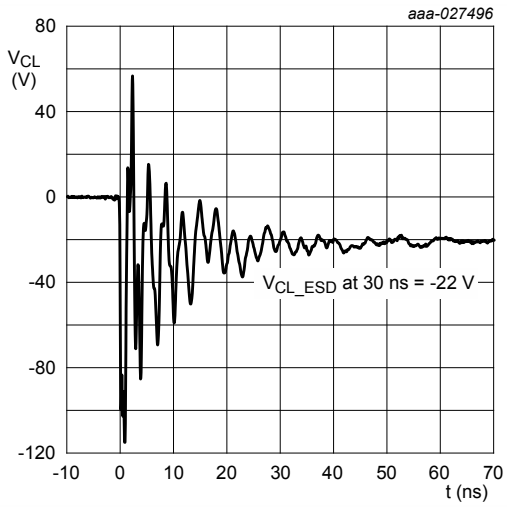


Fig. 11. Clamped -8 kV pulse waveform (IEC 61000-4-2 network)

10. Application information

The PESD2IVN24-T is designed for the protection of two automotive IVN bus line from the damage caused by ESD and surge pulses.

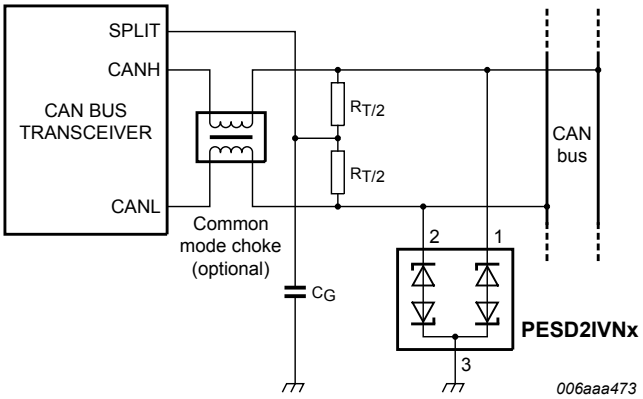


Fig. 12. Typical application: ESD protection of two automotive CAN bus lines

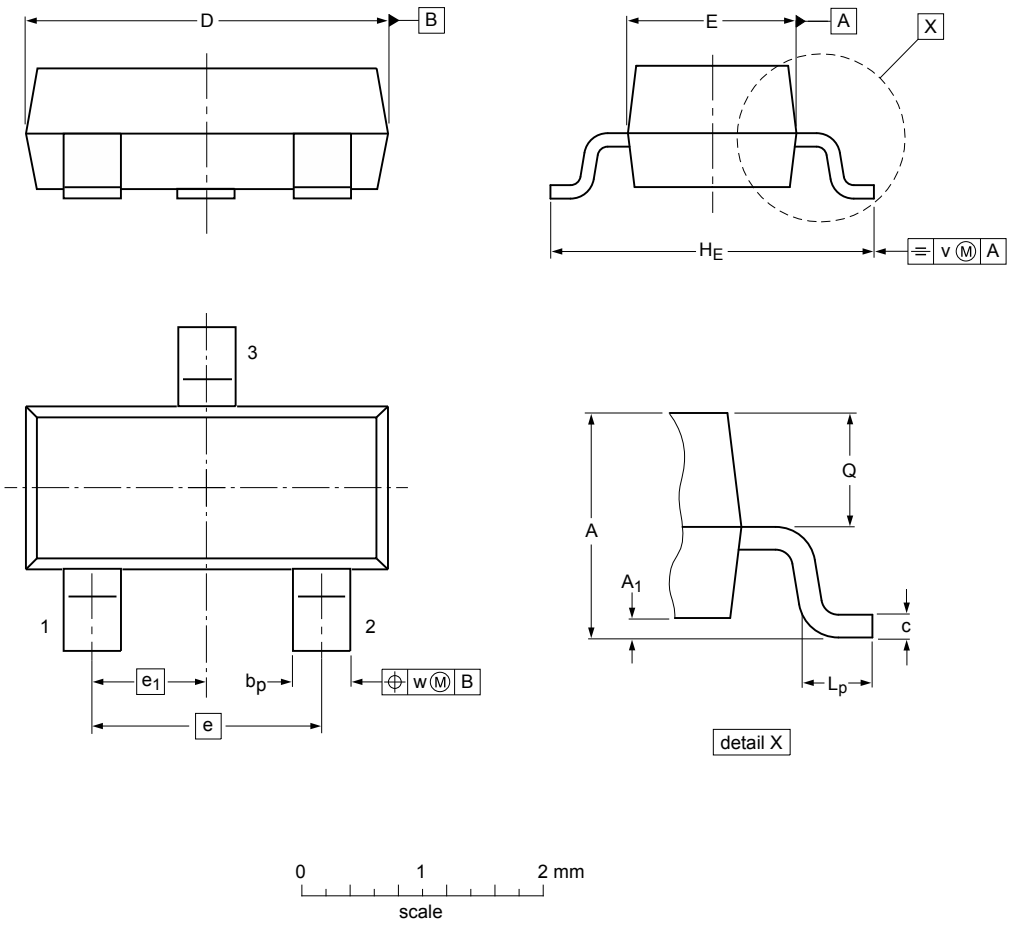
Circuit board layout and protection device placement

Circuit board layout is critical for the suppression of ESD, Electrical Fast Transient (EFT) and surge transients. The following guidelines are recommended:

1. Place the device as close to the input terminal or connector as possible.
2. Minimize the path length between the device and the protected line.
3. Keep parallel signal paths to a minimum.
4. Avoid running protected conductors in parallel with unprotected conductors.
5. Minimize all Printed-Circuit Board (PCB) conductive loops including power and ground loops.
6. Minimize the length of the transient return path to ground.
7. Avoid using shared transient return paths to a common ground point.
8. Use ground planes whenever possible. For multilayer PCBs, use ground vias.

11. Package outline

Plastic surface-mounted package; 3 leads **SOT23**



Dimensions (mm are the original dimensions)

Unit		A	A_1	b_p	c	D	E	e	e_1	H_E	L_p	Q	v	w
mm	max	1.1	0.1	0.48	0.15	3.0	1.4			2.5	0.45	0.55		
	nom							1.9	0.95				0.2	0.1
	min	0.9		0.38	0.09	2.8	1.2			2.1	0.15	0.45		

sot023_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT23		TO-236AB				~~14-06-19~~ 14-09-22

Fig. 13. Package outline TO-236AB (SOT23)

12. Soldering

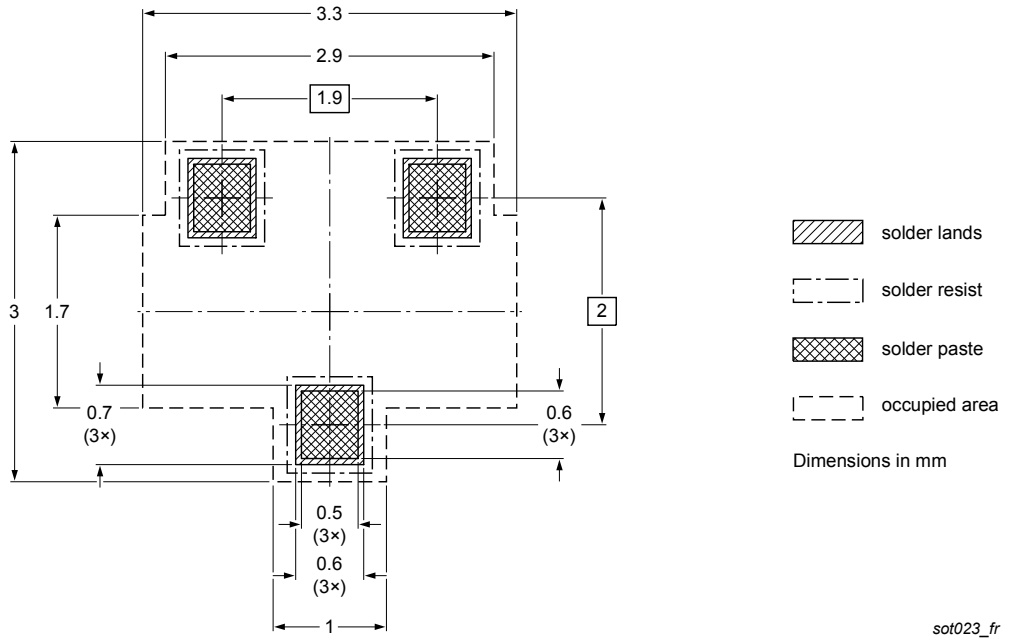


Fig. 14. Reflow soldering footprint for TO-236AB (SOT23)

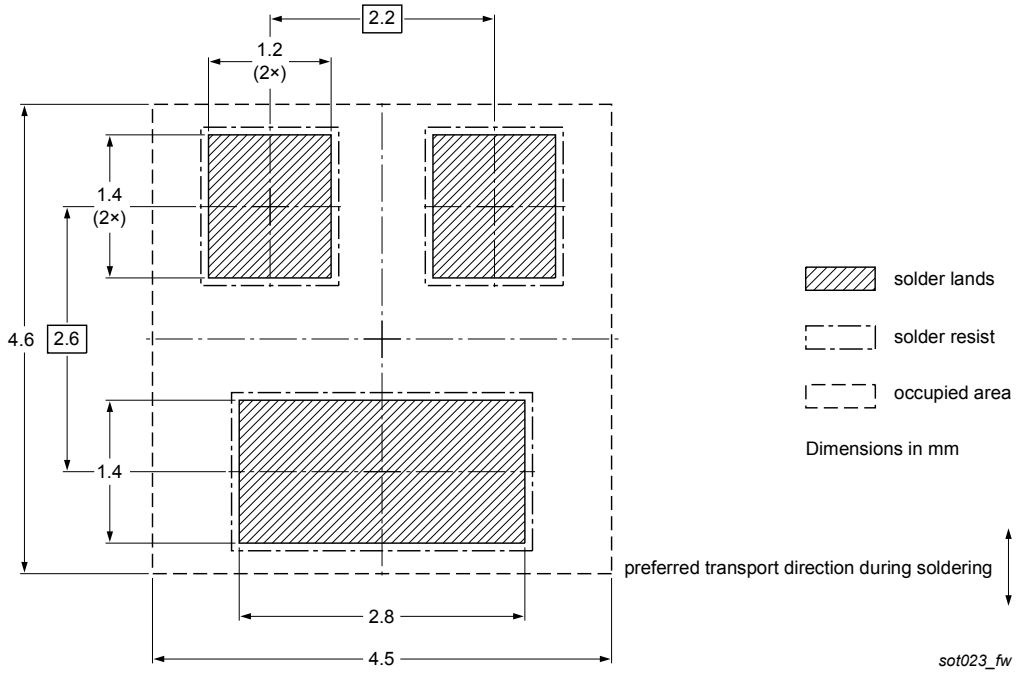


Fig. 15. Wave soldering footprint for TO-236AB (SOT23)

13. Revision history

Table 7. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PESD2IVN24-T v.2	20180201	Product data sheet	-	PESD2IVN24-T v.1
Modifications:	• Marking code: corrected			
PESD2IVN24-T v.1	20171012	Product data sheet	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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15. Contents

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Date of release: 1 February 2018