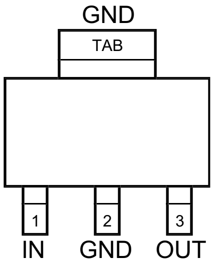
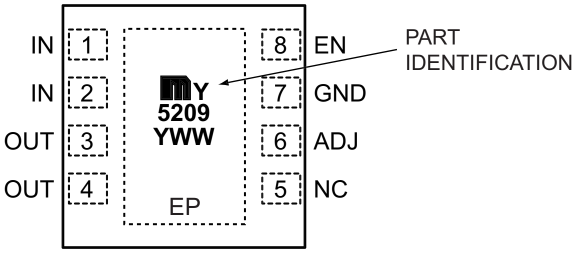
Package Types

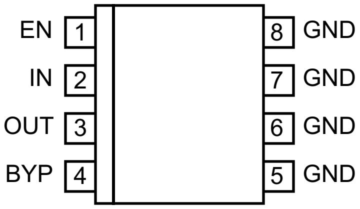
MIC5209-x.xYS
SOT-223 (S)
Fixed Voltages (Top View)



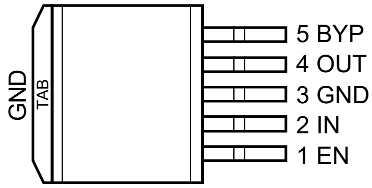
MIC5209YML
8-Pin 3x3 DFN (ML)
Adjustable Voltages (Top View)



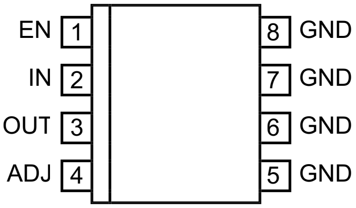
MIC5209-x.xYM
SOIC-8 (M)
Fixed Voltages (Top View)



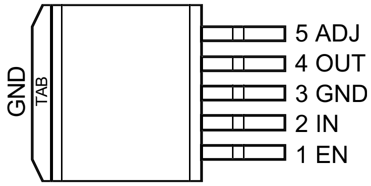
MIC5209-x.xYU
DDPAK (U)
Fixed Voltages (Top View)



MIC5209YM
SOIC-8 (M)
Adjustable Voltages (Top View)

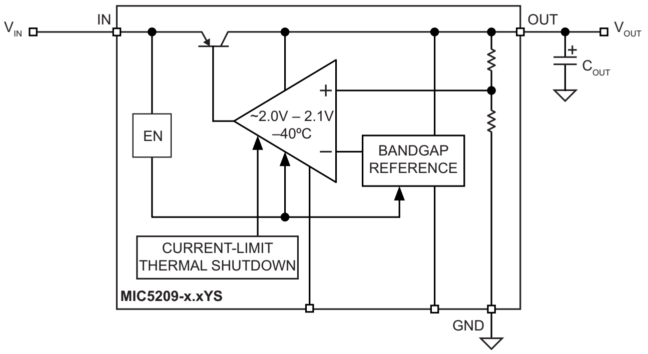


MIC5209YU
DDPAK (U)
Adjustable Voltages (Top View)

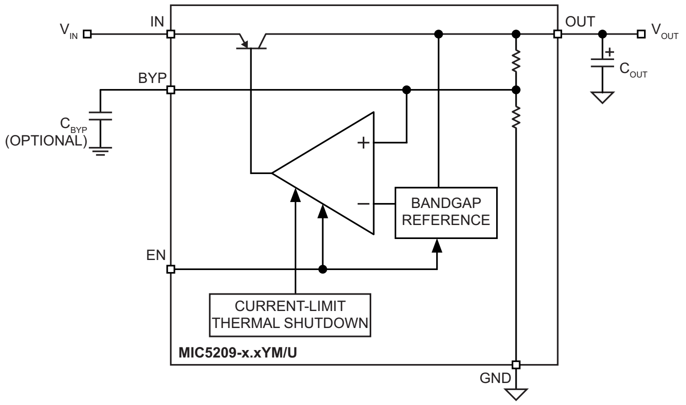


Functional Diagrams

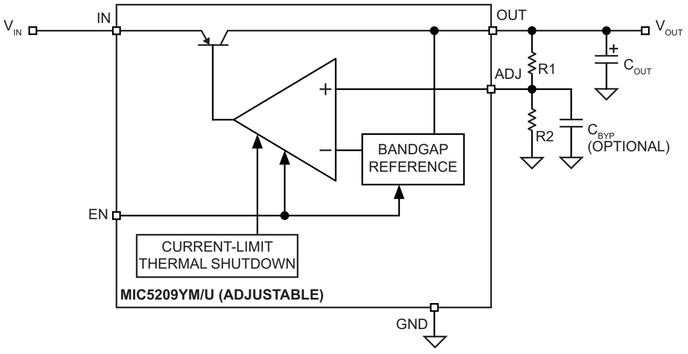
Low-Noise Fixed Regulator (SOT-223 Version Only)



Ultra-Low-Noise Fixed Regulator



Ultra-Low-Noise Adjustable Regulator



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Supply Voltage (V_{IN})	–20V to +20V
Power Dissipation (P_D) (Note 1)	Internally Limited
ESD Rating (SOT-223)	2 kV HBM/300V MM
ESD Rating (DFN, SOIC-8)	5 kV HBM/100V MM

Operating Ratings ‡

Supply Voltage (V_{IN})	+2.5V to +16V
Adjustable Output Voltage Range (V_{OUT})	+1.8V to +15V

† Notice: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

‡ Notice: The device is not guaranteed to function outside its operating ratings.

Note 1: The maximum allowable power dissipation at any T_A (ambient temperature) is $P_{D(max)} = (T_{J(max)} – T_A) \times \theta_{JA}$. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. See Table 4-1 and the Thermal Considerations sub-section in Applications Information for details.

TABLE 1-1: ELECTRICAL CHARACTERISTICS (Note 1)

Electrical Characteristics: $V_{IN} = V_{OUT} + 1V$; I_L = 100 µA; T_J = +25°C, **bold** values indicate –40°C ≤ T_J ≤ +125°C except 0°C ≤ T_J ≤ +125°C for 1.8V ≤ V_{OUT} ≤ 2.5V, unless noted.

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Output Voltage Accuracy	V_{OUT}	–1	—	1	%	Variation from nominal V_{OUT}
		–2	—	**2**		
Output Voltage Temperature Coefficient	$\Delta V_{OUT}/\Delta T$	—	**40**	—	ppm/°C	Note 2
Line Regulation	$\Delta V_{OUT}/V_{OUT}$	—	0.009	0.05	%	$V_{IN} = V_{OUT}$ + 1V to 16V
		—	—	**0.10**		
Load Regulation	$\Delta V_{OUT}/V_{OUT}$	—	0.05	0.5	%	I_L = 100 µA to 500 mA, Note 3
		—	—	**0.7**		
Dropout Voltage, (Note 4)	$V_{IN} - V_{OUT}$	—	10	60	mV	I_L = 100 µA
		—	—	**80**		
		—	115	175		I_L = 50 mA
		—	—	**250**		
		—	165	300		I_L = 150 mA
		—	—	**400**		
		—	350	500		I_L = 500 mA
		—	—	**600**		
Ground Pin Current (Note 5, Note 6)	I_{GND}	—	80	130	µA	V_{EN} ≥ 3.0V, I_{OUT} = 100 µA
		—	—	**170**		
		—	350	650		V_{EN} ≥ 3.0V, I_{OUT} = 50 mA
		—	—	**900**		
		—	1.8	2.5	mA	V_{EN} ≥ 3.0V, I_{OUT} = 150 mA
		—	—	**3.0**		
		—	8	20		V_{EN} ≥ 3.0V, I_{OUT} = 500 mA
		—	—	**25**		
Ground Pin Quiescent Current, (Note 6)	I_{GND}	—	0.05	**3**	µA	V_{EN} ≤ 0.4V (shutdown)
		—	0.10	**8**		V_{EN} ≤ 0.18V (shutdown)
Ripple Rejection	PSRR	—	75	—	dB	f = 120 Hz
Current Limit	I_{LIMIT}	—	700	900	mA	V_{OUT} = 0V
		—	—	**1000**		
Thermal Regulation	$\Delta V_{OUT}/\Delta P_D$	—	0.05	—	%/W	Note 7
Output Noise, (Note 8)	e_n	—	500	—	nV √Hz	V_{OUT} = 2.5V, I_{OUT} = 50 mA C_{OUT} = 2.2 µF, C_{BYP} = 0
		—	300	—		I_{OUT} = 50 mA, C_{OUT} = 2.2 µF C_{BYP} = 470 pF

TABLE 1-1: ELECTRICAL CHARACTERISTICS (Note 1) (CONTINUED)

Electrical Characteristics: $V_{IN} = V_{OUT} + 1V$; $I_L = 100$ µA; $T_J = +25°C$, **bold** values indicate $–40°C \le T_J \le +125°C$ except $0°C \le T_J \le +125°C$ for $1.8V \le V_{OUT} \le 2.5V$, unless noted.

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Enable Input						
Enable Input Logic-Low Voltage	V_{ENL}	—	—	0.4	V	V_{EN} = Logic-low (Regulator shutdown)
		—	—	**0.18**		
		2.0	—	—	V	V_{EN} = Logic-high (Regulator enabled)
Enable Input Current	I_{ENL}	—	0.01	–1	µA	$V_{ENL} \le 0.4V$
		—	**0.01**	**–2**		$V_{ENL} \le 0.18V$
—	I_{ENH}	—	5	20	µA	$V_{ENH} \ge 2.0V$
		—	—	**25**		
		—	—	30		$V_{ENH} \ge 16V$
		—	—	**50**		

Note 1: Specification for packaged product only.

2: Output voltage temperature coefficient is defined as the worst-case voltage change divided by the total temperature range.

3: Regulation is measured at constant junction temperature using low duty cycle pulse testing. Parts are tested for load regulation in the load range from 100 µA to 500 mA. Changes in output voltage due to heating effects are covered by the thermal regulation specification.

4: Dropout Voltage is defined as the input to output differential at which the output voltage drops 2% below its nominal value measured at 1V differential.

5: Ground pin current is the regulator quiescent current plus pass transistor base current. The total current drawn from the supply is the sum of the load current plus the ground pin current.

6: V_{EN} is the voltage externally applied to devices with the EN (enable) input pin. SOIC-8 (M) and DDPAK (U) packages only.

7: Thermal regulation is the change in output voltage at a time “t” after a change in power dissipation is applied, excluding load or line regulation effects. Specifications are for a 500 mA load pulse at $V_{IN} = 16V$ for t = 10 ms.

8: C_{BYP} is an optional, external bypass capacitor connected to devices with a BYP (bypass) or ADJ (adjust) pin. SOIC-8 (M) and DDPAK (U) packages only.

TEMPERATURE SPECIFICATIONS (Note 1)

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Storage Temperature Range	T_S	–65	—	+150	°C	—
Lead Temperature	—	—	—	+260	°C	Soldering, 5 sec.
Junction Temperature	T_J	–40	—	+125	°C	$2.5V \le V_{OUT} \le 15V$
Junction Temperature	T_J	0	—	+125	°C	$1.8V \le V_{OUT} < 2.5V$
Package Thermal Resistance						
Thermal Resistance SOT-223	θ_{JA}	—	62	—	°C/W	EIA/JEDEC JES51-751-7, 4 Layer Board
	θ_{JC}	—	15	—	°C/W	
Thermal Resistance SOIC-8	θ_{JA}	—	50	—	°C/W	See Thermal Considerations for more information.
	θ_{JC}	—	25	—	°C/W	
Thermal Resistance DDPAK	θ_{JA}	—	31.4	—	°C/W	EIA/JEDEC JES51-751-7, 4 Layer Board
	θ_{JC}	—	3	—	°C/W	
Thermal Resistance 3 mm x 3 mm DFN	θ_{JA}	—	64	—	°C/W	EIA/JEDEC JES51-751-7, 4 Layer Board
	θ_{JC}	—	12	—	°C/W	

Note 1: The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air (i.e., T_A, T_J, θ_{JA}). Exceeding the maximum allowable power dissipation will cause the device operating junction temperature to exceed the maximum +125°C rating. Sustained junction temperatures above +125°C can impact the device reliability.

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

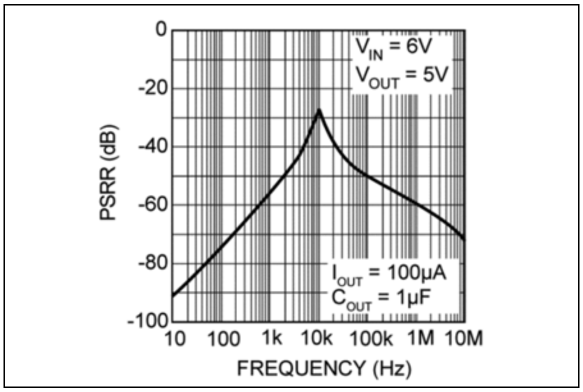


FIGURE 2-1: *Power Supply Rejection Ratio.*

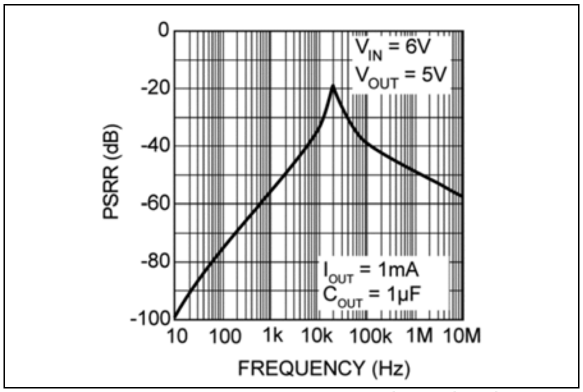


FIGURE 2-2: *Power Supply Rejection Ratio.*

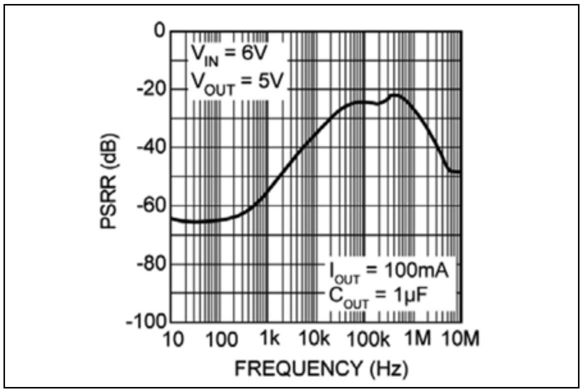


FIGURE 2-3: *Power Supply Rejection Ratio.*

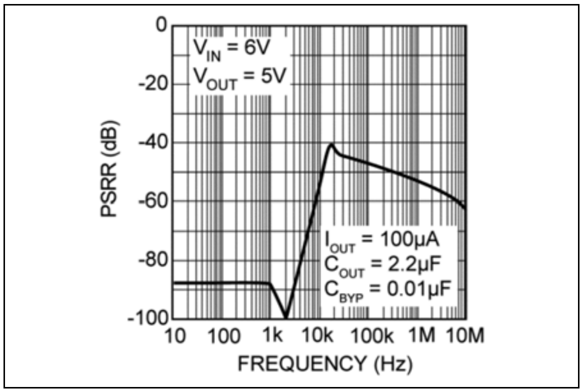


FIGURE 2-4: *Power Supply Rejection Ratio.*

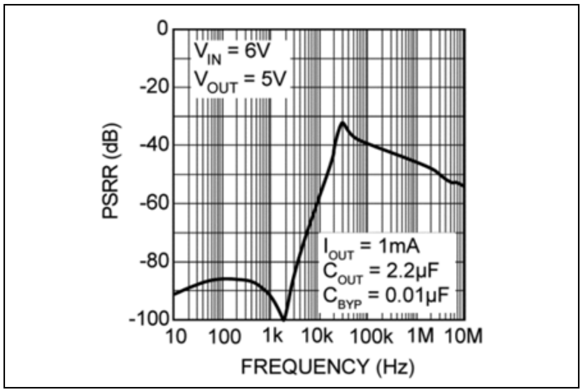


FIGURE 2-5: *Power Supply Rejection Ratio.*

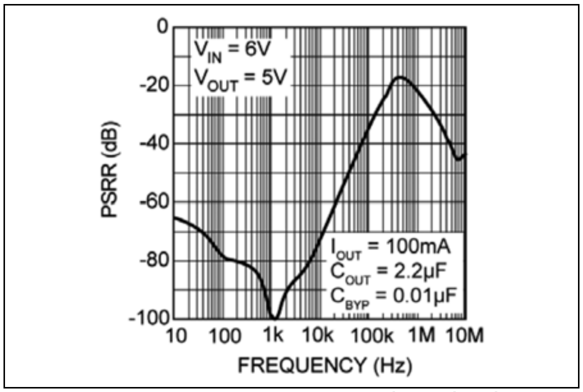


FIGURE 2-6: *Power Supply Rejection Ratio.*

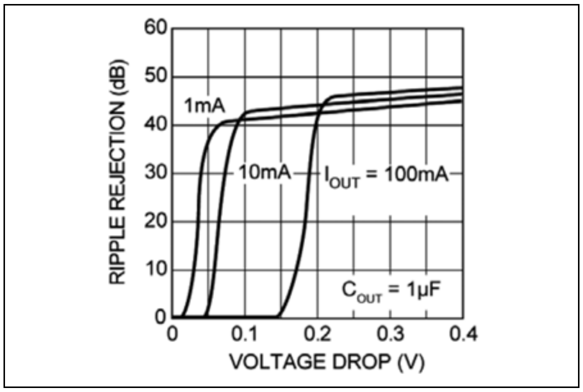


FIGURE 2-7: *Power Supply Ripple Rejection vs. Voltage Drop.*

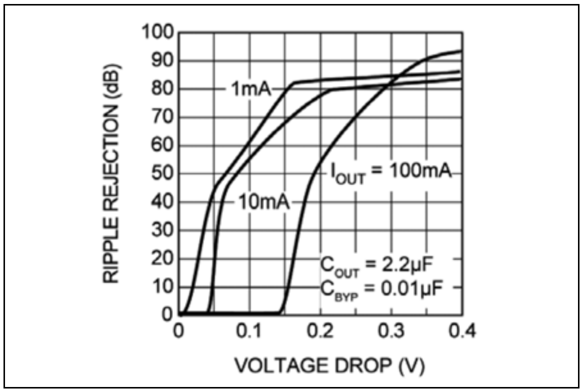


FIGURE 2-8: *Power Supply Ripple Rejection vs. Voltage Drop.*

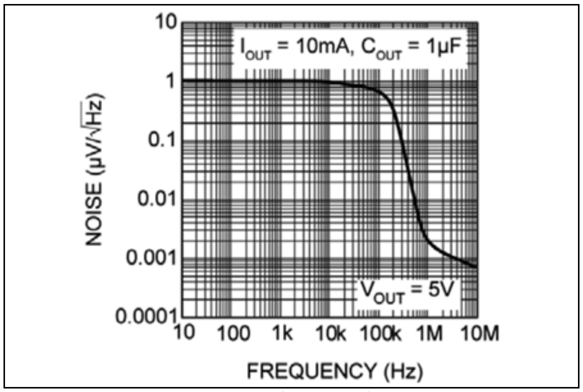


FIGURE 2-9: *Noise Performance.*

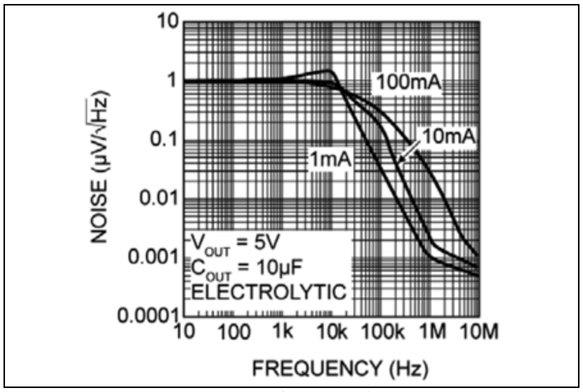


FIGURE 2-10: *Noise Performance.*

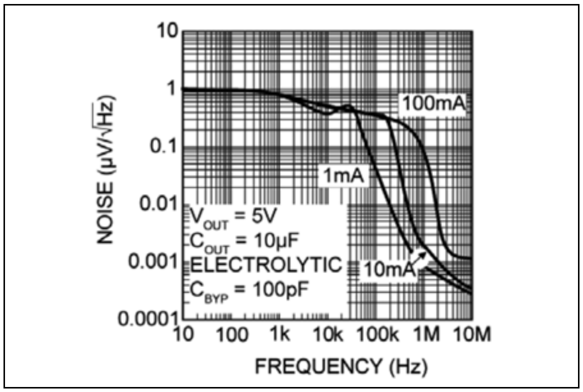


FIGURE 2-11: *Noise Performance.*

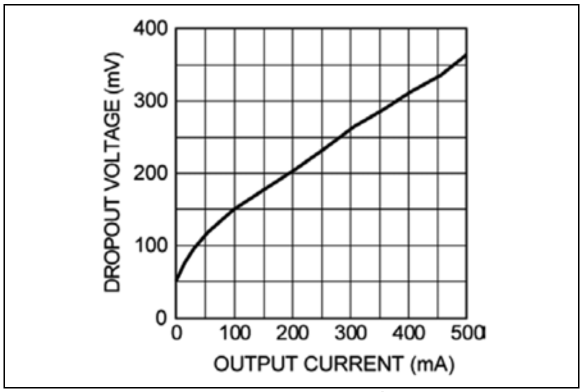


FIGURE 2-12: *Dropout Voltage vs. Output Current.*

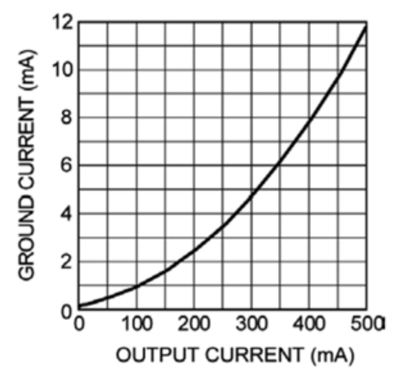


FIGURE 2-13: *Ground Current vs. Output Current.*

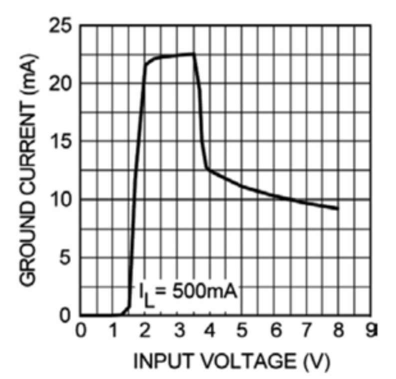


FIGURE 2-14: *Ground Current vs. Supply Voltage.*

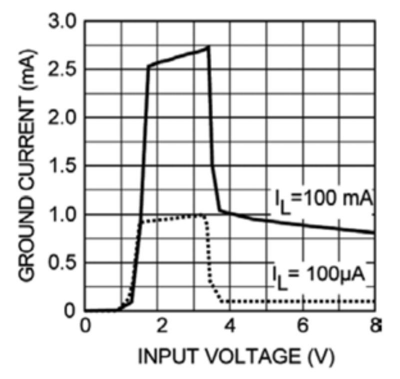


FIGURE 2-15: *Ground Current vs. Supply Voltage.*

3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

Pin Number 8-Pin DFN	Pin Number SOT-223	Pin Number SOIC-8	Pin Number DDPAK	Pin Name	Description
1, 2	1	2	2	IN	Supply Input.
7	2, TAB	5, 6, 7, 8	3, TAB	GND	Ground: SOT-223 Pin 2 and TAB are internally connected. SOIC-8 Pins 5 through 8 are internally connected.
3, 4	3	3	4	OUT	Regulator Output: Pins 3 and 4 must be tied together.
5	—	—	—	NC	Not Connected.
8	—	1	1	EN	Enable (Input): CMOS-compatible control input. Logic-High = Enable; Logic-Low = Shutdown.
—	—	4 (Fixed)	5 (Fixed)	BYP	Reference Bypass: Connect external 470 pF capacitor to GND to reduce output noise. Can be left open. For 1.8V or 2.5V operation, see Application Information.
6	—	4 (Adjustable)	5 (Adjustable)	ADJ	Adjust (Input): Feedback input. Connect to resistive voltage-divider network.
EP	—	—	—	ePad	Exposed Thermal Pad: Connect to GND for best thermal performance.

4.0 APPLICATIONS INFORMATION

4.1 Enable/Shutdown

Enable is not available on devices in the SOT-223 (S) package.

Forcing EN (enable/shutdown) high (> 2V) enables the regulator. EN is compatible with CMOS logic. If the enable/shutdown feature is not required, connect EN to IN (supply input).

4.2 Input Capacitor

A 1 µF capacitor should be placed from IN to GND if there is more than 10 inches of wire between the input and the AC filter capacitor or if a battery is used as the input.

4.3 Output Capacitor

An output capacitor is required between OUT and GND to prevent oscillation. The minimum size of the output capacitor is dependent upon whether a reference bypass capacitor is used. 1 µF minimum is recommended when C_{BYP} is not used (see Figure 4-1). 2.2 µF minimum is recommended when C_{BYP} is 470 pF (see Figure 4-2). Larger values improve the regulator's transient response.

The output capacitor should have an ESR (equivalent series resistance) of about 1Ω and a resonant frequency above 1 MHz. Ultra-low-ESR and ceramic capacitors can cause a low amplitude oscillation on the output and/or underdamped transient response. Most tantalum or aluminum electrolytic capacitors are adequate; film types will work, but are more expensive. Since many aluminum electrolytics have electrolytes that freeze at about –30°C, solid tantalums are recommended for operation below –25°C.

At lower values of output current, less output capacitance is needed for output stability. The capacitor can be reduced to 0.47 µF for current below 10 mA or 0.33 µF for currents below 1 mA.

4.4 No-Load Stability

The MIC5209 will remain stable and in regulation with no load (other than the internal voltage divider) unlike many other voltage regulators. This is especially important in CMOSRAM keep-alive applications.

4.5 Reference Bypass Capacitor

Reference bypass (BYP) is available only on devices in SOIC-8 and DDPAK packages.

BYP is connected to the internal voltage reference. A 470 pF capacitor (C_{BYP}) connected from BYP to GND quiets this reference, providing a significant reduction in output noise (ultra-low-noise performance). Because C_{BYP} reduces the phase margin, the output capacitor should be increased to at least 2.2 µF to maintain stability.

The start-up speed of the MIC5209 is inversely proportional to the size of the reference bypass capacitor. Applications requiring a slow ramp-up of output voltage should consider larger values of C_{BYP}. Likewise, if rapid turn-on is necessary, consider omitting C_{BYP}.

If output noise is not a major concern, omit C_{BYP} and leave BYP open.

4.6 Thermal Considerations

The SOT-223 has a ground tab that allows it to dissipate more power than the SOIC-8 (refer to the Slot-1 Power Supply sub-section for details). At +25°C ambient, it will operate reliably at 1.6W dissipation with "worst-case" mounting (no ground plane, minimum trace widths, and FR4 printed circuit board).

Thermal resistance values for the SOIC-8 represent typical mounting on a 1"-square, copper-clad, FR4 circuit board. For greater power dissipation, SOIC-8 versions of the MIC5209 feature a fused internal lead frame and die bonding arrangement that reduces thermal resistance when compared to standard SOIC-8 packages.

TABLE 4-1: MIC5209 THERMAL RESISTANCE

Package	θ_{JA}	θ_{JC}
SOT-223 (S)	62°C/W	15°C/W
SOIC-8 (M)	50°C/W	25°C/W
DDPAK (U)	31.4°C/W	3°C/W
3x3 DFN (ML)	64°C/W	12°C/W

Multilayer boards with a ground plane, wide traces near the pads, and large supply-bus lines will have better thermal conductivity and will also allow additional power dissipation.

For additional heat sink characteristics, refer to Application Hint 17. For a full discussion of heat sinking and thermal effects on voltage regulators, refer to the "Regulator Thermals" section of the Designing with Low-Dropout Voltage Regulators handbook.

4.7 Low-Voltage Operation

The MIC5209-1.8 and MIC5209-2.5 require special consideration when used in voltage-sensitive systems. They may momentarily overshoot their nominal output voltages unless appropriate output and bypass capacitor values are chosen.

During regulator power up, the pass transistor is fully saturated for a short time, while the error amplifier and voltage reference are being powered up more slowly from the output (see Functional Diagrams). Selecting larger output and bypass capacitors allows additional time for the error amplifier and reference to turn on and prevent overshoot.

To ensure that no overshoot is present when starting up into a light load (100 µA), use a 4.7 µF output capacitance and 470 pF bypass capacitance. This slows the turn-on enough to allow the regulator to react and keep the output voltage from exceeding its nominal value. At heavier loads, use a 10 µF output capacitance and 470 pF bypass capacitance. Lower values of output and bypass capacitance can be used, depending on the sensitivity of the system.

Applications that can withstand some overshoot on the output of the regulator can reduce the output capacitor and/or reduce or eliminate the bypass capacitor. Applications that are not sensitive to overshoot due to power-on reset delays can use normal output and bypass capacitor configurations.

Please note the junction temperature range of the regulator with an output less than 2.5V (fixed and adjustable) is 0°C to +125°C.

4.8 Fixed Regulator Applications

Figure 4-1 shows a basic MIC5209-x.xYM (SOIC-8) fixed-voltage regulator circuit. See Figure 5 for a similar configuration using the more thermally-efficient MIC5209-x.xYS (SOT-223). A 1 µF minimum output capacitor is required for basic fixed-voltage applications.

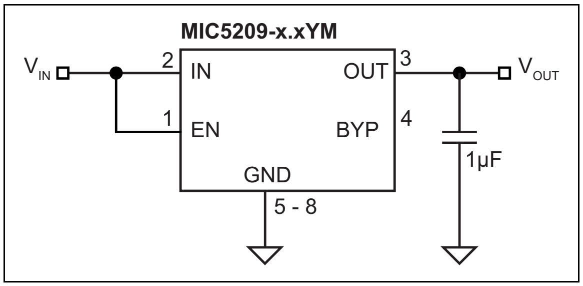


FIGURE 4-1: *Low-Noise Fixed-Voltage Application.*

Figure 4-2 includes the optional 470 pF noise bypass capacitor between BYP and GND to reduce output noise. Note that the minimum value of C_{OUT} must be increased when the bypass capacitor is used.

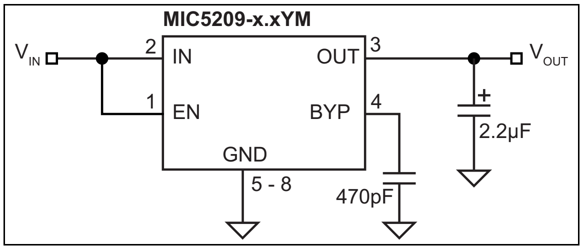


FIGURE 4-2: *Ultra-Low-Noise Fixed-Voltage Application.*

4.9 Adjustable Regulator Applications

The MIC5209YM, MIC5209YU, and MIC5209YML can be adjusted to a specific output voltage by using two external resistors (Figure 4-3). The resistors set the output voltage based on the equation:

EQUATION 4-1:

$$V_{OUT} = 1.242V \times \left(1 + \frac{R2}{R1}\right)$$

This equation is correct due to the configuration of the bandgap reference. The bandgap voltage is relative to the output, as seen in the Functional Diagrams. Traditional regulators normally have the reference voltage relative to ground; therefore, their equations are different from the equation for the MIC5209Y.

Although ADJ is a high-impedance input and, for best performance, R2 should not exceed 470 kΩ.

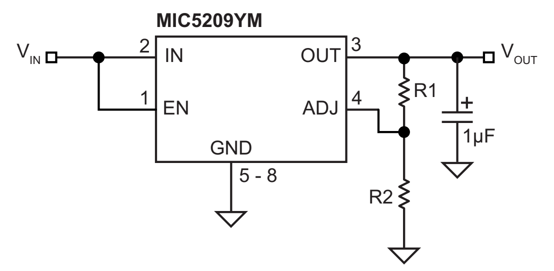


FIGURE 4-3: *Low-Noise Adjustable-Voltage Application.*

Figure 4-4 includes the optional 470 pF bypass capacitor from ADJ to GND to reduce output noise.

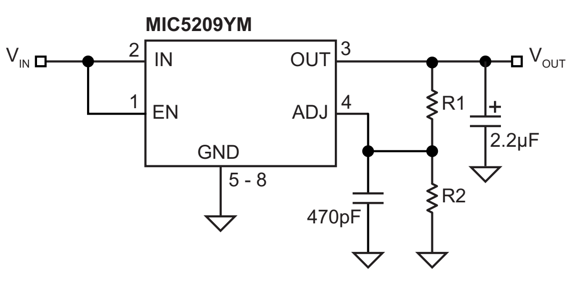


FIGURE 4-4: *Ultra-Low-Noise Adjustable Application.*

4.10 Slot-1 Power Supply

Intel's Pentium II processors have a requirement for a 2.5V ±5% power supply for a clock synthesizer and its associated loads. The current requirement for the 2.5V supply is dependent upon the clock synthesizer used, the number of clock outputs, and the type of level shifter (from core logic levels to 2.5V levels). Intel estimates a "worst-case" load of 320 mA.

The MIC5209 was designed to provide the 2.5V power requirement for Slot-1 applications. Its guaranteed performance of 2.5V ±3% at 500 mA allows adequate margin for all systems, and the dropout voltage of 500 mV means that it operates from a "worst-case" 3.3V supply where the voltage can be as low as 3.0V.

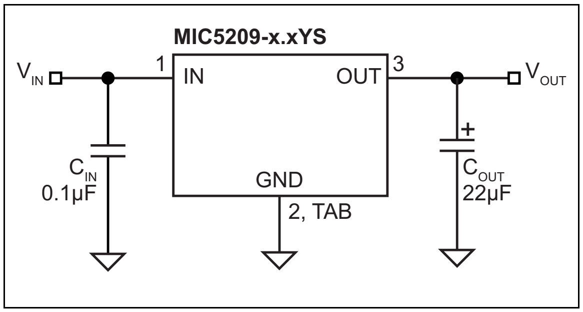


FIGURE 4-5: *Slot-1 Power Supply.*

A Slot-1 power supply (Figure 4-5) is easy to implement. Only two capacitors are necessary, and their values are not critical. C_{IN} bypasses the internal circuitry and should be at least 0.1 µF. C_{OUT} provides output filtering, improves transient response, and compensates the internal regulator control loop. Its value should be at least 22 µF. C_{IN} and C_{OUT} can be increased as much as desired.

4.10.1 SLOT-1 POWER SUPPLY POWER DISSIPATION

Powered from a 3.3V supply, the Slot-1 power supply illustrated in Figure 4-5 has a nominal efficiency of 75%. At the maximum anticipated Slot-1 load (320 mA), the nominal power dissipation is only 256 mW.

The SOT-223 package has sufficient thermal characteristics for wide design margins when mounted on a single-layer copper-clad printed circuit board. The power dissipation of the MIC5209 is calculated using the voltage drop across the device output current plus supply voltage ground current.

Considering "worst-case" tolerances, the power dissipation could be as high as:

EQUATION 4-2:

$$(V_{IN(MAX)} - V_{OUT(MAX)}) \times I_{OUT} + V_{IN(MAX)} \times I_{GND}$$

So:

EQUATION 4-3:

$$[(3.6V - 2.375V) \times 320mA] + (3.6V \times 4mA)$$

Resulting in:

EQUATION 4-4:

$$P_D = 407mW$$

Using the maximum junction temperature of +125°C and a θ_{JC} of 15°C/W for the SOT-223, 25°C/W for the SOIC-8, or 3°C/W for the DDPAK package, the following worst-case heat-sink thermal resistance (θ_{SA}) requirements are:

EQUATION 4-5:

$$\theta_{JA} = \frac{T_{J(MAX)} - T_A}{P_D}$$

Where: $\theta_{SA} = \theta_{JA} - \theta_{JC}$

Table 4-2 and Figure 4-6 show that the Slot-1 power supply application can be implemented with a minimum footprint layout.

TABLE 4-2: MAXIMUM ALLOWABLE THERMAL RESISTANCE

T_A	+40°C	+50°C	+60°C	+70°C
θ_{JA} Limit	209°C/W	184°C/W	160°C/W	135°C/W
θ_{SA} SOT-223	194°C/W	169°C/W	145°C/W	120°C/W
θ_{SA} SOIC-8	184°C/W	159°C/W	135°C/W	110°C/W
θ_{SA} DDPAK	206°C/W	181°C/W	157°C/W	132°C/W

Figure 4-6 shows the necessary copper pad area to obtain specific heatsink thermal resistance (θ_{SA}) values. The θ_{SA} values highlighted in Table 4-2 require much less than 500 mm^2 of copper and, per Figure 4-6, can be easily accomplished with the minimum footprint.

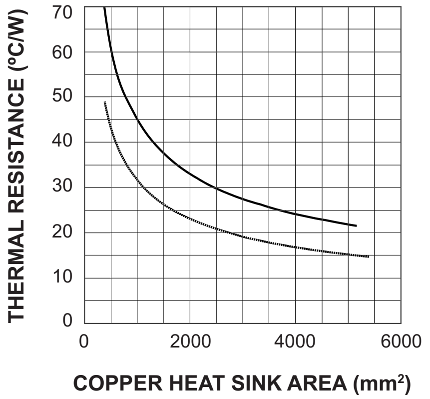
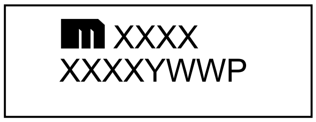


FIGURE 4-6: *PCB Heatsink Thermal Resistance.*

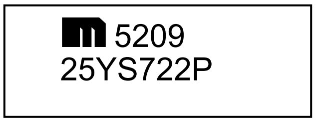
5.0 PACKAGING INFORMATION

5.1 Package Marking Information

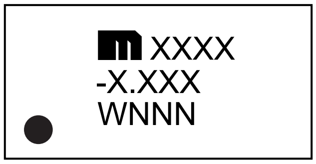
5-Pin SOT-223*



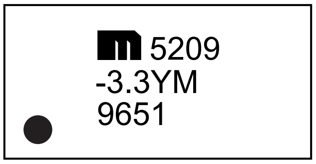
Example



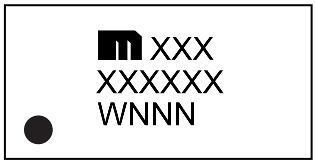
SOIC-8 (Fixed)*



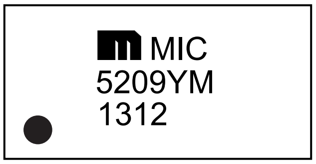
Example



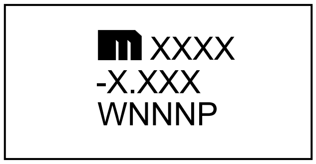
SOIC-8 (Adj.)*



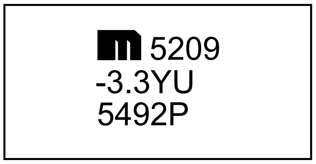
Example



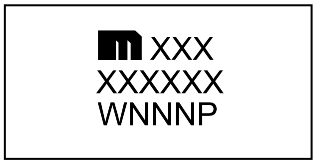
5-Pin DDPAK (Fixed)*



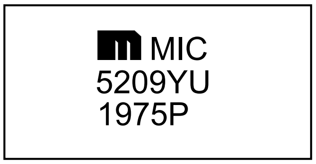
Example



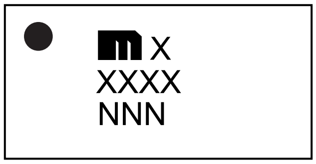
5-Pin DDPAK (Adj)*



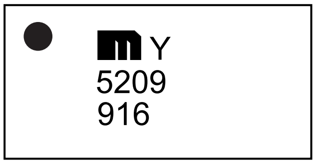
Example



8-Pin DFN*



Example



Legend:	XX...X	Product code or customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	e3	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.
	●, ▲, ▼	Pin one index is identified by a dot, delta up, or delta down (triangle mark).

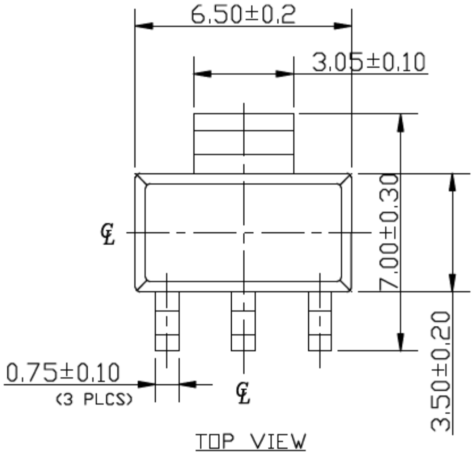
Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.

Underbar (_) and/or Overbar (¯) symbol may not be to scale.

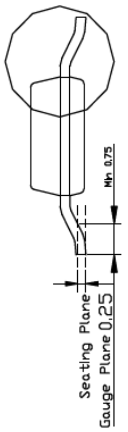
3-Lead SOT-223 Package Outline and Recommended Land Pattern

TITLE
3 LEAD SOT223 PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

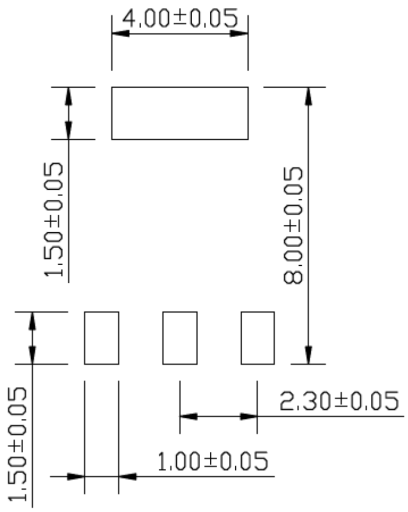
DRAWING #	SOT223-3LD-PL-1	**UNIT**	MM



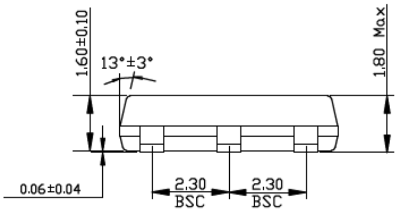
TOP VIEW



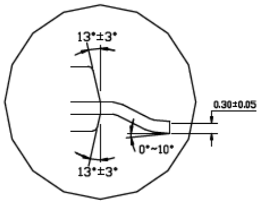
SIDE VIEW



RECOMMENDED
LAND PATTERN



SIDE VIEW



DETAILED VIEW

NOTE:

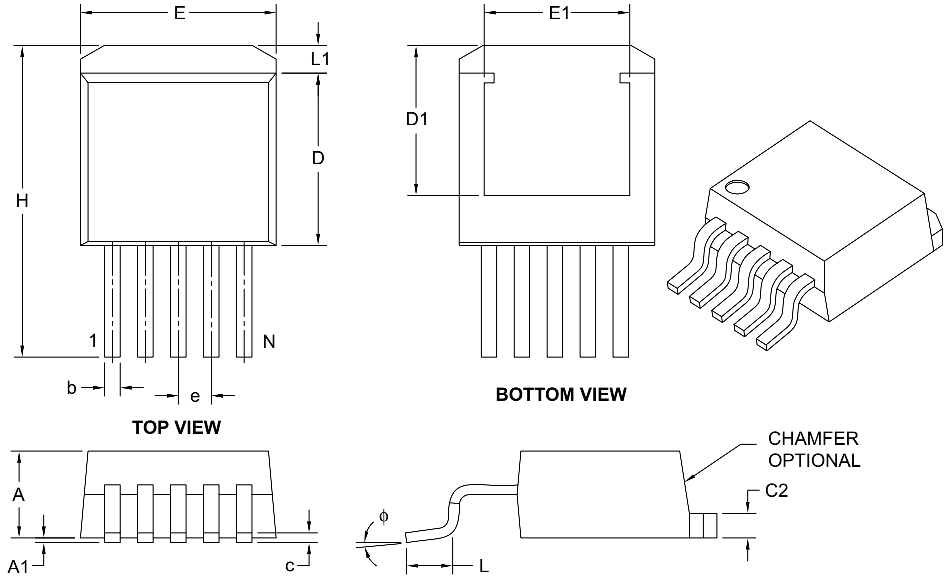
1. Dimensions and tolerances are as per ANSI Y14.5M, 1982.
2. Controlling dimension: Millimeters.
3. Dimensions are exclusive of mold flash and gate burr.
4. All specification comply to Jedec spec TO261 Issue C.

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

5-Lead DDPAK Package Outline and Recommended Land Pattern

5-Lead Plastic (ET) [DDPAK]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units	INCHES		
	Dimension Limits	MIN	NOM	MAX
Number of Pins	N		5	
Pitch	e		.067 BSC	
Overall Height	A	.160	–	.190
Standoff §	A1	.000	–	.010
Overall Width	E	.380	–	.420
Exposed Pad Width	E1	.245	–	–
Molded Package Length	D	.330	–	.380
Overall Length	H	.549	–	.625
Exposed Pad Length	D1	.270	–	–
Lead Thickness	c	.014	–	.029
Pad Thickness	C2	.045	–	.065
Lead Width	b	.020	–	.039
Foot Length	L	.068	–	.110
Pad Length	L1	–	–	.067
Foot Angle	ϕ	0°	–	8°

Notes:

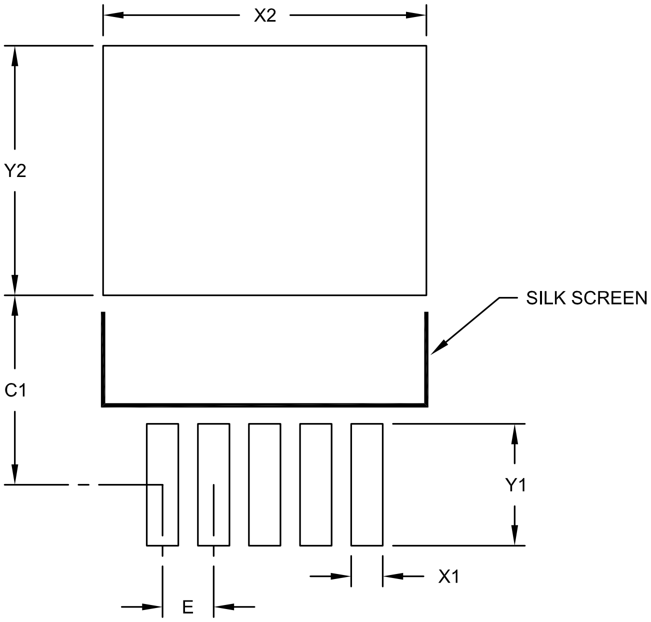
1. § Significant Characteristic.
2. Dimensions D and E do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .005" per side.
3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-012B

5-Lead Plastic (ET) [DDPAK]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

	Units	INCHES		
	Dimension Limits	MIN	NOM	MAX
Contact Pitch	E		.067 BSC	
Optional Center Pad Width	X2			.423
Optional Center Pad Length	Y2			.327
Contact Pad Spacing	C1		.248	
Contact Pad Width (X5)	X1			.041
Contact Pad Length (X5)	Y1			.159

Notes:

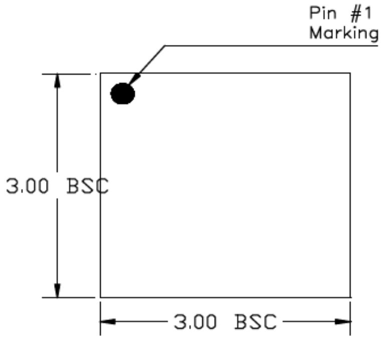
1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2012A

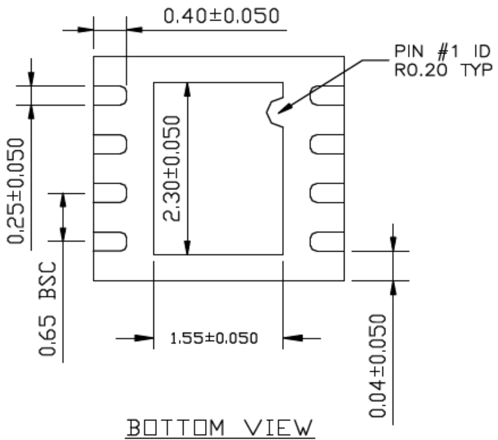
8-Lead 3 mm x 3 mm DFN Package Outline and Recommended Land Pattern

TITLE
8 LEAD DFN 3x3mm PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

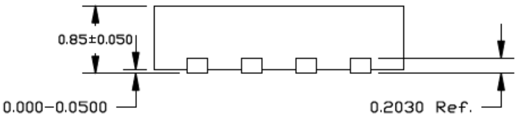
DRAWING #	DFN33-8LD-PL-1	**UNIT**	MM



TOP VIEW
NOTE: 1, 2, 3



BOTTOM VIEW
NOTE: 1, 2, 3

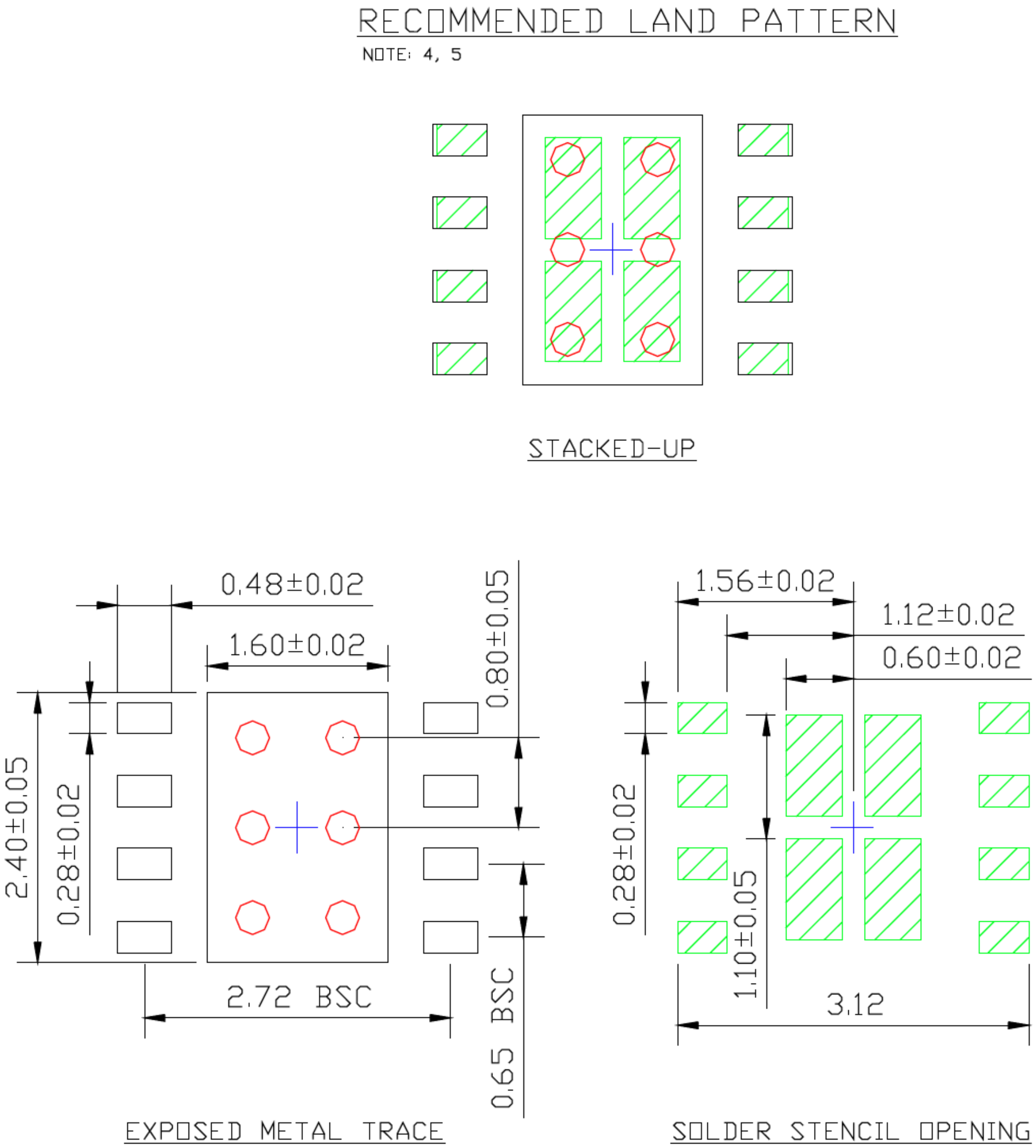


SIDE VIEW
NOTE: 1, 2, 3

NOTE:
1. MAX PACKAGE WARPAGE IS 0.05 MM
2. MAX ALLOWABLE BURR IS 0.076MM IN ALL DIRECTIONS
3. PIN #1 IS ON TOP WILL BE LASER MARKED
4. RED CIRCLE IN LAND PATTERN INDICATE THERMAL VIA. SIZE SHOULD BE 0.30–0.35 MM IN DIAMETER AND SHOULD BE CONNECTED TO GND FOR MAX THERMAL PERFORMANCE
5. GREEN RECTANGLES (SHADED AREA) INDICATE SOLDER STENCIL OPENING ON EXPOSED PAD AREA. SIZE SHOULD BE 0.50x0.90 MM IN SIZE, 0.20 MM SPACING.

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

POD-Land Pattern drawing #DFN33-8LD-PL-1

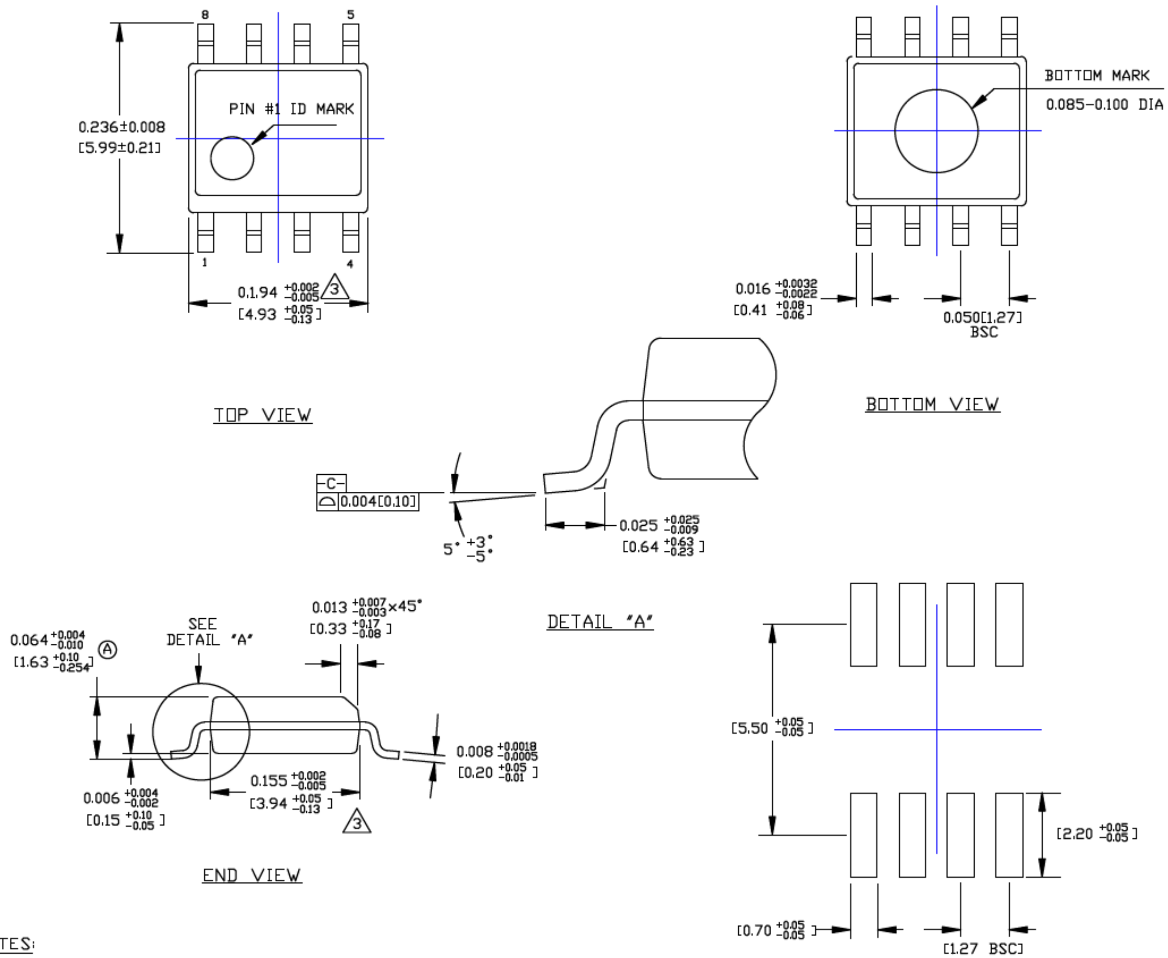


Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

8-Lead SOIC Package Outline and Recommended Land Pattern

TITLE
8 LEAD SOICN PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

DRAWING #	SOICN-8LD-PL-1	**UNIT**	INCH [MM]



NOTES:
1. DIMENSIONS ARE IN INCHES[MM].
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.010[0.25] PER SIDE.

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

NOTES:

APPENDIX A: REVISION HISTORY

Revision A (February 2017)

- Converted Micrel document MIC5209 to Microchip data sheet DS20005720A.
- Minor text changes throughout.
- Updated TO-263-5 packaging spec to DDPAK.
- Updated Thermal Resistance values to be current with Microchip packaging.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART NO.	**-**	**X.X**	**X**	**X**	**-**	**XX**
Device		**Voltage**	**Temperature**	**Package**		**Media Type**

Device: MIC5209: 500 mA Low Noise LDO Regulator

Voltage:
(blank) = Adjustable
1.8 = 1.8V
2.5 = 2.5V
3.0 = 3.0V
3.3 = 3.3V
3.6 = 3.6V
4.2 = 4.2V
5.0 = 5.0V

Temperature: Y = –40°C to +125°C

Package:
M = 8-Lead SOIC
ML = 8-Lead DFN
S = 3-Lead SOT-223
U = 5-Lead DDPAK

Media Type:
TR = 2,500/Reel (SOIC, SOT-223)
TR = 750/Reel (DDPAK)
TR = 5,000/Reel (DFN)
T5 = 500/Reel (DFN)
(blank)= 50/Tube (DDPAK)
(blank)= 78/Tube (SOT-223)
(blank)= 95/Tube (SOIC)

Examples:

a) MIC5209-1.8YM-TR:	500 mA Low-Noise LDO Regulator, 1.8V Voltage, –40°C to +125°C Temp. Range, 8-Lead SOIC, 2,500/Reel
b) MIC5209-1.8YM:	500 mA Low-Noise LDO Regulator, 1.8V Voltage, –40°C to +125°C Temp. Range, 8-Lead SOIC, 95/Tube
c) MIC5209-2.5YU-TR:	500 mA Low-Noise LDO Regulator, 2.5V Voltage, –40°C to +125°C Temp. Range, 5-Lead DDPAK, 750/Reel
d) MIC5209-2.5YU:	500 mA Low-Noise LDO Regulator, 2.5V Voltage, –40°C to +125°C Temp. Range, 5-Lead DDPAK, 50/Tube
e) MIC5209-3.0YS-TR:	500 mA Low-Noise LDO Regulator, 3.0V Voltage, –40°C to +125°C Temp. Range, 3-Lead SOT-223, 2,500/Reel
f) MIC5209-3.0YS:	500 mA Low-Noise LDO Regulator, 3.0V Voltage, –40°C to +125°C Temp. Range, 3-Lead SOT-223, 78/Tube
g) MIC5209YML-TR:	500 mA Low-Noise LDO Regulator, Adj. Voltage, –40°C to +125°C Temp. Range, 8-Lead DFN, 5,000/Reel
h) MIC5209YML-T5:	500 mA Low-Noise LDO Regulator, Adj. Voltage, –40°C to +125°C Temp. Range, 8-Lead DFN, 500/Reel

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

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- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

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