■ A/D converter
- SAR-type
- 8/10-bit resolution
- Signals interrupt on conversion end, single conversion mode, continuous conversion mode, stop conversion mode, activation by software, external trigger, reload timers and PPGs
- Range Comparator Function
- Scan Disable Function
- ADC Pulse Detection Function

■ Source Clock Timers

Three independent clock timers (23-bit RC clock timer, 23-bit Main clock timer, 17-bit Sub clock timer)

■ Hardware Watchdog Timer
- Hardware watchdog timer is active after reset
- Window function of Watchdog Timer is used to select the lower window limit of the watchdog interval

■ Reload Timers
- 16-bit wide
- Prescaler with $1/2^1$, $1/2^2$, $1/2^3$, $1/2^4$, $1/2^5$, $1/2^6$ of peripheral clock frequency
- Event count function

■ Free-Running Timers
- Signals an interrupt on overflow
- Prescaler with 1, $1/2^1$, $1/2^2$, $1/2^3$, $1/2^4$, $1/2^5$, $1/2^6$, $1/2^7$, $1/2^8$ of peripheral clock frequency

■ Input Capture Units
- 16-bit wide
- Signals an interrupt upon external event
- Rising edge, Falling edge or Both (rising & falling) edges sensitive

■ Programmable Pulse Generator
- 16-bit down counter, cycle and duty setting registers
- Can be used as 2 × 8-bit PPG
- Interrupt at trigger, counter borrow and/or duty match
- PWM operation and one-shot operation
- Internal prescaler allows 1, 1/4, 1/16, 1/64 of peripheral clock as counter clock or of selected Reload timer underflow as clock input
- Can be triggered by software or reload timer
- Can trigger ADC conversion
- Timing point capture

■ Stepping Motor Controller
- Stepping Motor Controller with integrated high current output drivers
- Four high current outputs for each channel
- Two synchronized 8/10-bit PWMs per channel
- Internal prescaling for PWM clock: 1, 1/4, 1/5, 1/6, 1/8, 1/10, 1/12, 1/16 of peripheral clock
- Dedicated power supply for high current output drivers

■ LCD Controller
- LCD controller with up to 4COM × 32SEG
- Internal or external voltage generation
- Duty cycle: Selectable from options: 1/2, 1/3 and 1/4
- Fixed 1/3 bias
- Programmable frame period
- Clock source selectable from four options (main clock, peripheral clock, subclock or RC oscillator clock)
- Internal divider resistors or external divider resistors
- On-chip data memory for display
- LCD display can be operated in Timer Mode
- Blank display: selectable
- All SEG, COM and V pins can be switched between general and specialized purposes

■ Sound Generator
- 8-bit PWM signal is mixed with tone frequency from 16-bit reload counter
- PWM clock by internal prescaler: 1, 1/2, 1/4, 1/8 of peripheral clock

■ Real Time Clock
- Operational on main oscillation (4MHz), sub oscillation (32kHz) or RC oscillation (100kHz/2MHz)
- Capable to correct oscillation deviation of Sub clock or RC oscillator clock (clock calibration)
- Read/write accessible second/minute/hour registers
- Can signal interrupt every half second/second/minute/hour/day
- Internal clock divider and prescaler provide exact 1s clock

■ External Interrupts
- Edge or Level sensitive
- Interrupt mask bit per channel
- Each available CAN channel RX has an external interrupt for wake-up
- Selected USART channels SIN have an external interrupt for wake-up

■ Non Maskable Interrupt
- Disabled after reset, can be enabled by Boot-ROM depending on ROM configuration block
- Once enabled, cannot be disabled other than by reset
- High or Low level sensitive
- Pin shared with external interrupt 0

■ I/O Ports
- Most of the external pins can be used as general purpose I/O
- All push-pull outputs (except when used as I^2C SDA/SCL line)
- Bit-wise programmable as input/output or peripheral signal
- Bit-wise programmable input enable
- One input level per GPIO-pin (either Automotive or CMOS hysteresis)
- Bit-wise programmable pull-up resistor

- Built-in On Chip Debugger (OCD)
  - One-wire debug tool interface
  - Break function:
    - Hardware break: 6 points (shared with code event)
    - Software break: 4096 points
  - Event function
    - Code event: 6 points (shared with hardware break)
    - Data event: 6 points
    - Event sequencer: 2 levels + reset
  - Execution time measurement function
  - Trace function: 42 branches
  - Security function
- Flash Memory
  - Dual operation flash allowing reading of one Flash bank while programming or erasing the other bank
  - Command sequencer for automatic execution of programming algorithm and for supporting DMA for programming of the Flash Memory
  - Supports automatic programming, Embedded Algorithm
  - Write/Erase/Erase-Suspend/Resume commands
  - A flag indicating completion of the automatic algorithm
  - Erase can be performed on each sector individually
  - Sector protection
  - Flash Security feature to protect the content of the Flash
  - Low voltage detection during Flash erases or writes

Contents

1. Product Lineup

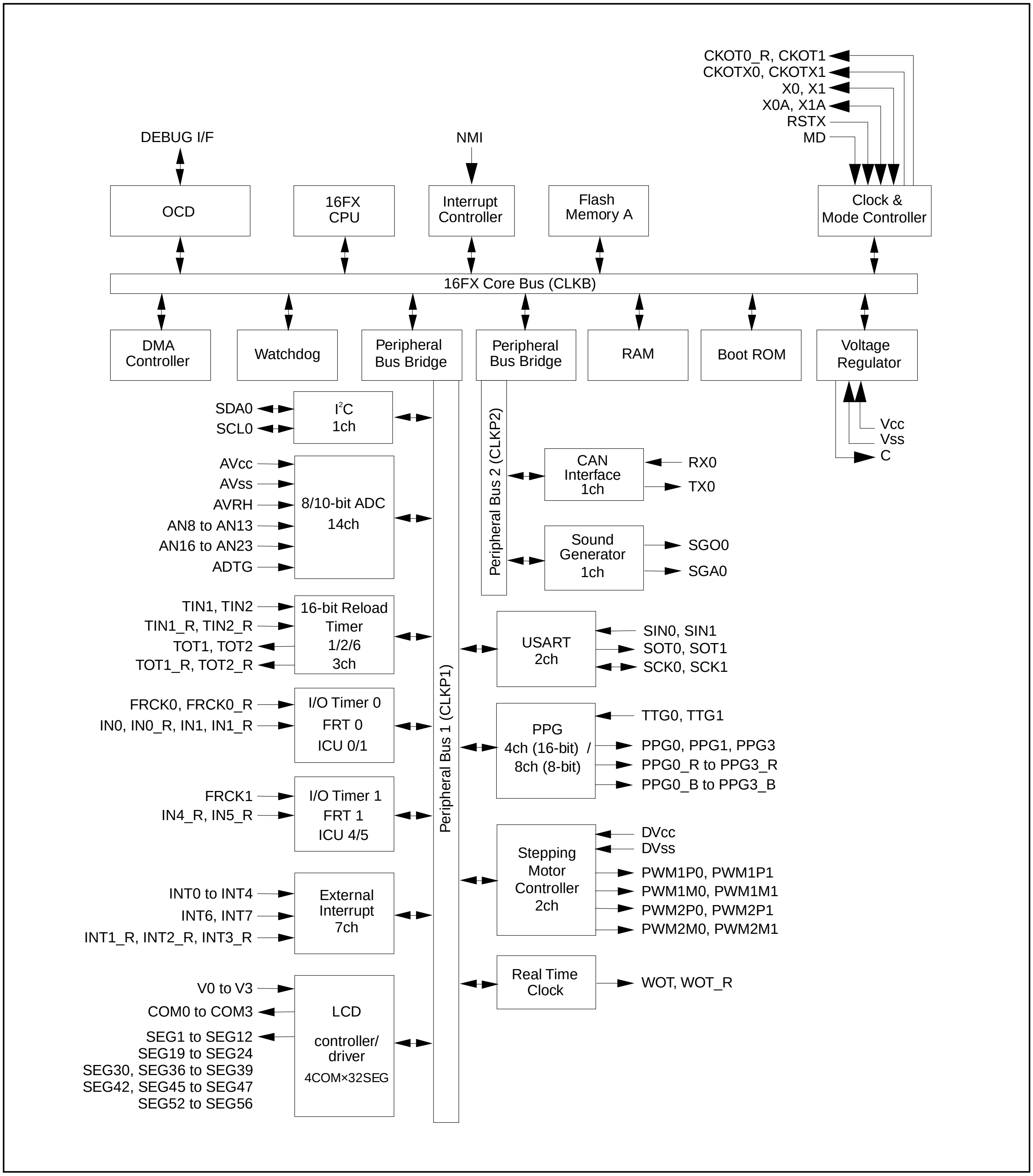
Features		MB96680	Remark
Product Type		Flash Memory Product	
Subclock		Subclock can be set by software	
Dual Operation Flash Memory	RAM	-	
64.5KB + 32KB	4KB	MB96F683R, MB96F683A	Product Options R: MCU with CAN A: MCU without CAN
128.5KB + 32KB	4KB	MB96F685R, MB96F685A	
Package		LQFP-80 FPT-80P-M21	
DMA		2ch	
USART		2ch	LIN-USART 0/1
	with automatic LIN-Header transmission/reception	Yes (only 1ch)	LIN-USART 0
	with 16 byte RX- and TX-FIFO	No	
I^2C		1ch	I^2C 0
8/10-bit A/D Converter		14ch	AN 8 to 13/16 to 23
	with Data Buffer	No	
	with Range Comparator	Yes	
	with Scan Disable	Yes	
	with ADC Pulse Detection	Yes	
16-bit Reload Timer (RLT)		3ch	RLT 1/2/6
16-bit Free-Running Timer (FRT)		2ch	FRT 0/1
16-bit Input Capture Unit (ICU)		4ch (2 channels for LIN-USART)	ICU 0/1/4/5 (ICU 0/1 for LIN-USART)
8/16-bit Programmable Pulse Generator (PPG)		4ch (16-bit) / 8ch (8-bit)	PPG 0 to 3
	with Timing point capture	Yes	
	with Start delay	No	
	with Ramp	No	
CAN Interface		1ch	CAN 0 32 Message Buffers
Stepping Motor Controller (SMC)		2ch	SMC 0/1
External Interrupts (INT)		7ch	INT 0 to 4/6/7
Non-Maskable Interrupt (NMI)		1ch	
Sound Generator (SG)		1ch	SG 0
LCD Controller		4COM × 32SEG	COM 0 to 3 SEG 1 to 12/19 to 24/ 30/36 to 39/42/45 to 47/ 52 to 56
Real Time Clock (RTC)		1ch	
I/O Ports		63 (Dual clock mode) 65 (Single clock mode)	
Clock Calibration Unit (CAL)		1ch	
Clock Output Function		2ch	
Low Voltage Detection Function		Yes	Low voltage detection function can be disabled by software
Hardware Watchdog Timer		Yes	
On-chip RC-oscillator		Yes	
On-chip Debugger		Yes	

Note:

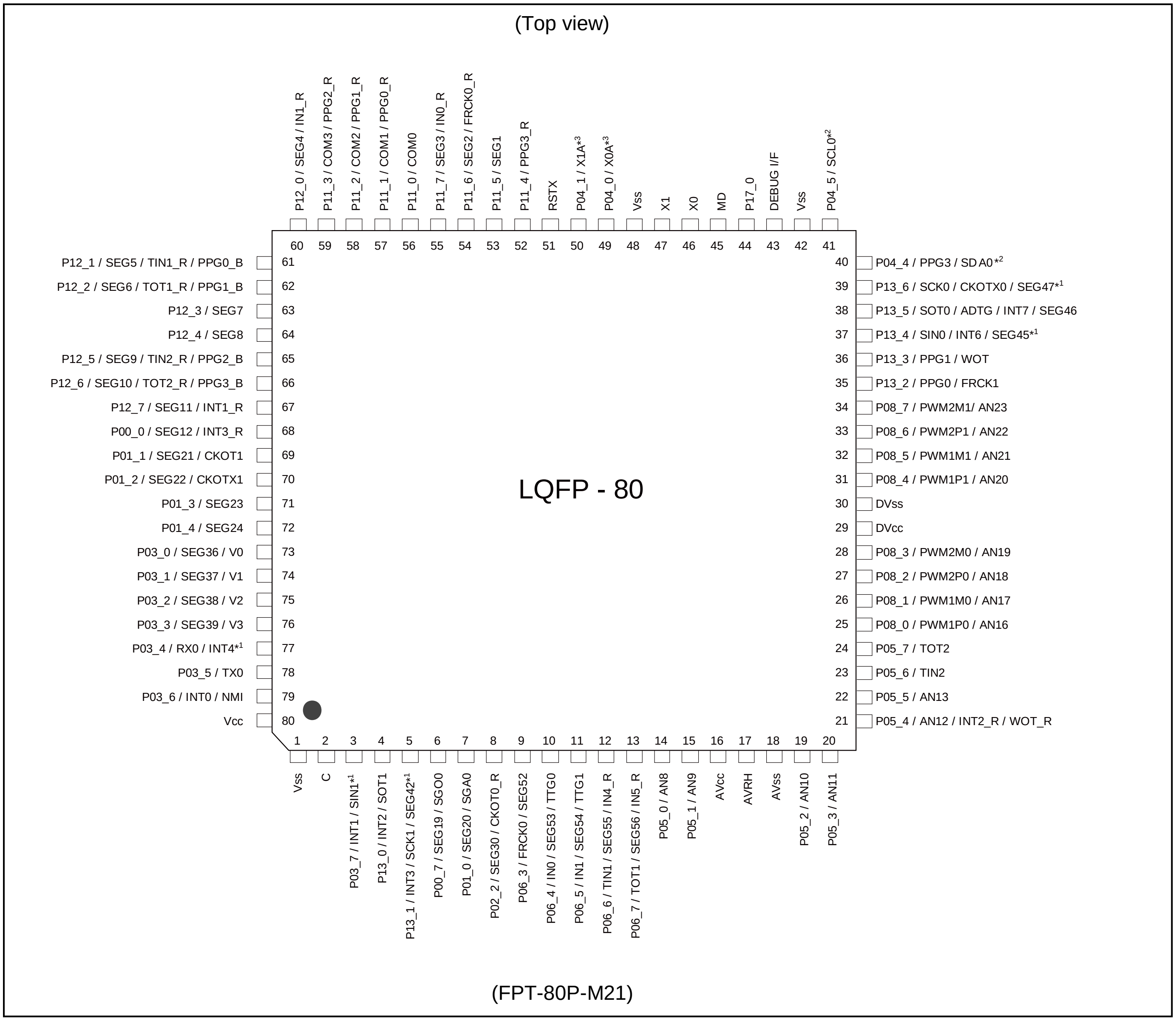
All signals of the peripheral function in each product cannot be allocated by limiting the pins of package.

It is necessary to use the port relocate function of the general I/O port according to your function use.

2. Block Diagram



3. Pin Assignment



*[1]: CMOS input level only

*[2]: CMOS input level only for I^2C

*[3]: Please set ROM Configuration Block (RCB) to use the sub clock.

Other than those above, general-purpose pins have only automotive input level.

4. Pin Description

Pin name	Feature	Description
ADTG	ADC	A/D converter trigger input pin
ANn	ADC	A/D converter channel n input pin
AVcc	Supply	Analog circuits power supply pin
AVRH	ADC	A/D converter high reference voltage input pin
AVss	Supply	Analog circuits power supply pin
C	Voltage regulator	Internally regulated power supply stabilization capacitor pin
CKOTn	Clock Output function	Clock Output function n output pin
CKOTn_R	Clock Output function	Relocated Clock Output function n output pin
CKOTXn	Clock Output function	Clock Output function n inverted output pin
COMn	LCD	LCD Common driver pin
DEBUG I/F	OCD	On Chip Debugger input/output pin
DVcc	Supply	SMC pins power supply
DVss	Supply	SMC pins power supply
FRCKn	Free-Running Timer	Free-Running Timer n input pin
FRCKn_R	Free-Running Timer	Relocated Free-Running Timer n input pin
INn	ICU	Input Capture Unit n input pin
INn_R	ICU	Relocated Input Capture Unit n input pin
INTn	External Interrupt	External Interrupt n input pin
INTn_R	External Interrupt	Relocated External Interrupt n input pin
MD	Core	Input pin for specifying the operating mode
NMI	External Interrupt	Non-Maskable Interrupt input pin
Pnn_m	GPIO	General purpose I/O pin
PPGn	PPG	Programmable Pulse Generator n output pin (16bit/8bit)
PPGn_R	PPG	Relocated Programmable Pulse Generator n output pin (16bit/8bit)
PPGn_B	PPG	Programmable Pulse Generator n output pin (16bit/8bit)
PWMn	SMC	SMC PWM high current output pin
RSTX	Core	Reset input pin
RXn	CAN	CAN interface n RX input pin
SCKn	USART	USART n serial clock input/output pin
SCLn	I^2C	I^2C interface n clock I/O input/output pin
SDAn	I^2C	I^2C interface n serial data I/O input/output pin
SEGn	LCD	LCD Segment driver pin
SGAn	Sound Generator	Sound Generator amplitude output pin
SGOn	Sound Generator	Sound Generator sound/tone output pin
SINn	USART	USART n serial data input pin
SOTn	USART	USART n serial data output pin
TINn	Reload Timer	Reload Timer n event input pin
TINn_R	Reload Timer	Relocated Reload Timer n event input pin
TOTn	Reload Timer	Reload Timer n output pin
TOTn_R	Reload Timer	Relocated Reload Timer n output pin

Pin name	Feature	Description
TTGn	PPG	Programmable Pulse Generator n trigger input pin
TXn	CAN	CAN interface n TX output pin
Vn	LCD	LCD voltage reference pin
Vcc	Supply	Power supply pin
Vss	Supply	Power supply pin
WOT	RTC	Real Time clock output pin
WOT_R	RTC	Relocated Real Time clock output pin
X0	Clock	Oscillator input pin
X0A	Clock	Subclock Oscillator input pin
X1	Clock	Oscillator output pin
X1A	Clock	Subclock Oscillator output pin

5. Pin Circuit Type

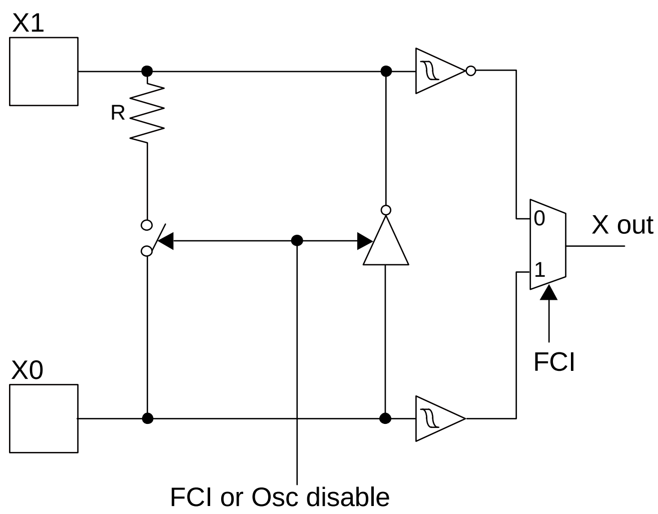
Pin no.	I/O circuit type*	Pin name
1	Supply	V_{ss}
2	F	C
3	M	P03_7 / INT1 / SIN1
4	H	P13_0 / INT2 / SOT1
5	P	P13_1 / INT3 / SCK1 / SEG42
6	J	P00_7 / SEG19 / SGO0
7	J	P01_0 / SEG20 / SGA0
8	J	P02_2 / SEG30 / CKOT0_R
9	J	P06_3 / FRCK0 / SEG52
10	J	P06_4 / IN0 / SEG53 / TTG0
11	J	P06_5 / IN1 / SEG54 / TTG1
12	J	P06_6 / TIN1 / SEG55 / IN4_R
13	J	P06_7 / TOT1 / SEG56 / IN5_R
14	K	P05_0 / AN8
15	K	P05_1 / AN9
16	Supply	AV_{cc}
17	G	AVRH
18	Supply	AV_{ss}
19	K	P05_2 / AN10
20	K	P05_3 / AN11
21	K	P05_4 / AN12 / INT2_R / WOT_R
22	K	P05_5 / AN13
23	H	P05_6 / TIN2
24	H	P05_7 / TOT2
25	R	P08_0 / PWM1P0 / AN16
26	R	P08_1 / PWM1M0 / AN17
27	R	P08_2 / PWM2P0 / AN18
28	R	P08_3 / PWM2M0 / AN19
29	Supply	DV_{cc}
30	Supply	DV_{ss}
31	R	P08_4 / PWM1P1 / AN20
32	R	P08_5 / PWM1M1 / AN21
33	R	P08_6 / PWM2P1 / AN22
34	R	P08_7 / PWM2M1 / AN23
35	H	P13_2 / PPG0 / FRCK1
36	H	P13_3 / PPG1 / WOT
37	P	P13_4 / SIN0 / INT6 / SEG45

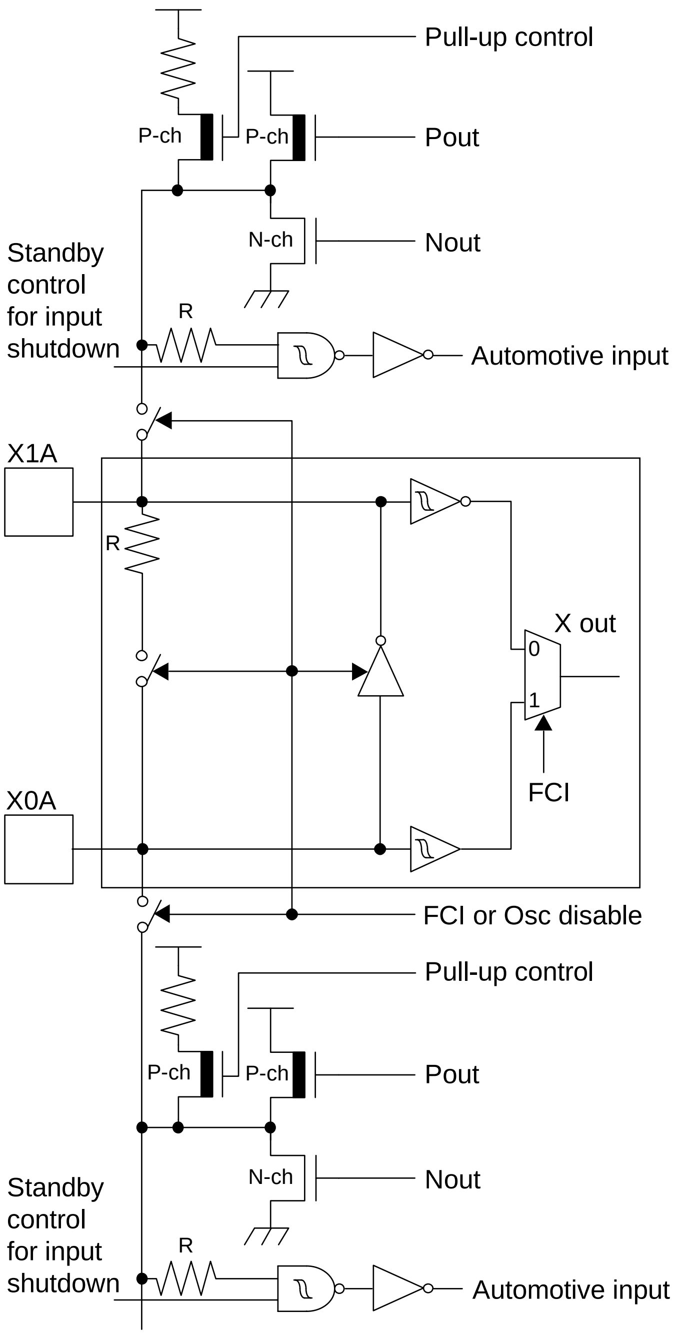
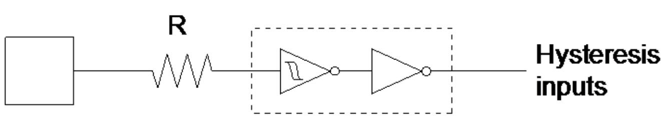
Pin no.	I/O circuit type*	Pin name
38	J	P13_5 / SOT0 / ADTG / INT7 / SEG46
39	P	P13_6 / SCK0 / CKOTX0 / SEG47
40	N	P04_4 / PPG3 / SDA0
41	N	P04_5 / SCL0
42	Supply	V_{SS}
43	O	DEBUG I/F
44	H	P17_0
45	C	MD
46	A	X0
47	A	X1
48	Supply	V_{SS}
49	B	P04_0 / X0A
50	B	P04_1 / X1A
51	C	RSTX
52	H	P11_4 / PPG3_R
53	J	P11_5 / SEG1
54	J	P11_6 / SEG2 / FRCK0_R
55	J	P11_7 / SEG3 / IN0_R
56	J	P11_0 / COM0
57	J	P11_1 / COM1 / PPG0_R
58	J	P11_2 / COM2 / PPG1_R
59	J	P11_3 / COM3 / PPG2_R
60	J	P12_0 / SEG4 / IN1_R
61	J	P12_1 / SEG5 / TIN1_R / PPG0_B
62	J	P12_2 / SEG6 / TOT1_R / PPG1_B
63	J	P12_3 / SEG7
64	J	P12_4 / SEG8
65	J	P12_5 / SEG9 / TIN2_R / PPG2_B
66	J	P12_6 / SEG10 / TOT2_R / PPG3_B
67	J	P12_7 / SEG11 / INT1_R
68	J	P00_0 / SEG12 / INT3_R
69	J	P01_1 / SEG21 / CKOT1
70	J	P01_2 / SEG22 / CKOTX1
71	J	P01_3 / SEG23
72	J	P01_4 / SEG24
73	L	P03_0 / SEG36 / V0
74	L	P03_1 / SEG37 / V1
75	L	P03_2 / SEG38 / V2
76	L	P03_3 / SEG39 / V3

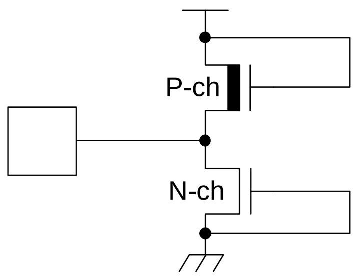
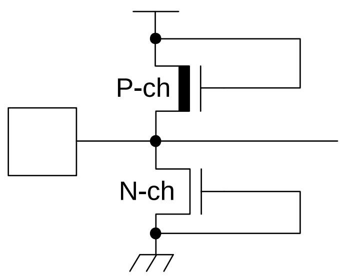
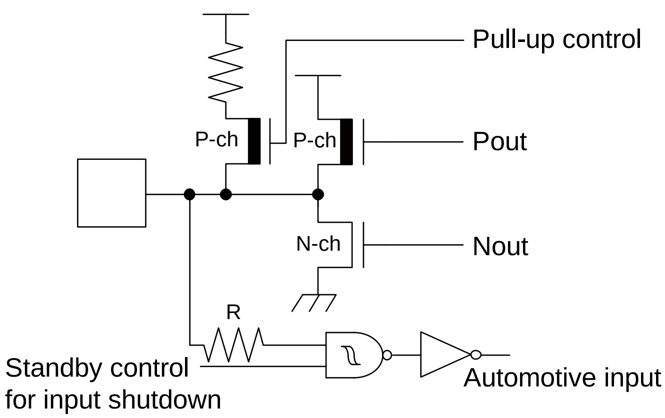
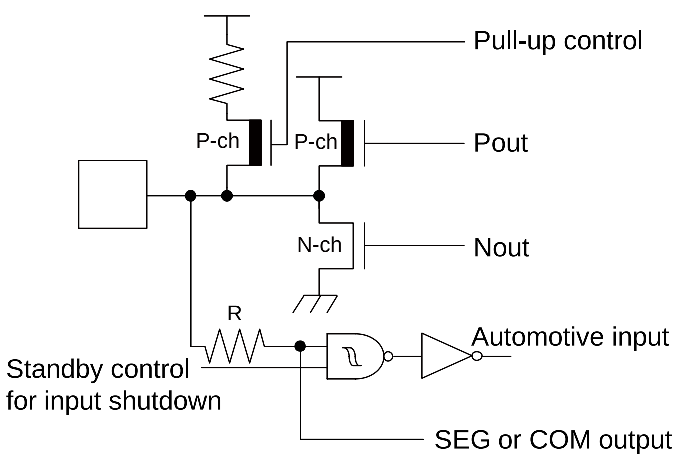
Pin no.	I/O circuit type*	Pin name
77	M	P03_4 / RX0 / INT4
78	H	P03_5 / TX0
79	H	P03_6 / INT0 / NMI
80	Supply	V_{cc}

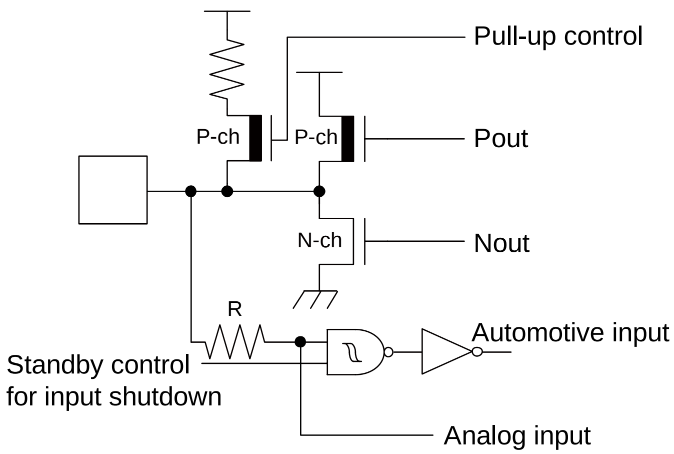
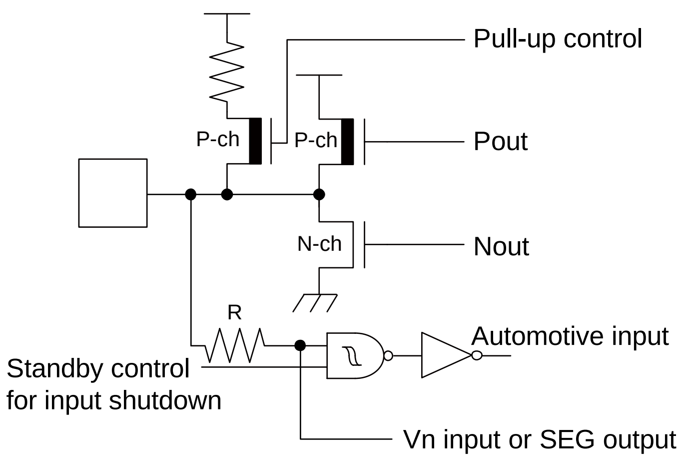
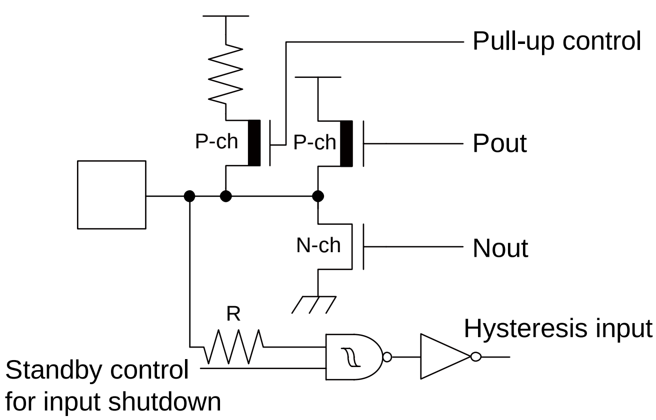
*: See “I/O Circuit Type” for details on the I/O circuit types.

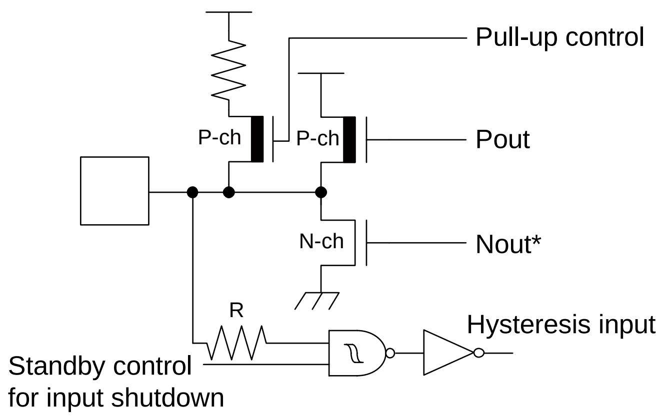
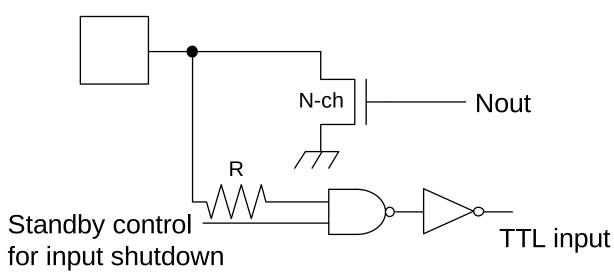
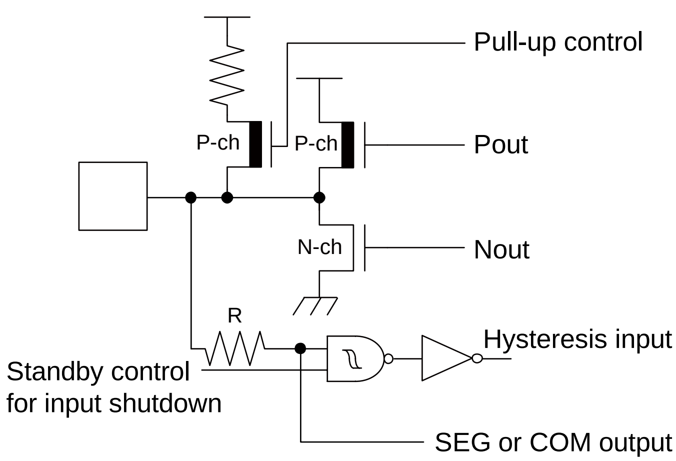
6. I/O Circuit Type

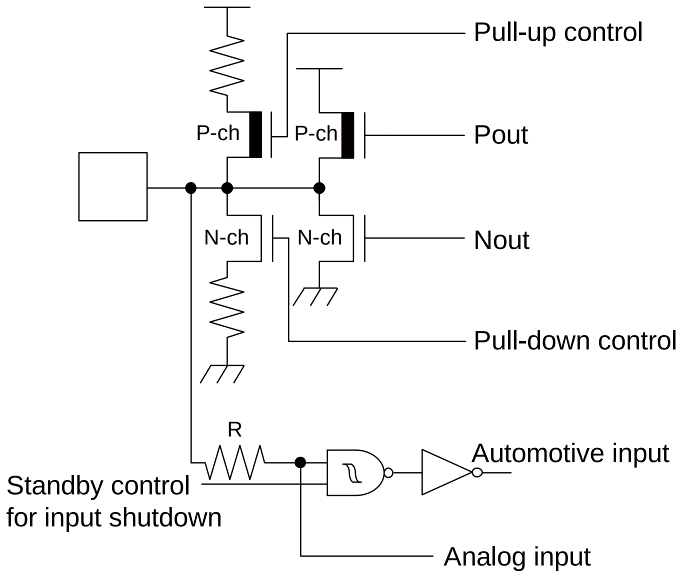
Type	Circuit	Remarks
A		High-speed oscillation circuit: • Programmable between oscillation mode (external crystal or resonator connected to X0/X1 pins) and Fast external Clock Input (FCI) mode (external clock connected to X0 pin) • Feedback resistor = approx. 1.0MΩ • The amplitude: 1.8V±0.15V to operate by the internal supply voltage

Type	Circuit	Remarks
B		Low-speed oscillation circuit shared with GPIO functionality: • Feedback resistor = approx. 5.0MΩ • GPIO functionality selectable (CMOS level output (I_{OL} = 4mA, I_{OH} = -4mA), Automotive input with input shutdown function and programmable pull-up resistor)
C		CMOS hysteresis input pin

Type	Circuit	Remarks
F		Power supply input protection circuit
G		• A/D converter ref+ (AVRH) power supply input pin with protection circuit • Without protection circuit against V_{CC} for pins AVRH
H		• CMOS level output (I_{OL} = 4mA, I_{OH} = -4mA) • Automotive input with input shutdown function • Programmable pull-up resistor
J		• CMOS level output (I_{OL} = 4mA, I_{OH} = -4mA) • Automotive input with input shutdown function • Programmable pull-up resistor • SEG or COM output

Type	Circuit	Remarks
K		• CMOS level output (I_{OL} = 4mA, I_{OH} = -4mA) • Automotive input with input shutdown function • Programmable pull-up resistor • Analog input
L		• CMOS level output (I_{OL} = 4mA, I_{OH} = -4mA) • Automotive input with input shutdown function • Programmable pull-up resistor • Vn input or SEG output
M		• CMOS level output (I_{OL} = 4mA, I_{OH} = -4mA) • CMOS hysteresis input with input shutdown function • Programmable pull-up resistor

<table>
<tr><th>Type</th><th>Circuit</th><th>Remarks</th></tr>
<tr><td>N</td><td>
</td><td>• CMOS level output
(I_{OL} = 3mA, I_{OH} = -3mA)
• CMOS hysteresis input with input shutdown function
• Programmable pull-up resistor
*: N-channel transistor has slew rate control according to I^2C spec, irrespective of usage.</td></tr>
<tr><td>O</td><td>
</td><td>• Open-drain I/O
• Output 25mA, V_{cc} = 2.7V
• TTL input</td></tr>
<tr><td>P</td><td>
</td><td>• CMOS level output
(I_{OL} = 4mA, I_{OH} = -4mA)
• CMOS hysteresis inputs with input shutdown function
• Programmable pull-up resistor
• SEG or COM output</td></tr>
</table>

Type	Circuit	Remarks
R		• CMOS level output (programmable I_{OL} = 4mA, I_{OH} = -4mA and I_{OL} = 30mA, I_{OH} = -30mA) • Automotive input with input shutdown function • Programmable pull-up / pull-down resistor • Analog input

7. Memory Map

Address	Area
FF:FFFF$_H$ – DE:0000$_H$	USER ROM*1
DD:FFFF$_H$ – 10:0000$_H$	Reserved
0F:C000$_H$	Boot-ROM
0E:9000$_H$	Peripheral
01:0000$_H$	Reserved
00:8000$_H$	ROM/RAM MIRROR
RAMSTART0*2	Internal RAM bank0
00:0C00$_H$	Reserved
00:0380$_H$	Peripheral
00:0180$_H$	GPR*3
00:0100$_H$	DMA
00:00F0$_H$	Reserved
00:0000$_H$	Peripheral

*1: For details about USER ROM area, see “User ROM Memory Map For Flash Devices” on the following pages.

*2: For RAMSTART addresses see the table on the next page.

*3: Unused GPR banks can be used as RAM area.

GPR: General-Purpose Register

The DMA area is only available if the device contains the corresponding resource.

The available RAM and ROM area depends on the device.

8. RAMSTART Addresses

Devices	Bank 0 RAM size	RAMSTART0
MB96F683 MB96F685	4KB	$00{:}7200_H$

9. User ROM Memory Map For Flash Devices

CPU mode address	Flash memory mode address	MB96F683 Flash size 64.5KB + 32KB	MB96F685 Flash size 128.5KB + 32KB	
FF:FFFF$_H$ FF:0000$_H$	3F:FFFF$_H$ 3F:0000$_H$	SA39 - 64KB	SA39 - 64KB	Bank A of Flash A
FE:FFFF$_H$ FE:0000$_H$	3E:FFFF$_H$ 3E:0000$_H$	Reserved	SA38 - 64KB	Bank A of Flash A
FD:FFFF$_H$ DF:A000$_H$		Reserved	Reserved	
DF:9FFF$_H$ DF:8000$_H$	1F:9FFF$_H$ 1F:8000$_H$	SA4 - 8KB	SA4 - 8KB	Bank B of Flash A
DF:7FFF$_H$ DF:6000$_H$	1F:7FFF$_H$ 1F:6000$_H$	SA3 - 8KB	SA3 - 8KB	Bank B of Flash A
DF:5FFF$_H$ DF:4000$_H$	1F:5FFF$_H$ 1F:4000$_H$	SA2 - 8KB	SA2 - 8KB	Bank B of Flash A
DF:3FFF$_H$ DF:2000$_H$	1F:3FFF$_H$ 1F:2000$_H$	SA1 - 8KB	SA1 - 8KB	Bank B of Flash A
DF:1FFF$_H$ DF:0000$_H$	1F:1FFF$_H$ 1F:0000$_H$	SAS - 512B*	SAS - 512B*	Bank A of Flash A
DE:FFFF$_H$ DE:0000$_H$		Reserved	Reserved	

*: Physical address area of SAS-512B is from DF:0000$_H$ to DF:01FF$_H$.
Others (from DF:0200$_H$ to DF:1FFF$_H$) is mirror area of SAS-512B.
Sector SAS contains the ROM configuration block RCBA at CPU address DF: 0000$_H$ -DF:01FF$_H$.
SAS cannot be used for E^2PROM emulation.

10. Serial Programming Communication Interface

USART pins for Flash serial programming (MD = 0, DEBUG I/F = 0, Serial Communication mode)

MB96680		
Pin Number	**USART Number**	**Normal Function**
37	USART0	SIN0
38		SOT0
39		SCK0
3	USART1	SIN1
4		SOT1
5		SCK1

11. Interrupt Vector Table

Vector number	Offset in vector table	Vector name	Cleared by DMA	Index in ICR to program	Description
0	$3FC_H$	CALLV0	No	-	CALLV instruction
1	$3F8_H$	CALLV1	No	-	CALLV instruction
2	$3F4_H$	CALLV2	No	-	CALLV instruction
3	$3F0_H$	CALLV3	No	-	CALLV instruction
4	$3EC_H$	CALLV4	No	-	CALLV instruction
5	$3E8_H$	CALLV5	No	-	CALLV instruction
6	$3E4_H$	CALLV6	No	-	CALLV instruction
7	$3E0_H$	CALLV7	No	-	CALLV instruction
8	$3DC_H$	RESET	No	-	Reset vector
9	$3D8_H$	INT9	No	-	INT9 instruction
10	$3D4_H$	EXCEPTION	No	-	Undefined instruction execution
11	$3D0_H$	NMI	No	-	Non-Maskable Interrupt
12	$3CC_H$	DLY	No	12	Delayed Interrupt
13	$3C8_H$	RC_TIMER	No	13	RC Clock Timer
14	$3C4_H$	MC_TIMER	No	14	Main Clock Timer
15	$3C0_H$	SC_TIMER	No	15	Sub Clock Timer
16	$3BC_H$	LVDI	No	16	Low Voltage Detector
17	$3B8_H$	EXTINT0	Yes	17	External Interrupt 0
18	$3B4_H$	EXTINT1	Yes	18	External Interrupt 1
19	$3B0_H$	EXTINT2	Yes	19	External Interrupt 2
20	$3AC_H$	EXTINT3	Yes	20	External Interrupt 3
21	$3A8_H$	EXTINT4	Yes	21	External Interrupt 4
22	$3A4_H$	-	-	22	Reserved
23	$3A0_H$	EXTINT6	Yes	23	External Interrupt 6
24	$39C_H$	EXTINT7	Yes	24	External Interrupt 7
25	398_H	-	-	25	Reserved
26	394_H	-	-	26	Reserved
27	390_H	-	-	27	Reserved
28	$38C_H$	-	-	28	Reserved
29	388_H	-	-	29	Reserved
30	384_H	-	-	30	Reserved
31	380_H	-	-	31	Reserved
32	$37C_H$	-	-	32	Reserved
33	378_H	CAN0	No	33	CAN Controller 0
34	374_H	-	-	34	Reserved
35	370_H	-	-	35	Reserved
36	$36C_H$	-	-	36	Reserved
37	368_H	-	-	37	Reserved
38	364_H	PPG0	Yes	38	Programmable Pulse Generator 0
39	360_H	PPG1	Yes	39	Programmable Pulse Generator 1

Vector number	Offset in vector table	Vector name	Cleared by DMA	Index in ICR to program	Description
40	$35C_H$	PPG2	Yes	40	Programmable Pulse Generator 2
41	358_H	PPG3	Yes	41	Programmable Pulse Generator 3
42	354_H	-	-	42	Reserved
43	350_H	-	-	43	Reserved
44	$34C_H$	-	-	44	Reserved
45	348_H	-	-	45	Reserved
46	344_H	-	-	46	Reserved
47	340_H	-	-	47	Reserved
48	$33C_H$	-	-	48	Reserved
49	338_H	-	-	49	Reserved
50	334_H	-	-	50	Reserved
51	330_H	-	-	51	Reserved
52	$32C_H$	-	-	52	Reserved
53	328_H	-	-	53	Reserved
54	324_H	-	-	54	Reserved
55	320_H	-	-	55	Reserved
56	$31C_H$	-	-	56	Reserved
57	318_H	-	-	57	Reserved
58	314_H	-	-	58	Reserved
59	310_H	RLT1	Yes	59	Reload Timer 1
60	$30C_H$	RLT2	Yes	60	Reload Timer 2
61	308_H	-	-	61	Reserved
62	304_H	-	-	62	Reserved
63	300_H	-	-	63	Reserved
64	$2FC_H$	RLT6	Yes	64	Reload Timer 6
65	$2F8_H$	ICU0	Yes	65	Input Capture Unit 0
66	$2F4_H$	ICU1	Yes	66	Input Capture Unit 1
67	$2F0_H$	-	-	67	Reserved
68	$2EC_H$	-	-	68	Reserved
69	$2E8_H$	ICU4	Yes	69	Input Capture Unit 4
70	$2E4_H$	ICU5	Yes	70	Input Capture Unit 5
71	$2E0_H$	-	-	71	Reserved
72	$2DC_H$	-	-	72	Reserved
73	$2D8_H$	-	-	73	Reserved
74	$2D4_H$	-	-	74	Reserved
75	$2D0_H$	-	-	75	Reserved
76	$2CC_H$	-	-	76	Reserved
77	$2C8_H$	-	-	77	Reserved
78	$2C4_H$	-	-	78	Reserved
79	$2C0_H$	-	-	79	Reserved
80	$2BC_H$	-	-	80	Reserved

Vector number	Offset in vector table	Vector name	Cleared by DMA	Index in ICR to program	Description
81	$2B8_H$	-	-	81	Reserved
82	$2B4_H$	-	-	82	Reserved
83	$2B0_H$	-	-	83	Reserved
84	$2AC_H$	-	-	84	Reserved
85	$2A8_H$	-	-	85	Reserved
86	$2A4_H$	-	-	86	Reserved
87	$2A0_H$	-	-	87	Reserved
88	$29C_H$	-	-	88	Reserved
89	298_H	FRT0	Yes	89	Free-Running Timer 0
90	294_H	FRT1	Yes	90	Free-Running Timer 1
91	290_H	-	-	91	Reserved
92	$28C_H$	-	-	92	Reserved
93	288_H	RTC0	No	93	Real Time Clock
94	284_H	CAL0	No	94	Clock Calibration Unit
95	280_H	SG0	No	95	Sound Generator 0
96	$27C_H$	IIC0	Yes	96	I^2C interface 0
97	278_H	-	-	97	Reserved
98	274_H	ADC0	Yes	98	A/D Converter 0
99	270_H	-	-	99	Reserved
100	$26C_H$	-	-	100	Reserved
101	268_H	LINR0	Yes	101	LIN USART 0 RX
102	264_H	LINT0	Yes	102	LIN USART 0 TX
103	260_H	LINR1	Yes	103	LIN USART 1 RX
104	$25C_H$	LINT1	Yes	104	LIN USART 1 TX
105	258_H	-	-	105	Reserved
106	254_H	-	-	106	Reserved
107	250_H	-	-	107	Reserved
108	$24C_H$	-	-	108	Reserved
109	248_H	-	-	109	Reserved
110	244_H	-	-	110	Reserved
111	240_H	-	-	111	Reserved
112	$23C_H$	-	-	112	Reserved
113	238_H	-	-	113	Reserved
114	234_H	-	-	114	Reserved
115	230_H	-	-	115	Reserved
116	$22C_H$	-	-	116	Reserved
117	228_H	-	-	117	Reserved
118	224_H	-	-	118	Reserved
119	220_H	-	-	119	Reserved
120	$21C_H$	-	-	120	Reserved

Vector number	Offset in vector table	Vector name	Cleared by DMA	Index in ICR to program	Description
121	218_H	-	-	121	Reserved
122	214_H	-	-	122	Reserved
123	210_H	-	-	123	Reserved
124	$20C_H$	-	-	124	Reserved
125	208_H	-	-	125	Reserved
126	204_H	-	-	126	Reserved
127	200_H	-	-	127	Reserved
128	$1FC_H$	-	-	128	Reserved
129	$1F8_H$	-	-	129	Reserved
130	$1F4_H$	-	-	130	Reserved
131	$1F0_H$	-	-	131	Reserved
132	$1EC_H$	-	-	132	Reserved
133	$1E8_H$	FLASHA	Yes	133	Flash memory A interrupt
134	$1E4_H$	-	-	134	Reserved
135	$1E0_H$	-	-	135	Reserved
136	$1DC_H$	-	-	136	Reserved
137	$1D8_H$	-	-	137	Reserved
138	$1D4_H$	-	-	138	Reserved
139	$1D0_H$	ADCRC0	No	139	A/D Converter 0 - Range Comparator
140	$1CC_H$	ADCPD0	No	140	A/D Converter 0 - Pulse detection
141	$1C8_H$	-	-	141	Reserved
142	$1C4_H$	-	-	142	Reserved
143	$1C0_H$	-	-	143	Reserved

12. Handling Precautions

Any semiconductor devices have inherently a certain rate of failure. The possibility of failure is greatly affected by the conditions in which they are used (circuit conditions, environmental conditions, etc.). This page describes precautions that must be observed to minimize the chance of failure and to obtain higher reliability from your Cypress semiconductor devices.

12.1 Precautions for Product Design

This section describes precautions when designing electronic equipment using semiconductor devices.

■Absolute Maximum Ratings

Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of certain established limits, called absolute maximum ratings. Do not exceed these ratings.

■Recommended Operating Conditions

Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their sales representative beforehand.

■Processing and Protection of Pins

These precautions must be followed when handling the pins which connect semiconductor devices to power supply and input/output functions.

1. Preventing Over-Voltage and Over-Current Conditions

   Exposure to voltage or current levels in excess of maximum ratings at any pin is likely to cause deterioration within the device, and in extreme cases leads to permanent damage of the device. Try to prevent such overvoltage or over-current conditions at the design stage.
2. Protection of Output Pins

   Shorting of output pins to supply pins or other output pins, or connection to large capacitance can cause large current flows. Such conditions if present for extended periods of time can damage the device.
   Therefore, avoid this type of connection.
3. Handling of Unused Input Pins

   Unconnected input pins with very high impedance levels can adversely affect stability of operation. Such pins should be connected through an appropriate resistance to a power supply pin or ground pin.

■Latch-up

Semiconductor devices are constructed by the formation of P-type and N-type areas on a substrate. When subjected to abnormally high voltages, internal parasitic PNPN junctions (called thyristor structures) may be formed, causing large current levels in excess of several hundred mA to flow continuously at the power supply pin. This condition is called latch-up.

CAUTION: The occurrence of latch-up not only causes loss of reliability in the semiconductor device, but can cause injury or damage from high heat, smoke or flame. To prevent this from happening, do the following:

1. Be sure that voltages applied to pins do not exceed the absolute maximum ratings. This should include attention to abnormal noise, surge levels, etc.
2. Be sure that abnormal current flows do not occur during the power-on sequence.

■Observance of Safety Regulations and Standards

Most countries in the world have established standards and regulations regarding safety, protection from electromagnetic interference, etc. Customers are requested to observe applicable regulations and standards in the design of products.

■Fail-Safe Design

Any semiconductor devices have inherently a certain rate of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

■Precautions Related to Usage of Devices
Cypress semiconductor devices are intended for use in standard applications (computers, office automation and other office equipment, industrial, communications, and measurement equipment, personal or household devices, etc.).

CAUTION: Customers considering the use of our products in special applications where failure or abnormal operation may directly affect human lives or cause physical injury or property damage, or where extremely high levels of reliability are demanded (such as aerospace systems, atomic energy controls, sea floor repeaters, vehicle operating controls, medical devices for life support, etc.) are requested to consult with sales representatives before such use. The company will not be responsible for damages arising from such use without prior approval.

12.2 Precautions for Package Mounting

Package mounting may be either lead insertion type or surface mount type. In either case, for heat resistance during soldering, you should only mount under Cypress's recommended conditions. For detailed information about mount conditions, contact your sales representative.

■Lead Insertion Type
Mounting of lead insertion type packages onto printed circuit boards may be done by two methods: direct soldering on the board, or mounting by using a socket.

Direct mounting onto boards normally involves processes for inserting leads into through-holes on the board and using the flow soldering (wave soldering) method of applying liquid solder. In this case, the soldering process usually causes leads to be subjected to thermal stress in excess of the absolute ratings for storage temperature. Mounting processes should conform to Cypress recommended mounting conditions.

If socket mounting is used, differences in surface treatment of the socket contacts and IC lead surfaces can lead to contact deterioration after long periods. For this reason it is recommended that the surface treatment of socket contacts and IC leads be verified before mounting.

■Surface Mount Type
Surface mount packaging has longer and thinner leads than lead-insertion packaging, and therefore leads are more easily deformed or bent. The use of packages with higher pin counts and narrower pin pitch results in increased susceptibility to open connections caused by deformed pins, or shorting due to solder bridges.

You must use appropriate mounting techniques. Cypress recommends the solder reflow method, and has established a ranking of mounting conditions for each product. Users are advised to mount packages in accordance with Cypress ranking of recommended conditions.

■Lead-Free Packaging
CAUTION: When ball grid array (BGA) packages with Sn-Ag-Cu balls are mounted using Sn-Pb eutectic soldering, junction strength may be reduced under some conditions of use.

■Storage of Semiconductor Devices
Because plastic chip packages are formed from plastic resins, exposure to natural environmental conditions will cause absorption of moisture. During mounting, the application of heat to a package that has absorbed moisture can cause surfaces to peel, reducing moisture resistance and causing packages to crack. To prevent, do the following:

1. Avoid exposure to rapid temperature changes, which cause moisture to condense inside the product. Store products in locations where temperature changes are slight.
2. Use dry boxes for product storage. Products should be stored below 70% relative humidity, and at temperatures between 5°C and 30°C.
   When you open Dry Package that recommends humidity 40% to 70% relative humidity.
3. When necessary, Cypress packages semiconductor devices in highly moisture-resistant aluminum laminate bags, with a silica gel desiccant. Devices should be sealed in their aluminum laminate bags for storage.
4. Avoid storing packages where they are exposed to corrosive gases or high levels of dust.

■Baking
Packages that have absorbed moisture may be de-moisturized by baking (heat drying). Follow the Cypress recommended conditions for baking.

Condition: 125°C/24 h

■Static Electricity

Because semiconductor devices are particularly susceptible to damage by static electricity, you must take the following precautions:

1. Maintain relative humidity in the working environment between 40% and 70%. Use of an apparatus for ion generation may be needed to remove electricity.
2. Electrically ground all conveyors, solder vessels, soldering irons and peripheral equipment.
3. Eliminate static body electricity by the use of rings or bracelets connected to ground through high resistance (on the level of 1 MΩ).
   Wearing of conductive clothing and shoes, use of conductive floor mats and other measures to minimize shock loads is recommended.
4. Ground all fixtures and instruments, or protect with anti-static measures.
5. Avoid the use of Styrofoam or other highly static-prone materials for storage of completed board assemblies.

12.3 Precautions for Use Environment

Reliability of semiconductor devices depends on ambient temperature and other conditions as described above.

For reliable performance, do the following:

1. Humidity

   Prolonged use in high humidity can lead to leakage in devices as well as printed circuit boards. If high humidity levels are anticipated, consider anti-humidity processing.
2. Discharge of Static Electricity

   When high-voltage charges exist close to semiconductor devices, discharges can cause abnormal operation. In such cases, use anti-static measures or processing to prevent discharges.
3. Corrosive Gases, Dust, or Oil

   Exposure to corrosive gases or contact with dust or oil may lead to chemical reactions that will adversely affect the device. If you use devices in such conditions, consider ways to prevent such exposure or to protect the devices.
4. Radiation, Including Cosmic Radiation

   Most devices are not designed for environments involving exposure to radiation or cosmic radiation. Users should provide shielding as appropriate.
5. Smoke, Flame

   CAUTION: Plastic molded devices are flammable, and therefore should not be used near combustible substances.
   If devices begin to smoke or burn, there is danger of the release of toxic gases.

Customers considering the use of Cypress products in other special environmental conditions should consult with sales representatives.

13. Handling Devices

Special care is required for the following when handling the device:

- Latch-up prevention
- Unused pins handling
- External clock usage
- Notes on PLL clock mode operation
- Power supply pins (V_{cc}/V_{ss})
- Crystal oscillator and ceramic resonator circuit
- Turn on sequence of power supply to A/D converter and analog inputs
- Pin handling when not using the A/D converter
- Notes on Power-on
- Stabilization of power supply voltage
- SMC power supply pins
- Serial communication
- Mode Pin (MD)

13.1 Latch-up prevention

CMOS IC chips may suffer latch-up under the following conditions:

- A voltage higher than V_{CC} or lower than V_{SS} is applied to an input or output pin.
- A voltage higher than the rated voltage is applied between V_{cc} pins and V_{ss} pins.
- The AV_{CC} power supply is applied before the V_{CC} voltage.

Latch-up may increase the power supply current dramatically, causing thermal damages to the device.

For the same reason, extra care is required to not let the analog power-supply voltage (AV_{CC}, AVRH) exceed the digital power-supply voltage.

13.2 Unused pins handling

Unused input pins can be left open when the input is disabled (corresponding bit of Port Input Enable register PIER = 0).

Leaving unused input pins open when the input is enabled may result in misbehavior and possible permanent damage of the device. To prevent latch-up, they must therefore be pulled up or pulled down through resistors which should be more than 2kΩ.

Unused bidirectional pins can be set either to the output state and be then left open, or to the input state with either input disabled or external pull-up/pull-down resistor as described above.

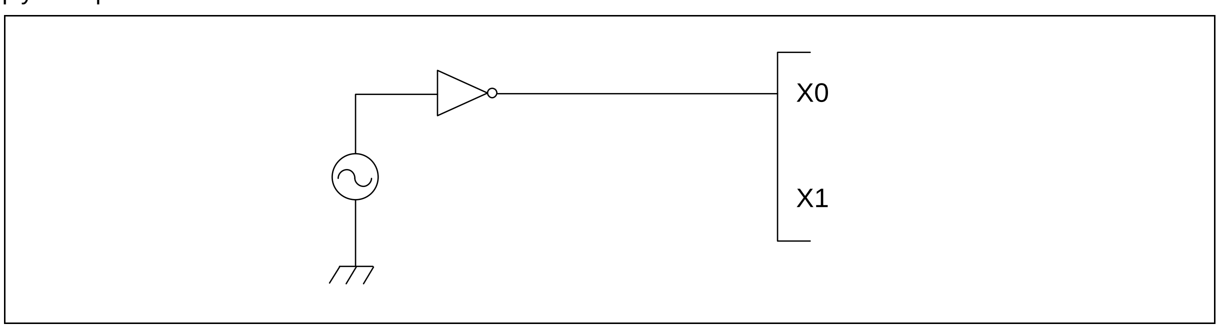
13.3 External clock usage

The permitted frequency range of an external clock depends on the oscillator type and configuration.

See AC Characteristics for detailed modes and frequency limits. Single and opposite phase external clocks must be connected as follows:

13.3.1 Single phase external clock for Main oscillator

When using a single phase external clock for the Main oscillator, X0 pin must be driven and X1 pin left open.
And supply 1.8V power to the external clock.

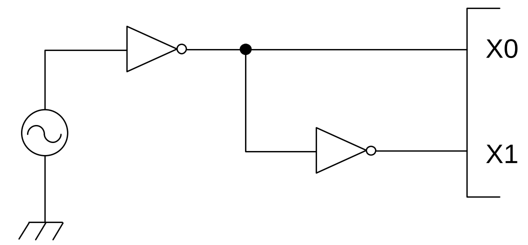


13.3.2 Single phase external clock for Sub oscillator

When using a single phase external clock for the Sub oscillator, “External clock mode” must be selected and X0A/P04_0 pin must be driven. X1A/P04_1 pin can be configured as GPIO.

13.3.3 Opposite phase external clock

When using an opposite phase external clock, X1 (X1A) pins must be supplied with a clock signal which has the opposite phase to the X0 (X0A) pins. Supply level on X0 and X1 pins must be 1.8V.



13.4 Notes on PLL clock mode operation

If the microcontroller is operated with PLL clock mode and no external oscillator is operating or no external clock is supplied, the microcontroller attempts to work with the free oscillating PLL. Performance of this operation, however, cannot be guaranteed.

13.5 Power supply pins (V_{cc}/V_{ss})

It is required that all V_{CC}-level as well as all V_{SS}-level power supply pins are at the same potential. If there is more than one V_{CC} or V_{SS} level, the device may operate incorrectly or be damaged even within the guaranteed operating range.

V_{cc} and V_{ss} pins must be connected to the device from the power supply with lowest possible impedance.

The smoothing capacitor at V_{cc} pin must use the one of a capacity value that is larger than Cs.

Besides this, as a measure against power supply noise, it is required to connect a bypass capacitor of about 0.1μF between V_{cc} and V_{ss} pins as close as possible to V_{cc} and V_{ss} pins.

13.6 Crystal oscillator and ceramic resonator circuit

Noise at X0, X1 pins or X0A, X1A pins might cause abnormal operation. It is required to provide bypass capacitors with shortest possible distance to X0, X1 pins and X0A, X1A pins, crystal oscillator (or ceramic resonator) and ground lines, and, to the utmost effort, that the lines of oscillation circuit do not cross the lines of other circuits.

It is highly recommended to provide a printed circuit board art work surrounding X0, X1 pins and X0A, X1A pins with a ground area for stabilizing the operation.

It is highly recommended to evaluate the quartz/MCU or resonator/MCU system at the quartz or resonator manufacturer, especially when using low-Q resonators at higher frequencies.

13.7 Turn on sequence of power supply to A/D converter and analog inputs

It is required to turn the A/D converter power supply (AV_{CC}, AVRH) and analog inputs (ANn) on after turning the digital power supply (V_{CC}) on.

It is also required to turn the digital power off after turning the A/D converter supply and analog inputs off. In this case, AVRH must not exceed AV_{CC} . Input voltage for ports shared with analog input ports also must not exceed AV_{CC} (turning the analog and digital power supplies simultaneously on or off is acceptable).

13.8 Pin handling when not using the A/D converter

If the A/D converter is not used, the power supply pins for A/D converter should be connected such as AV_{CC} = V_{CC} , AV_{SS} = AVRH = V_{SS}.

13.9 Notes on Power-on

To prevent malfunction of the internal voltage regulator, supply voltage profile while turning the power supply on should be slower than 50µs from 0.2V to 2.7V.

13.10 Stabilization of power supply voltage

If the power supply voltage varies acutely even within the operation safety range of the V_{CC} power supply voltage, a malfunction may occur. The V_{CC} power supply voltage must therefore be stabilized. As stabilization guidelines, the power supply voltage must be stabilized in such a way that V_{CC} ripple fluctuations (peak to peak value) in the commercial frequencies (50Hz to 60Hz) fall within 10% of the standard V_{CC} power supply voltage and the transient fluctuation rate becomes 0.1V/µs or less in instantaneous fluctuation for power supply switching.

13.11 SMC power supply pins

All DVcc /DVss pins must be set to the same level as the Vcc /Vss pins.

Note that the SMC I/O pin state is undefined if DV_{CC} is powered on and V_{CC} is below 3V. To avoid this, V_{CC} must always be powered on before DV_{CC}.

DV_{cc}/DV_{ss} must be applied when using SMC I/O pin as GPIO.

13.12 Serial communication

There is a possibility to receive wrong data due to noise or other causes on the serial communication.

Therefore, design a printed circuit board so as to avoid noise.

Consider receiving of wrong data when designing the system. For example apply a checksum and retransmit the data if an error occurs.

13.13 Mode Pin (MD)

Connect the mode pin directly to Vcc or Vss pin. To prevent the device unintentionally entering test mode due to noise, lay out the printed circuit board so as to minimize the distance from the mode pin to Vcc or Vss pin and provide a low-impedance connection.

14. Electrical Characteristics

14.1 Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating		Unit	Remarks
			Min	Max		
Power supply voltage*[1]	V_{CC}	-	V_{SS} - 0.3	V_{SS} + 6.0	V	
Analog power supply voltage*[1]	AV_{CC}	-	V_{SS} - 0.3	V_{SS} + 6.0	V	$V_{CC} = AV_{CC}$*[2]
Analog reference voltage*[1]	AVRH	-	V_{SS} - 0.3	V_{SS} + 6.0	V	$AV_{CC} \geq$ AVRH, AVRH $\geq AV_{SS}$
SMC Power supply*[1]	DV_{CC}	-	V_{SS} - 0.3	V_{SS} + 6.0	V	$V_{CC} = AV_{CC} = DV_{CC}$*[2]
LCD power supply voltage*[1]	V0 to V3	-	V_{SS} - 0.3	V_{SS} + 6.0	V	V0 to V3 must not exceed V_{CC}
Input voltage*[1]	V_I	-	V_{SS} - 0.3	V_{SS} + 6.0	V	$V_I \leq$ (D)V_{CC} + 0.3V*[3]
Output voltage*[1]	V_O	-	V_{SS} - 0.3	V_{SS} + 6.0	V	$V_O \leq$ (D)V_{CC} + 0.3V*[3]
Maximum Clamp Current	I_{CLAMP}	-	-4.0	+4.0	mA	Applicable to general purpose I/O pins *[4]
Total Maximum Clamp Current	$\Sigma\|I_{CLAMP}\|$	-	-	21	mA	Applicable to general purpose I/O pins *[4]
"L" level maximum output current	I_{OL}	-	-	15	mA	Normal port
	I_{OLSMC}	T_A= -40°C	-	52	mA	High current port
		T_A= +25°C	-	39	mA	
		T_A= +85°C	-	32	mA	
		T_A= +105°C	-	30	mA	
"L" level average output current	I_{OLAV}	-	-	4	mA	Normal port
	$I_{OLAVSMC}$	T_A= -40°C	-	40	mA	High current port
		T_A= +25°C	-	30	mA	
		T_A= +85°C	-	25	mA	
		T_A= +105°C	-	23	mA	
"L" level maximum overall output current	ΣI_{OL}	-	-	46	mA	Normal port
	ΣI_{OLSMC}	-	-	180	mA	High current port
"L" level average overall output current	ΣI_{OLAV}	-	-	23	mA	Normal port
	$\Sigma I_{OLAVSMC}$	-	-	90	mA	High current port
"H" level maximum output current	I_{OH}	-	-	-15	mA	Normal port
	I_{OHSMC}	T_A= -40°C	-	-52	mA	High current port
		T_A= +25°C	-	-39	mA	
		T_A= +85°C	-	-32	mA	
		T_A= +105°C	-	-30	mA	
"H" level average output current	I_{OHAV}	-	-	-4	mA	Normal port
	$I_{OHAVSMC}$	T_A= -40°C	-	-40	mA	High current port
		T_A= +25°C	-	-30	mA	
		T_A= +85°C	-	-25	mA	
		T_A= +105°C	-	-23	mA	
"H" level maximum overall output current	ΣI_{OH}	-	-	-46	mA	Normal port
	ΣI_{OHSMC}	-	-	-180	mA	High current port
"H" level average overall output current	ΣI_{OHAV}	-	-	-23	mA	Normal port
	$\Sigma I_{OHAVSMC}$	-	-	-90	mA	High current port
Power consumption*[5]	P_D	T_A= +105°C	-	317*[6]	mW	
Operating ambient temperature	T_A	-	-40	+105	°C	
Storage temperature	T_{STG}	-	-55	+150	°C	

*1: This parameter is based on $V_{SS} = AV_{SS} = DV_{SS} = 0V$.

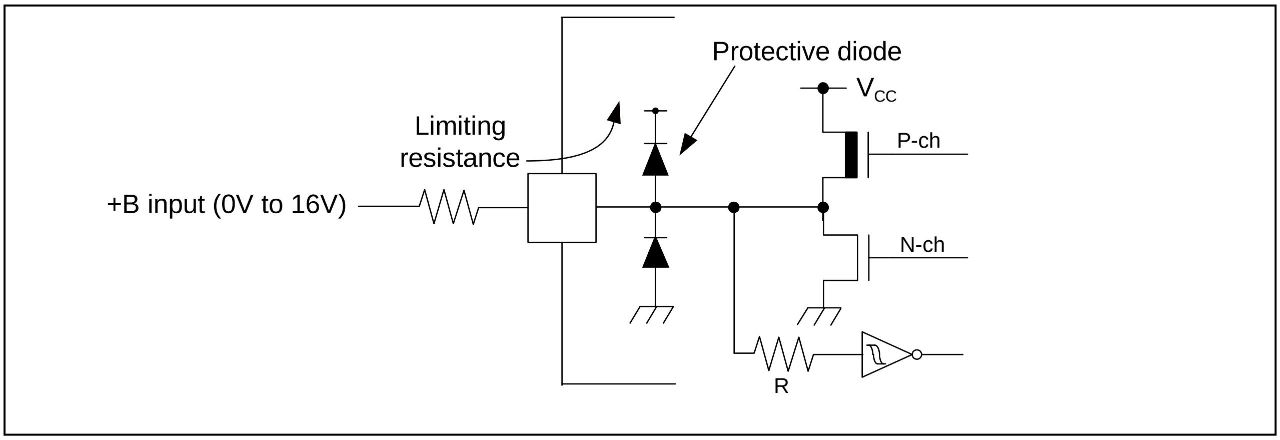
*2: AV_{CC} and V_{CC} and D_{VCC} must be set to the same voltage. It is required that AVCC does not exceed V_{CC}, DV_{CC} and that the voltage at the analog inputs does not exceed AV_{CC} when the power is switched on.

*3: V_I and V_O should not exceed V_{CC} + 0.3V. VI should also not exceed the specified ratings. However if the maximum current to/from an input is limited by some means with external components, the ICLAMP rating supersedes the VI rating. Input/Output voltages of high current ports depend on DV_{CC}. Input/Output voltages of standard ports depend on V_{CC}.

*4:

- Applicable to all general purpose I/O pins (Pnn_m).
- Use within recommended operating conditions.
- Use at DC voltage (current).
- The +B signal should always be applied a limiting resistance placed between the +B signal and the microcontroller.
- The value of the limiting resistance should be set so that when the +B signal is applied the input current to the microcontroller pin does not exceed rated values, either instantaneously or for prolonged periods.
- Note that when the microcontroller drive current is low, such as in the power saving modes, the +B input potential may pass through the protective diode and increase the potential at the V_{CC} pin, and this may affect other devices.
- Note that if a +B signal is input when the microcontroller power supply is off (not fixed at 0V), the power supply is provided from the pins, so that incomplete operation may result.
- Note that if the +B input is applied during power-on, the power supply is provided from the pins and the resulting supply voltage may not be sufficient to operate the Power reset.
- The DEBUG I/F pin has only a protective diode against VSS. Hence it is only permitted to input a negative clamping current (4mA). For protection against positive input voltages, use an external clamping diode which limits the input voltage to maximum 6.0V.

- Sample recommended circuits:



*5: The maximum permitted power dissipation depends on the ambient temperature, the air flow velocity and the thermal conductance of the package on the PCB.
The actual power dissipation depends on the customer application and can be calculated as follows:
$P_D = P_{IO} + P_{INT}$
$PIO = \Sigma (V_{OL} \times I_{OL} + V_{OH} \times I_{OH})$ (I/O load power dissipation, sum is performed on all I/O ports)
$P_{INT} = V_{CC} \times (I_{CC} + I_A)$ (internal power dissipation)
I_{CC} is the total core current consumption into V_{CC} as described in the "DC characteristics" and depends on the selected operation mode and clock frequency and the usage of functions like Flash programming.
I_A is the analog current consumption into AV_{CC}.

*6: Worst case value for a package mounted on single layer PCB at specified T_A without air flow.

WARNING

Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

14.2 Recommended Operating Conditions

(V_{SS} = AV_{SS} = DV_{SS} = 0V)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Power supply voltage	V_{CC}, AV_{CC}, DV_{CC}	2.7	-	5.5	V	
		2.0	-	5.5	V	Maintains RAM data in stop mode
Smoothing capacitor at C pin	C_S	0.5	1.0 to 3.9	4.7	µF	1.0µF (Allowance within ± 50%) 3.9µF (Allowance within ± 20%) Please use the ceramic capacitor or the capacitor of the frequency response of this level. The smoothing capacitor at V_{CC} must use the one of a capacity value that is larger than C_S.

WARNING

The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure. No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

14.3 DC Characteristics

14.3.1 Current Rating

(V_{CC} = AV_{CC} = DV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = DV_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current in Run modes[*1]	I_{CCPLL}	V_{cc}	PLL Run mode with CLKS1/2 = CLKB = CLKP1/2 = 32MHz Flash 0 wait (CLKRC and CLKSC stopped)	-	25	-	mA	T_A = +25°C
				-	-	34	mA	T_A = +105°C
	I_{CCMAIN}		Main Run mode with CLKS1/2 = CLKB = CLKP1/2 = 4MHz Flash 0 wait (CLKPLL, CLKSC and CLKRC stopped)	-	3.5	-	mA	T_A = +25°C
				-	-	7.5	mA	T_A = +105°C
	I_{CCRCH}		RC Run mode with CLKS1/2 = CLKB = CLKP1/2 = CLKRC = 2MHz Flash 0 wait (CLKMC, CLKPLL and CLKSC stopped)	-	1.7	-	mA	T_A = +25°C
				-	-	5.5	mA	T_A = +105°C
	I_{CCRCL}		RC Run mode with CLKS1/2 = CLKB = CLKP1/2 = CLKRC = 100kHz Flash 0 wait (CLKMC, CLKPLL and CLKSC stopped)	-	0.15	-	mA	T_A = +25°C
				-	-	3.2	mA	T_A = +105°C
	I_{CCSUB}		Sub Run mode with CLKS1/2 = CLKB = CLKP1/2 = 32kHz Flash 0 wait (CLKMC, CLKPLL and CLKRC stopped)	-	0.1	-	mA	T_A = +25°C
				-	-	3	mA	T_A = +105°C

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current in Sleep modes[*1]	I_{CCSPLL}	V_{cc}	PLL Sleep mode with CLKS1/2 = CLKP1/2 = 32MHz (CLKRC and CLKSC stopped)	-	6.5	-	mA	T_A = +25°C
				-	-	13	mA	T_A = +105°C
	$I_{CCSMAIN}$		Main Sleep mode with CLKS1/2 = CLKP1/2 = 4MHz, SMCR:LPMSS = 0 (CLKPLL, CLKRC and CLKSC stopped)	-	0.9	-	mA	T_A = +25°C
				-	-	4	mA	T_A = +105°C
	I_{CCSRCH}		RC Sleep mode with CLKS1/2 = CLKP1/2 = CLKRC = 2MHz, SMCR:LPMSS = 0 (CLKMC, CLKPLL and CLKSC stopped)	-	0.5	-	mA	T_A = +25°C
				-	-	3.5	mA	T_A = +105°C
	I_{CCSRCL}		RC Sleep mode with CLKS1/2 = CLKP1/2 = CLKRC = 100kHz (CLKMC, CLKPLL and CLKSC stopped)	-	0.06	-	mA	T_A = +25°C
				-	-	2.7	mA	T_A = +105°C
	I_{CCSSUB}		Sub Sleep mode with CLKS1/2 = CLKP1/2 = 32kHz, (CLKMC, CLKPLL and CLKRC stopped)	-	0.04	-	mA	T_A = +25°C
				-	-	2.5	mA	T_A = +105°C

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current in Timer modes[*2]	I_{CCTPLL}	V_{cc}	PLL Timer mode with CLKPLL = 32MHz (CLKRC and CLKSC stopped)	-	1800	2245	μA	T_A = +25°C
				-	-	3140	μA	T_A = +105°C
	$I_{CCTMAIN}$		Main Timer mode with CLKMC = 4MHz, SMCR:LPMSS = 0 (CLKPLL, CLKRC and CLKSC stopped)	-	285	325	μA	T_A = +25°C
				-	-	1055	μA	T_A = +105°C
	I_{CCTRCH}		RC Timer mode with CLKRC = 2MHz, SMCR:LPMSS = 0 (CLKPLL, CLKMC and CLKSC stopped)	-	160	210	μA	T_A = +25°C
				-	-	970	μA	T_A = +105°C
	I_{CCTRCL}		RC Timer mode with CLKRC = 100kHz (CLKPLL, CLKMC and CLKSC stopped)	-	30	70	μA	T_A = +25°C
				-	-	820	μA	T_A = +105°C
	I_{CCTSUB}		Sub Timer mode with CLKSC = 32kHz (CLKMC, CLKPLL and CLKRC stopped)	-	25	55	μA	T_A = +25°C
				-	-	800	μA	T_A = +105°C

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current in Stop mode*3	I_{CCH}	Vcc	-	-	20	55	μA	T_A = +25°C
				-	-	800	μA	T_A = +105°C
Flash Power Down current	$I_{CCFLASHPD}$	Vcc	-	-	36	70	μA	
Power supply current for active Low Voltage detector*4	I_{CCLVD}	Vcc	Low voltage detector enabled	-	5	-	μA	T_A = +25°C
				-	-	12.5	μA	T_A = +105°C
Flash Write/ Erase current*5	$I_{CCFLASH}$	Vcc	-	-	12.5	-	mA	T_A = +25°C
				-	-	20	mA	T_A = +105°C

*1: The power supply current is measured with a 4MHz external clock connected to the Main oscillator and a 32kHz external clock connected to the Sub oscillator. See chapter “Standby mode and voltage regulator control circuit” of the Hardware Manual for further details about voltage regulator control. Current for "On Chip Debugger" part is not included. Power supply current in Run mode does not include Flash Write / Erase current.

*2: The power supply current in Timer mode is the value when Flash is in Power-down / reset mode.

When Flash is not in Power-down / reset mode, $I_{CCFLASHPD}$ must be added to the Power supply current.

The power supply current is measured with a 4MHz external clock connected to the Main oscillator and a 32kHz external clock connected to the Sub oscillator. The current for "On Chip Debugger" part is not included.

*3: The power supply current in Stop mode is the value when Flash is in Power-down / reset mode.

When Flash is not in Power-down / reset mode, $I_{CCFLASHPD}$ must be added to the Power supply current.

*4: When low voltage detector is enabled, I_{CCLVD} must be added to Power supply current.

*5: When Flash Write / Erase program is executed, $I_{CCFLASH}$ must be added to Power supply current.

14.3.2 Pin Characteristics

(V_{CC} = AV_{CC} = DV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = DV_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
"H" level input voltage	V_{IH}	Port inputs Pnn_m	-	V_{CC} × 0.7	-	V_{CC} + 0.3	V	CMOS Hysteresis input
			-	V_{CC} × 0.8	-	V_{CC} + 0.3	V	AUTOMOTIVE Hysteresis input
	V_{IHX0S}	X0	External clock in "Fast Clock Input mode"	VD × 0.8	-	VD	V	VD=1.8V±0.15V
	V_{IHX0AS}	X0A	External clock in "Oscillation mode"	V_{CC} × 0.8	-	V_{CC} + 0.3	V	
	V_{IHR}	RSTX	-	V_{CC} × 0.8	-	V_{CC} + 0.3	V	CMOS Hysteresis input
	V_{IHM}	MD	-	V_{CC} - 0.3	-	V_{CC} + 0.3	V	CMOS Hysteresis input
	V_{IHD}	DEBUG I/F	-	2.0	-	V_{CC} + 0.3	V	TTL Input
"L" level input voltage	V_{IL}	Port inputs Pnn_m	-	V_{SS} - 0.3	-	V_{CC} × 0.3	V	CMOS Hysteresis input
			-	V_{SS} - 0.3	-	V_{CC} × 0.5	V	AUTOMOTIVE Hysteresis input
	V_{ILX0S}	X0	External clock in "Fast Clock Input mode"	V_{SS}	-	VD × 0.2	V	VD=1.8V±0.15V
	V_{ILX0AS}	X0A	External clock in "Oscillation mode"	V_{SS} - 0.3	-	V_{CC} × 0.2	V	
	V_{ILR}	RSTX	-	V_{SS} - 0.3	-	V_{CC} × 0.2	V	CMOS Hysteresis input
	V_{ILM}	MD	-	V_{SS} - 0.3	-	V_{SS} + 0.3	V	CMOS Hysteresis input
	V_{ILD}	DEBUG I/F	-	V_{SS} - 0.3	-	0.8	V	TTL Input

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
"H" level output voltage	V_{OH4}	4mA type	4.5V ≤ (D)V_{CC} ≤ 5.5V I_{OH} = -4mA	(D)V_{CC} - 0.5	-	(D)V_{CC}	V	
			2.7V ≤ (D)V_{CC} < 4.5V I_{OH} = -1.5mA					
	V_{OH30}	High Drive type*	4.5V ≤ DV_{CC} ≤ 5.5V I_{OH} = -52mA	DV_{CC} - 0.5	-	DV_{CC}	V	T_A = -40°C
			2.7V ≤ DV_{CC} < 4.5V I_{OH} = -18mA					
			4.5V ≤ DV_{CC} ≤ 5.5V I_{OH} = -39mA					T_A = +25°C
			2.7V ≤ DV_{CC} < 4.5V I_{OH} = -16mA					
			4.5V ≤ DV_{CC} ≤ 5.5V I_{OH} = -32mA					T_A = +85°C
			2.7V ≤ DV_{CC} < 4.5V I_{OH} = -14.5mA					
			4.5V ≤ DV_{CC} ≤ 5.5V I_{OH} = -30mA					T_A = +105°C
			2.7V ≤ DV_{CC} < 4.5V I_{OH} = -14mA					
	V_{OH3}	3mA type	4.5V ≤ V_{CC} ≤ 5.5V I_{OH} = -3mA	V_{CC} - 0.5	-	V_{CC}	V	
			2.7V ≤ V_{CC} < 4.5V I_{OH} = -1.5mA					
"L" level output voltage	V_{OL4}	4mA type	4.5V ≤ (D)V_{CC} ≤ 5.5V I_{OL} = +4mA	-	-	0.4	V	
			2.7V ≤ (D)V_{CC} < 4.5V I_{OL} = +1.7mA					
	V_{OL30}	High Drive type*	4.5V ≤ DV_{CC} ≤ 5.5V I_{OL} = +52mA	-	-	0.5	V	T_A = -40°C
			2.7V ≤ DV_{CC} < 4.5V I_{OL} = +22mA					
			4.5V ≤ DV_{CC} ≤ 5.5V I_{OL} = +39mA					T_A = +25°C
			2.7V ≤ DV_{CC} < 4.5V I_{OL} = +18mA					
			4.5V ≤ DV_{CC} ≤ 5.5V I_{OL} = +32mA					T_A = +85°C
			2.7V ≤ DV_{CC} < 4.5V I_{OL} = +14mA					
			4.5V ≤ DV_{CC} ≤ 5.5V I_{OL} = +30mA					T_A = +105°C
			2.7V ≤ DV_{CC} < 4.5V I_{OL} = +13.5mA					
	V_{OL3}	3mA type	2.7V ≤ V_{CC} < 5.5V I_{OL} = +3mA	-	-	0.4	V	
	V_{OLD}	DEBUG I/F	V_{CC} = 2.7V I_{OL} = +25mA	0	-	0.25	V	

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Input leak current	I_{IL}	Pnn_m	$V_{SS} < V_I < V_{CC}$ $AV_{SS} < V_I < AV_{CC}$, AVRH	- 1	-	+ 1	μA	Single port pin except high current output I/O for SMC
		P08_m	$DV_{SS} < V_I < DV_{CC}$ $AV_{SS} < V_I < AV_{CC}$, AVRH	- 3	-	+ 3	μA	
Total LCD leak current	$\Sigma\|I_{ILCD}\|$	All SEG/ COM pin	V_{CC} = 5.0V	-	0.5	10	μA	Maximum leakage current of all LCD pins
Internal LCD divide resistance	R_{LCD}	Between V3 and V2, V2 and V1, V1 and V0	V_{CC} = 5.0V	6.25	12.5	25	kΩ	
Pull-up resistance value	R_{PU}	Pnn_m	V_{CC} = 5.0V ±10%	25	50	100	kΩ	
Pull-down resistance value	R_{DOWN}	P08_m	V_{CC} = 5.0V ±10%	25	50	100	kΩ	
Input capacitance	C_{IN}	Other than C, Vcc, Vss, DVcc DVss, AVcc, AVss, AVRH, P08_m	-	-	5	15	pF	
		P08_m	-	-	15	30	pF	

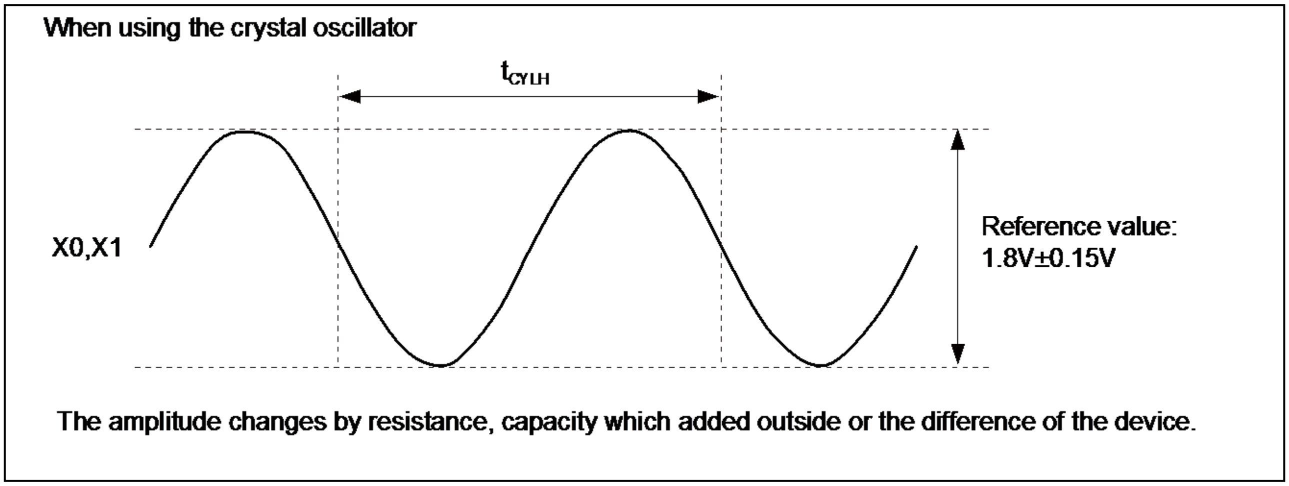
*: In the case of driving stepping motor directly or high current outputs, set "1" to the bit in the Port High Drive Register (PHDRnn:HDx="1").

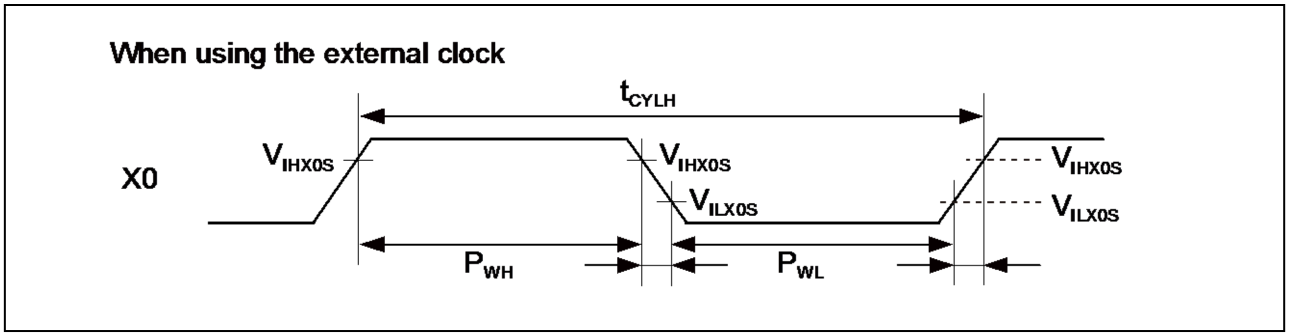
14.4 AC Characteristics

14.4.1 Main Clock Input Characteristics

(V_{CC} = AV_{CC} = DV_{CC} = 2.7V to 5.5V, VD=1.8V±0.15V, V_{SS} = AV_{SS} = DV_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Input frequency	f_C	X0, X1	4	-	8	MHz	When using a crystal oscillator, PLL off
			-	-	8	MHz	When using an opposite phase external clock, PLL off
			4	-	8	MHz	When using a crystal oscillator or opposite phase external clock, PLL on
Input frequency	f_{FCI}	X0	-	-	8	MHz	When using a single phase external clock in “Fast Clock Input mode”, PLL off
			4	-	8	MHz	When using a single phase external clock in “Fast Clock Input mode”, PLL on
Input clock cycle	t_{CYLH}	-	125	-	-	ns	
Input clock pulse width	P_{WH}, P_{WL}	-	55	-	-	ns	

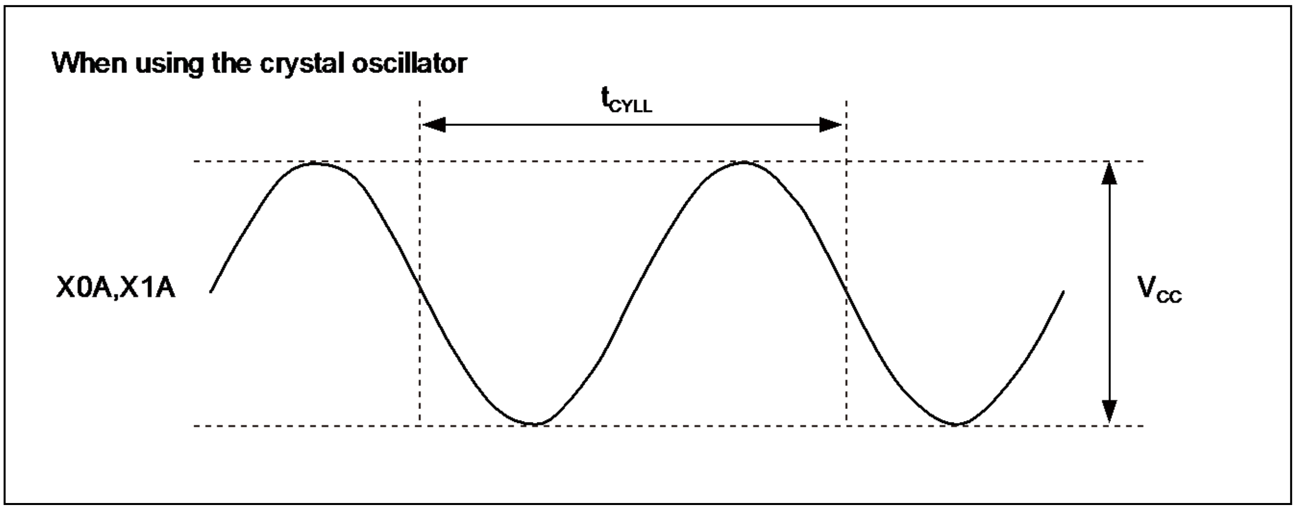


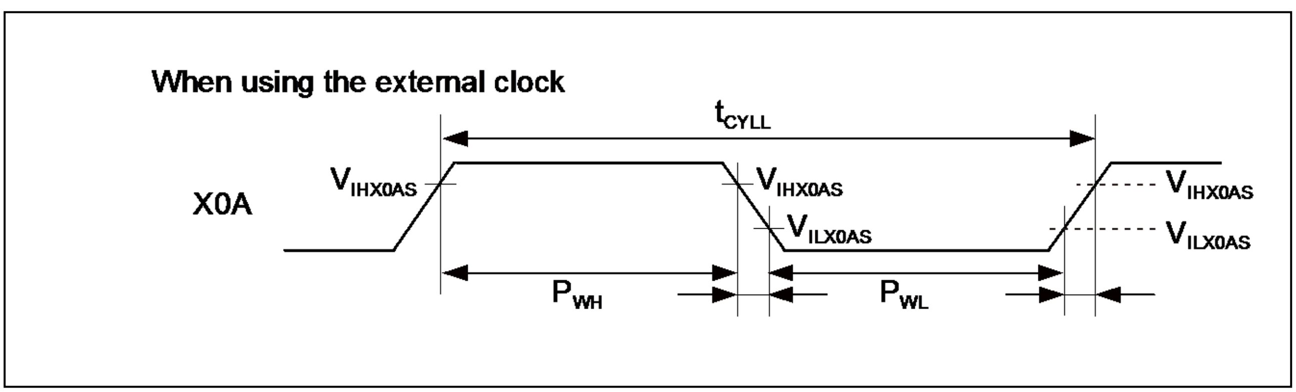


14.4.2 Sub Clock Input Characteristics

(V_{CC} = AV_{CC} = DV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = DV_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Input frequency	f_{CL}	X0A, X1A	-	-	32.768	-	kHz	When using an oscillation circuit
			-	-	-	100	kHz	When using an opposite phase external clock
		X0A	-	-	-	50	kHz	When using a single phase external clock
Input clock cycle	t_{CYLL}	-	-	10	-	-	µs	
Input clock pulse width	-	-	P_{WH}/t_{CYLL}, P_{WL}/t_{CYLL}	30	-	70	%	





14.4.3 Built-in RC Oscillation Characteristics

($V_{CC} = AV_{CC} = DV_{CC}$ = 2.7V to 5.5V, $V_{SS} = AV_{SS} = DV_{SS}$ = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Clock frequency	f_{RC}	50	100	200	kHz	When using slow frequency of RC oscillator
		1	2	4	MHz	When using fast frequency of RC oscillator
RC clock stabilization time	t_{RCSTAB}	80	160	320	µs	When using slow frequency of RC oscillator (16 RC clock cycles)
		64	128	256	µs	When using fast frequency of RC oscillator (256 RC clock cycles)

14.4.4 Internal Clock Timing

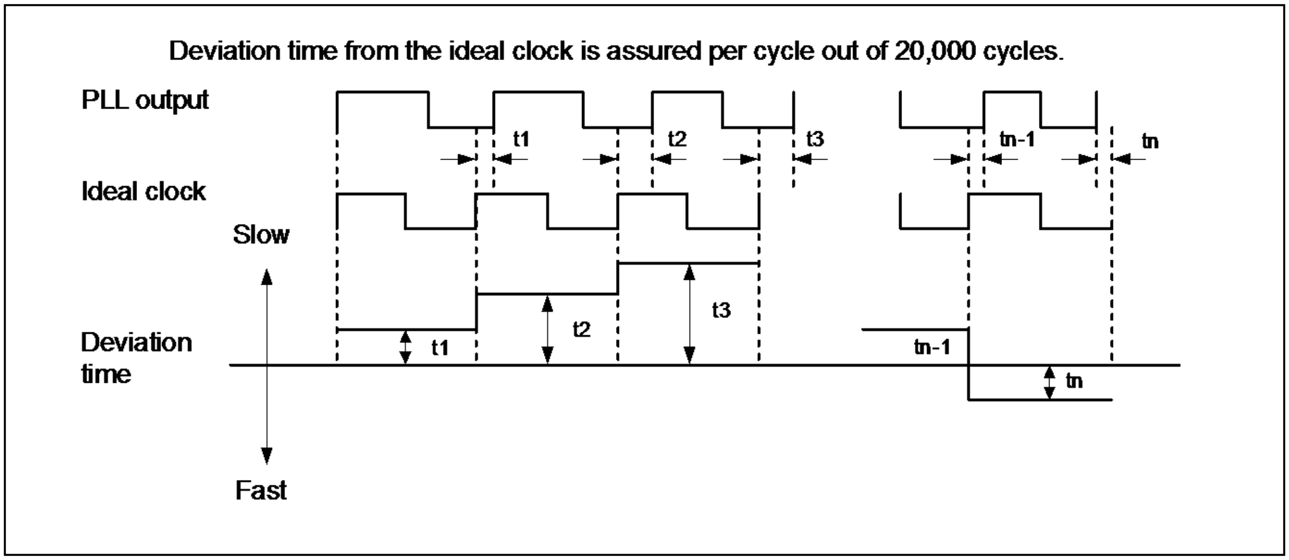
($V_{CC} = AV_{CC} = DV_{CC}$ = 2.7V to 5.5V, $V_{SS} = AV_{SS} = DV_{SS}$ = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Value		Unit
		Min	Max	
Internal System clock frequency (CLKS1 and CLKS2)	f_{CLKS1}, f_{CLKS2}	-	54	MHz
Internal CPU clock frequency (CLKB), Internal peripheral clock frequency (CLKP1)	f_{CLKB}, f_{CLKP1}	-	32	MHz
Internal peripheral clock frequency (CLKP2)	f_{CLKP2}	-	32	MHz

14.4.5 Operating Conditions of PLL

(V_{CC} = AV_{CC} = DV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = DV_{SS} = 0V, T_A = - 40°C to + 105°C)

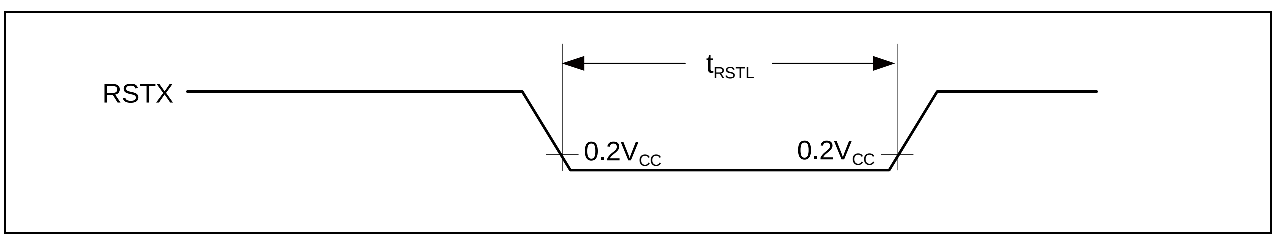
Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
PLL oscillation stabilization wait time	t_{LOCK}	1	-	4	ms	For CLKMC = 4MHz
PLL input clock frequency	f_{PLLI}	4	-	8	MHz	
PLL oscillation clock frequency	f_{CLKVCO}	56	-	108	MHz	Permitted VCO output frequency of PLL (CLKVCO)
PLL phase jitter	t_{PSKEW}	-5	-	+5	ns	For CLKMC (PLL input clock) ≥ 4MHz



14.4.6 Reset Input

(V_{CC} = AV_{CC} = DV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = DV_{SS} = 0V, T_A = - 40°C to + 105°C)

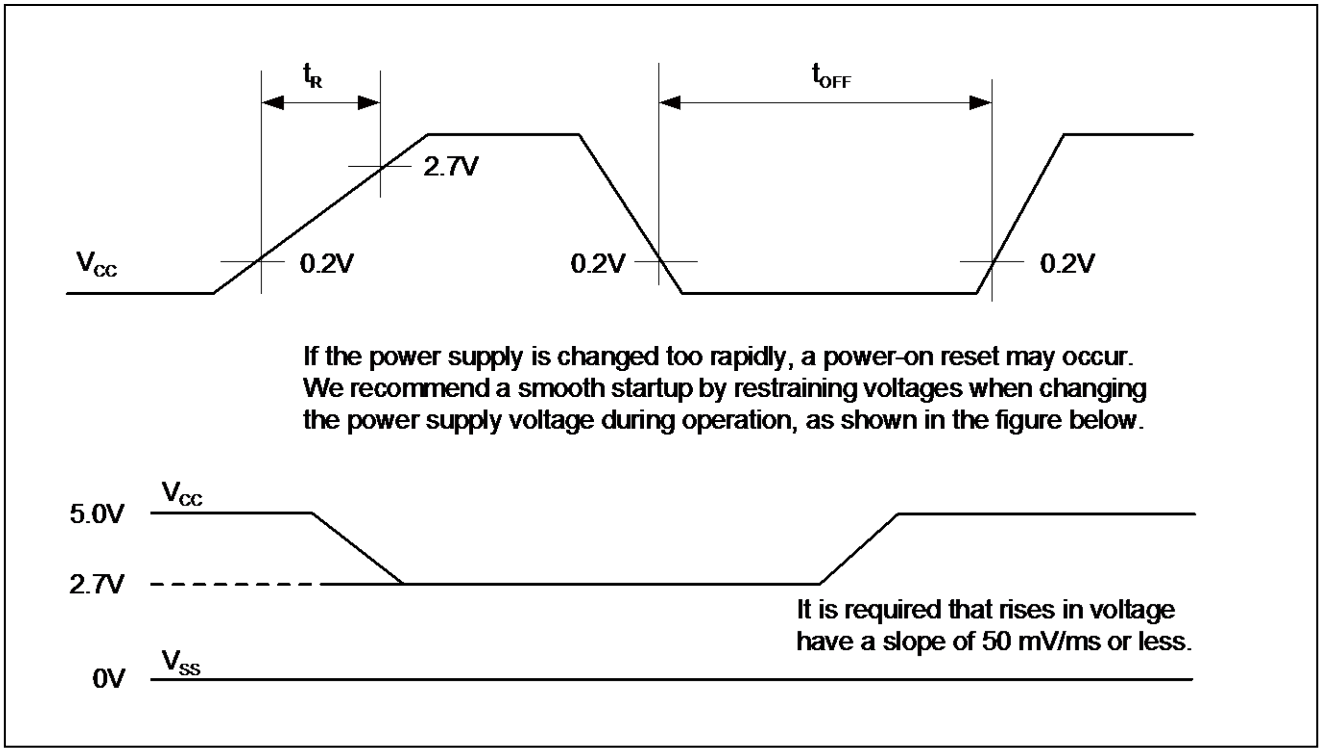
Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
Reset input time	t_{RSTL}	RSTX	10	-	µs
Rejection of reset input time			1	-	µs



14.4.7 Power-on Reset Timing

(V_{CC} = AV_{CC} = DV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = DV_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Value			Unit
			Min	Typ	Max	
Power on rise time	t_R	V_{cc}	0.05	-	30	ms
Power off time	t_{OFF}	V_{cc}	1	-	-	ms



14.4.8 USART Timing

($V_{CC} = AV_{CC} = DV_{CC}$ = 2.7V to 5.5V, $V_{SS} = AV_{SS} = DV_{SS}$ = 0V, T_A = - 40°C to + 105°C, C_L=50pF)

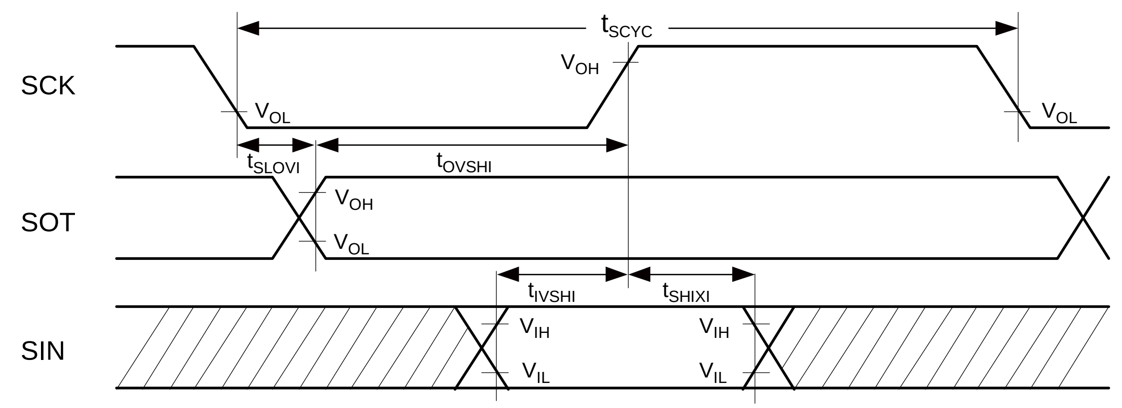
Parameter	Symbol	Pin name	Conditions	$4.5V \leq V_{CC} < 5.5V$		$2.7V \leq V_{CC} < 4.5V$		Unit
				Min	Max	Min	Max	
Serial clock cycle time	t_{SCYC}	SCKn	Internal shift clock mode	$4t_{CLKP1}$	-	$4t_{CLKP1}$	-	ns
SCK ↓ → SOT delay time	t_{SLOVI}	SCKn, SOTn		- 20	+ 20	- 30	+ 30	ns
SOT → SCK ↑ delay time	t_{OVSHI}	SCKn, SOTn		$N \times t_{CLKP1} - 20^*$	-	$N \times t_{CLKP1} - 30^*$	-	ns
SIN → SCK ↑ setup time	t_{IVSHI}	SCKn, SINn		$t_{CLKP1} + 45$	-	$t_{CLKP1} + 55$	-	ns
SCK ↑ → SIN hold time	t_{SHIXI}	SCKn, SINn		0	-	0	-	ns
Serial clock "L" pulse width	t_{SLSH}	SCKn	External shift clock mode	$t_{CLKP1} + 10$	-	$t_{CLKP1} + 10$	-	ns
Serial clock "H" pulse width	t_{SHSL}	SCKn		$t_{CLKP1} + 10$	-	$t_{CLKP1} + 10$	-	ns
SCK ↓ → SOT delay time	t_{SLOVE}	SCKn, SOTn		-	$2t_{CLKP1} + 45$	-	$2t_{CLKP1} + 55$	ns
SIN → SCK ↑ setup time	t_{IVSHE}	SCKn, SINn		$t_{CLKP1}/2 + 10$	-	$t_{CLKP1}/2 + 10$	-	ns
SCK ↑ → SIN hold time	t_{SHIXE}	SCKn, SINn		$t_{CLKP1} + 10$	-	$t_{CLKP1} + 10$	-	ns
SCK fall time	t_F	SCKn		-	20	-	20	ns
SCK rise time	t_R	SCKn		-	20	-	20	ns

Notes:
- AC characteristic in CLK synchronized mode.
- C_L is the load capacity value of pins when testing.
- Depending on the used machine clock frequency, the maximum possible baud rate can be limited by some parameters. These parameters are shown in “MB96600 series HARDWARE MANUAL”.
- tCLKP1 indicates the peripheral clock 1 (CLKP1), Unit: ns
- These characteristics only guarantee the same relocate port number.
  For example, the combination of SCKn and SOTn_R is not guaranteed.

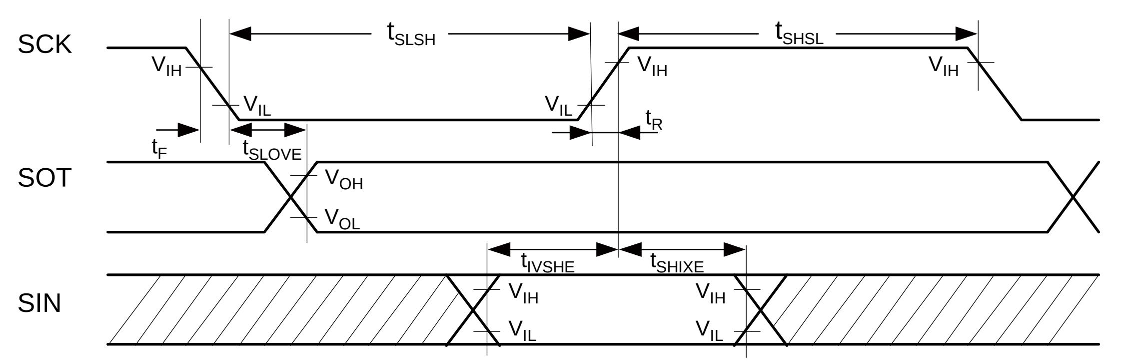
*: Parameter N depends on t_{SCYC} and can be calculated as follows:
- If $t_{SCYC} = 2 \times k \times t_{CLKP1}$, then N = k, where k is an integer > 2
- If $t_{SCYC} = (2 \times k + 1) \times t_{CLKP1}$, then N = k + 1, where k is an integer > 1

Examples:

t_{SCYC}	N
$4 \times t_{CLKP1}$	2
$5 \times t_{CLKP1}$, $6 \times t_{CLKP1}$	3
$7 \times t_{CLKP1}$, $8 \times t_{CLKP1}$	4
...	...



Internal shift clock mode



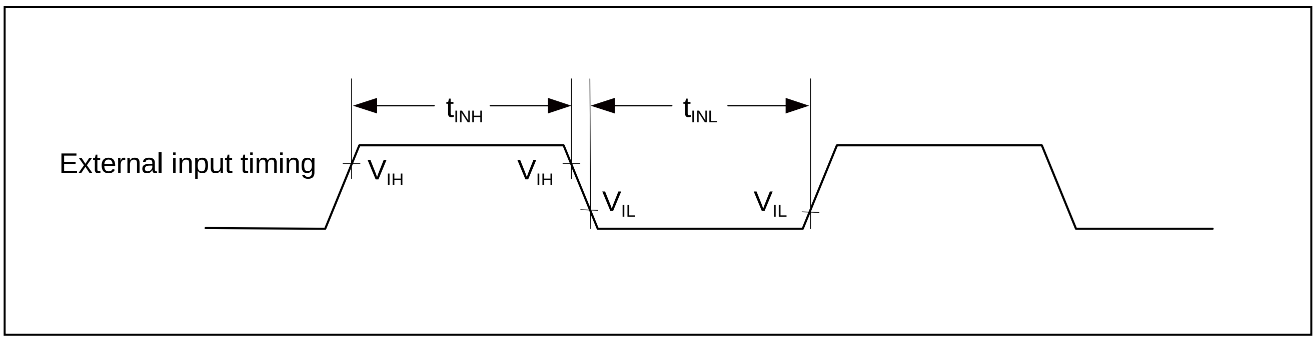
External shift clock mode

14.4.9 External Input Timing

(V_{CC} = AV_{CC} = DV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = DV_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Value		Unit	Remarks
			Min	Max		
Input pulse width	t_{INH}, t_{INL}	Pnn_m	2t_{CLKP1} +200 (t_{CLKP1}= 1/f_{CLKP1})*	-	ns	General Purpose I/O
		ADTG				A/D Converter trigger input
		TINn, TINn_R				Reload Timer
		TTGn				PPG trigger input
		FRCKn, FRCKn_R				Free-Running Timer input clock
		INn, INn_R				Input Capture
		INTn, INTn_R	200	-	ns	External Interrupt
		NMI				Non-Maskable Interrupt

*: t_{CLKP1} indicates the peripheral clock1 (CLKP1) cycle time except stop when in stop mode.



14.4.10 I^2C Timing

($V_{CC} = AV_{CC} = DV_{CC}$ = 2.7V to 5.5V, $V_{SS} = AV_{SS} = DV_{SS}$ = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Conditions	Typical mode		High-speed mode*4		Unit
			Min	Max	Min	Max	
SCL clock frequency	f_{SCL}	C_L = 50pF, R = (Vp/I_{OL})*1	0	100	0	400	kHz
(Repeated) START condition hold time SDA↓ → SCL ↓	t_{HDSTA}		4.0	-	0.6	-	μs
SCL clock "L" width	t_{LOW}		4.7	-	1.3	-	μs
SCL clock "H" width	t_{HIGH}		4.0	-	0.6	-	μs
(Repeated) START condition setup time SCL↑ → SDA↓	t_{SUSTA}		4.7	-	0.6	-	μs
Data hold time SCL↓ → SDA↓↑	t_{HDDAT}		0	3.45*2	0	0.9*3	μs
Data setup time SDA↓↑ → SCL↑	t_{SUDAT}		250	-	100	-	ns
STOP condition setup time SCL↑ → SDA↑	t_{SUSTO}		4.0	-	0.6	-	μs
Bus free time between "STOP condition" and "START condition"	t_{BUS}		4.7	-	1.3	-	μs
Pulse width of spikes which will be suppressed by input noise filter	t_{SP}	-	0	(1-1.5) × t_{CLKP1}*5	0	(1-1.5) × t_{CLKP1}*5	ns

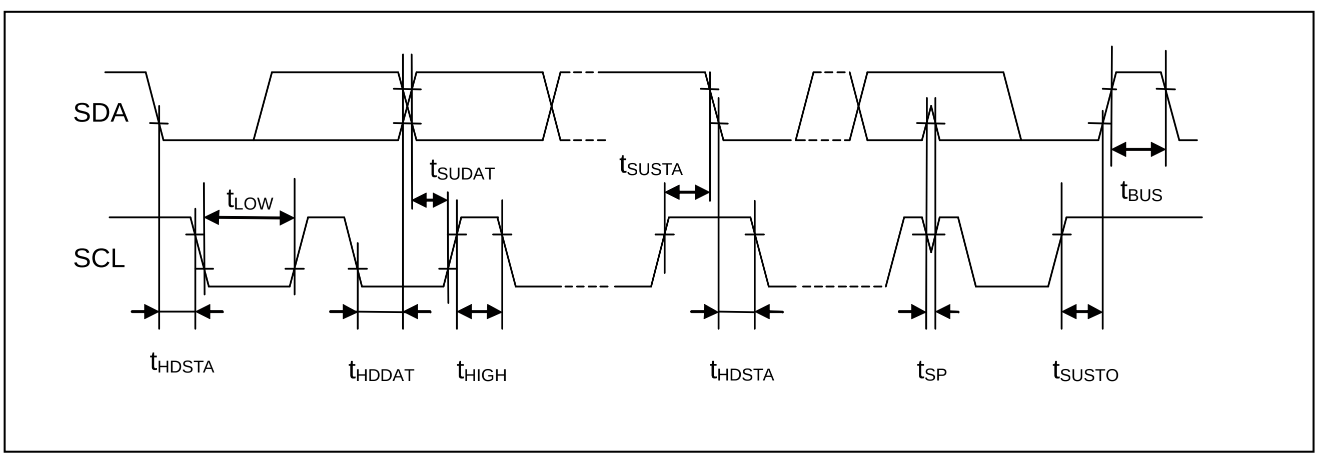
*1: R and C_L represent the pull-up resistance and load capacitance of the SCL and SDA lines, respectively.
Vp indicates the power supply voltage of the pull-up resistance and I_{OL} indicates V_{OL} guaranteed current.

*2: The maximum t_{HDDAT} only has to be met if the device does not extend the "L" width (t_{LOW}) of the SCL signal.

*3: A high-speed mode I^2C bus device can be used on a standard mode I^2C bus system as long as the device satisfies the requirement of "t_{SUDAT} ≥ 250ns".

*4: For use at over 100kHz, set the peripheral clock1 (CLKP1) to at least 6MHz.

*5: t_{CLKP1} indicates the peripheral clock1 (CLKP1) cycle time.



14.5 A/D Converter

14.5.1 Electrical Characteristics for the A/D Converter

(V_{CC} = AV_{CC} = DV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = DV_{SS} = 0V, T_A = - 40°C to + 105°C)

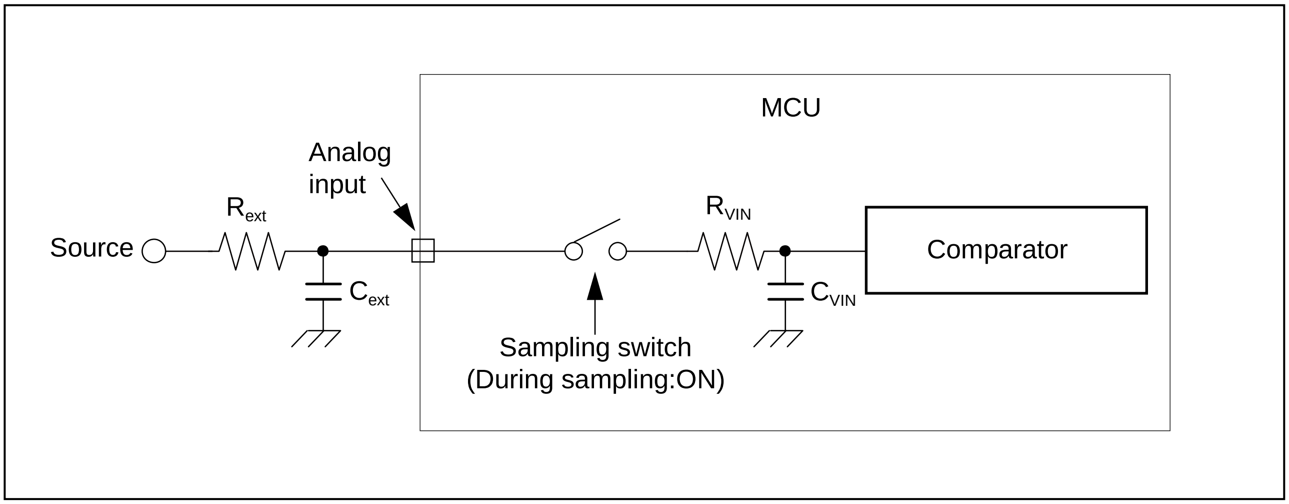
Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	-	-	-	-	10	bit	
Total error	-	-	- 3.0	-	+ 3.0	LSB	
Nonlinearity error	-	-	- 2.5	-	+ 2.5	LSB	
Differential Nonlinearity error	-	-	- 1.9	-	+ 1.9	LSB	
Zero transition voltage	V_{OT}	ANn	Typ - 20	AV_{SS} + 0.5LSB	Typ + 20	mV	
Full scale transition voltage	V_{FST}	ANn	Typ - 20	AVRH - 1.5LSB	Typ + 20	mV	
Compare time*	-	-	1.0	-	5.0	μs	4.5V ≤ AV_{CC} ≤ 5.5V
			2.2	-	8.0	μs	2.7V ≤ AV_{CC} < 4.5V
Sampling time*	-	-	0.5	-	-	μs	4.5V ≤ AV_{CC} ≤ 5.5V
			1.2	-	-	μs	2.7V ≤ AV_{CC} < 4.5V
Power supply current	I_A	AV_{CC}	-	2.0	3.1	mA	A/D Converter active
	I_{AH}		-	-	3.3	μA	A/D Converter not operated
Reference power supply current (between AVRH and AV_{SS})	I_R	AVRH	-	520	810	μA	A/D Converter active
	I_{RH}		-	-	1.0	μA	A/D Converter not operated
Analog input capacity	C_{VIN}	AN8 to 13	-	-	15.5	pF	Normal outputs
		AN16 to 23	-	-	17.4	pF	High current outputs
Analog impedance	R_{VIN}	ANn	-	-	1450	Ω	4.5V ≤ AV_{CC} ≤ 5.5V
			-	-	2700	Ω	2.7V ≤ AV_{CC} < 4.5V
Analog port input current (during conversion)	I_{AIN}	AN8 to 13	- 1.0	-	+ 1.0	μA	AV_{SS} < V_{AIN} < AV_{CC}, AVRH
		AN16 to 23	- 3.0	-	+ 3.0	μA	
Analog input voltage	V_{AIN}	ANn	AV_{SS}	-	AVRH	V	
Reference voltage range	-	AVRH	AV_{CC} - 0.1	-	AV_{CC}	V	
Variation between channels	-	ANn	-	-	4.0	LSB	

*: Time for each channel.

14.5.2 Accuracy and Setting of the A/D Converter Sampling Time

If the external impedance is too high or the sampling time too short, the analog voltage charged to the internal sample and hold capacitor is insufficient, adversely affecting the A/D conversion precision.

To satisfy the A/D conversion precision, a sufficient sampling time must be selected. The required sampling time (T_{samp}) depends on the external driving impedance R_{ext}, the board capacitance of the A/D converter input pin C_{ext} and the AV_{CC} voltage level. The following replacement model can be used for the calculation:



Rext: External driving impedance

Cext: Capacitance of PCB at A/D converter input

CVIN: Analog input capacity (I/O, analog switch and ADC are contained)

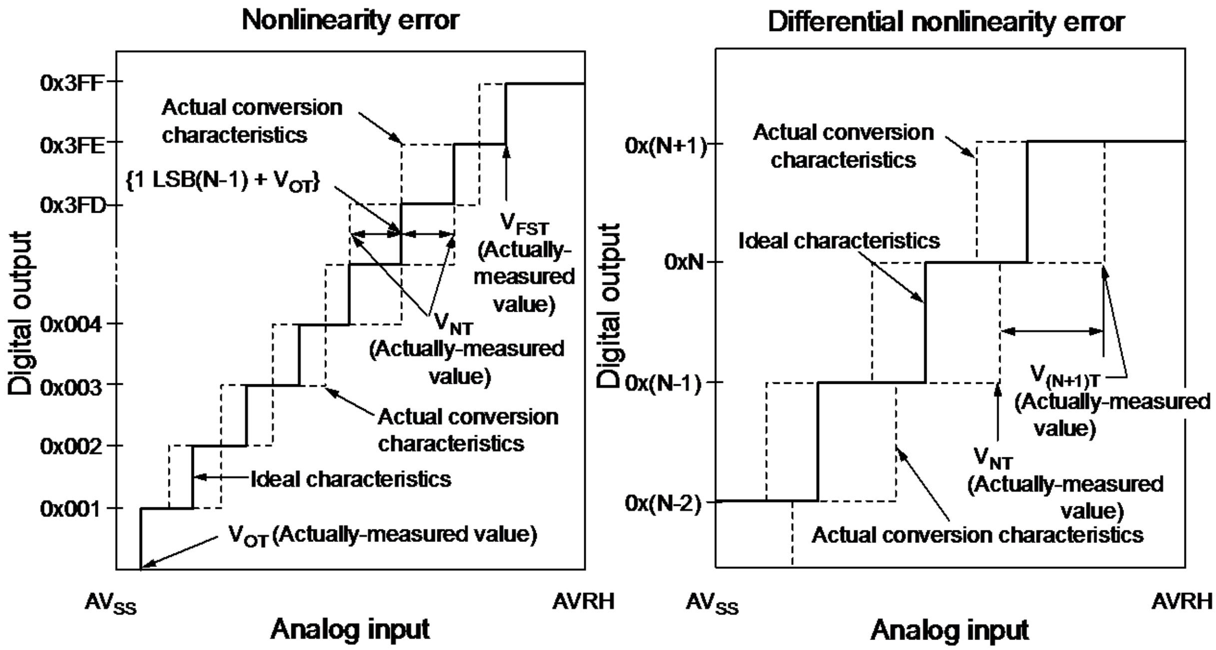
RVIN: Analog input impedance (I/O, analog switch and ADC are contained)

The following approximation formula for the replacement model above can be used:
$T_{samp} = 7.62 \times (R_{ext} \times C_{ext} + (R_{ext} + R_{VIN}) \times C_{VIN})$

- Do not select a sampling time below the absolute minimum permitted value.
  ($0.5\mu s$ for $4.5V \le AV_{CC} \le 5.5V$, $1.2\mu s$ for $2.7V \le AV_{CC} < 4.5V$)
- If the sampling time cannot be sufficient, connect a capacitor of about $0.1\mu F$ to the analog input pin.
- A big external driving impedance also adversely affects the A/D conversion precision due to the pin input leakage current IIL (static current before the sampling switch) or the analog input leakage current IAIN (total leakage current of pin input and comparator during sampling). The effect of the pin input leakage current IIL cannot be compensated by an external capacitor.
- The accuracy gets worse as $|AVRH - AV_{SS}|$ becomes smaller.

14.5.3 Definition of A/D Converter Terms

- Resolution : Analog variation that is recognized by an A/D converter.
- Nonlinearity error : Deviation of the actual conversion characteristics from a straight line that connects the zero transition point (0b0000000000 ←→ 0b0000000001) to the full-scale transition point (0b1111111110 ←→ 0b1111111111).
- Differential nonlinearity error: Deviation from the ideal value of the input voltage that is required to change the output code by 1LSB.
- Total error : Difference between the actual value and the theoretical value. The total error includes zero transition error, full-scale transition error and nonlinearity error.
- Zero transition voltage : Input voltage which results in the minimum conversion value.
- Full scale transition voltage: Input voltage which results in the maximum conversion value.

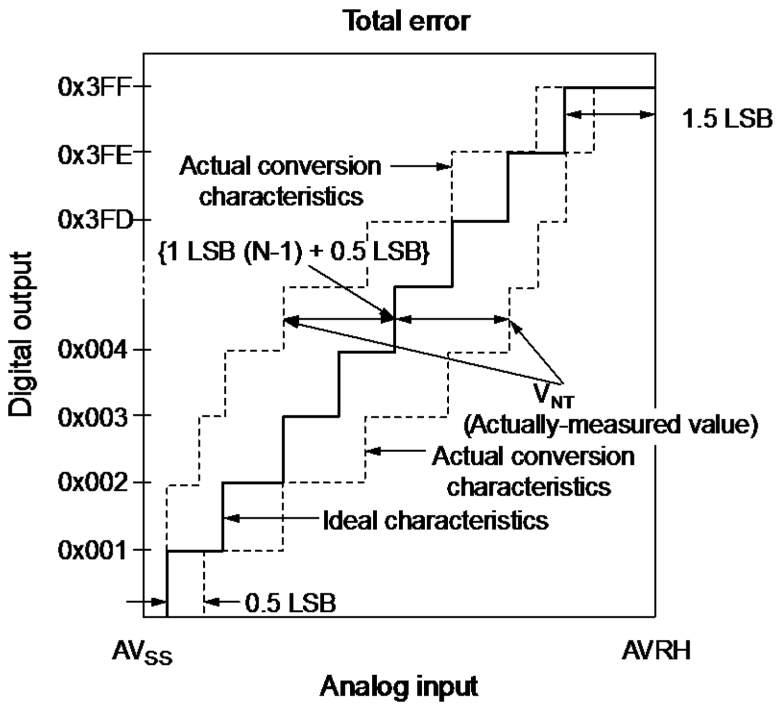


Nonlinearity error of digital output N = $\dfrac{V_{NT} - \{1LSB \times (N - 1) + V_{OT}\}}{1LSB}$ [LSB]

Differential nonlinearity error of digital output N = $\dfrac{V_{(N+1)T} - V_{NT}}{1LSB} - 1$ [LSB]

$1LSB = \dfrac{V_{FST} - V_{OT}}{1022}$

N : A/D converter digital output value.
V_{OT} : Voltage at which the digital output changes from 0x000 to 0x001.
V_{FST} : Voltage at which the digital output changes from 0x3FE to 0x3FF.
V_{NT} : Voltage at which the digital output changes from 0x(N − 1) to 0xN.



$$1\text{LSB (Ideal value)} = \frac{AVRH - AV_{SS}}{1024} \text{ [V]}$$

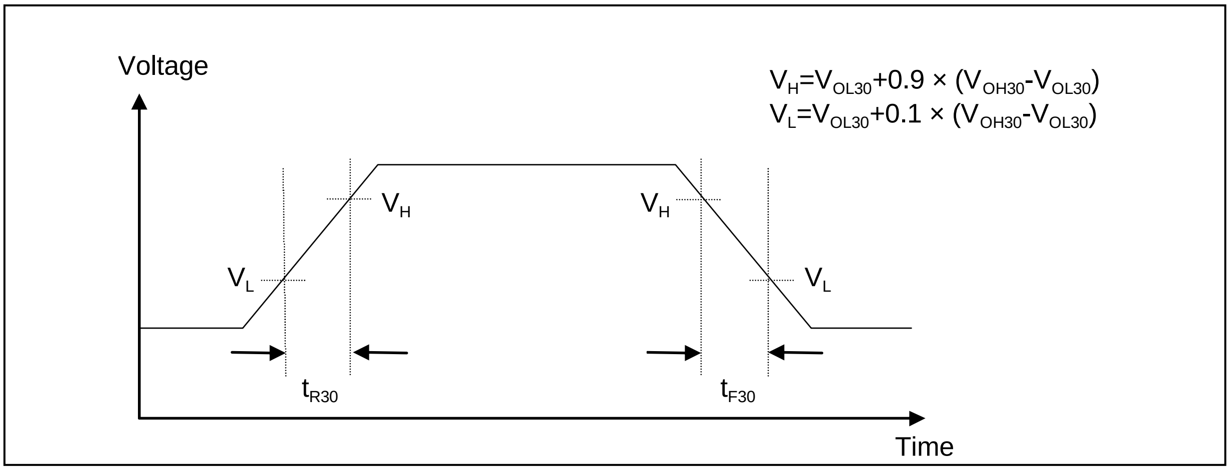
$$\text{Total error of digital output N} = \frac{V_{NT} - \{1\text{LSB} \times (N - 1) + 0.5\text{LSB}\}}{1\text{LSB}}$$

N : A/D converter digital output value.
V_{NT} : Voltage at which the digital output changes from 0x(N + 1) to 0xN.
V_{OT} (Ideal value) = AV_{SS} + 0.5LSB[V]
V_{FST} (Ideal value) = AVRH - 1.5LSB[V]

14.6 High Current Output Slew Rate

(V_{CC} = AV_{CC} = DV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = DV_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Output rise/fall time	t_{R30}, t_{F30}	P08_m	Outputs driving strength set to "30mA"	15	-	75	ns	C_L=85pF



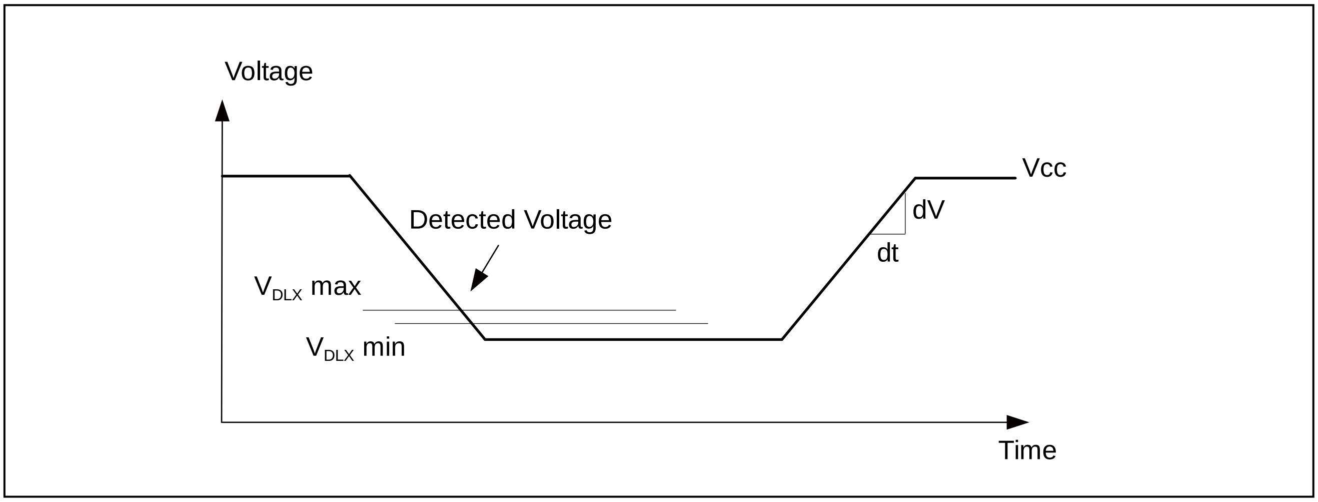
14.7 Low Voltage Detection Function Characteristics

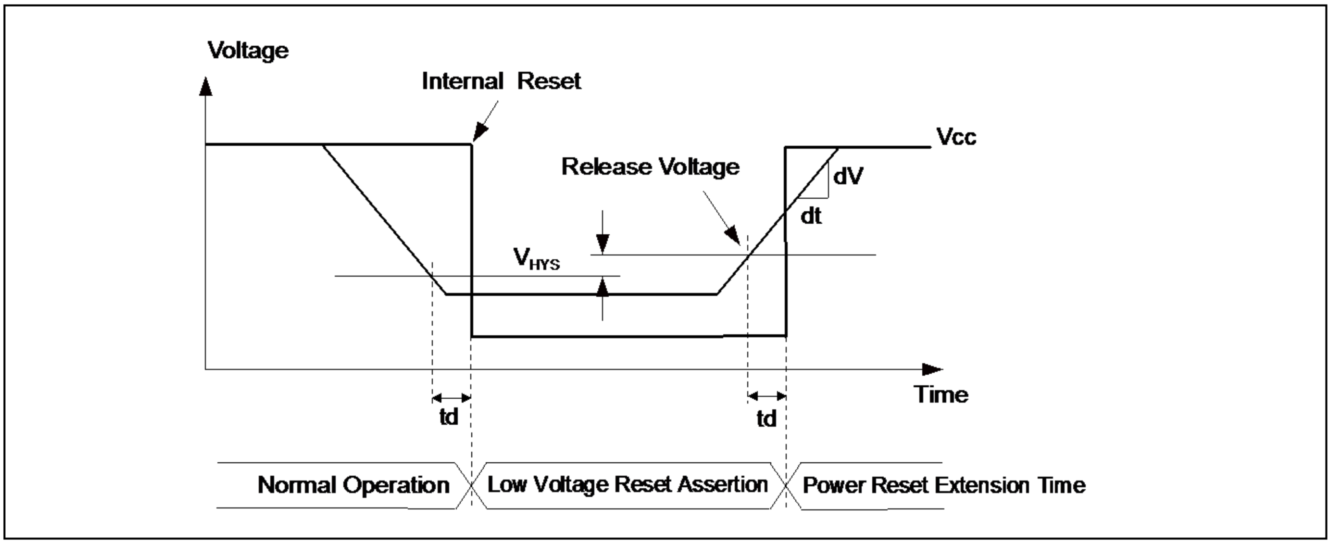
(V_{CC} = AV_{CC} = DV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = DV_{SS} = 0V, T_A = - 40°C to + 105°C)

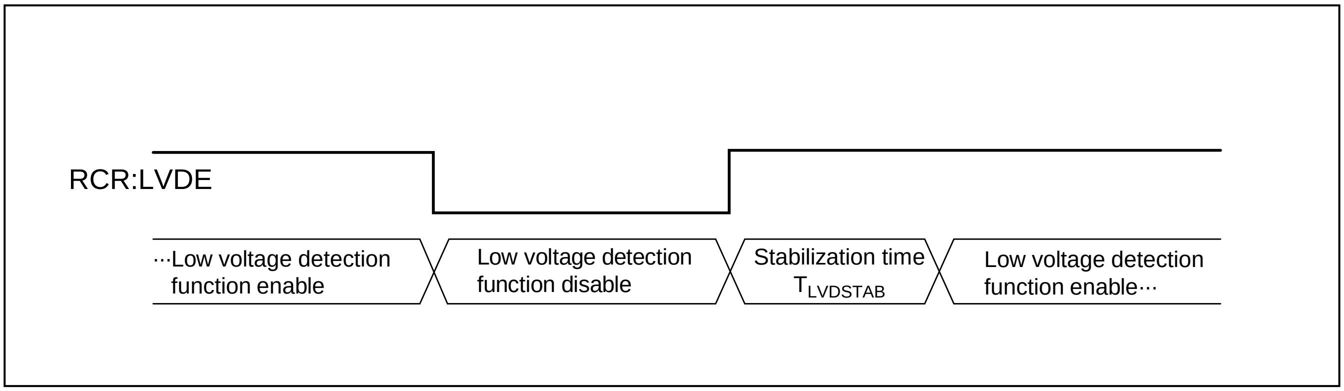
Parameter	Symbol	Conditions	Value			Unit
			Min	Typ	Max	
Detected voltage*1	V_{DL0}	CILCR:LVL = 0000_B	2.70	2.90	3.10	V
	V_{DL1}	CILCR:LVL = 0001_B	2.79	3.00	3.21	V
	V_{DL2}	CILCR:LVL = 0010_B	2.98	3.20	3.42	V
	V_{DL3}	CILCR:LVL = 0011_B	3.26	3.50	3.74	V
	V_{DL4}	CILCR:LVL = 0100_B	3.45	3.70	3.95	V
	V_{DL5}	CILCR:LVL = 0111_B	3.73	4.00	4.27	V
	V_{DL6}	CILCR:LVL = 1001_B	3.91	4.20	4.49	V
Power supply voltage change rate*2	dV/dt	-	- 0.004	-	+ 0.004	V/µs
Hysteresis width	V_{HYS}	CILCR:LVHYS=0	-	-	50	mV
		CILCR:LVHYS=1	80	100	120	mV
Stabilization time	$T_{LVDSTAB}$	-	-	-	75	µs
Detection delay time	t_d	-	-	-	30	µs

*1: If the power supply voltage fluctuates within the time less than the detection delay time (t_d), there is a possibility that the low voltage detection will occur or stop after the power supply voltage passes the detection range.

*2: In order to perform the low voltage detection at the detection voltage (V_{DLX}), be sure to suppress fluctuation of the power supply voltage within the limits of the change ration of power supply voltage.


Voltage
Vcc
Detected Voltage
dV
dt
V_{DLX} max
V_{DLX} min
Time


Voltage
Internal Reset
Vcc
Release Voltage
dV
dt
V_{HYS}
Time
td
td
Normal Operation
Low Voltage Reset Assertion
Power Reset Extension Time


RCR:LVDE
···Low voltage detection function enable
Low voltage detection function disable
Stabilization time $T_{LVDSTAB}$
Low voltage detection function enable···

14.8 Flash Memory Write/Erase Characteristics

(V_{CC} = AV_{CC} = DV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = DV_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter		Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Sector erase time	Large Sector	-	-	1.6	7.5	s	Includes write time prior to internal erase.
	Small Sector	-	-	0.4	2.1	s	
	Security Sector	-	-	0.31	1.65	s	
Word (16-bit) write time		-	-	25	400	µs	Not including system-level overhead time.
Chip erase time		-	-	5.11	25.05	s	Includes write time prior to internal erase.

Note:

While the Flash memory is written or erased, shutdown of the external power (V_{CC}) is prohibited. In the application system where the external power (V_{CC}) might be shut down while writing or erasing, be sure to turn the power off by using a low voltage detection function.

To put it concrete, change the external power in the range of change ration of power supply voltage (-0.004V/µs to +0.004V/µs) after the external power falls below the detection voltage (V_{DLX})[*1].

Write/Erase cycles and data hold time

Write/Erase cycles (cycle)	Data hold time (year)
1,000	20 [*2]
10,000	10 [*2]
100,000	5 [*2]

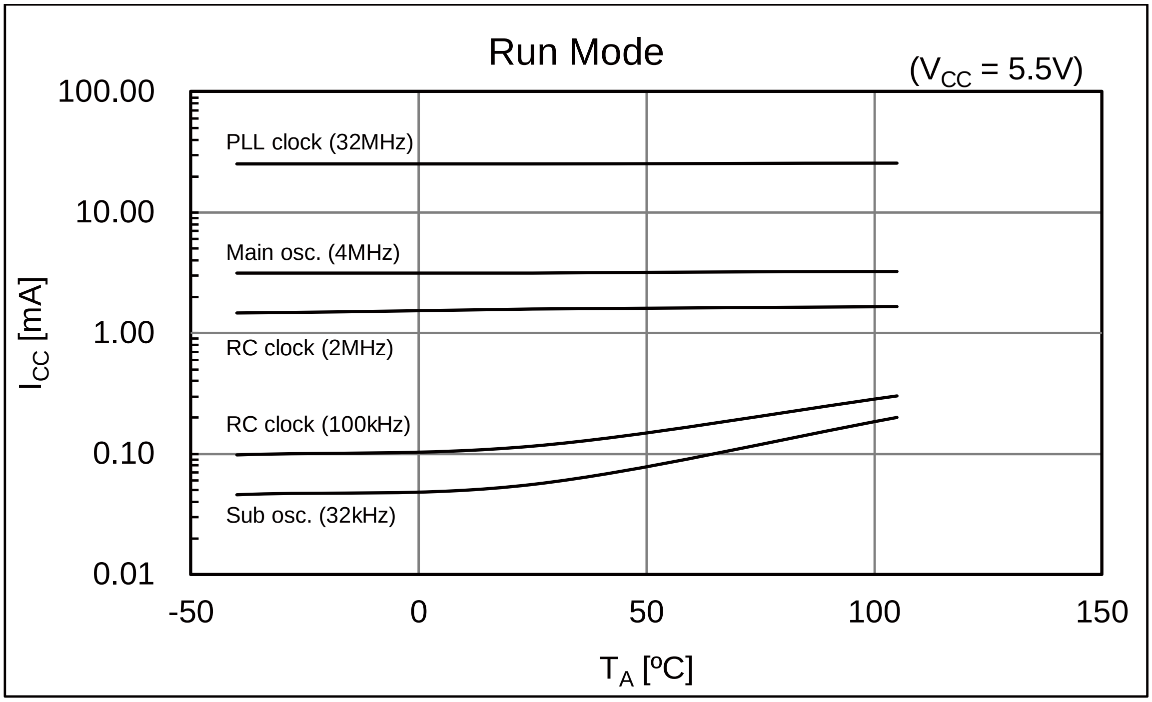
*1: See "14.7 Low Voltage Detection Function Characteristics".

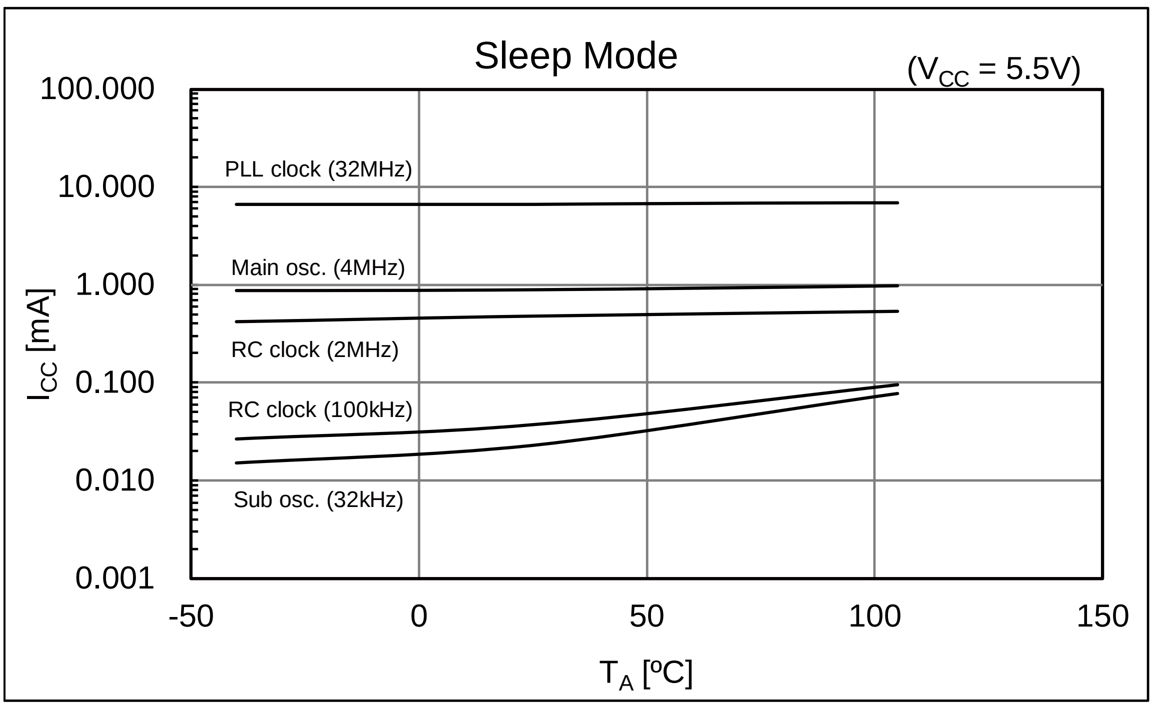
*2: This value comes from the technology qualification (using Arrhenius equation to translate high temperature measurements into normalized value at + 85°C).

15. Example Characteristics

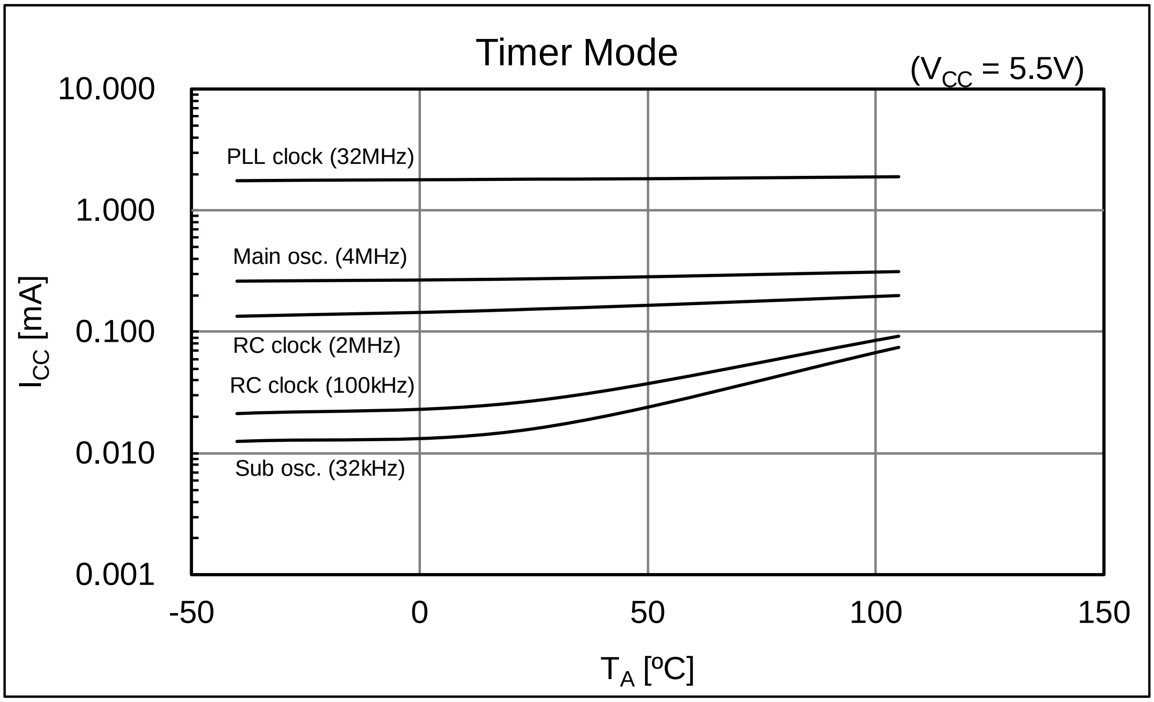
This characteristic is an actual value of the arbitrary sample. It is not the guaranteed value.

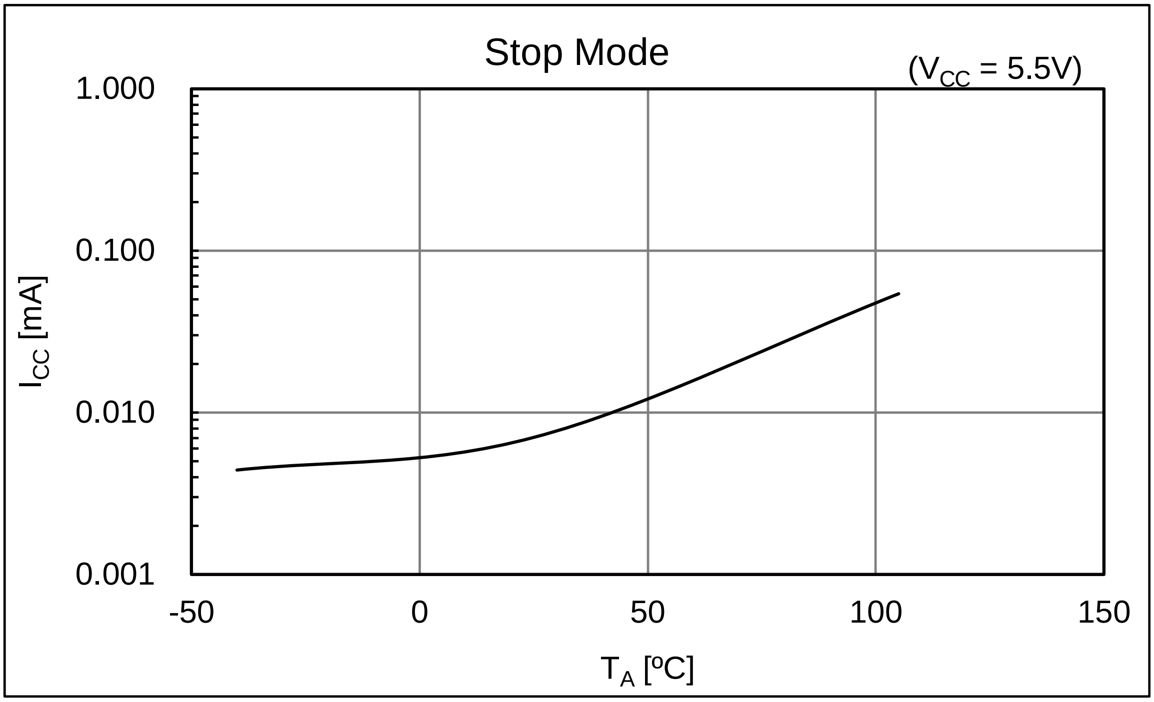
■MB96F685





■MB96F685


Timer Mode
(VCC = 5.5V)
10.000
1.000
0.100
0.010
0.001
ICC [mA]
PLL clock (32MHz)
Main osc. (4MHz)
RC clock (2MHz)
RC clock (100kHz)
Sub osc. (32kHz)
-50
0
50
100
150
TA [ºC]


Stop Mode
(VCC = 5.5V)
1.000
0.100
0.010
0.001
ICC [mA]
-50
0
50
100
150
TA [ºC]

■Used setting

Mode	Selected Source Clock	Clock/Regulator and FLASH Settings
Run mode	PLL	CLKS1 = CLKS2 = CLKB = CLKP1 = CLKP2 = 32MHz
	Main osc.	CLKS1 = CLKS2 = CLKB = CLKP1 = CLKP2 = 4MHz
	RC clock fast	CLKS1 = CLKS2 = CLKB = CLKP1 = CLKP2 = 2MHz
	RC clock slow	CLKS1 = CLKS2 = CLKB = CLKP1 = CLKP2 = 100kHz
	Sub osc.	CLKS1 = CLKS2 = CLKB = CLKP1 = CLKP2 = 32kHz
Sleep mode	PLL	CLKS1 = CLKS2 = CLKP1 = CLKP2 = 32MHz Regulator in High Power Mode, (CLKB is stopped in this mode)
	Main osc.	CLKS1 = CLKS2 = CLKP1 = CLKP2 = 4MHz Regulator in High Power Mode, (CLKB is stopped in this mode)
	RC clock fast	CLKS1 = CLKS2 = CLKP1 = CLKP2 = 2MHz Regulator in High Power Mode, (CLKB is stopped in this mode)
	RC clock slow	CLKS1 = CLKS2 = CLKP1 = CLKP2 = 100kHz Regulator in Low Power Mode, (CLKB is stopped in this mode)
	Sub osc.	CLKS1 = CLKS2 = CLKP1 = CLKP2 = 32kHz Regulator in Low Power Mode, (CLKB is stopped in this mode)
Timer mode	PLL	CLKMC = 4MHz, CLKPLL = 32MHz (System clocks are stopped in this mode) Regulator in High Power Mode, FLASH in Power-down / reset mode
	Main osc.	CLKMC = 4MHz (System clocks are stopped in this mode) Regulator in High Power Mode, FLASH in Power-down / reset mode
	RC clock fast	CLKMC = 2MHz (System clocks are stopped in this mode) Regulator in High Power Mode, FLASH in Power-down / reset mode
	RC clock slow	CLKMC = 100kHz (System clocks are stopped in this mode) Regulator in Low Power Mode, FLASH in Power-down / reset mode
	Sub osc.	CLKMC = 32 kHz (System clocks are stopped in this mode) Regulator in Low Power Mode, FLASH in Power-down / reset mode
Stop mode	stopped	(All clocks are stopped in this mode) Regulator in Low Power Mode, FLASH in Power-down / reset mode

16. Ordering Information

MCU with CAN controller

Part number	Flash memory	Package*
MB96F683RBPMC-GSE1	Flash A (96.5KB)	80-pin plastic LQFP (FPT-80P-M21)
MB96F683RBPMC-GSE2		
MB96F685RBPMC-GSE1	Flash A (160.5KB)	80-pin plastic LQFP (FPT-80P-M21)
MB96F685RBPMC-GSE2		

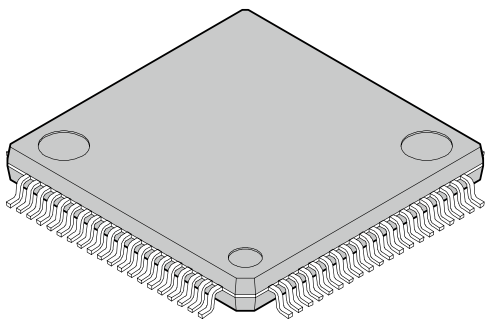
*: For details about package, see "Package Dimension".

MCU without CAN controller

Part number	Flash memory	Package*
MB96F683ABPMC-GSE1	Flash A (96.5KB)	80-pin plastic LQFP (FPT-80P-M21)
MB96F683ABPMC-GSE2		
MB96F685ABPMC-GSE1	Flash A (160.5KB)	80-pin plastic LQFP (FPT-80P-M21)
MB96F685ABPMC-GSE2		

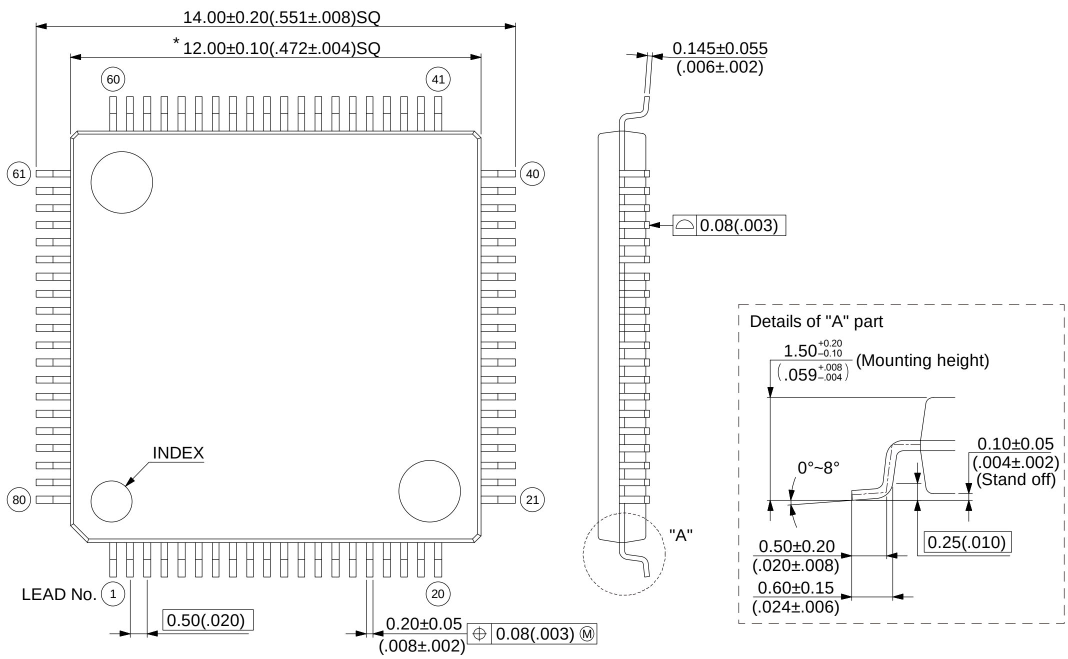
*: For details about package, see "Package Dimension".

17. Package Dimension

80-pin plastic LQFP	Lead pitch	0.50 mm
	Package width × package length	12 mm × 12 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.70 mm Max
	Weight	0.47 g
(FPT-80P-M21)	Code (Reference)	P-LFQFP80-12×12-0.50

80-pin plastic LQFP
(FPT-80P-M21)

Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.



Dimensions in mm (inches).
Note: The values in parentheses are reference values

18. Major Changes

Spansion Publication Number: MB96680_DS704-00002

Page	Section	Change Results
Revision 2.0		
40	Electrical Characteristics 3. DC Characteristics (1) Current Rating	Changed the Value of “Power supply current in Timer modes” I_{CCTPLL} Typ: 1880μA → 1800μA (T_A = +25°C)
Revision 2.1		
-	-	Company name and layout design change

NOTE: Please see “Document History” about later revised information.

Document History

Document Title: MB96680 Series F^{2}MC-16FX 16-Bit Microcontroller
Document Number: 002-04705

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	-	TORS	01/31/2014	Migrated to Cypress and assigned document number 002-04705 No change to document contents or format.
*A	5147098	TORS	08/22/2016	Updated to Cypress format.

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