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# 1 Description

The devices are Electrically Erasable PROgrammable Memories (EEPROMs) organized as as 2048x8 bits, 1024x8 bits, 512x8 bits, 256x8 bits (M24C16, M24C08, M24C04 and M24C02).

The devices are compatible with all I²C modes up to 400 kHz and can operate with a supply voltage range from 2.5 V up to 5.5 V. The devices are guaranteed over the -40°C/+125°C temperature range and are compliant with the Automotive standard AEC-Q100 Grade 1.

**Figure 1. Logic diagram**

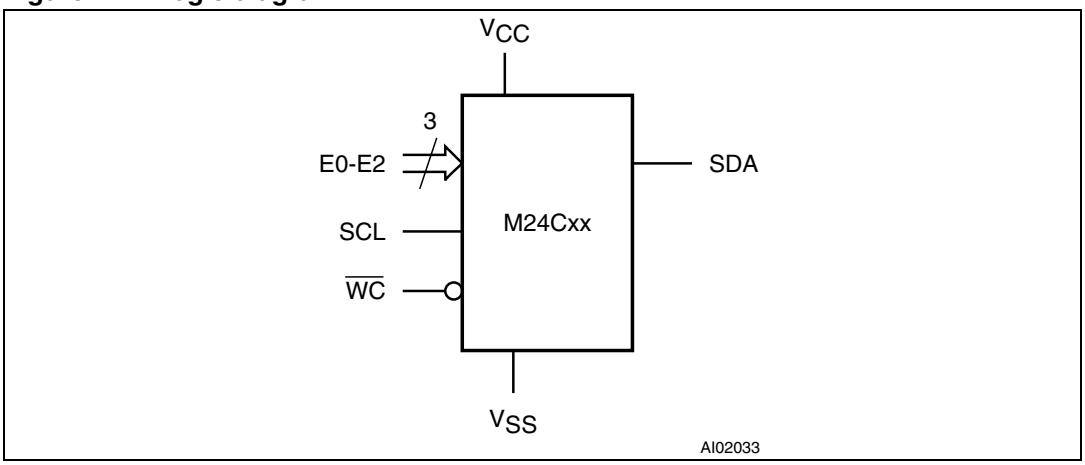
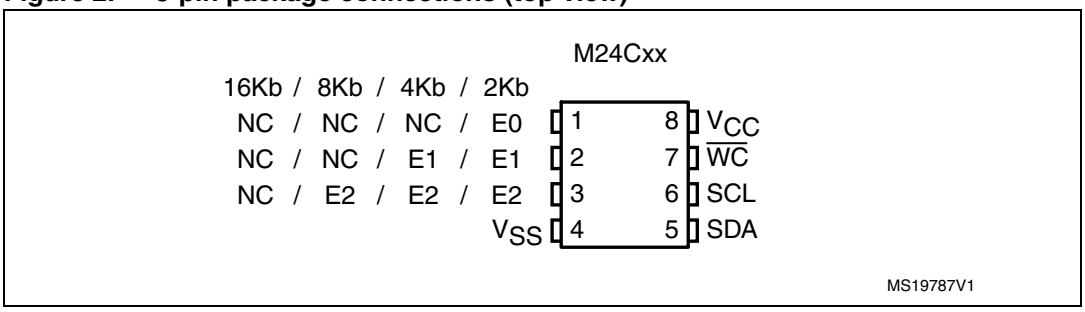



**Table 1. Signal names**

| Signal name | Function | Direction |
|---|---|---|
| E0, E1, E2 | Chip Enable | Input |
| SDA | Serial Data | Input/output |
| SCL | Serial Clock | Input |
| $\overline{WC}$ | Write Control | Input |
| $V_{CC}$ | Supply voltage | |
| $V_{SS}$ | Ground | |

**Figure 2. 8-pin package connections (top view)**




1. NC = Not connected
2. See *Section 7: Package mechanical data* for package dimensions, and how to identify pin-1.

# 2 Signal description

## 2.1 Serial Clock (SCL)

This input signal is used to strobe all data in and out of the device. In applications where this signal is used by slave devices to synchronize the bus to a slower clock, the bus master must have an open drain output, and a pull-up resistor can be connected from Serial Clock (SCL) to $V_{CC}$. (*Figure 4* indicates how the value of the pull-up resistor can be calculated). In most applications, though, this method of synchronization is not employed, and so the pull-up resistor is not necessary, provided that the bus master has a push-pull (rather than open drain) output.

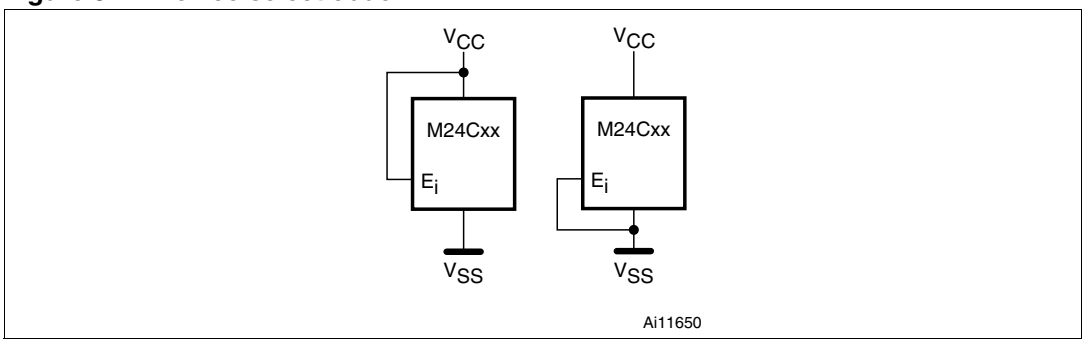
## 2.2 Serial Data (SDA)

This bidirectional signal is used to transfer data in or out of the device. It is an open drain output that may be wire-ORed with other open drain or open collector signals on the bus. A pull up resistor must be connected from Serial Data (SDA) to $V_{CC}$. (*Figure 4* indicates how the value of the pull-up resistor can be calculated).

## 2.3 Chip Enable (E0, E1, E2)

These input signals are used to set the value that is to be looked for on the least significant bits of the 7-bit device select code. These inputs must be tied to $V_{CC}$ or $V_{SS}$, to establish the device select code as shown in *Figure 3*. When not connected (left floating), Ei inputs are read as low (0).

**Figure 3. Device select code**




### 2.3.1 Write Control ($\overline{WC}$)

This input signal is useful for protecting the entire contents of the memory from inadvertent write operations. Write operations are disabled to the entire memory array when Write Control ($\overline{WC}$) is driven High. When unconnected, the signal is internally read as $V_{IL}$, and Write operations are allowed.

When Write Control ($\overline{WC}$) is driven High, device select and address bytes are acknowledged, data bytes are not acknowledged.

## 2.4 Supply voltage ($V_{CC}$)

### 2.4.1 Operating supply voltage $V_{CC}$

Prior to selecting the memory and issuing instructions to it, a valid and stable $V_{CC}$ voltage within the specified [$V_{CC}$(min), $V_{CC}$(max)] range must be applied (see Operating conditions in *Section 6: DC and AC parameters*). In order to secure a stable DC supply voltage, it is recommended to decouple the $V_{CC}$ line with a suitable capacitor (usually of the order of 10 nF to 100 nF) close to the $V_{CC}$/$V_{SS}$ package pins.

This voltage must remain stable and valid until the end of the transmission of the instruction and, for a Write instruction, until the completion of the internal write cycle ($t_W$).

### 2.4.2 Power-up conditions

The $V_{CC}$ voltage has to rise continuously from 0 V up to the minimum $V_{CC}$ operating voltage defined in Operating conditions in *Section 6: DC and AC parameters* and the rise time must *not* vary faster than 1 V/µs.

### 2.4.3 Device reset

In order to prevent inadvertent write operations during power-up, a power-on-reset (POR) circuit is included. At power-up (continuous rise of $V_{CC}$), the device does not respond to any instruction until $V_{CC}$ reaches the power-on-reset threshold voltage (this threshold is lower than the minimum $V_{CC}$ operating voltage defined in Operating conditions in *Section 6: DC and AC parameters*). When $V_{CC}$ passes over the POR threshold, the device is reset and enters the Standby Power mode. The device, however, must not be accessed until $V_{CC}$ reaches a valid and stable $V_{CC}$ voltage within the specified [$V_{CC}$(min), $V_{CC}$(max)] range.

In a similar way, during power-down (continuous decrease in $V_{CC}$), as soon as $V_{CC}$ drops below the power-on-reset threshold voltage, the device stops responding to any instruction sent to it.

### 2.4.4 Power-down conditions

During power-down (continuous decrease in $V_{CC}$), the device must be in the Standby Power mode (mode reached after decoding a Stop condition, assuming that there is no internal write cycle in progress).

**Figure 4. $I^2C$ Fast mode ($f_C$ = 400 kHz): maximum Rbus value versus bus parasitic capacitance ($C_{bus}$)**

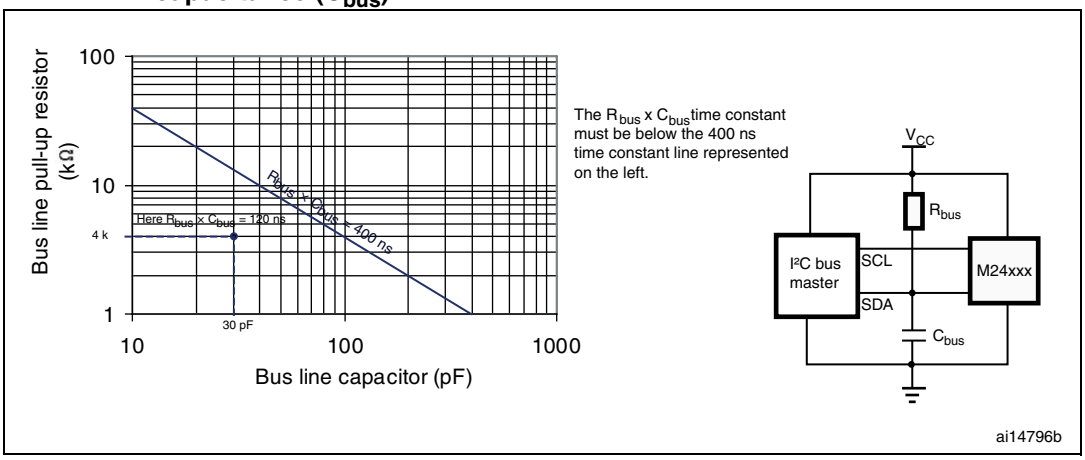



**Figure 5. I²C bus protocol**

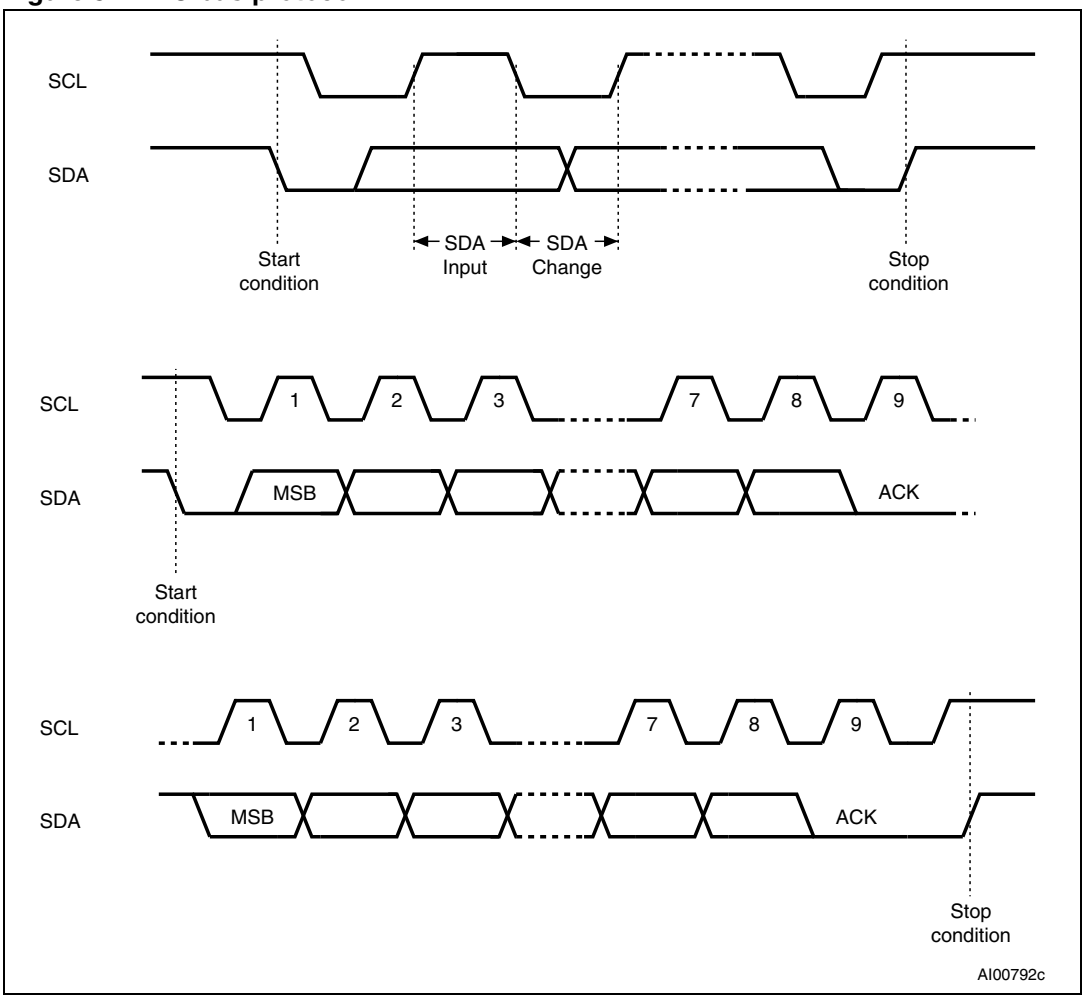


**Table 2. Device select code**

| | Device type identifier(1) | | | | Chip Enable(2),(3) | | | RW |
|---|---|---|---|---|---|---|---|---|
| | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
| M24C02 select code | 1 | 0 | 1 | 0 | E2 | E1 | E0 | RW |
| M24C04 select code | 1 | 0 | 1 | 0 | E2 | E1 | A8 | RW |
| M24C08 select code | 1 | 0 | 1 | 0 | E2 | A9 | A8 | RW |
| M24C16 select code | 1 | 0 | 1 | 0 | A10 | A9 | A8 | RW |

1. The most significant bit, b7, is sent first.
2. E0, E1 and E2 are compared against the respective external pins on the memory device.
3. A10, A9 and A8 represent most significant bits of the address.

# 3 Device operation

The device supports the I²C protocol. This is summarized in *Figure 5*. Any device that sends data on to the bus is defined to be a transmitter, and any device that reads the data to be a receiver. The device that controls the data transfer is known as the bus master, and the other as the slave device. A data transfer can only be initiated by the bus master, which will also provide the serial clock for synchronization. The device is always a slave in all communication.

## 3.1 Start condition

Start is identified by a falling edge of Serial Data (SDA) while Serial Clock (SCL) is stable in the High state. A Start condition must precede any data transfer command. The device continuously monitors (except during a Write cycle) Serial Data (SDA) and Serial Clock (SCL) for a Start condition.

## 3.2 Stop condition

Stop is identified by a rising edge of Serial Data (SDA) while Serial Clock (SCL) is stable and driven High. A Stop condition terminates communication between the device and the bus master. A Read command that is followed by NoAck can be followed by a Stop condition to force the device into the Standby mode. A Stop condition at the end of a Write command triggers the internal Write cycle.

## 3.3 Acknowledge bit (ACK)

The acknowledge bit is used to indicate a successful byte transfer. The bus transmitter, whether it be bus master or slave device, releases Serial Data (SDA) after sending eight bits of data. During the 9$^{th}$ clock pulse period, the receiver pulls Serial Data (SDA) Low to acknowledge the receipt of the eight data bits.

## 3.4 Data input

During data input, the device samples Serial Data (SDA) on the rising edge of Serial Clock (SCL). For correct device operation, Serial Data (SDA) must be stable during the rising edge of Serial Clock (SCL), and the Serial Data (SDA) signal must change *only* when Serial Clock (SCL) is driven Low.

## 3.5 Memory addressing

To start communication between the bus master and the slave device, the bus master must initiate a Start condition. Following this, the bus master sends the device select code, shown in *Table 2* (on Serial Data (SDA), most significant bit first).

The device select code consists of a 4-bit Device Type Identifier, and a 3-bit Chip Enable "Address" (E2, E1, E0). To address the memory array, the 4-bit Device Type Identifier is 1010b.

Each device is given a unique 3-bit code on the Chip Enable (E0, E1, E2) inputs. When the device select code is received, the device only responds if the Chip Enable Address is the same as the value on the Chip Enable (E0, E1, E2) inputs. However, those devices with larger memory capacities (the M24C16, M24C08 and M24C04) need more address bits. E0 is not available for use on devices that need to use address line A8; E1 is not available for devices that need to use address line A9, and E2 is not available for devices that need to use address line A10 (see *Figure 2* and *Table 2* for details). Using the E0, E1 and E2 inputs, up to eight M24C02, four M24C04, two M24C08 or one M24C16 devices can be connected to one I²C bus.

The 8th bit is the Read/$\overline{\text{Write}}$ bit ($\overline{\text{RW}}$). This bit is set to 1 for Read and 0 for Write operations.

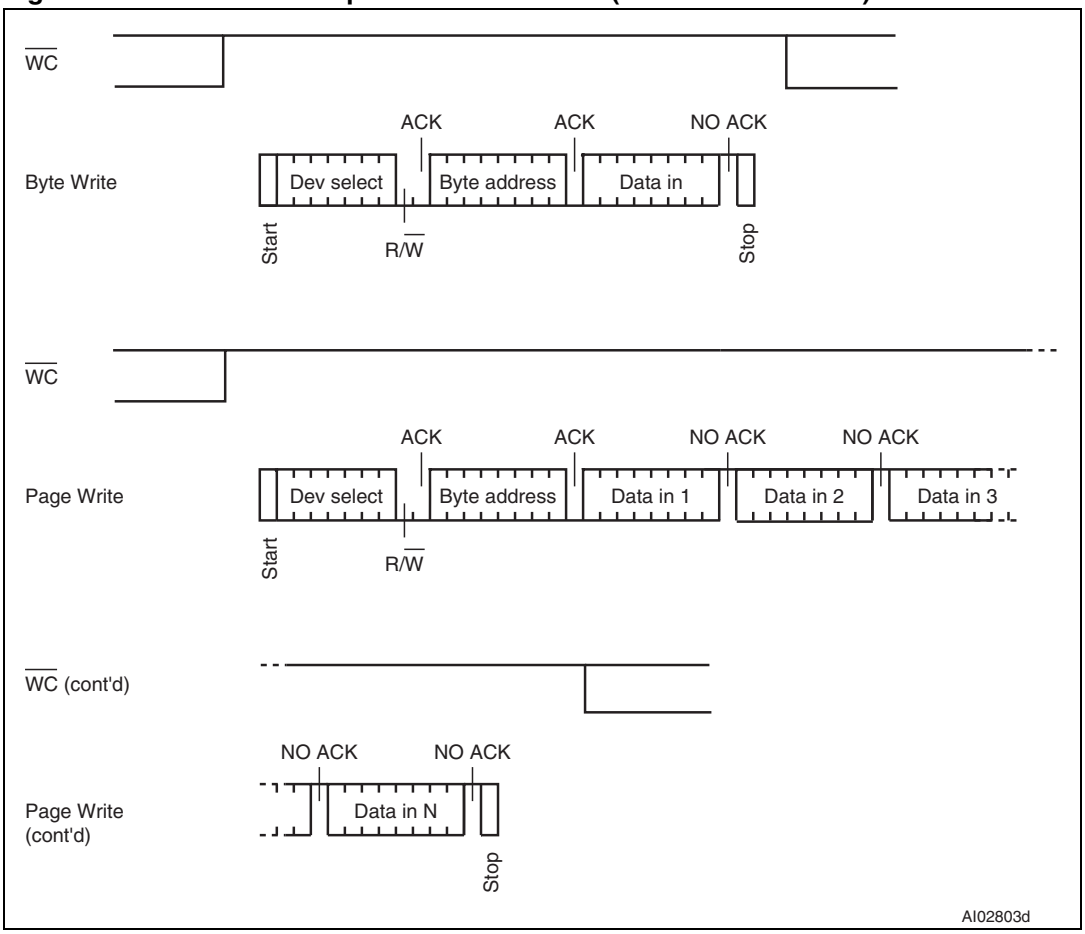
If a match occurs on the device select code, the corresponding device gives an acknowledgment on Serial Data (SDA) during the 9th bit time. If the device does not match the device select code, it deselects itself from the bus, and goes into Standby mode.

**Table 3. Operating modes**

| Mode | $\overline{\text{RW}}$ bit | $\overline{\text{WC}}$(1) | Bytes | Initial sequence |
|---|---|---|---|---|
| Current Address Read | 1 | X | 1 | Start, Device Select, $\overline{\text{RW}}$ = 1 |
| Random Address Read | 0 | X | 1 | Start, Device Select, $\overline{\text{RW}}$ = 0, Address |
| | 1 | X | | reStart, Device Select, $\overline{\text{RW}}$ = 1 |
| Sequential Read | 1 | X | ≥ 1 | Similar to Current or Random Address Read |
| Byte Write | 0 | $V_{IL}$ | 1 | Start, Device Select, $\overline{\text{RW}}$ = 0 |
| Page Write | 0 | $V_{IL}$ | ≤16 | Start, Device Select, $\overline{\text{RW}}$ = 0 |

1. X = $V_{IH}$ or $V_{IL}$.

**Figure 6. Write mode sequences with $\overline{WC}$ = 1 (data write inhibited)**




## 3.6 Write operations

Following a Start condition the bus master sends a device select code with the Read/$\overline{Write}$ bit ($R\overline{W}$) reset to 0. The device acknowledges this, as shown in *Figure 7*, and waits for an address byte. The device responds to the address byte with an acknowledge bit, and then waits for the data byte.

When the bus master generates a Stop condition immediately after a data byte Ack bit (in the "$10^{th}$ bit" time slot), either at the end of a Byte Write or a Page Write, the internal write cycle is triggered. A Stop condition at any other time slot does not trigger the internal write cycle.

After the Stop condition, the $t_w$ delay, and the successful completion of a Write operation, the device internal address counter is automatically incremented, to point to the next byte address after the last one that was modified. During the internal Write cycle, Serial Data (SDA) is disabled internally, and the device does not respond to any request.

If the Write Control (WC) input is driven High, the Write instruction is not executed and the corresponding data bytes are not acknowledged as shown in *Figure 6*.

### 3.6.1 Byte Write

After the device select code and the address byte, the bus master sends one data byte. If the addressed location is Write-protected, by Write Control ($\overline{WC}$) being driven High, the device replies to the data byte with NoAck, as shown in *Figure 6*, and the location is not modified. If, instead, the addressed location is not Write-protected, the device replies with Ack. The bus master terminates the transfer by generating a Stop condition, as shown in *Figure 7*.

### 3.6.2 Page Write

The Page Write mode allows up to 16 bytes to be written in a single Write cycle, provided that they are all located in the same page in the memory: that is, the most significant memory address bits are the same. If more bytes are sent than will fit up to the end of the page, a condition known as ‘roll-over’ occurs. This should be avoided, as data starts to become overwritten in an implementation dependent way.

The bus master sends from 1 to 16 bytes of data, each of which is acknowledged by the device if Write Control ($\overline{WC}$) is Low. If the addressed location is Write-protected, by Write Control ($\overline{WC}$) being driven High, the device replies to the data bytes with NoAck, as shown in *Figure 6*, and the locations are not modified. After each byte is transferred, the internal byte address counter (the 4 least significant address bits only) is incremented. The transfer is terminated by the bus master generating a Stop condition.

**Figure 7. Write mode sequences with $\overline{WC}$ = 0 (data write enabled)**

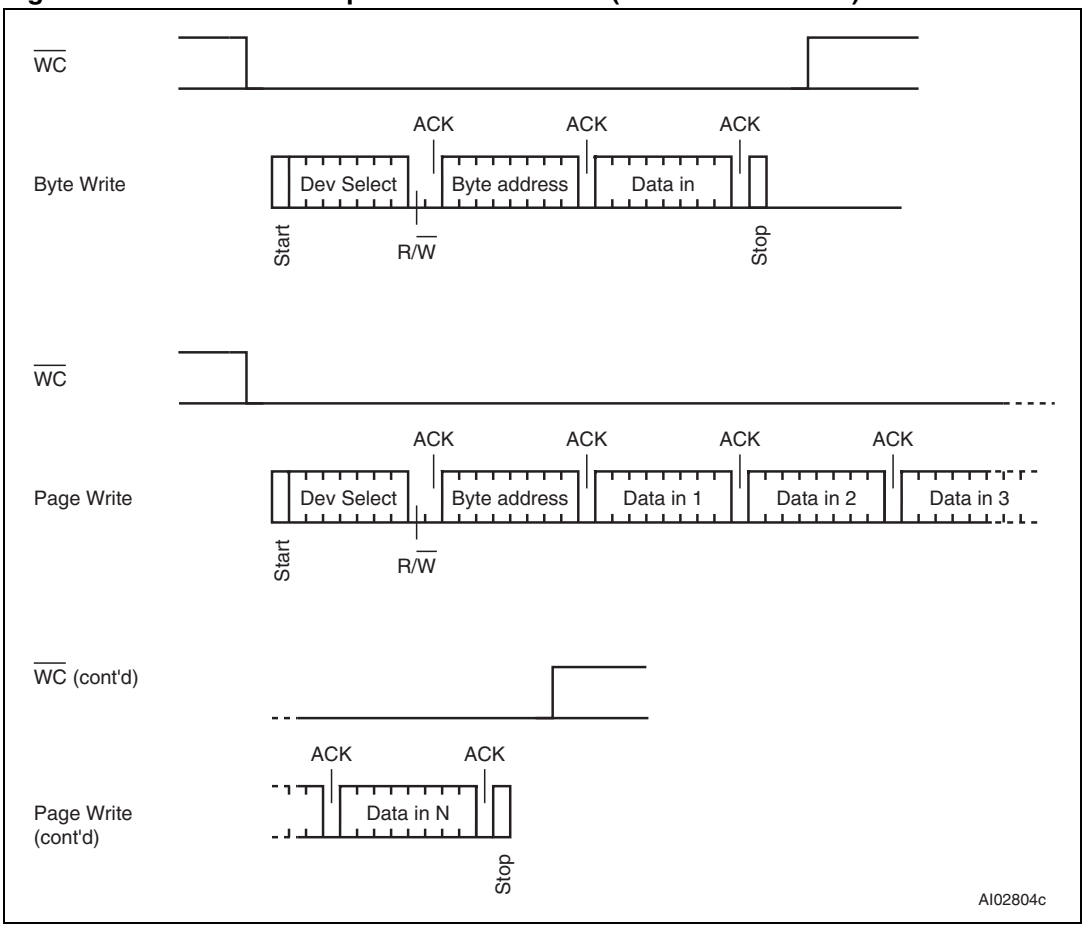
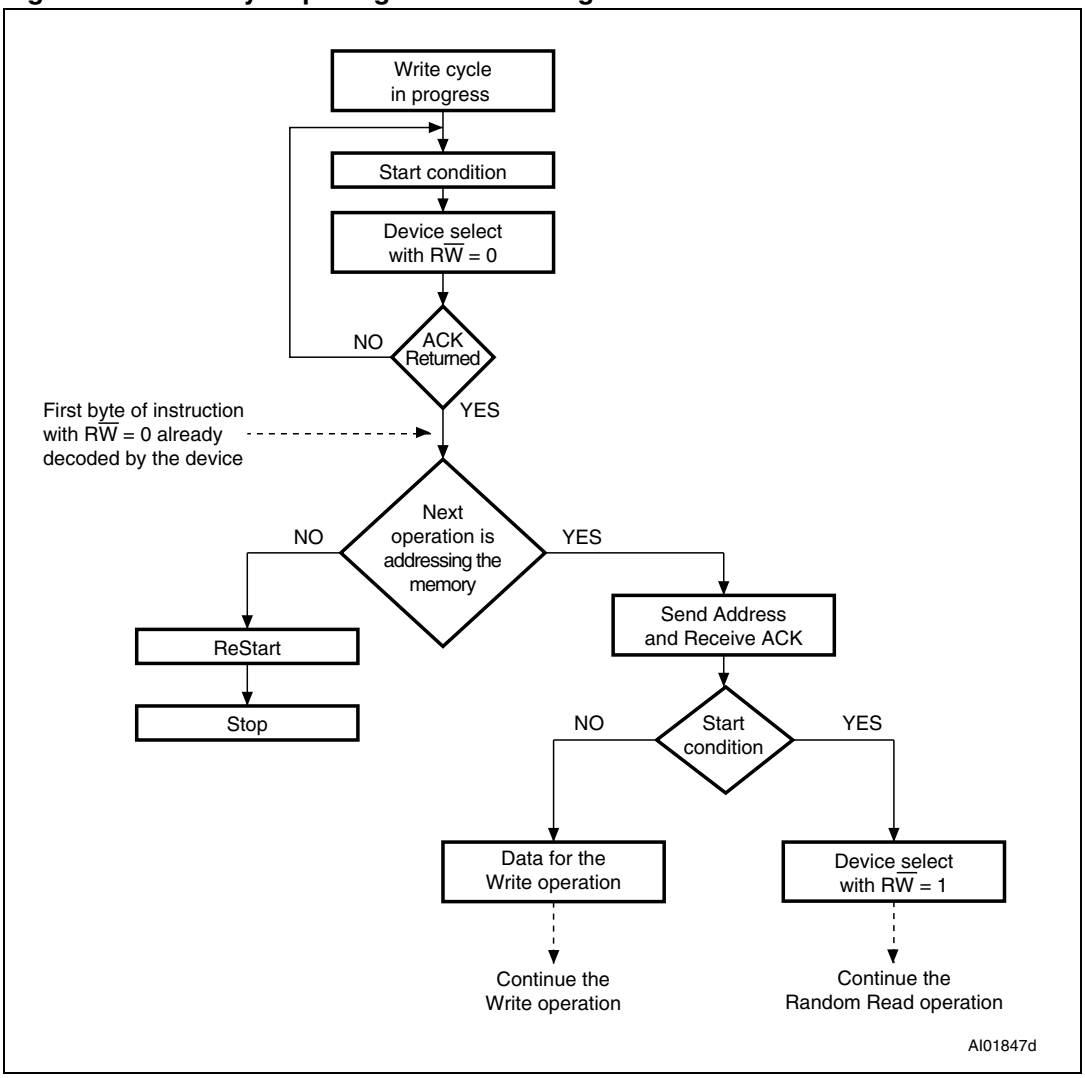


**Figure 8. Write cycle polling flowchart using ACK**



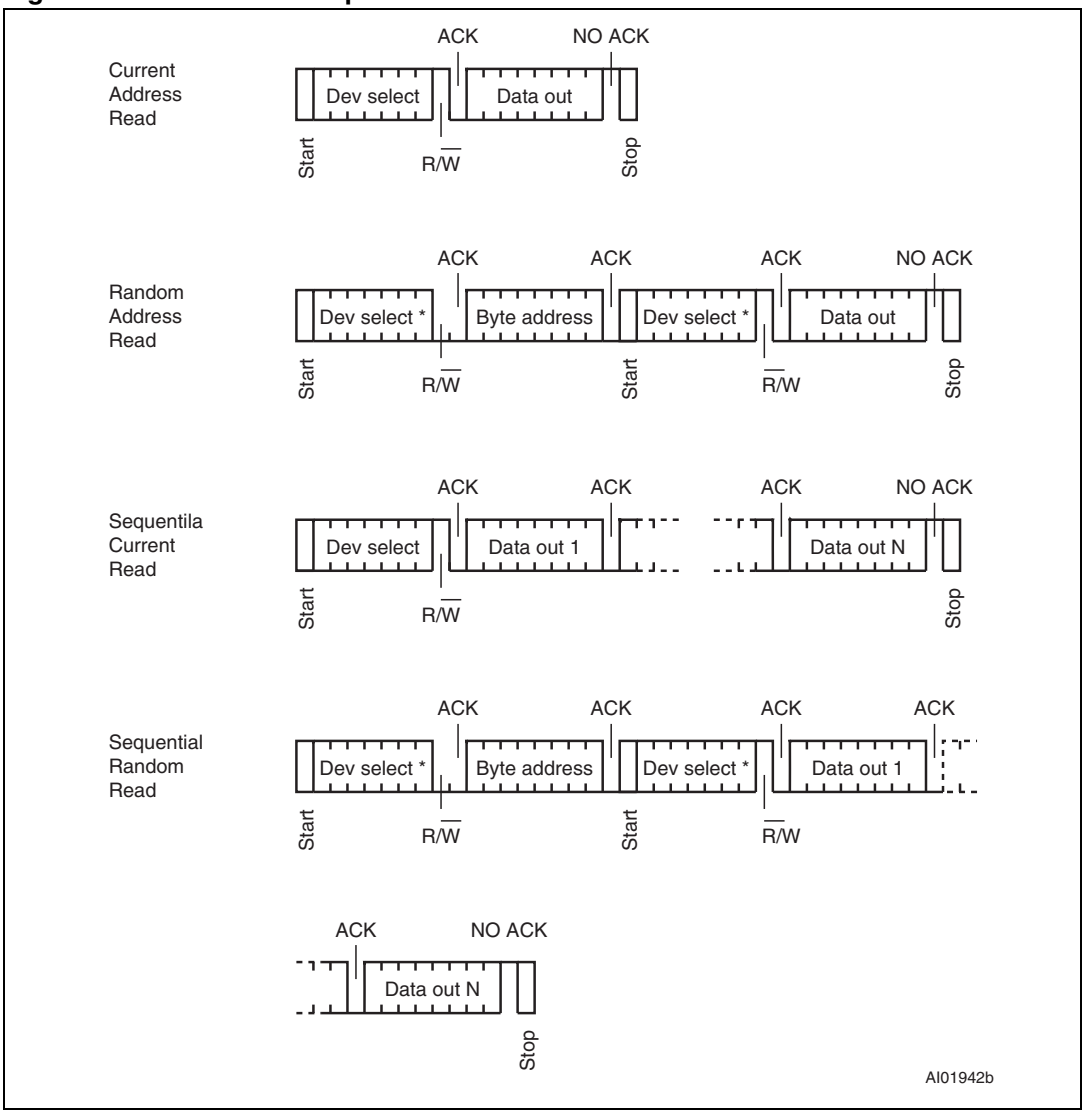

### 3.6.3 Minimizing system delays by polling on ACK

During the internal Write cycle, the device disconnects itself from the bus, and writes a copy of the data from its internal latches to the memory cells. The maximum Write time ($t_w$) is shown in *Table 9*, but the typical time is shorter. To make use of this, a polling sequence can be used by the bus master.

The sequence, as shown in *Figure 8*, is:

- Initial condition: a Write cycle is in progress.
- Step 1: the bus master issues a Start condition followed by a device select code (the first byte of the new instruction).
- Step 2: if the device is busy with the internal Write cycle, no Ack will be returned and the bus master goes back to Step 1. If the device has terminated the internal Write cycle, it responds with an Ack, indicating that the device is ready to receive the second part of the instruction (the first byte of this instruction having been sent during Step 1).

**Figure 9. Read mode sequences**




1. The seven most significant bits of the device select code of a Random Read (in the 1st and 3rd bytes) must be identical.

## 3.7 Read operations

Read operations are performed independently of the state of the Write Control ($\overline{WC}$) signal.

The device has an internal address counter which is incremented each time a byte is read.

### 3.7.1 Random Address Read

A dummy Write is first performed to load the address into this address counter (as shown in *Figure 9*) but *without* sending a Stop condition. Then, the bus master sends another Start condition, and repeats the device select code, with the Read/$\overline{Write}$ bit ($R\overline{W}$) set to 1. The device acknowledges this, and outputs the contents of the addressed byte. The bus master must *not* acknowledge the byte, and terminates the transfer with a Stop condition.

### 3.7.2 Current Address Read

For the Current Address Read operation, following a Start condition, the bus master only sends a device select code with the Read/$\overline{\text{Write}}$ bit (R$\overline{\text{W}}$) set to 1. The device acknowledges this, and outputs the byte addressed by the internal address counter. The counter is then incremented. The bus master terminates the transfer with a Stop condition, as shown in *Figure 9*, *without* acknowledging the byte.

### 3.7.3 Sequential Read

This operation can be used after a Current Address Read or a Random Address Read. The bus master *does* acknowledge the data byte output, and sends additional clock pulses so that the device continues to output the next byte in sequence. To terminate the stream of bytes, the bus master must *not* acknowledge the last byte, and *must* generate a Stop condition, as shown in *Figure 9*.

The output data comes from consecutive addresses, with the internal address counter automatically incremented after each byte output. After the last memory address, the address counter 'rolls-over', and the device continues to output data from memory address 00h.

### 3.7.4 Acknowledge in Read mode

For all Read commands, the device waits, after each byte read, for an acknowledgment during the 9$^{th}$ bit time. If the bus master does not drive Serial Data (SDA) Low during this time, the device terminates the data transfer and switches to its Standby mode.

# 4 Initial delivery state

The device is delivered with all bits in the memory array set to 1 (each byte contains FFh).

# 5 Maximum rating

Stressing the device outside the ratings listed in *Table 4* may cause permanent damage to the device. These are stress ratings only, and operation of the device at these, or any other conditions outside those indicated in the operating sections of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Table 4. Absolute maximum ratings**

| Symbol | Parameter | Min. | Max. | Unit |
|---|---|---|---|---|
| | Ambient operating temperature | –40 | 130 | °C |
| $T_{STG}$ | Storage temperature | –65 | 150 | °C |
| $T_{LEAD}$ | Lead temperature during soldering | see note (1) | | °C |
| $I_{OL}$ | DC output current (SDA = 0) | - | 5 | mA |
| $V_{IO}$ | Input or output range | –0.50 | 6.5 | V |
| $V_{CC}$ | Supply voltage | –0.50 | 6.5 | V |
| $V_{ESD}$ | Electrostatic pulse (human body model)(2) | - | 4000 | V |

1. Compliant with JEDEC Std J-STD-020C (for small body, Sn-Pb or Pb assembly), the ST ECOPACK® 7191395 specification, and the European directive on Restrictions on Hazardous Substances (RoHS) 2002/95/EU.
2. Positive and negative pulses applied on pin pairs, according to AEC-Q100-002 (compliant with JEDEC Std JESD22-A114, C1=100 pF, R1=1500 Ω, R2=500 Ω).

# 6 DC and AC parameters

This section summarizes the operating and measurement conditions, and the DC and AC characteristics of the device. The parameters in the DC and AC characteristic tables that follow are derived from tests performed under the measurement conditions summarized in the relevant tables. Designers should check that the operating conditions in their circuit match the measurement conditions when relying on the quoted parameters.

**Table 5. Operating conditions**

| Symbol | Parameter | Min. | Max. | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | 2.5 | 5.5 | V |
| | Ambient operating temperature | –40 | 125 | °C |

**Table 6. AC measurement conditions**

| Symbol | Parameter | Min. | Max. | Unit |
|---|---|---|---|---|
| $C_{bus}$ | Load capacitance | 100 | | pF |
| | SCL input rise/fall time, SDA input fall time | - | 50 | ns |
| | Input levels | 0.2 $V_{CC}$ to 0.8 $V_{CC}$ | | V |
| | Input and output timing reference levels | 0.3 $V_{CC}$ to 0.7 $V_{CC}$ | | V |

**Figure 10. AC measurement I/O waveform**

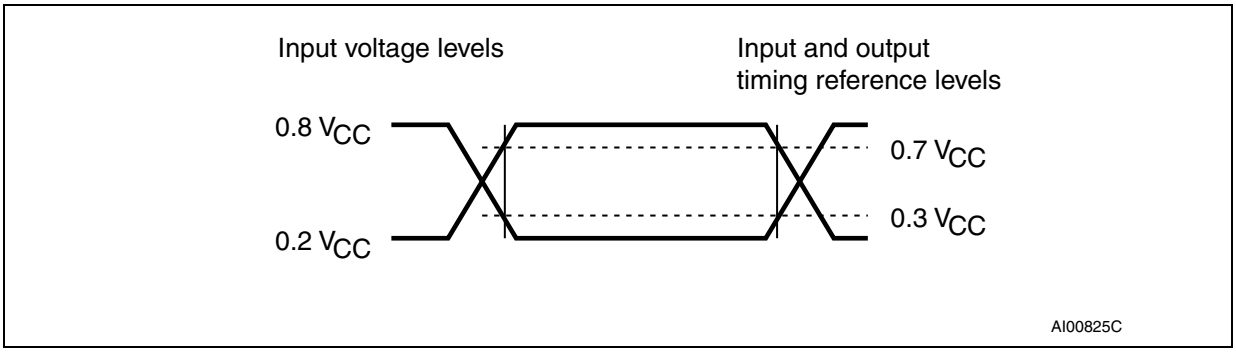



**Table 7. Input parameters**

| Symbol | Parameter[1] | Test condition | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $C_{IN}$ | Input capacitance (SDA) | | - | 8 | pF |
| $C_{IN}$ | Input capacitance (other pins) | | - | 6 | pF |
| $Z_{WCL}$ | $\overline{WC}$ input impedance | $V_{IN}$ < 0.3 V | 15 | 70 | kΩ |
| $Z_{WCH}$ | $\overline{WC}$ input impedance | $V_{IN}$ > 0.7$V_{CC}$ | 500 | - | kΩ |
| $t_{NS}$ | Pulse width ignored (input filter on SCL and SDA) | Single glitch | - | 100 | ns |

1. Characterized only.

**Table 8. DC characteristics**

| Symbol | Parameter | Test condition (in addition to those in *Table 5*) | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $I_{LI}$ | Input leakage current (SCL, SDA, E0, E1,and E2) | $V_{IN} = V_{SS}$ or $V_{CC}$, device in Standby mode | - | ± 2 | µA |
| $I_{LO}$ | Output leakage current | SDA in Hi-Z, external voltage applied on SDA: $V_{SS}$ or $V_{CC}$ | - | ± 2 | µA |
| $I_{CC}$ | Supply current | $V_{CC}$ = 5 V, $f_C$= 400 kHz (rise/fall time < 50 ns) | - | 3 | mA |
| | | $V_{CC}$ = 2.5 V, $f_C$ = 400 kHz (rise/fall time < 50 ns) | - | 3 | mA |
| $I_{CC1}$ | Standby supply current | Device not selected(1), $V_{IN} = V_{SS}$ or $V_{CC}$, $V_{CC}$ = 5 V | - | 5 | µA |
| | | Device not selected(1), $V_{IN} = V_{SS}$ or $V_{CC}$, $V_{CC}$ = 2.5 V | - | 2 | µA |
| $V_{IL}$ | Input low voltage (SDA, SCL, $\overline{WC}$) | | –0.45 | 0.3 $V_{CC}$ | V |
| $V_{IH}$ | Input high voltage (SDA, SCL, $\overline{WC}$) | | 0.7 $V_{CC}$ | $V_{CC}$+1 | V |
| $V_{OL}$ | Output low voltage | $I_{OL}$ = 2.1 mA when $V_{CC}$ = 2.5 V or $I_{OL}$ = 3 mA when $V_{CC}$ = 5.5 V | - | 0.4 | V |

1. The device is not selected after a power-up, after a read command (after the Stop condition), or after the completion of the internal write cycle $t_W$ ($t_W$ is triggered by the correct decoding of a write command).

**Table 9. AC characteristics at 400 kHz ($I^2C$ Fast mode)**

| Test conditions specified in *Section 6: DC and AC parameters* | | | | | |
|---|---|---|---|---|---|
| **Symbol** | **Alt.** | **Parameter** | **Min.(1)** | **Max.(1)** | **Unit** |
| $f_C$ | $f_{SCL}$ | Clock frequency | - | 400 | kHz |
| $t_{CHCL}$ | $t_{HIGH}$ | Clock pulse width high | 600 | - | ns |
| $t_{CLCH}$ | $t_{LOW}$ | Clock pulse width low | 1300 | - | ns |
| $t_{QL1QL2}$(2) | $t_F$ | SDA (out) fall time | 20(3) | 120 | ns |
| $t_{XH1XH2}$ | $t_R$ | Input signal rise time | (4) | (4) | ns |
| $t_{XL1XL2}$ | $t_F$ | Input signal fall time | (4) | (4) | ns |
| $t_{DXCX}$ | $t_{SU:DAT}$ | Data in set up time | 100 | - | ns |
| $t_{CLDX}$ | $t_{HD:DAT}$ | Data in hold time | 0 | - | ns |
| $t_{CLQX}$(5) | $t_{DH}$ | Data out hold time | 100 | - | ns |
| $t_{CLQV}$(6) | $t_{AA}$ | Clock low to next data valid (access time) | 200 | 900 | ns |
| $t_{CHDL}$ | $t_{SU:STA}$ | Start condition setup time | 600 | - | ns |
| $t_{DLCL}$ | $t_{HD:STA}$ | Start condition hold time | 600 | - | ns |
| $t_{CHDH}$ | $t_{SU:STO}$ | Stop condition set up time | 600 | - | ns |
| $t_{DHDL}$ | $t_{BUF}$ | Time between Stop condition and next Start condition | 1300 | - | ns |
| $t_W$ | $t_{WR}$ | Write time | - | 5 | ms |

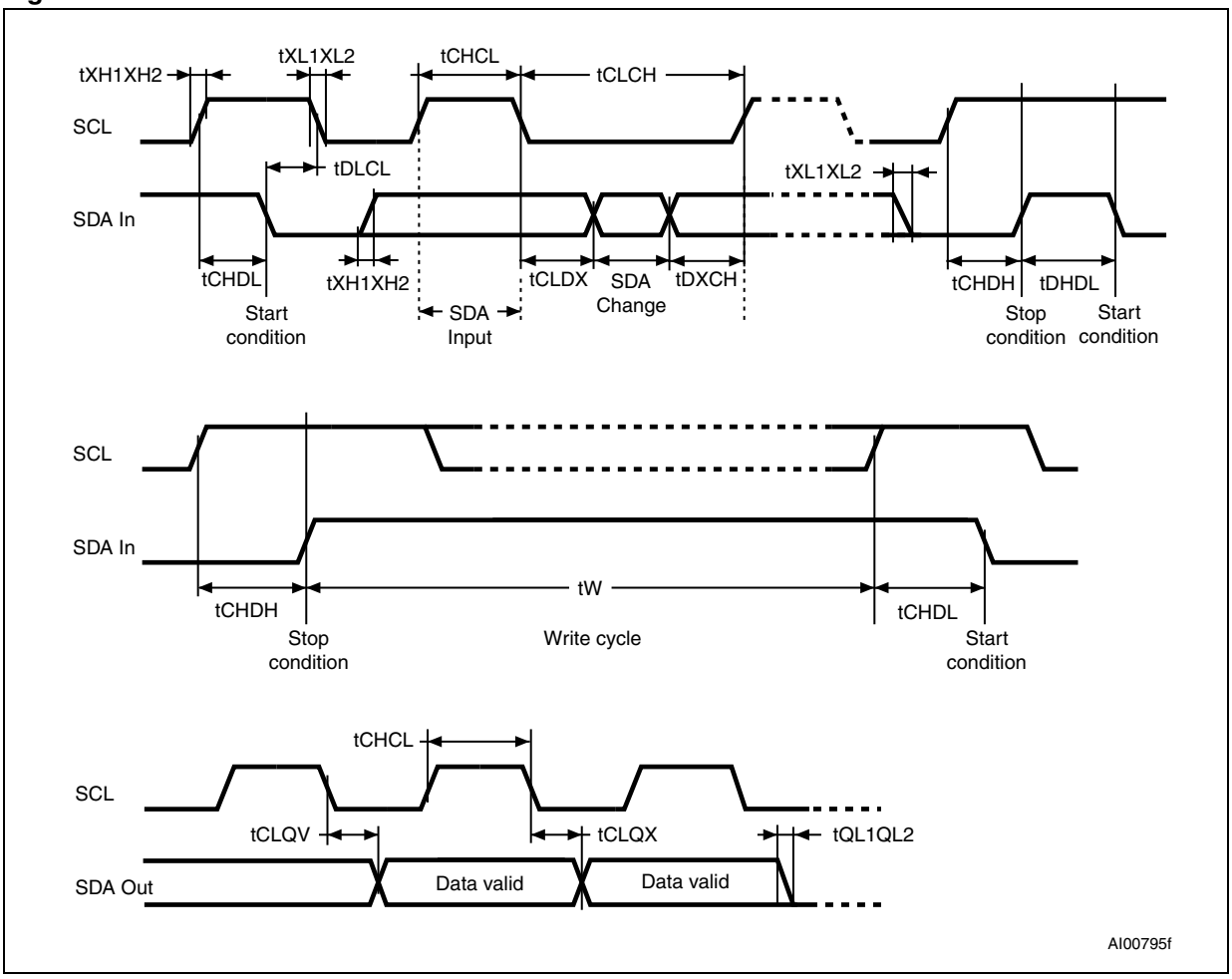
1. All values are referred to $V_{IL}$(max) and $V_{IH}$(min).
2. Characterized only, not tested in production.
3. With $C_L$ = 10 pF.
4. There is no min. or max. values for the input signal rise and fall times. It is however recommended by the I²C specification that the input signal rise and fall times be more than 20 ns and less than 300 ns when $f_C$ < 400 kHz.
5. To avoid spurious Start and Stop conditions, a minimum delay is placed between SCL=1 and the falling or rising edge of SDA.
6. $t_{CLQV}$ is the time (from the falling edge of SCL) required by the SDA bus line to reach either $0.3V_{CC}$ or $0.7V_{CC}$, assuming that $R_{bus} \times C_{bus}$ time constant is within the values specified in *Figure 4*.

**Table 10. AC characteristics at 100 kHz ($I^2C$ Standard mode)(1)**

| Test conditions specified in *Section 6: DC and AC parameters* | | | | | |
|---|---|---|---|---|---|
| **Symbol** | **Alt.** | **Parameter** | **Min.** | **Max.** | **Unit** |
| $f_C$ | $f_{SCL}$ | Clock frequency | - | 100 | kHz |
| $t_{CHCL}$ | $t_{HIGH}$ | Clock pulse width high | 4 | - | µs |
| $t_{CLCH}$ | $t_{LOW}$ | Clock pulse width low | 4.7 | - | µs |
| $t_{XH1XH2}$ | $t_R$ | Input signal rise time | - | 1 | µs |
| $t_{XL1XL2}$ | $t_F$ | Input signal fall time | - | 300 | ns |
| $t_{QL1QL2}$(2) | $t_F$ | SDA fall time | - | 300 | ns |
| $t_{DXCX}$ | $t_{SU:DAT}$ | Data in setup time | 250 | - | ns |
| $t_{CLDX}$ | $t_{HD:DAT}$ | Data in hold time | 0 | - | ns |
| $t_{CLQX}$(3) | $t_{DH}$ | Data out hold time | 200 | - | ns |
| $t_{CLQV}$ | $t_{AA}$ | Clock low to next data valid (access time) | 200 | 3450 | ns |
| $t_{CHDX}$(4) | $t_{SU:STA}$ | Start condition setup time | 4.7 | - | µs |
| $t_{DLCL}$ | $t_{HD:STA}$ | Start condition hold time | 4 | - | µs |
| $t_{CHDH}$ | $t_{SU:STO}$ | Stop condition setup time | 4 | - | µs |
| $t_{DHDL}$ | $t_{BUF}$ | Time between Stop condition and next Start condition | 4.7 | - | µs |
| $t_W$ | $t_{WR}$ | Write time | - | 5 | ms |

1. Values recommended by the $I^2C$ bus Standard-mode specification for a robust design of the $I^2C$ bus application. Note that the M24xxx devices decode correctly faster timings as specified in *Table 9: AC characteristics at 400 kHz (I2C Fast mode)*.
2. Characterized only.
3. To avoid spurious Start and Stop conditions, a minimum delay is placed between SCL=1 and the falling or rising edge of SDA.
4. For a reStart condition, or following a Write cycle.

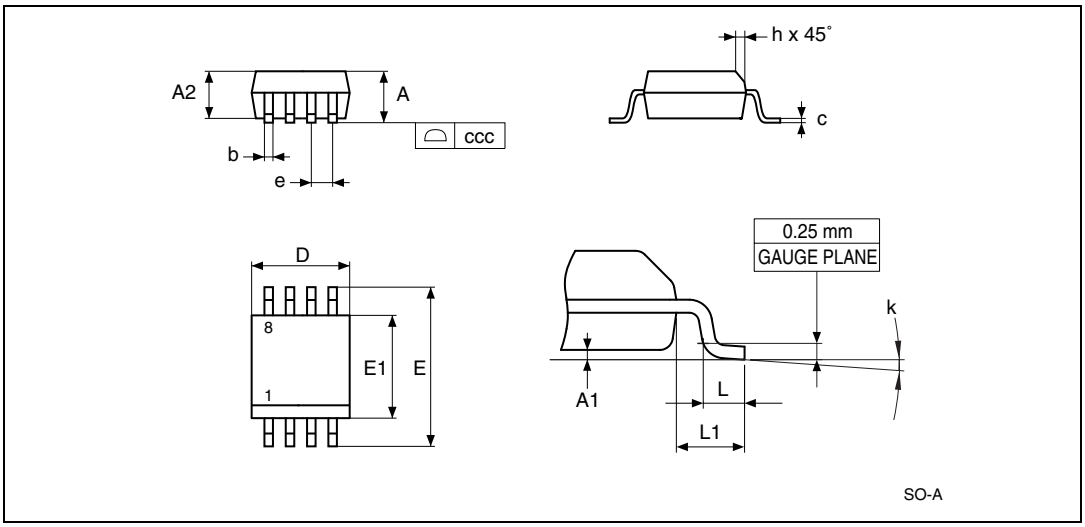
**Figure 11. AC waveforms**



# 7 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

**Figure 12. SO8 narrow – 8 lead plastic small outline, 150 mils body width, package outline**



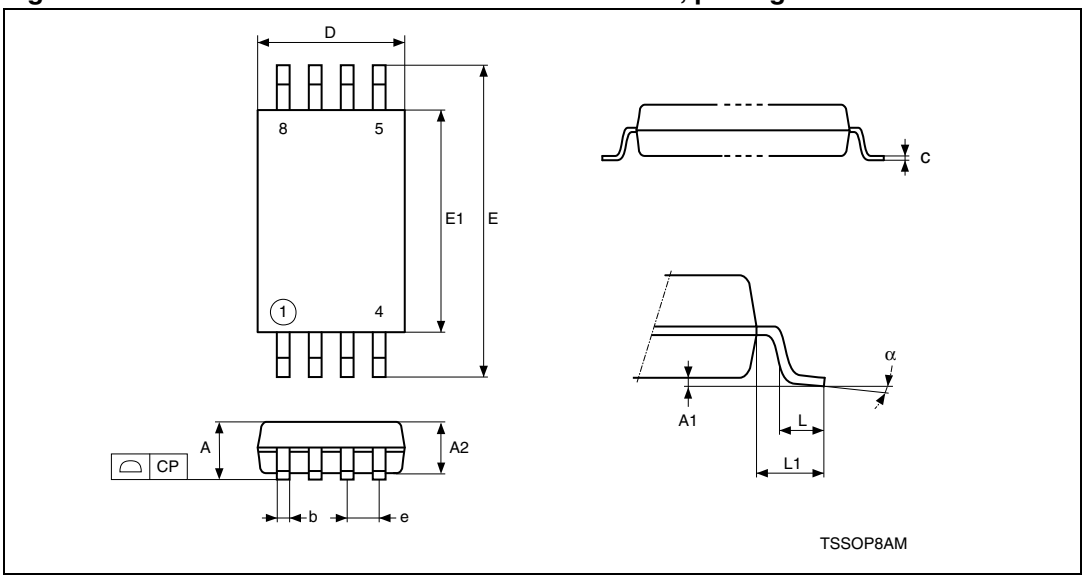

1. Drawing is not to scale.
2. The “1” that appears in the top view of the package shows the position of pin 1 and the “N” indicates the total number of pins.

**Table 11. SO8 narrow – 8 lead plastic small outline, 150 mils body width, package mechanical data**

| Symbol | millimeters | | | inches[1] | | |
|---|---|---|---|---|---|---|
| | Typ | Min | Max | Typ | Min | Max |
| A | - | - | 1.750 | - | - | 0.0689 |
| A1 | - | 0.100 | 0.250 | - | 0.0039 | 0.0098 |
| A2 | - | 1.250 | - | - | 0.0492 | - |
| b | - | 0.280 | 0.480 | - | 0.0110 | 0.0189 |
| c | - | 0.170 | 0.230 | - | 0.0067 | 0.0091 |
| ccc | - | - | 0.100 | - | - | 0.0039 |
| D | 4.900 | 4.800 | 5 | 0.1929 | 0.1890 | 0.1969 |
| E | 6.000 | 5.800 | 6.200 | 0.2362 | 0.2283 | 0.2441 |
| E1 | 3.900 | 3.800 | 4.000 | 0.1535 | 0.1496 | 0.1575 |
| e | 1.270 | - | - | 0.0500 | - | - |
| h | - | 0.250 | 0.500 | - | 0.0098 | 0.0197 |
| k | - | 0° | 8° | - | 0° | 8° |
| L | - | 0.400 | 1.270 | - | 0.0157 | 0.0500 |
| L1 | 1.040 | | | 0.0409 | | |

1. Values in inches are converted from mm and rounded to 4 decimal digits.

**Figure 13. TSSOP8 – 8 lead thin shrink small outline, package outline**




1. Drawing is not to scale.
2. The circle in the top view of the package indicates the position of pin 1.

**Table 12. TSSOP8 – 8 lead thin shrink small outline, package mechanical data**

| Symbol | millimeters | | | inches[1] | | |
|---|---|---|---|---|---|---|
| | Typ. | Min. | Max. | Typ. | Min. | Max. |
| A | - | - | 1.200 | - | - | 0.0472 |
| A1 | - | 0.050 | 0.150 | - | 0.0020 | 0.0059 |
| A2 | 1.000 | 0.800 | 1.050 | 0.0394 | 0.0315 | 0.0413 |
| b | - | 0.190 | 0.300 | - | 0.0075 | 0.0118 |
| c | - | 0.090 | 0.200 | - | 0.0035 | 0.0079 |
| CP | - | - | 0.100 | - | - | 0.0039 |
| D | 3.000 | 2.900 | 3.100 | 0.1181 | 0.1142 | 0.1220 |
| e | 0.650 | - | - | 0.0256 | - | - |
| E | 6.400 | 6.200 | 6.600 | 0.2520 | 0.2441 | 0.2598 |
| E1 | 4.400 | 4.300 | 4.500 | 0.1732 | 0.1693 | 0.1772 |
| L | 0.600 | 0.450 | 0.750 | 0.0236 | 0.0177 | 0.0295 |
| L1 | 1.000 | - | - | 0.0394 | - | - |
| α | - | 0° | 8° | - | 0° | 8° |

1. Values in inches are converted from mm and rounded to 4 decimal digits.

# 8 Part numbering

**Table 13. Ordering information scheme**

Example: M24C16 – W DW 3 T P /S

**Device type**
M24 = $I^2C$ serial access EEPROM

**Device Function**
16 = 16 Kbit (2048 x 8)
08 = 8 Kbit (1024 x 8)
04 = 4 Kbit (512 x 8)
02 = 2 Kbit (256 x 8)

**Operating voltage**
W = $V_{CC}$ = 2.5 V to 5.5 V (400 kHz)

**Package**
MN = SO8 (150 mil width)
DW = TSSOP8 (169 mil width)

**Device grade**
3 = Automotive: device tested with high reliability certified flow over –40 to 125 °C

**Option**
T = Tape and reel packing

**Plating technology**
P = ECOPACK® (RoHS compliant)

**Process**
/S = Manufacturing technology code

For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest ST sales office.

# 9 Revision history

Table 14. Document revision history

| Date | Version | Changes |
|---|---|---|
| 13-Mar-2012 | 1 | Initial release. |

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