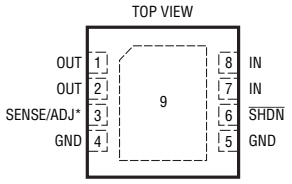
ABSOLUTE MAXIMUM RATINGS (Note 1)

IN Pin Voltage ..... ±22V
OUT Pin Voltage ..... ±22V
Input to Output Differential Voltage (Note 2) ..... ±22V
SENSE Pin Voltage ..... ±22V
ADJ Pin Voltage ..... ±9V
$\overline{\text{SHDN}}$ Pin Voltage ..... ±22V

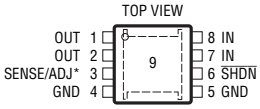
Output Short-Circuit Duration ..... Indefinite
Operating Junction Temperature Range (Notes 3, 5, 13)
E-, I-Grades ..... –40°C to 125°C
H-Grade ..... –40°C to 150°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec)
(Only for MSOP, TO-220, DD-Pak Packages) .... 300°C

PIN CONFIGURATION



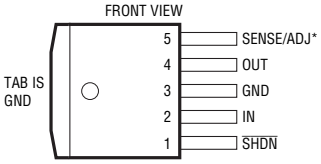
DD PACKAGE
8-LEAD (3mm × 3mm) PLASTIC DFN

T_{JMAX} = 150°C, θ_{JA} = 65°C/W, θ_{JC} = 3°C/W
EXPOSED PAD (PIN 9) IS GND, MUST BE SOLDERED TO PCB
*PIN 3 = SENSE FOR LT1965-1.5/LT1965-1.8/LT1965-2.5/LT1965-3.3
*PIN 3 = ADJ FOR LT1965



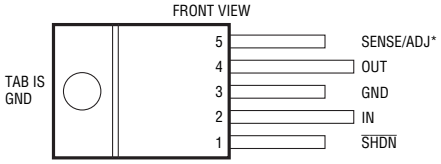
MS8E PACKAGE
8-LEAD PLASTIC MSOP

T_{JMAX} = 125°C, θ_{JA} = 60°C/W, θ_{JC} = 10°C/W
EXPOSED PAD (PIN 9) IS GND, MUST BE SOLDERED TO PCB
*PIN 3 = SENSE FOR LT1965-1.5/LT1965-1.8/LT1965-2.5/LT1965-3.3
*PIN 3 = ADJ FOR LT1965



Q PACKAGE
5-LEAD PLASTIC DD-PAK

T_{JMAX} = 150°C, θ_{JA} = 30°C/W, θ_{JC} = 3°C/W
*PIN 5 = SENSE FOR LT1965-1.5/LT1965-1.8/LT1965-2.5/LT1965-3.3
*PIN 5 = ADJ FOR LT1965



T PACKAGE
5-LEAD PLASTIC TO-220

T_{JMAX} = 150°C, θ_{JA} = 50°C/W, θ_{JC} = 3°C/W
*PIN 5 = SENSE FOR LT1965-1.5/LT1965-1.8/LT1965-2.5/LT1965-3.3
*PIN 5 = ADJ FOR LT1965

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT1965EDD#PBF	LT1965EDD#TRPBF	LCXW	8-Lead (3mm × 3mm) Plastic DFN	–40°C to 125°C
LT1965IDD#PBF	LT1965IDD#TRPBF	LCXW	8-Lead (3mm × 3mm) Plastic DFN	–40°C to 125°C
LT1965EDD-1.5#PBF	LT1965EDD-1.5#TRPBF	LDKW	8-Lead (3mm × 3mm) Plastic DFN	–40°C to 125°C
LT1965IDD-1.5#PBF	LT1965IDD-1.5#TRPBF	LDKW	8-Lead (3mm × 3mm) Plastic DFN	–40°C to 125°C
LT1965EDD-1.8#PBF	LT1965EDD-1.8#TRPBF	LDKY	8-Lead (3mm × 3mm) Plastic DFN	–40°C to 125°C
LT1965IDD-1.8#PBF	LT1965IDD-1.8#TRPBF	LDKY	8-Lead (3mm × 3mm) Plastic DFN	–40°C to 125°C
LT1965EDD-2.5#PBF	LT1965EDD-2.5#TRPBF	LDMB	8-Lead (3mm × 3mm) Plastic DFN	–40°C to 125°C
LT1965IDD-2.5#PBF	LT1965IDD-2.5#TRPBF	LDMB	8-Lead (3mm × 3mm) Plastic DFN	–40°C to 125°C
LT1965EDD-3.3#PBF	LT1965EDD-3.3#TRPBF	LDMD	8-Lead (3mm × 3mm) Plastic DFN	–40°C to 125°C

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LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT1965IDD-3.3#PBF	LT1965IDD-3.3#TRPBF	LDMD	8-Lead (3mm × 3mm) Plastic DFN	–40°C to 125°C
LT1965EMS8E#PBF	LT1965EMS8E#TRPBF	LTCXX	8-Lead Plastic MSOP	–40°C to 125°C
LT1965IMS8E#PBF	LT1965IMS8E#TRPBF	LTCXX	8-Lead Plastic MSOP	–40°C to 125°C
LT1965EMS8E-1.5#PBF	LT1965EMS8E-1.5#TRPBF	LTDKX	8-Lead Plastic MSOP	–40°C to 125°C
LT1965IMS8E-1.5#PBF	LT1965IMS8E-1.5#TRPBF	LTDKX	8-Lead Plastic MSOP	–40°C to 125°C
LT1965EMS8E-1.8#PBF	LT1965EMS8E-1.8#TRPBF	LTDKZ	8-Lead Plastic MSOP	–40°C to 125°C
LT1965IMS8E-1.8#PBF	LT1965IMS8E-1.8#TRPBF	LTDKZ	8-Lead Plastic MSOP	–40°C to 125°C
LT1965EMS8E-2.5#PBF	LT1965EMS8E-2.5#TRPBF	LTDMC	8-Lead Plastic MSOP	–40°C to 125°C
LT1965IMS8E-2.5#PBF	LT1965IMS8E-2.5#TRPBF	LTDMC	8-Lead Plastic MSOP	–40°C to 125°C
LT1965EMS8E-3.3#PBF	LT1965EMS8E-3.3#TRPBF	LTDMF	8-Lead Plastic MSOP	–40°C to 125°C
LT1965IMS8E-3.3#PBF	LT1965IMS8E-3.3#TRPBF	LTDMF	8-Lead Plastic MSOP	–40°C to 125°C
LT1965EQ#PBF	LT1965EQ#TRPBF	LT1965Q	5-Lead Plastic DD-Pak	–40°C to 125°C
LT1965IQ#PBF	LT1965IQ#TRPBF	LT1965Q	5-Lead Plastic DD-Pak	–40°C to 125°C
LT1965HQ#PBF	LT1965HQ#TRPBF	LT1965Q	5-Lead Plastic DD-Pak	–40°C to 150°C
LT1965EQ-1.5#PBF	LT1965EQ-1.5#TRPBF	LT1965Q-1.5	5-Lead Plastic DD-Pak	–40°C to 125°C
LT1965IQ-1.5#PBF	LT1965IQ-1.5#TRPBF	LT1965Q-1.5	5-Lead Plastic DD-Pak	–40°C to 125°C
LT1965EQ-1.8#PBF	LT1965EQ-1.8#TRPBF	LT1965Q-1.8	5-Lead Plastic DD-Pak	–40°C to 125°C
LT1965IQ-1.8#PBF	LT1965IQ-1.8#TRPBF	LT1965Q-1.8	5-Lead Plastic DD-Pak	–40°C to 125°C
LT1965EQ-2.5#PBF	LT1965EQ-2.5#TRPBF	LT1965Q-2.5	5-Lead Plastic DD-Pak	–40°C to 125°C
LT1965IQ-2.5#PBF	LT1965IQ-2.5#TRPBF	LT1965Q-2.5	5-Lead Plastic DD-Pak	–40°C to 125°C
LT1965EQ-3.3#PBF	LT1965EQ-3.3#TRPBF	LT1965Q-3.3	5-Lead Plastic DD-Pak	–40°C to 125°C
LT1965IQ-3.3#PBF	LT1965IQ-3.3#TRPBF	LT1965Q-3.3	5-Lead Plastic DD-Pak	–40°C to 125°C
LT1965ET#PBF	N/A	LT1965T	5-Lead Plastic TO-220	–40°C to 125°C
LT1965IT#PBF	N/A	LT1965T	5-Lead Plastic TO-220	–40°C to 125°C
LT1965HT#PBF	N/A	LT1965T	5-Lead Plastic TO-220	–40°C to 150°C
LT1965ET-1.5#PBF	N/A	LT1965T-1.5	5-Lead Plastic TO-220	–40°C to 125°C
LT1965IT-1.5#PBF	N/A	LT1965T-1.5	5-Lead Plastic TO-220	–40°C to 125°C
LT1965ET-1.8#PBF	N/A	LT1965T-1.8	5-Lead Plastic TO-220	–40°C to 125°C
LT1965IT-1.8#PBF	N/A	LT1965T-1.8	5-Lead Plastic TO-220	–40°C to 125°C
LT1965ET-2.5#PBF	N/A	LT1965T-2.5	5-Lead Plastic TO-220	–40°C to 125°C
LT1965IT-2.5#PBF	N/A	LT1965T-2.5	5-Lead Plastic TO-220	–40°C to 125°C
LT1965ET-3.3#PBF	N/A	LT1965T-3.3	5-Lead Plastic TO-220	–40°C to 125°C
LT1965IT-3.3#PBF	N/A	LT1965T-3.3	5-Lead Plastic TO-220	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *Temperature grades are identified by a label on the shipping container.
Consult LTC Marketing for information on nonstandard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

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ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 3)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Minimum Input Voltage (Notes 4, 12)	I_{LOAD} = 0.5A			1.65		V
	I_{LOAD} = 1.1A (T_J < 125°C)	●		1.8	2.3	V
	I_{LOAD} = 1A (H-Grade, T_J > 125°C)				2.3	V
Regulated Output Voltage (Note 5)	LT1965-1.5, V_{IN} = 2.1V, I_{LOAD} = 1mA		1.477	1.5	1.523	V
	LT1965-1.5, 2.5 < V_{IN} < 20V, 1mA < I_{LOAD} < 1.1A	●	1.455	1.5	1.545	V
	LT1965-1.8, V_{IN} = 2.3V, I_{LOAD} = 1mA		1.773	1.8	1.827	V
	LT1965-1.8, 2.8 < V_{IN} < 20V, 1mA < I_{LOAD} < 1.1A	●	1.746	1.8	1.854	V
	LT1965-2.5, V_{IN} = 3V, I_{LOAD} = 1mA		2.462	2.5	2.538	V
	LT1965-2.5, 3.5 < V_{IN} < 20V, 1mA < I_{LOAD} < 1.1A	●	2.425	2.5	2.575	V
	LT1965-3.3, V_{IN} = 3.8V, I_{LOAD} = 1mA		3.25	3.3	3.35	V
	LT1965-3.3, 4.3 < V_{IN} < 20V, 1mA < I_{LOAD} < 1.1A	●	3.201	3.3	3.399	V
ADJ Pin Voltage (Notes 4, 5)	V_{IN} = 2.1V, I_{LOAD} = 1mA		1.182	1.2	1.218	V
	2.3V < V_{IN} < 20V, 1mA < I_{LOAD} < 1.1A (T_J < 125°C)	●	1.164	1.2	1.236	V
	2.3V < V_{IN} < 20V, 1mA < I_{LOAD} < 1A (H-Grade, T_J > 125°C)		1.158		1.236	V
Line Regulation	LT1965-1.5, ΔV_{IN} = 2.1V to 20V, I_{LOAD} = 1mA	●		3.5	9	mV
	LT1965-1.8, ΔV_{IN} = 2.3V to 20V, I_{LOAD} = 1mA	●		4	10	mV
	LT1965-2.5, ΔV_{IN} = 3V to 20V, I_{LOAD} = 1mA	●		4.5	11.5	mV
	LT1965-3.3, ΔV_{IN} = 3.8V to 20V, I_{LOAD} = 1mA	●		5.5	16	mV
	LT1965, ΔV_{IN} = 2.1V to 20V, I_{LOAD} = 1mA (E-, I-Grades) (Note 4)	●		3	8	mV
	LT1965, ΔV_{IN} = 2.1V to 20V, I_{LOAD} = 1mA (H-Grade) (Note 4)	●		3	12	mV
Load Regulation	LT1965-1.5, V_{IN} = 2.5V, ΔI_{LOAD} = 1mA to 1.1A			5.25	10	mV
	LT1965-1.5, V_{IN} = 2.5V, ΔI_{LOAD} = 1mA to 1.1A	●			20	mV
	LT1965-1.8, V_{IN} = 2.8V, ΔI_{LOAD} = 1mA to 1.1A			6.25	12	mV
	LT1965-1.8, V_{IN} = 2.8V, ΔI_{LOAD} = 1mA to 1.1A	●			24	mV
	LT1965-2.5, V_{IN} = 3.5V, ΔI_{LOAD} = 1mA to 1.1A			8.75	16.5	mV
	LT1965-2.5, V_{IN} = 3.5V, ΔI_{LOAD} = 1mA to 1.1A	●			33	mV
	LT1965-3.3, V_{IN} = 4.3V, ΔI_{LOAD} = 1mA to 1.1A			11.5	22	mV
	LT1965-3.3, V_{IN} = 4.3V, ΔI_{LOAD} = 1mA to 1.1A	●			44	mV
	LT1965, V_{IN} = 2.3V, ΔI_{LOAD} = 1mA to 1.1A (Note 4)			4.25	8	mV
	LT1965, V_{IN} = 2.3V, ΔI_{LOAD} = 1mA to 1.1A (T_J < 125°C)	●			16	mV
	LT1965, V_{IN} = 2.3V, ΔI_{LOAD} = 1mA to 1A (H-Grade, T_J > 125°C)				22	mV
Dropout Voltage V_{IN} = $V_{OUT(NOMINAL)}$ (Notes 6, 7, 12)	I_{LOAD} = 1mA			0.055	0.08	V
	I_{LOAD} = 1mA	●			0.14	V
	I_{LOAD} = 100mA			0.12	0.175	V
	I_{LOAD} = 100mA	●			0.28	V
	I_{LOAD} = 500mA			0.21	0.25	V
	I_{LOAD} = 500mA	●			0.36	V
	I_{LOAD} = 1.1A			0.31	0.36	V
	I_{LOAD} = 1.1A (T_J < 125°C)	●			0.49	V
	I_{LOAD} = 1A (H-Grade, T_J > 125°C)				0.49	V
GND Pin Current V_{IN} = $V_{OUT(NOMINAL)}$ + 1V (Notes 6, 8)	I_{LOAD} = 0mA	●		0.5	1.1	mA
	I_{LOAD} = 1mA	●		0.6	1.5	mA
	I_{LOAD} = 100mA	●		2.2	5.5	mA
	I_{LOAD} = 500mA	●		8.2	20	mA
	I_{LOAD} = 1.1A (T_J < 125°C)	●		21	40	mA
	I_{LOAD} = 1A (H-Grade, T_J > 125°C)				40	mA
Output Voltage Noise	C_{OUT} = 10µF, I_{LOAD} = 1.1A, BW = 10Hz to 100kHz			40		μV_{RMS}
ADJ Pin Bias Current (Notes 4, 9)				1.3	4.5	µA
Shutdown Threshold	V_{OUT} = Off to On	●		0.85	2	V
	V_{OUT} = On to Off	●	0.2	0.45		V

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ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 3)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$\overline{SHDN}$ Pin Current (Note 10)	$V_{\overline{SHDN}}$ = 0V $V_{\overline{SHDN}}$ = 20V			0.01 5.5	1 10	µA µA
Quiescent Current in Shutdown	V_{IN} = 6V, $V_{\overline{SHDN}}$ = 0V			0.01	1	µA
Ripple Rejection	$V_{IN} – V_{OUT}$ = 1.5V (AVG), V_{RIPPLE} = 0.5V_{P-P}, f_{RIPPLE} = 120Hz, I_{LOAD} = 0.75A		57	75		dB
Current Limit	V_{IN} = 7V, V_{OUT} = 0 $V_{IN} = V_{OUT(NOMINAL)}$ + 1V, ΔV_{OUT} = –0.1V (T_J < 125°C) (Note 6) $V_{IN} = V_{OUT(NOMINAL)}$ + 1V, ΔV_{OUT} = –0.1V, (H-Grade, T_J > 125°C) (Note 6)	 ● 	 1.2 1.1	2.4		A A A
Input Reverse-Leakage Current	V_{IN} = –20V, V_{OUT} = 0				1	mA
Reverse-Output Current (Note 11)	LT1965-1.5, V_{OUT} = 1.5V, V_{IN} = 0 LT1965-1.8, V_{OUT} = 1.8V, V_{IN} = 0 LT1965-2.5, V_{OUT} = 2.5V, V_{IN} = 0 LT1965-3.3, V_{OUT} = 3.3V, V_{IN} = 0 LT1965 (Note 4), V_{OUT} = 1.2V, V_{IN} = 0			275 275 275 275 175	525 525 525 525 400	µA µA µA µA µA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: Absolute maximum input to output differential voltage is not achievable with all combinations of rated IN pin and OUT pin voltages. With the IN pin at 22V, the OUT pin may not be pulled below 0V. The total measured voltage from IN to OUT must not exceed ±22V.

Note 3: The LT1965 regulators are tested and specified under pulse load conditions such that $T_J \cong T_A$. The LT1965E regulators are 100% tested at T_A = 25°C and performance is guaranteed from 0°C to 125°C. Performance of the LT1965E over the full –40°C to 125°C operating junction temperature range is assured by design, characterization and correlation with statistical process controls. The LT1965I regulators are guaranteed over the full –40°C to 125°C operating junction temperature range. The LT1965H is tested at 150°C operating junction temperature. High junction temperatures degrade operating lifetimes. Operating lifetime is derated at junction temperatures greater than 125°C.

Note 4: The LT1965 adjustable version is tested and specified for these conditions with the ADJ connected to the OUT pin.

Note 5: Maximum junction temperature limits operating conditions. The regulated output voltage specification does not apply for all possible combinations of input voltage and output current. Limit the output current range if operating at the maximum input voltage. Limit the input-to-output voltage differential if operating at the maximum output current.

Note 6: To satisfy minimum input voltage requirements, the LT1965 adjustable version is tested and specified for these conditions with an external resistor divider (bottom 4.02k, top 4.32k) for an output voltage of 2.5V. The external resistor divider adds 300µA of output DC load current. This external current is not factored into GND pin current.

Note 7: Dropout voltage is the minimum input-to-output voltage differential needed to maintain regulation at a specified output current. In dropout, the output voltage equals: ($V_{IN} – V_{DROPOUT}$)

Note 8: GND pin current is tested with $V_{IN} = V_{OUT(NOMINAL)}$ + 1V and a current source load. GND pin current increases slightly in dropout. For the fixed output versions, an internal resistor divider will typically add 100µA to the GND pin current. See GND pin current curves in the Typical Performance Characteristics section.

Note 9: ADJ pin bias current flows into the ADJ pin.

Note 10: $\overline{SHDN}$ pin current flows into the $\overline{SHDN}$ pin.

Note 11: Reverse-output current is tested with the IN pin grounded and the OUT pin forced to the rated output voltage. This current flows into the OUT pin and out of the GND pin.

Note 12: For the LT1965, LT1965-1.5 and LT1965-1.8, the minimum input voltage specification limits the dropout voltage under some output voltage/load conditions.

Note 13: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 125°C (LT1965E, LT1965I) or 150°C (LT1965H) when overtemperature is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

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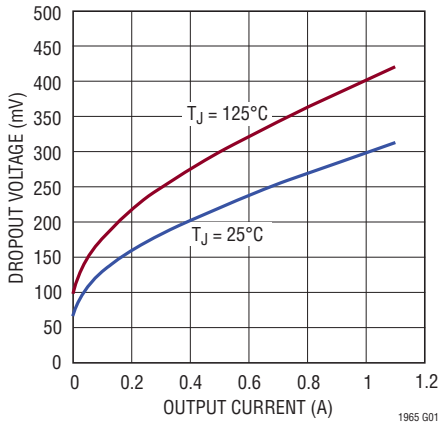
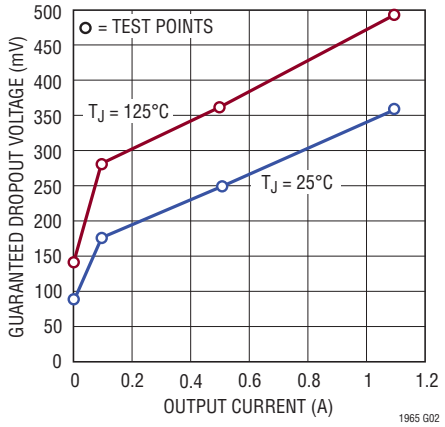
TYPICAL PERFORMANCE CHARACTERISTICS

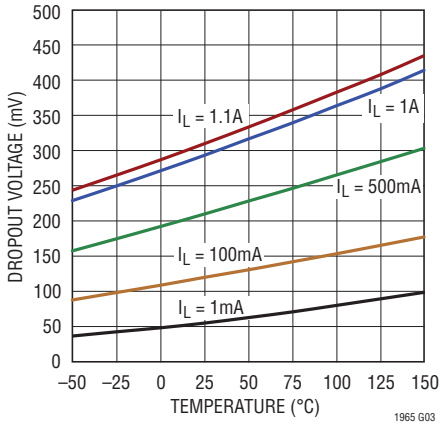
Typical Dropout Voltage



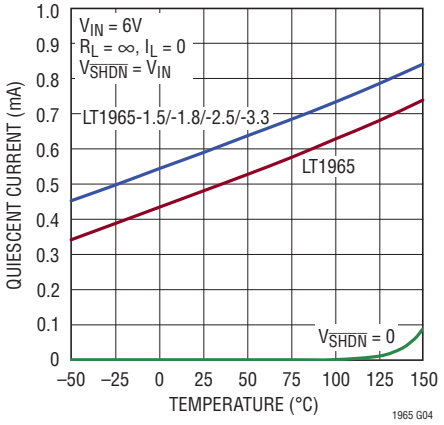
Guaranteed Dropout Voltage



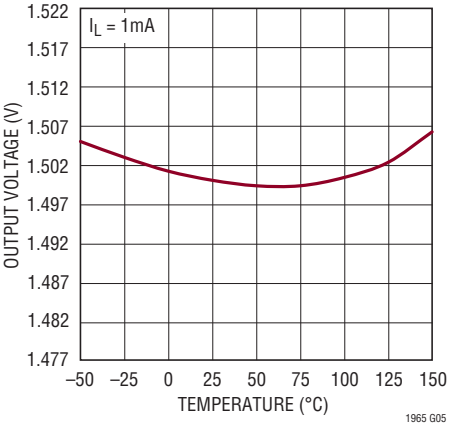
Dropout Voltage



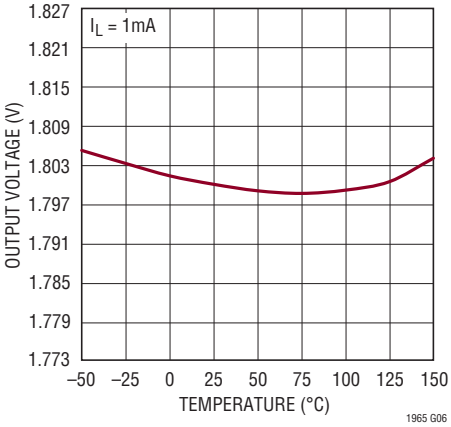
Quiescent Current



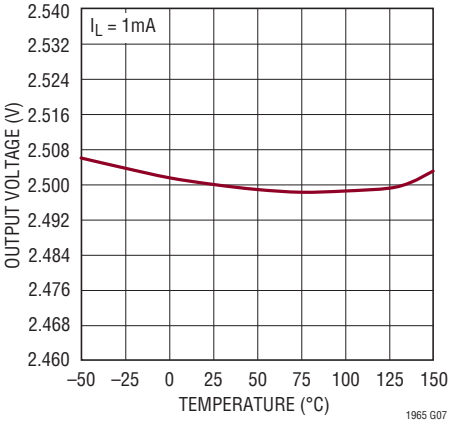
LT1965-1.5 Output Voltage



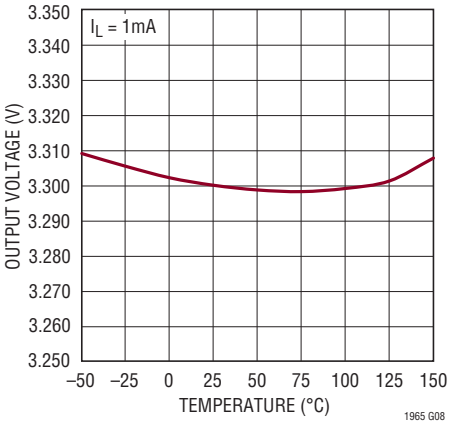
LT1965-1.8 Output Voltage



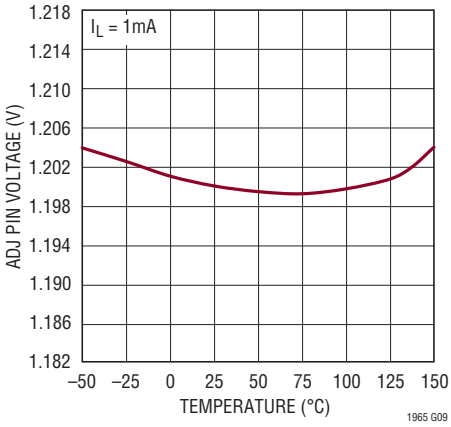
LT1965-2.5 Output Voltage



LT1965-3.3 Output Voltage



LT1965 ADJ Pin Voltage



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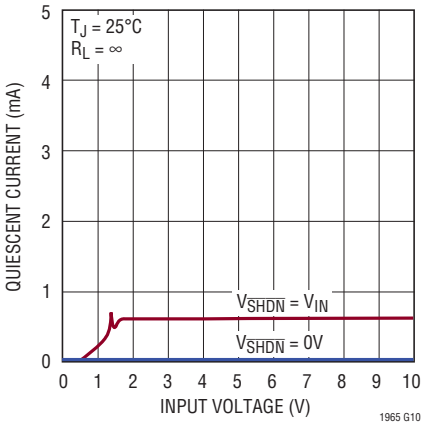
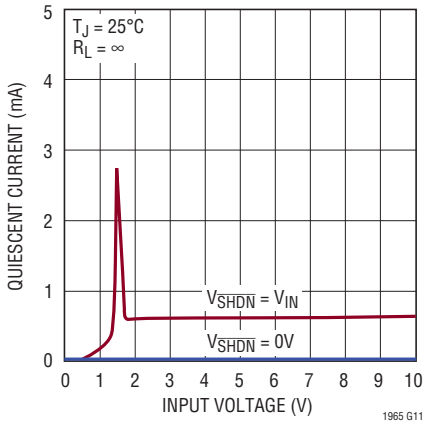
TYPICAL PERFORMANCE CHARACTERISTICS

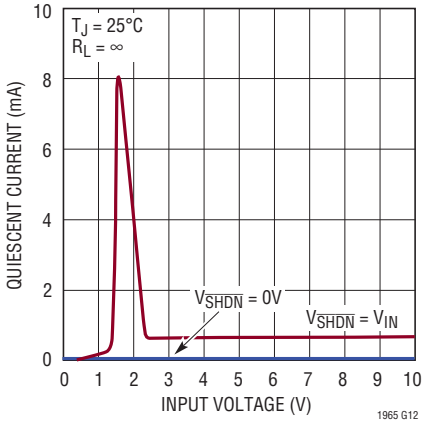
LT1965-1.5 Quiescent Current



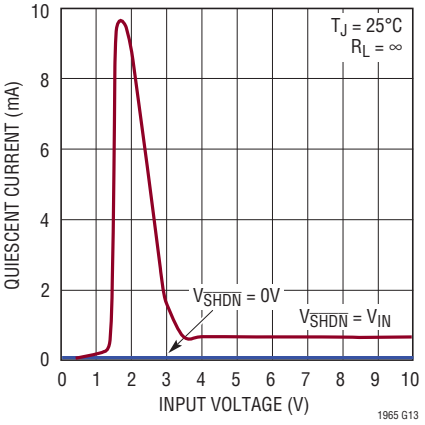
LT1965-1.8 Quiescent Current



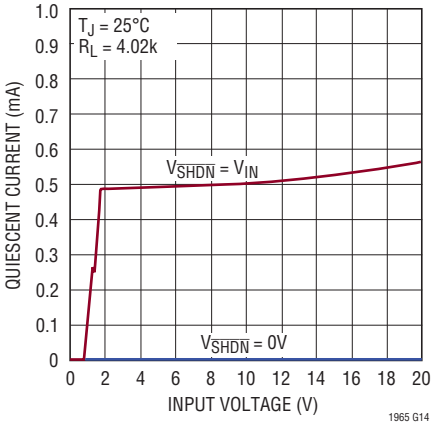
LT1965-2.5 Quiescent Current



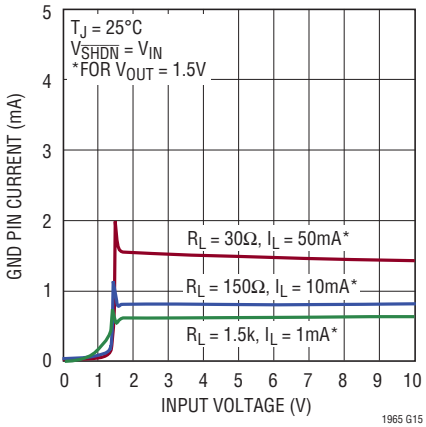
LT1965-3.3 Quiescent Current



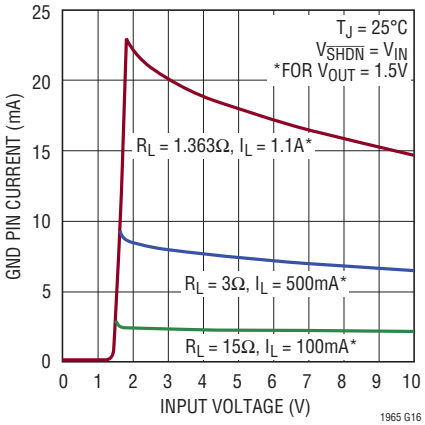
LT1965 Quiescent Current



LT1965-1.5 GND Pin Current (Light Load)



LT1965-1.5 GND Pin Current (Heavy Load)



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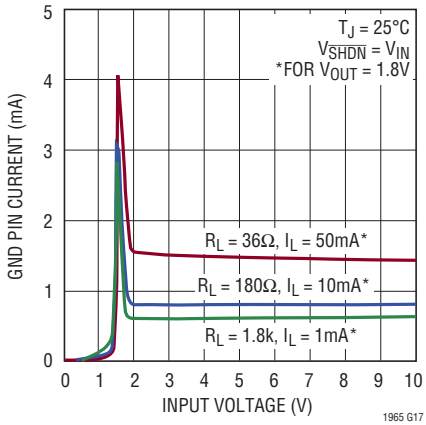
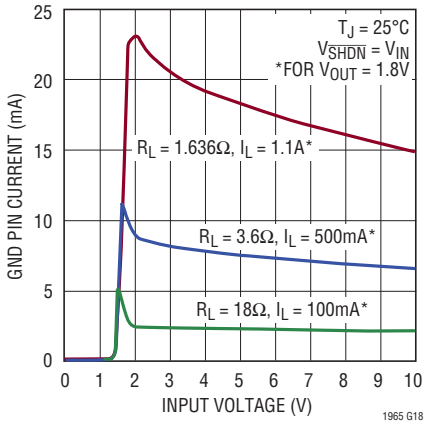


LT1965-1.8 GND Pin Current (Heavy Load)



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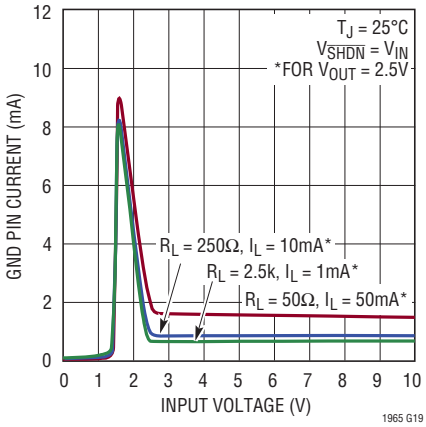
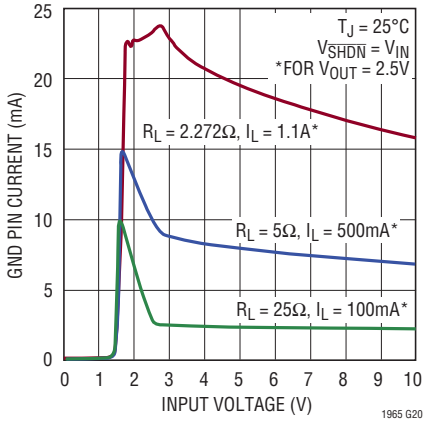
TYPICAL PERFORMANCE CHARACTERISTICS

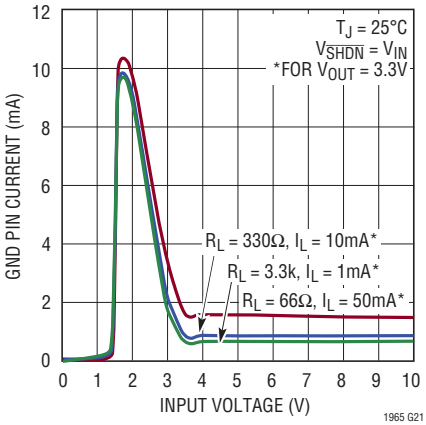
LT1965-2.5 GND Pin Current (Light Load)



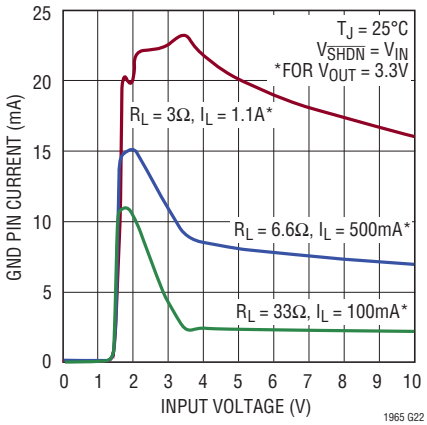
LT1965-2.5 GND Pin Current (Heavy Load)



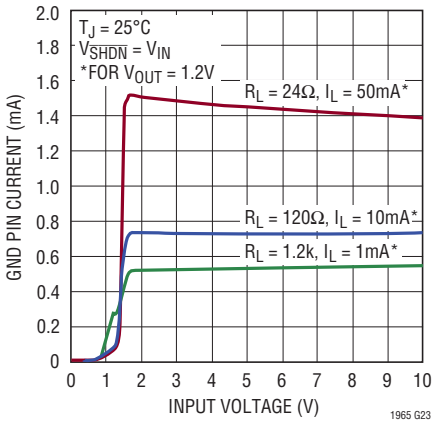
LT1965-3.3 GND Pin Current (Light Load)



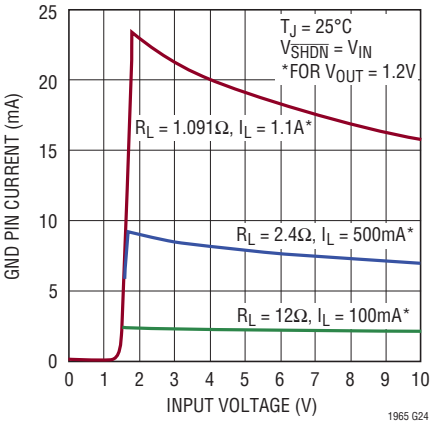
LT1965-3.3 GND Pin Current (Heavy Load)



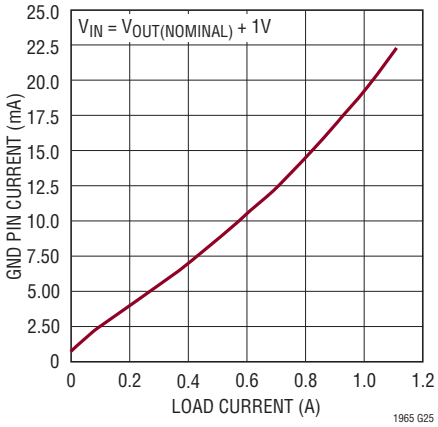
LT1965 GND Pin Current (Light Load)



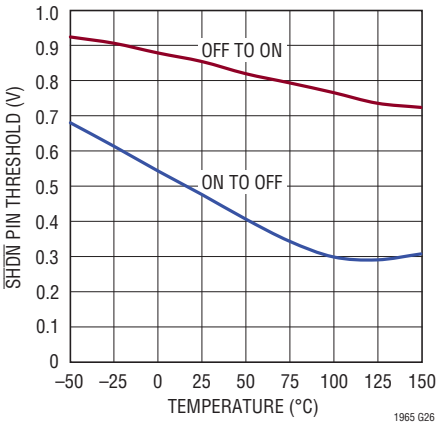
LT1965 GND Pin Current (Heavy Load)



GND Pin Current vs I_{LOAD}



$\overline{SHDN}$ Pin Threshold



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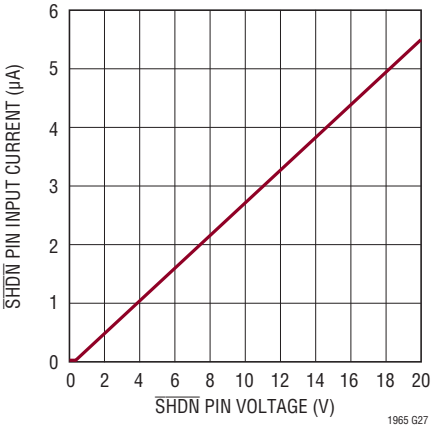
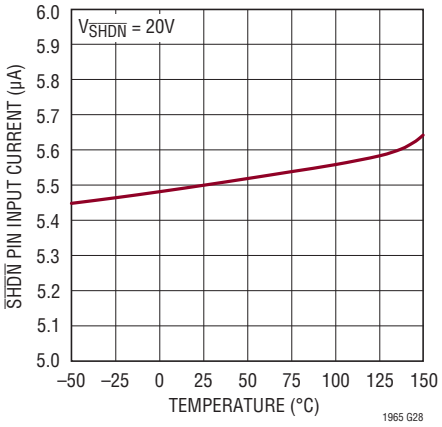
TYPICAL PERFORMANCE CHARACTERISTICS

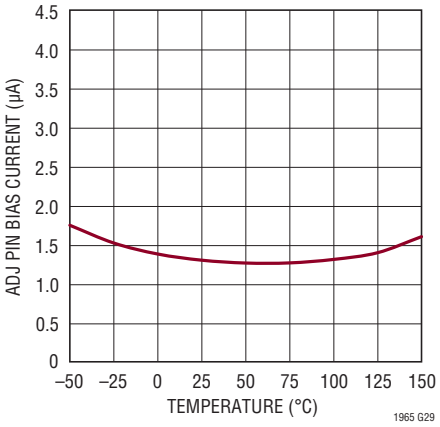
$\overline{SHDN}$ Pin Input Current



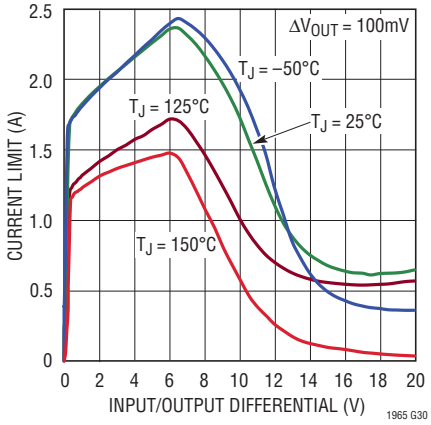
$\overline{SHDN}$ Pin Input Current



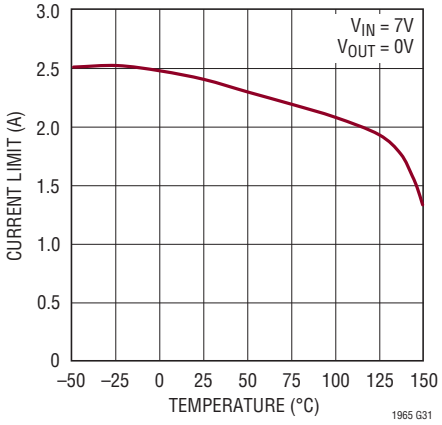
ADJ Pin Bias Current



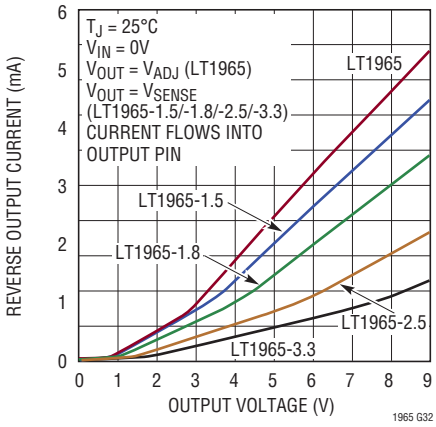
Current Limit vs $V_{IN} - V_{OUT}$



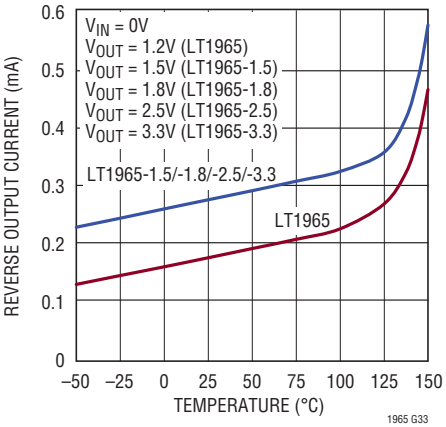
Current Limit vs Temperature



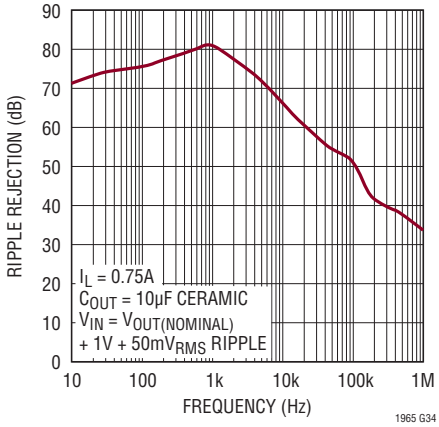
Reverse-Output Current



Reverse-Output Current



Ripple Rejection vs Frequency



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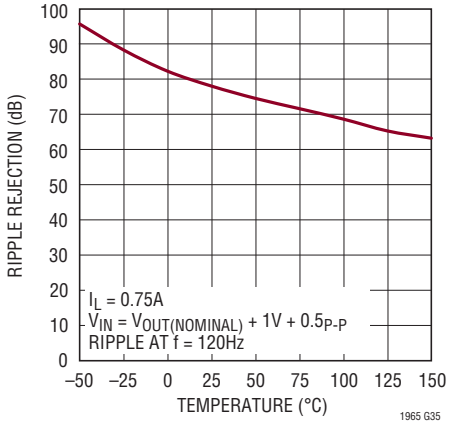
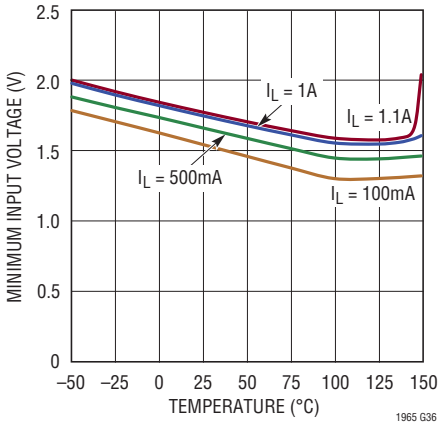
TYPICAL PERFORMANCE CHARACTERISTICS

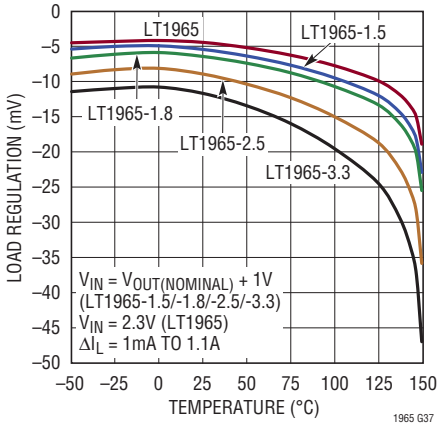
Ripple Rejection vs Temperature



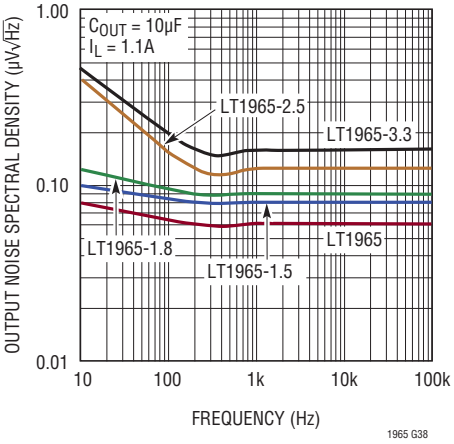
LT1965 Minimum Input Voltage



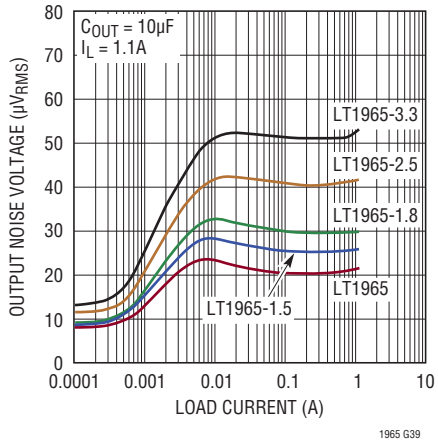
Load Regulation



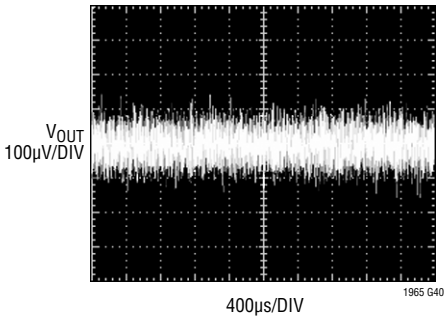
Output Noise Spectral Density



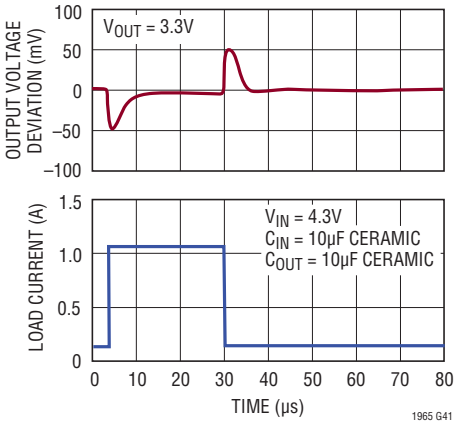
RMS Output Noise vs Load Current (10Hz to 100kHz)



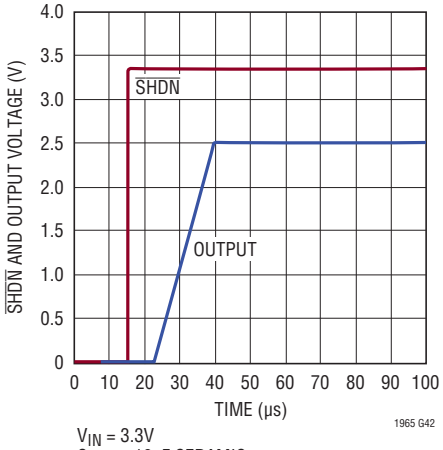
LT1965-1.8 10Hz to 100kHz Output Noise



LT1965-3.3 Transient Response



LT1965-2.5 $\overline{SHDN}$ Transient Response



V_{IN} = 3.3V
C_{OUT} = 10μF CERAMIC
R_L = 2.5k, I_L = 1mA FOR V_{OUT} = 2.5V

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PIN FUNCTIONS (DFN/MSOP/DD-Pak/TO-220)

OUT (Pins 1, 2 / 1, 2 / 4 / 4): Output. This pin supplies power to the load. Use a minimum output capacitor of 10µF to prevent oscillations. Large load transient applications require larger output capacitors to limit peak voltage transients. See the Applications Information section for more information on output capacitance and reverse-output characteristics.

SENSE (Pin 3 / 3 / 5 / 5): Sense. For fixed voltage versions of the LT1965 (LT1965-1.5/LT1965-1.8/ LT1965-2.5/ LT1965-3.3), the SENSE pin is the input to the error amplifier. Optimum regulation is obtained when the SENSE pin is connected to the OUT pin of the regulator. In critical applications, small voltage drops are caused by the resistance (R_P) of PCB traces between the regulator and the load. These drops may be eliminated by connecting the SENSE pin to the output at the load as shown in Figure 1 (Kelvin Sense Connection). Note that the voltage drop across the external PCB traces will add to the dropout voltage of the regulator. The SENSE pin bias current is 100µA at the nominal rated output voltage.

ADJ (Pin 3 / 3 / 5 / 5): Adjust. This pin is the input to the error amplifier. It has a typical bias current of 1.3µA that flows into the pin. The ADJ pin voltage is 1.20V referenced to ground.

GND (Pins 4, 5 / 4, 5 / 3 / 3): Ground. For the adjustable LT1965, connect the bottom of the resistor divider, setting output voltage, directly to GND for optimum regulation.

$\overline{\text{SHDN}}$ (Pin 6 / 6 / 1 / 1): Shutdown. Pulling the $\overline{\text{SHDN}}$ pin low puts the LT1965 into a low power state and turns the output off. Drive the $\overline{\text{SHDN}}$ pin with either logic or an open collector/drain with a pull-up resistor. The resistor supplies the pull-up current to the open collector/drain logic, normally several microamperes and the $\overline{\text{SHDN}}$ pin current, typically less than 5.5µA. If unused, connect the $\overline{\text{SHDN}}$ pin to V_{IN}. The $\overline{\text{SHDN}}$ pin cannot be driven below GND unless it is tied to the IN pin. If the $\overline{\text{SHDN}}$ pin is driven below GND while IN is powered, the output will turn on. $\overline{\text{SHDN}}$ pin logic cannot be referenced to a negative supply rail.

IN (Pins 7, 8 / 7, 8 / 2 / 2): Input. This pin supplies power to the device. The LT1965 requires a bypass capacitor at IN if located more than six inches from the main input filter capacitor. Include a bypass capacitor in battery-powered circuits as a battery's output impedance generally rises with frequency. A bypass capacitor in the range of 1µF to 10µF suffices. The LT1965's design withstands reverse voltages on the IN pin with respect to ground and the OUT pin. In the case of a reversed input, which occurs if a battery is plugged in backwards, the LT1965 behaves as if a diode is in series with its input. No reverse current flows into the LT1965 and no reverse voltage appears at the load. The device protects itself and the load.

Exposed Pad (Pin 9 / 9, DFN and MSOP Packages Only): Ground. Tie this pin directly to Pins 4 and 5 and the PCB ground. This pin provides enhanced thermal performance with its connection to the PCB ground. See the Applications Information section for thermal considerations and calculating junction temperature.

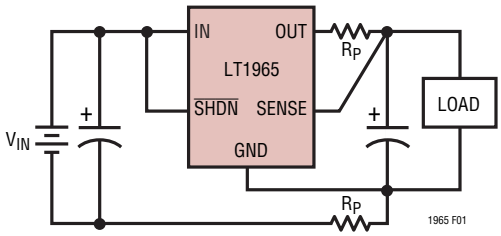

Figure 1. Kelvin Sense Connection

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APPLICATIONS INFORMATION

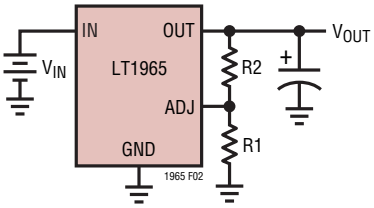
The LT1965 series are 1.1A low dropout regulators with shutdown. The devices are capable of supplying 1.1A at a typical dropout voltage of 310mV. The low operating quiescent current (500µA for the adjustable version, 600µA for the fixed voltage versions) drops to less than 1µA in shutdown. In addition to the low quiescent current, the LT1965 regulators incorporate several protection features that makes them ideal for use in battery-powered systems. The devices protect themselves against both reverse-input and reverse-output voltages. In battery backup applications, if a backup battery holds up the output when the input is pulled to ground, the LT1965 performs like it has a diode in series with its output, preventing reverse-current flow.

Adjustable Operation

The LT1965 adjustable version has an output voltage range of 1.20V to 19.5V. Figure 2 illustrates that the ratio of two external resistors sets the output voltage. The device servos the output to maintain the ADJ pin voltage at 1.20V referenced to ground. R1's current equals 1.20V/R1. R2's current equals R1's current plus the ADJ pin bias current. The ADJ pin bias current, 1.3µA at 25°C, flows through R2 into the ADJ pin. Use the formula in Figure 2 to calculate output voltage. Linear Technology recommends that R1's value be less than 12.1k to minimize output voltage errors due to the ADJ pin bias current. In shutdown, the output turns off and the divider current is zero. For curves depicting ADJ Pin Voltage vs Temperature and ADJ Pin Bias Current vs Temperature, see the Typical Performance Characteristics section.

The adjustable device is tested and specified with the ADJ pin tied to the OUT pin for an output voltage of 1.20V. Specifications for output voltages greater than 1.20V are proportional to the ratio of the desired output voltage to 1.20V: V_{OUT}/1.20V. For example, load regulation for an output current change of 1mA to 1.1A is typically –4.25mV at V_{OUT} = 1.20V. At V_{OUT} = 5V, load regulation is:

$$\frac{5V}{1.20V} \bullet -4.25mV = -17.71mV$$



$$V_{OUT} = 1.20V\left(1+\frac{R2}{R1}\right)+I_{ADJ} \bullet R2$$

$V_{ADJ} = 1.20V$

$I_{ADJ} = 1.3\mu A$ AT 25°C

OUTPUT RANGE = 1.20V TO 19.5V

Figure 2. Adjustable Operation

Output Capacitance

The LT1965's design is stable with a wide range of output capacitors. The ESR of the output capacitor affects stability, most notably with small capacitors. A minimum output capacitor of 10µF with an ESR of 0.3Ω or less is recommended to prevent oscillations. The LT1965 is a low quiescent current device and output load transient response is a function of output capacitance. Larger values of output capacitance decrease the peak deviations and provide improved transient response for larger current changes.

Ceramic capacitors require extra consideration. Manufacturers make ceramic capacitors with a variety of dielectrics, each with different behavior across temperature and applied voltage. The most common dielectrics used are specified with EIA temperature characteristic codes of Z5U, Y5V, X5R and X7R. The Z5U and Y5V dielectrics provide high C-V products in a small package at low cost, but exhibit strong voltage and temperature coefficients as shown in Figures 3 and 4. When used with a 5V regulator, a 16V 10µF Y5V capacitor can exhibit an effective value as low as 1µF to 2µF for the DC bias applied and over the operating temperature range. The X5R and X7R dielectrics yield much more stable characteristics and are more suitable for use as the output capacitor. The X7R type works over a wider temperature range and has better temperature stability whereas X5R is less expensive and is available in higher values. Care still must be exercised when using X5R and X7R capacitors; the X5R and X7R codes only specify operating temperature range and maximum capacitance change over temperature. Capacitance change due to DC bias with X5R and X7R capacitors is better than Y5V and Z5U capacitors, but can still be significant enough to drop capacitor values below appropriate levels. Capacitor DC bias characteristics tend to improve as component case size increases, but expected capacitance at operating voltages should be verified.

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APPLICATIONS INFORMATION

Voltage and temperature coefficients are not the only sources of problems. Some ceramic capacitors have a piezoelectric response. A piezoelectric device generates voltage across its terminals due to mechanical stress, similar to the way a piezoelectric accelerometer or microphone works. For a ceramic capacitor, the stress can be induced by vibrations in the system or thermal transients. The resulting voltages produced can cause appreciable amounts of noise. A ceramic capacitor produced the trace in Figure 5 in response to light tapping from a pencil. Similar vibration induced behavior can masquerade as increased output voltage noise.

Overload Recovery

Like many IC power regulators, the LT1965 has safe operating area protection. The safe area protection decreases current limit as input-to-output voltage increases and keeps the power transistor inside a safe operating region for all values of input-to-output voltage. The protective design provides some output current at all values of input-to-output voltage up to the device breakdown.

When power is first applied, as input voltage rises, the output follows the input, allowing the regulator to start up into very heavy loads. During start-up, as the input voltage

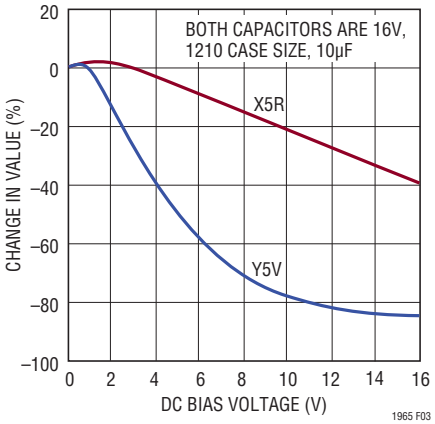

Figure 3. Ceramic Capacitor DC Bias Characteristics

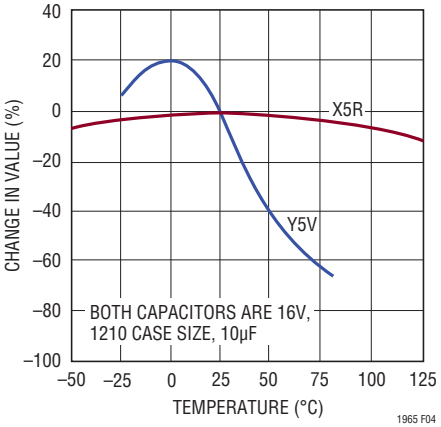

Figure 4. Ceramic Capacitor Temperature Characteristics

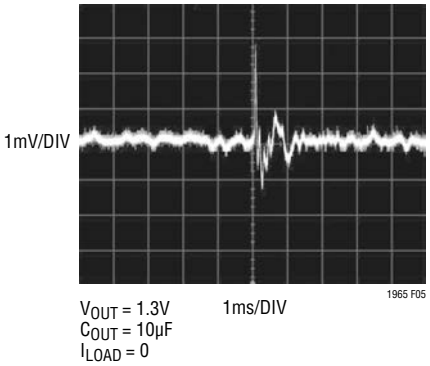

Figure 5. Noise Resulting from Tapping on a Ceramic Capacitor

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APPLICATIONS INFORMATION

is rising, the input-to-output voltage differential is small, allowing the regulator to supply large output currents. With a high input voltage, a problem can occur wherein removal of an output short will not allow the output to recover. Other regulators, such as the LT1083/LT1084/LT1085 family, also exhibit this phenomenon, so it is not unique to the LT1965.

The problem occurs with a heavy output load when the input voltage is high and the output voltage is low. Common situations occur immediately after the removal of a short-circuit or if the shutdown pin is pulled high after the input voltage has already been turned on. The load line for such a load may intersect the output current curve at two points. If this happens, there are two stable output operating points for the regulator. With this double intersection, the input power supply may need to be cycled down to zero and brought up again to make the output recover.

Output Voltage Noise

The LT1965 regulators are designed to provide low output voltage noise over the 10Hz to 100kHz bandwidth while operating at full load. Output voltage noise is approximately $80nV/\sqrt{Hz}$ over this frequency bandwidth for the LT1965 adjustable version. For higher output voltages (generated by using a resistor divider), the output voltage noise gains up accordingly.

Higher values of output voltage noise may be measured if care is not exercised with regard to circuit layout and testing. Crosstalk from nearby traces can induce unwanted noise onto the LT1965's output. Power supply ripple rejection must also be considered; the LT1965 regulators do not have unlimited power supply rejection and will pass a small portion of the input noise through to the output.

Thermal Considerations

The LT1965's maximum rated junction temperature of 125°C (LT1965E, LT1965I) or 150°C (LT1965H) limits its power handling capability. Two components comprise the power dissipated by the device:

1. Output current multiplied by the input/output voltage differential: $I_{OUT} \bullet (V_{IN} – V_{OUT})$, and
2. GND pin current multiplied by the input voltage: $I_{GND} \bullet V_{IN}$

GND pin current is determined using the GND Pin Current curves in the Typical Performance Characteristics section. Power dissipation equals the sum of the two components listed.

The LT1965 regulators have internal thermal limiting that protect the device during overload conditions. For continuous normal conditions, do not exceed the maximum junction temperature rating of 125°C (E-grade, I-grade) or 150°C (H-grade). Carefully consider all sources of thermal resistance from junction to ambient including other heat sources mounted in proximity to the LT1965.

The underside of the LT1965 DFN package has exposed metal ($4mm^2$) from the lead frame to the die attachment. The underside of the LT1965 MSOP package also has exposed metal ($3.7mm^2$). Both packages allow heat to directly transfer from the die junction to the printed circuit board metal to control maximum operating junction temperature. The dual-in-line pin arrangement allows metal to extend beyond the ends of the package on the topside (component side) of a PCB. Connect this metal to GND on the PCB. The multiple IN and OUT pins of the LT1965 also assist in spreading heat to the PCB.

For surface mount devices, heat sinking is accomplished by using the heat spreading capabilities of the PC board and its copper traces. Copper board stiffeners and plated through-holes can also be used to spread the heat generated by power devices.

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APPLICATIONS INFORMATION

The following tables list thermal resistance for several different board sizes and copper areas. All measurements were taken in still air on a 2-layer 1/16" FR-4 board with one ounce copper.

Table 1. Measured Thermal Resistance for DFN Package

Copper Area Topside*	Copper Area Backside	Board Area	Thermal Resistance (Junction-to-Ambient)
2500mm^2	2500mm^2	2500mm^2	60°C/W
1000mm^2	2500mm^2	2500mm^2	62°C/W
225mm^2	2500mm^2	2500mm^2	65°C/W
100mm^2	2500mm^2	2500mm^2	68°C/W
50mm^2	2500mm^2	2500mm^2	70°C/W

*Device is mounted on topside

Table 2. Measured Thermal Resistance for MSOP Package

Copper Area Topside*	Copper Area Backside	Board Area	Thermal Resistance (Junction-to-Ambient)
2500mm^2	2500mm^2	2500mm^2	55°C/W
1000mm^2	2500mm^2	2500mm^2	57°C/W
225mm^2	2500mm^2	2500mm^2	60°C/W
100mm^2	2500mm^2	2500mm^2	65°C/W
50mm^2	2500mm^2	2500mm^2	68°C/W

*Device is mounted on topside

Table 3. Measured Thermal Resistance for DD-Pak Package

Copper Area Topside*	Copper Area Backside	Board Area	Thermal Resistance (Junction-to-Ambient)
2500mm^2	2500mm^2	2500mm^2	25°C/W
1000mm^2	2500mm^2	2500mm^2	30°C/W
125mm^2	2500mm^2	2500mm^2	35°C/W

*Device is mounted on topside

Measured Thermal Resistance for TO-220 Package

Thermal Resistance (Junction-to-Case) = 3°C/W

Calculating Junction Temperature

Example: Given an output voltage of 2.5V, an input voltage range of 3.3V ± 5%, an output current range of 0mA to 500mA and a maximum ambient temperature of 85°C, what will the maximum junction temperature be?

The power dissipated by the device equals:

$$I_{OUT(MAX)} \bullet (V_{IN(MAX)} - V_{OUT}) + I_{GND} \bullet V_{IN(MAX)}$$

where:

$I_{OUT(MAX)} = 500mA$

$V_{IN(MAX)} = 3.465V$

I_{GND} at ($I_{OUT} = 500mA$, $V_{IN} = 3.465V$) = 8.2mA

So,

$$P = 500mA(3.465V - 2.5V) + 8.2mA(3.465V) = 0.511W$$

Using a DFN package, the thermal resistance will be in the range of 60°C/W to 70°C/W depending on the copper area. So the junction temperature rise above ambient approximately equals:

$$0.511W \bullet 65°C/W = 33.22°C$$

The maximum junction temperature equals the maximum ambient temperature plus the maximum junction temperature rise above ambient or:

$$T_{JMAX} = 85°C + 33.22°C = 118.22°C$$

Protection Features

The LT1965 regulators incorporate several protection features that makes them ideal for use in battery-powered circuits. In addition to the normal protection features associated with monolithic regulators, such as current limiting and thermal limiting, the devices also protect against reverse-input voltages, reverse-output voltages and reverse output-to-input voltages.

Current-limit protection and thermal overload protection protect the device against current overload conditions at its output. For normal operation, do not exceed the maximum rated junction temperature of 125°C (LT1965E, LT1965I) or 150°C (LT1965H).

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APPLICATIONS INFORMATION

The input of the device withstands reverse voltages of 22V. The LT1965 limits current flow to less than 1mA (typically less than 300µA) and no negative voltage appears at the output. The device protects both itself and the load against batteries that are plugged in backwards.

The LT1965 incurs no damage if its output is pulled below ground. If the input is left open-circuit or grounded, the output can be pulled below ground by 22V. For fixed voltage versions, the output will act like a large resistor, typically 5k or higher, limiting current flow to typically less than 300µA. For the adjustable version, the output acts like an open circuit and no current flows from the output. However, current flows out of (but is limited by) the resistor divider that sets the output voltage. If the input is powered by a voltage source, the LT1965 protects itself by shutting off the output.

The LT1965 adjustable version incurs no damage if the ADJ pin is pulled above or below ground by 9V. If the input is left open-circuit or grounded, the ADJ pin performs like a diode in series with typically 1.5k of resistance when pulled below ground and like a large resistor (typically 5k up to 3V on the ADJ pin and then 1.5k up to 9V) in series with a diode when pulled above ground.

In situations where the ADJ pin connects to a resistor divider that would pull the ADJ pin above its 9V clamp voltage if the output is pulled high, the ADJ pin input current must be limited to less than 5mA. For example, a resistor divider is used to provide a regulated 1.5V output from the 1.20V reference when the output is forced to 20V. The top resistor of the resistor divider must be chosen to limit the current into the ADJ pin to less than 5mA when the ADJ pin is at 9V. The 11V difference between the OUT and ADJ pins divided by the 5mA maximum current into the ADJ pin yields a minimum top resistor value of 2.2k.

In circuits where a backup battery is required, several different input/output conditions can occur. The output voltage may be held up while the input is either pulled to ground, pulled to some intermediate voltage, or is left open-circuit. Current flow back into the output follows the curve shown in Figure 6.

If the LT1965's IN pin is forced below the OUT pin or the OUT pin is pulled above the IN pin, input current typically drops to less than 2µA. This occurs if the LT1965 input is connected to a discharged (low voltage) battery and either a backup battery or a second regulator holds up the output. The state of the $\overline{SHDN}$ pin has no effect on the reverse-output current if the output is pulled above the input.

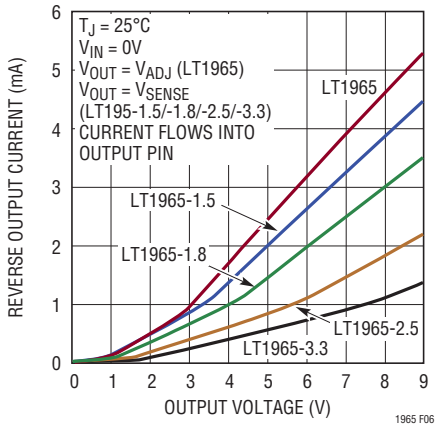

Figure 6. Reverse-Output Current

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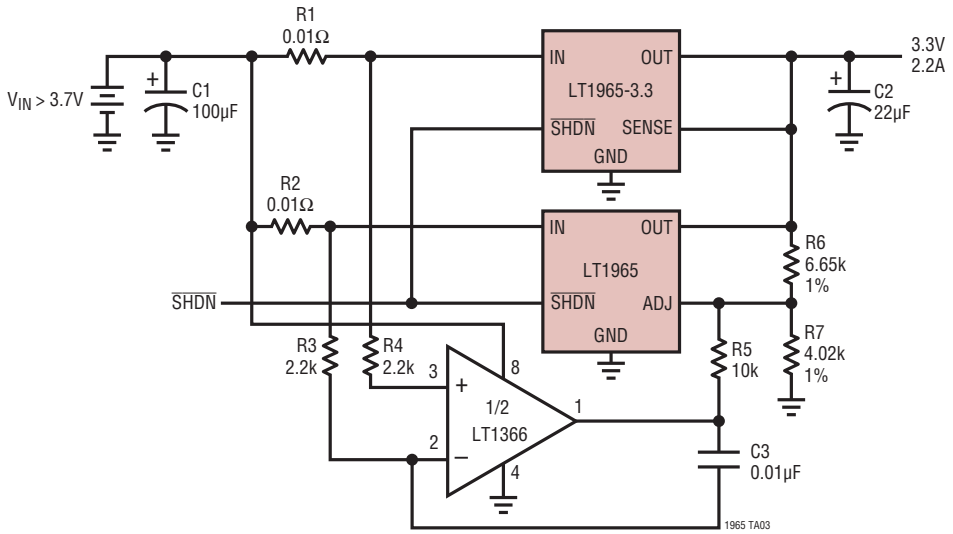
TYPICAL APPLICATIONS

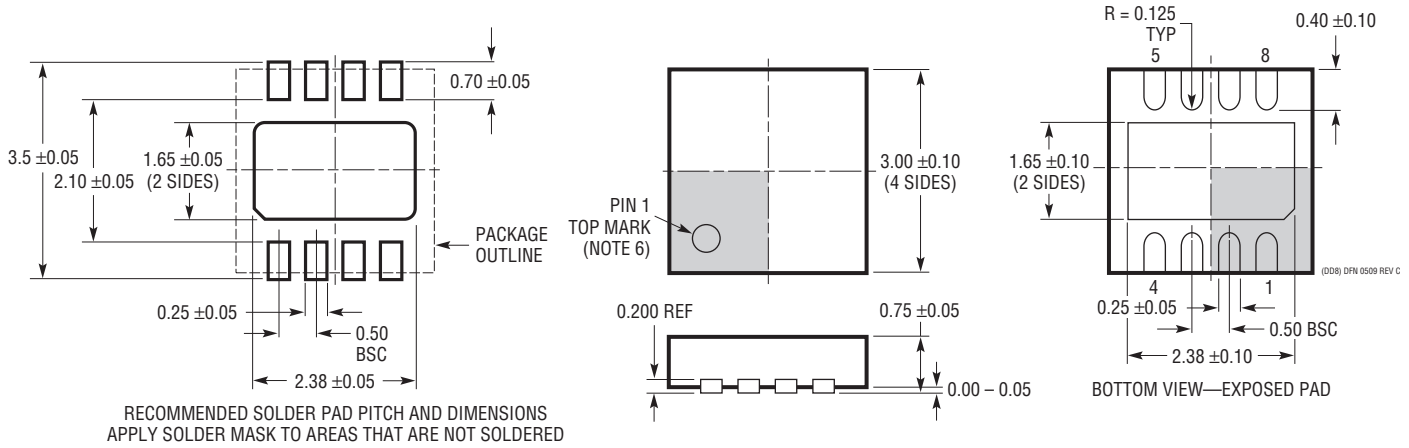
Paralleling of Regulators for Higher Output Current



PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

DD Package
8-Lead Plastic DFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1698 Rev C)



NOTE:
1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (WEED-1)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON TOP AND BOTTOM OF PACKAGE

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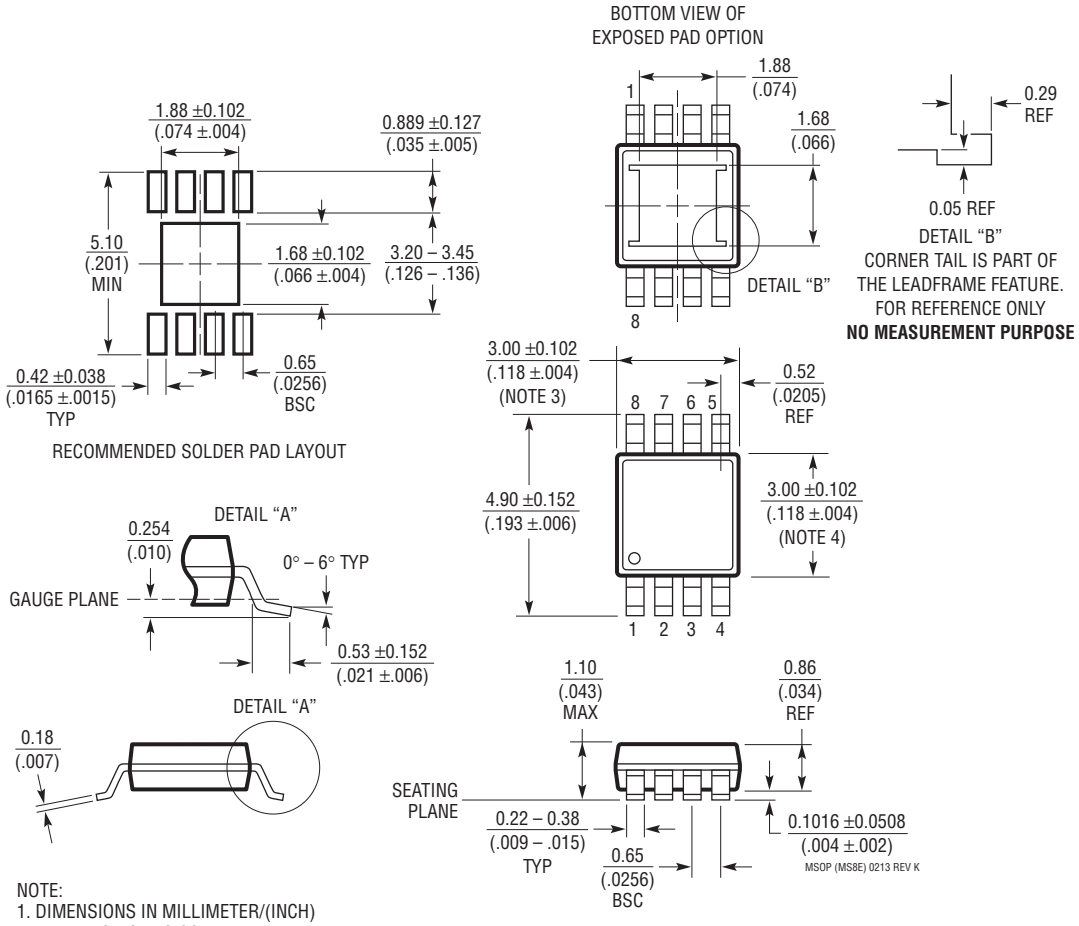
PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

MS8E Package
8-Lead Plastic MSOP, Exposed Die Pad
(Reference LTC DWG # 05-08-1662 Rev K)



NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX
6. EXPOSED PAD DIMENSION DOES INCLUDE MOLD FLASH. MOLD FLASH ON E-PAD
   SHALL NOT EXCEED 0.254mm (.010") PER SIDE.

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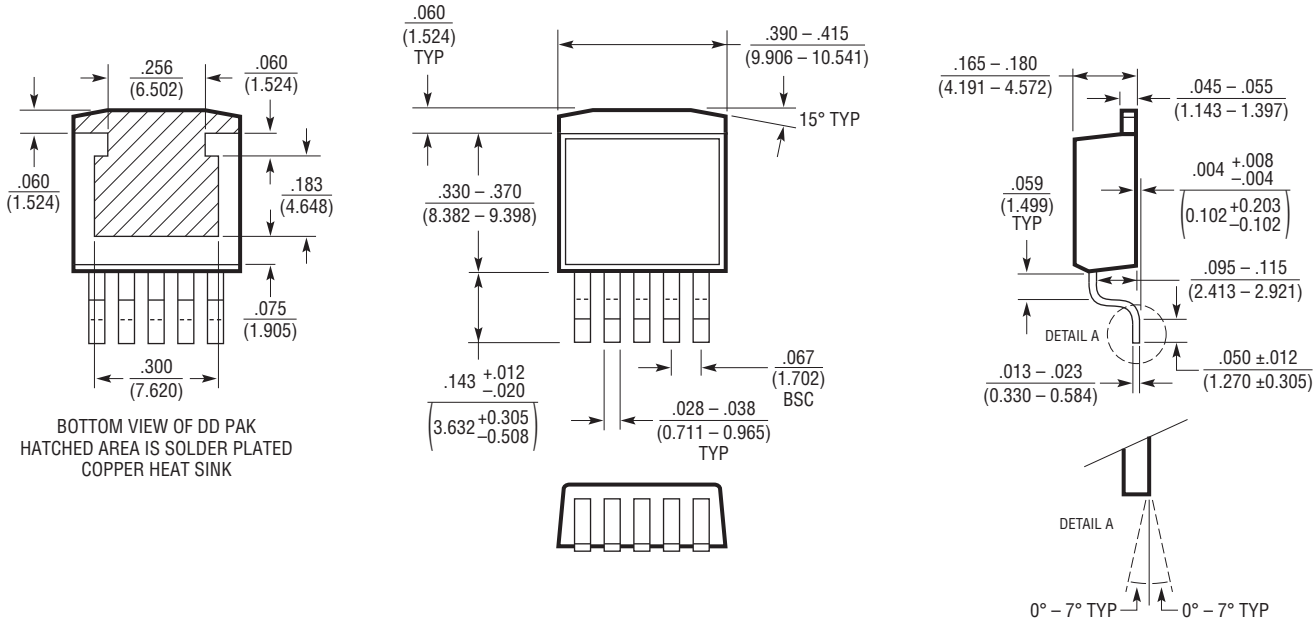
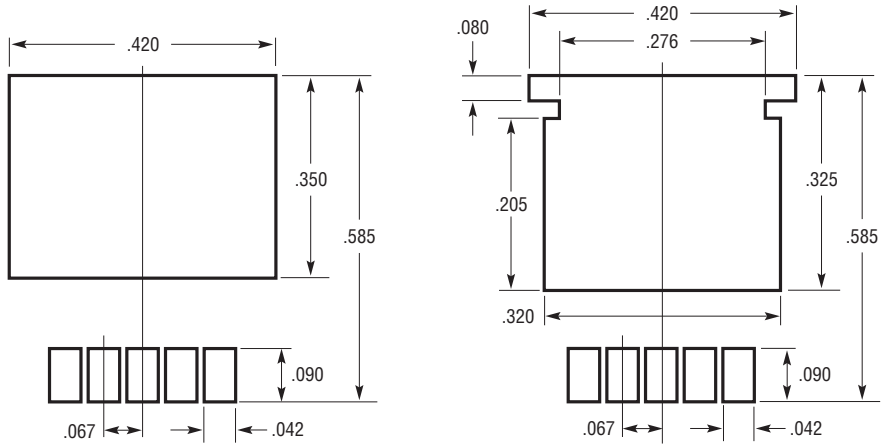
PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

Q Package
5-Lead Plastic DD Pak
(Reference LTC DWG # 05-08-1461 Rev F)





RECOMMENDED SOLDER PAD LAYOUT

RECOMMENDED SOLDER PAD LAYOUT
FOR THICKER SOLDER PASTE APPLICATIONS

NOTE:
1. DIMENSIONS IN INCH/(MILLIMETER)
2. DRAWING NOT TO SCALE

Q(DD5) 0811 REV F

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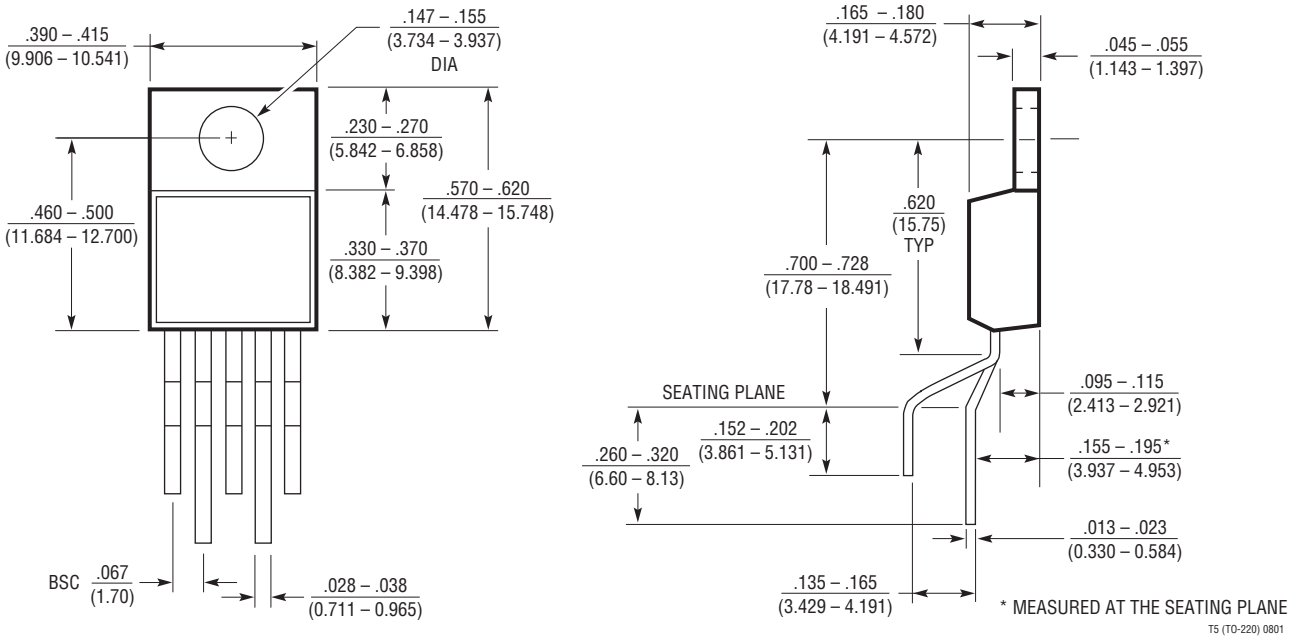
PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

T-Package
5-Lead Plastic TO-220 (Standard)
(Reference LTC DWG # 05-08-1421)



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REVISION HISTORY (Revision history begins at Rev B)

REV	DATE	DESCRIPTION	PAGE NUMBER
B	08/13	Added H-grade, specs and curves	2-10
		Lowered max ESR to 0.3Ω	12
		Removed references to “starting up from negative output”	11, 12, 16

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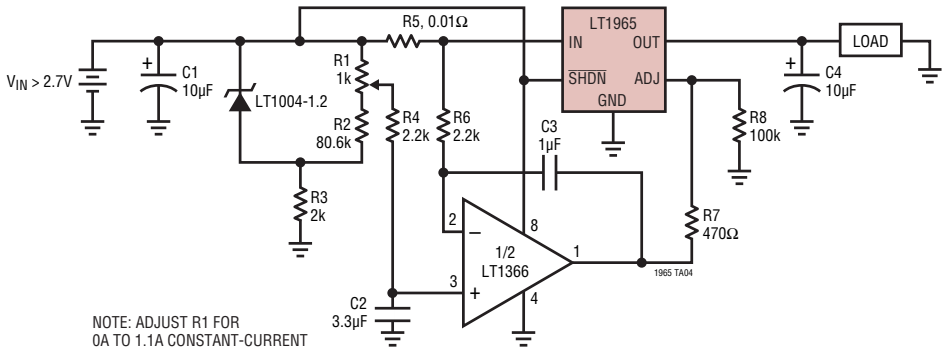
TYPICAL APPLICATION

Adjustable Current Source



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1129	700mA, Micropower, LDO	V_{IN}: 4.2V to 30V, $V_{OUT(MIN)}$ = 3.8V, V_{DO} = 0.40V, I_Q = 50µA, I_{SD} = 16µA; DD, SOT-223, S8, TO220-5 and TSSOP20 Packages
LT1761	100mA, Low Noise Micropower, LDO	V_{IN}: 1.8V to 20V, $V_{OUT(MIN)}$ = 1.22V, V_{DO} = 0.30V, I_Q = 20µA, I_{SD} = < 1µA, Low Noise < 20µV_{RMS}, Stable with 1µF Ceramic Capacitors, ThinSOT™ Package
LT1762	150mA, Low Noise Micropower, LDO	V_{IN}: 1.8V to 20V, $V_{OUT(MIN)}$ = 1.22V, V_{DO} = 0.30V, I_Q = 25µA, I_{SD} = < 1µA, Low Noise < 20µV_{RMS}, MS8 Package
LT1763	500mA, Low Noise Micropower, LDO	V_{IN}: 1.8V to 20V, $V_{OUT(MIN)}$ = 1.22V, V_{DO} = 0.30V, I_Q = 30µA, I_{SD} = < 1µA, Low Noise < 20µV_{RMS}, S8 Package
LT1764/ LT1764A	3A, Low Noise, Fast Transient Response, LDO	V_{IN}: 2.7V to 20V, $V_{OUT(MIN)}$ = 1.21V, V_{DO} = 0.34V, I_Q = 1mA, I_{SD} = < 1µA, Low Noise < 40µV_{RMS}, "A" Version Stable with Ceramic Capacitors, DD and TO220-5 Packages
LTC1844	150mA, Very Low Drop-Out LDO	V_{IN}: 1.6V to 6.5V, $V_{OUT(MIN)}$ = 1.25V, V_{DO} = 0.08V, I_Q = 35µA, I_{SD} = < 1µA, Low Noise < 60µV_{RMS}, ThinSOT™ Package
LT1962	300mA, Low Noise Micropower, LDO	V_{IN}: 1.8V to 20V, $V_{OUT(MIN)}$ = 1.22V, V_{DO} = 0.27V, I_Q = 30µA, I_{SD} = < 1µA, Low Noise < 20µV_{RMS}, MS8 Package
LT1963/ LT1963A	1.5A, Low Noise, Fast Transient Response, LDO	V_{IN}: 2.1V to 20V, $V_{OUT(MIN)}$ = 1.21V, V_{DO} = 0.34V, I_Q = 1mA, I_{SD} = < 1µA, Low Noise < 40µV_{RMS}, "A" Version Stable with Ceramic Capacitors; DD, TO220-5, SOT-223 and S8 Packages
LT3020	100mA, Low Voltage V_{DO}, $V_{IN(MIN)}$ = 0.9V, LDO	V_{IN}: 0.9V to 10V, $V_{OUT(MIN)}$ = 0.20V, V_{DO} = 0.15V, I_Q = 120µA, I_{SD} = 3µA, DFN and MS8 Packages
LT3021	500mA, Low Voltage V_{DO}, $V_{IN(MIN)}$ = 0.9V, LDO	V_{IN}: 0.9V to 10V, $V_{OUT(MIN)}$ = 0.20V, V_{DO} = 0.16V, I_Q = 120µA, I_{SD} = 3µA, DFN and S8 Packages
LT3023	Dual, 2x 100mA, Low Noise Micropower, LDO	V_{IN}: 1.8V to 20V, $V_{OUT(MIN)}$ = 1.22V, V_{DO} = 0.30V, I_Q = 40µA, I_{SD} = < 1µA, DFN and MS10 Packages
LT3024	Dual, 100mA/500mA, Low Noise Micropower, LDO	V_{IN}: 1.8V to 20V, $V_{OUT(MIN)}$ = 1.22V, V_{DO} = 0.30V, I_Q = 60µA, I_{SD} = < 1µA, DFN and TSSOP Packages
LT3027	Dual, 2x 100mA, Low Noise Micropower, LDO with Independent Inputs	V_{IN}: 1.8V to 20V, $V_{OUT(MIN)}$ = 1.22V, V_{DO} = 0.30V, I_Q = 25µA, I_{SD} = < 1µA, Low Noise < 20µV_{RMS}, DFN and MS10 Packages
LT3028	Dual, 100mA/500mA, Low Noise Micropower, LDO with Independent Inputs	V_{IN}: 1.8V to 20V, $V_{OUT(MIN)}$ = 1.22V, V_{DO} = 0.30V, I_Q = 30µA, I_{SD} = < 1µA, Low Noise < 20µV_{RMS}, DFN and TSSOP Packages
LT3080/ LT3080-1	1.1A Parallelable, Low Noise, Low Dropout Linear Regulator	300mV Dropout Voltage (2-Supply Operation), Low Noise: 40µV_{RMS}, V_{IN}: 1.2V to 36V, V_{OUT}: 0V to 35.7V, Current-Based Reference with 1-Resistor V_{OUT} Set; Directly Parallelable (No Op Amp Required), Stable with Ceramic Caps, TO-220, SOT-223, MSOP and 3mm × 3mm DFN Packages; LT3080-1 Version Has Integrated Internal Ballast Resistor

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