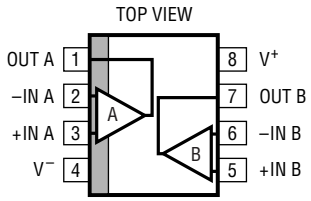
ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage (V^+ to V^-) 40V
Differential Input Voltage (Note 2) ..... ±10V
Input Voltage ..... V^+ to V^-
Input Current (Note 2) ..... ±10mA
Output Short-Circuit Duration (Note 3) ..... Indefinite

Operating Temperature Range (Note 4) .. –40°C to 85°C
Specified Temperature Range (Note 5) ... –40°C to 85°C
Maximum Junction Temperature ..... 150°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



N8 PACKAGE
8-LEAD PDIP

S8 PACKAGE
8-LEAD PLASTIC SO

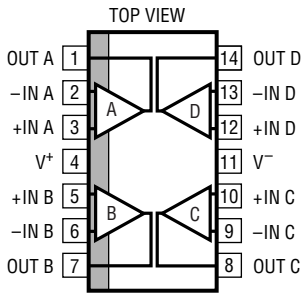
T_{JMAX} = 150°C, θ_{JA} = 130°C/W (N8)
T_{JMAX} = 150°C, θ_{JA} = 190°C/W (S8)

ORDER PART NUMBER

LT1884CN8
LT1884CS8
LT1884ACN8
LT1884ACS8
LT1884IN8
LT1884IS8
LT1884AIN8
LT1884AIS8

S8 PART MARKING

1884 1884I
1884A 1884AI



S PACKAGE
14-LEAD PLASTIC SO

T_{JMAX} = 150°C, θ_{JA} = 110°C/W

ORDER PART NUMBER

LT1885CS
LT1885IS

Consult factory for Military grade parts.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. Single supply operation V_{EE} = 0, V_{CC} = 5V; V_{CM} = V_{CC}/2 unless otherwise noted. (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage (LT1884A)				25	50	µV
		0°C < T_A < 70°C	●			85	µV
		–40°C < T_A < 85°C	●			110	µV
	Input Offset Voltage (LT1884/LT1885)				30	80	µV
		0°C < T_A < 70°C	●			125	µV
		–40°C < T_A < 85°C	●			150	µV
	Input Offset Voltage Drift (Note 6)	0°C < T_A < 70°C	●		0.3	0.8	µV/°C
		–40°C < T_A < 85°C	●		0.3	0.8	µV/°C
I_{OS}	Input Offset Current (LT1884A)				100	300	pA
		0°C < T_A < 70°C	●			400	pA
		–40°C < T_A < 85°C	●			500	pA
	Input Offset Current (LT1884/LT1885)				150	900	pA
		0°C < T_A < 70°C	●			1200	pA
		–40°C < T_A < 85°C	●			1400	pA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. Single supply operation V_{EE} = 0, V_{CC} = 5V; V_{CM} = V_{CC}/2 unless otherwise noted. (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_B	Input Bias Current (LT1884A)				100	400	pA
		0°C < T_A < 70°C	●			500	pA
		–40°C < T_A < 85°C	●			600	pA
	Input Bias Current (LT1884/LT1885)				150	900	pA
		0°C < T_A < 70°C	●			1200	pA
		–40°C < T_A < 85°C	●			1400	pA
	Input Noise Voltage	0.1Hz to 10Hz			0.4		μV_{P-P}
e_n	Input Noise Voltage Density	f = 1kHz			9.5		$nV/\sqrt{Hz}$
i_n	Input Noise Current Density	f = 1kHz			0.05		$pA/\sqrt{Hz}$
V_{CM}	Input Voltage Range			V_{EE} + 1.0		V_{CC} – 1.0	V
			●	V_{EE} + 1.2		V_{CC} – 1.2	V
CMRR	Common Mode Rejection Ratio	1V < V_{CM} < 4V		108	128		dB
		1.2V < V_{CM} < 3.8V	●	106			dB
PSRR	Power Supply Rejection Ratio	V_{EE} = 0, V_{CM} = 1.5V					
		0°C < T_A < 85°C, 2.7V < V_{CC} < 32V	●	108	132		dB
		T_A = –40°C, 3V < V_{CC} < 32V		108	132		dB
	Minimum Operating Supply Voltage		●		2.4	2.7	V
A_{VOL}	Large-Signal Voltage Gain	R_L = 10k; 1V < V_{OUT} < 4V		500	1600		V/mV
			●	350			V/mV
		R_L = 2k; 1V < V_{OUT} < 4V		400	800		V/mV
			●	300			V/mV
		R_L = 1k; 1V < V_{OUT} < 4V		300	400		V/mV
			●	200			V/mV
V_{OL}	Output Voltage Swing Low	No Load	●		20	40	mV
		I_{SINK} = 100µA	●		25	50	mV
		I_{SINK} = 1mA	●		70	150	mV
		I_{SINK} = 5mA	●		270	600	mV
V_{OH}	Output Voltage Swing High (Referred to V_{CC})	No Load	●		120	220	mV
		I_{SOURCE} = 100µA	●		130	230	mV
		I_{SOURCE} = 1mA	●		180	300	mV
		I_{SOURCE} = 5mA	●		360	600	mV
I_S	Supply Current per Amplifier	V_{CC} = 3V		0.45	0.65	0.85	mA
			●			1.30	mA
		V_{CC} = 5V		0.50	0.65	0.9	mA
			●			1.4	mA
		V_{CC} = 12V		0.50	0.70	1.0	mA
			●			1.5	mA
I_{SC}	Short-Circuit Current	V_{OUT} Short to GND	●	15	30		mA
		V_{OUT} Short to V_{CC}	●	15	30		mA
GBW	Gain-Bandwidth Product	f = 20kHz		1.2	2		MHz
t_S	Settling Time	0.01%, V_{OUT} = 1.5V to 3.5V, A_V = –1, R_L = 2k			10		µs
SR^+	Positive Slew Rate	A_V = –1		0.45	0.9		V/µs
			●	0.36			V/µs
SR^-	Negative Slew Rate	A_V = –1		0.35	0.7		V/µs
			●	0.25			V/µs

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. Single supply operation V_{EE} = 0, V_{CC} = 5V; V_{CM} = V_{CC}/2 unless otherwise noted. (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
ΔV_{OS}	Offset Voltage Match (LT1884A)				30	70	µV
		0°C < T_A < 70°C	●			125	µV
		–40°C < T_A < 85°C	●			160	µV
	Offset Voltage Match (LT1884/LT1885)	(Note 7)			35	125	µV
		0°C < T_A < 70°C	●			195	µV
		–40°C < T_A < 85°C	●			235	µV
	Offset Voltage Match Drift	(Notes 6, 7)	●		0.4	1.2	µV/°C
ΔI_{B+}	Noninverting Bias Current Match (LT1884A)				200	600	pA
		0°C < T_A < 70°C	●			700	pA
		–40°C < T_A < 85°C	●			850	pA
	Noninverting Bias Current Match (LT1884/LT1885)	(Notes 7, 9)			250	1200	pA
		0°C < T_A < 70°C	●			1600	pA
		–40°C < T_A < 85°C	●			1900	pA
ΔCMRR	Common Mode Rejection Match	(Notes 7, 9)	●	104	125		dB
ΔPSRR	Positive Power Supply Rejection Match (Notes 7, 9)	V_{EE} = 0, V_{CM} = 1.5V					
		0°C < T_A < 85°C, 2.7V < V_{CC} < 32V	●	104	126		dB
		T_A = –40°C, 3V < V_{CC} < 32V		104	126		dB

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. Split supply operation V_S = ±15V; V_{CM} = 0V unless otherwise noted. (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage (LT1884A)				25	50	µV
		0°C < T_A < 70°C	●			85	µV
		–40°C < T_A < 85°C	●			110	µV
	Input Offset Voltage (LT1884/LT1885)				30	80	µV
		0°C < T_A < 70°C	●			125	µV
		–40°C < T_A < 85°C	●			150	µV
	Input Offset Voltage Drift (Note 6)	0°C < T_A < 70°C	●		0.3	0.8	µV/°C
		–40°C < T_A < 85°C	●		0.3	0.8	µV/°C
I_{OS}	Input Offset Current (LT1884A)				150	300	pA
		0°C < T_A < 70°C	●			400	pA
		–40°C < T_A < 85°C	●			500	pA
	Input Offset Current (LT1884/LT1885)				150	900	pA
		0°C < T_A < 70°C	●			1200	pA
		–40°C < T_A < 85°C	●			1400	pA
I_B	Input Bias Current (LT1884A)				150	400	pA
		0°C < T_A < 70°C	●			500	pA
		–40°C < T_A < 85°C	●			600	pA
	Input Bias Current (LT1884/LT1885)				150	900	pA
		0°C < T_A < 70°C	●			1200	pA
		–40°C < T_A < 85°C	●			1400	pA
	Input Noise Voltage	0.1Hz to 10Hz			0.4		μV_{P-P}
e_n	Input Noise Voltage Density	f = 1kHz			9.5		$nV/\sqrt{Hz}$
i_n	Input Noise Current Density	f = 1kHz			0.05		$pA/\sqrt{Hz}$
V_{CM}	Input Voltage Range			V_{EE} + 1.0		V_{CC} – 1.0	V
			●	V_{EE} + 1.2		V_{CC} – 1.2	V
CMRR	Common Mode Rejection Ratio	–13.5V < V_{CM} < 13.5V	●	114	130		dB

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. Split supply operation V_S = ±15V; V_{CM} = 0V unless otherwise noted. (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
+PSRR	Positive Power Supply Rejection Ratio	V_{EE} = –15V, V_{CM} = 0V; 1.5V < V_{CC} < 18V	●	114	132		dB
–PSRR	Negative Power Supply Rejection Ratio	V_{CC} = 15V, V_{CM} = 0V; –1.5V < V_{EE} < –18V	●	106	132		dB
	Minimum Operating Supply Voltage		●		±1.2	±1.35	V
A_{VOL}	Large-Signal Voltage Gain	R_L = 10k; –13.5V < V_{OUT} < 13.5V	 ●	1000 700	1600		V/mV V/mV
		R_L = 2k; –13.5V < V_{OUT} < 13.5V	 ●	250 175	420		V/mV V/mV
		R_L = 1k; –12V < V_{OUT} < 12V	 ●	100 75	230		V/mV V/mV
V_{OL}	Output Voltage Swing Low (Referred to V_{EE})	No Load I_{SINK} = 100µA I_{SINK} = 1mA I_{SINK} = 5mA	● ● ● ●		20 25 70 270	40 50 150 600	mV mV mV mV
V_{OH}	Output Voltage Swing High (Referred to V_{CC})	No Load I_{SOURCE} = 100µA I_{SOURCE} = 1mA I_{SOURCE} = 5mA	● ● ● ●		160 160 180 360	220 230 300 600	mV mV mV mV
I_S	Supply Current Per Amplifier	V_S = ±15V	 ●		0.85	1.1 1.6	mA mA
I_{SC}	Short-Circuit Current	V_{OUT} Short to V_{EE} V_{OUT} Short to V_{CC}	● ●	15 15	50 30		mA mA
GBW	Gain-Bandwidth Product	f = 20kHz		1.5	2.2		MHz
t_S	Settling Time	0.01%, V_{OUT} = –5V to 5V, A_V = –1, R_L = 2k			17		µs
SR^+	Positive Slew Rate	A_V = –1	 ●	0.5 0.4	1.0		V/µs V/µs
SR^-	Negative Slew Rate	A_V = –1	 ●	0.40 0.26	0.7		V/µs V/µs
ΔV_{OS}	Offset Voltage Match (LT1884A)	(Note 7) 0°C < T_A < 70°C –40°C < T_A < 85°C	 ● ●		35	70 125 160	µV µV µV
	Offset Voltage Match (LT1884/LT1885)	(Note 7) 0°C < T_A < 70°C –40°C < T_A < 85°C	 ● ●		35	125 175 235	µV µV µV
	Offset Voltage Match Drift	(Note 6, 7)	●		0.4	1.1	µV/°C
ΔI_B^+	Noninverting Bias Current Match (LT1884A)	(Notes 7, 8) 0°C < T_A < 70°C –40°C < T_A < 85°C	 ● ●		200	600 700 850	pA pA pA
	Noninverting Bias Current Match (LT1884/LT1885)	(Notes 7, 8) 0°C < T_A < 70°C –40°C < T_A < 85°C	 ● ●		240	1200 1600 1900	pA pA pA
ΔCMRR	Common Mode Rejection Match	(Notes 7, 9)	●	106	125		dB
Δ+PSRR	Positive Power Supply Rejection Match	V_{EE} = –15V, V_{CM} = 0V, 1.5V < V_{CC} < 18V, (Notes 7, 9)	●	108	124		dB
Δ–PSRR	Negative Power Supply Rejection Match	V_{CC} = 15V, V_{CM} = 0V, –1.5V < V_{EE} < –18V, (Notes 7, 9)	●	102	132		dB

ELECTRICAL CHARACTERISTICS

Note 1: Absolute Maximum Ratings are those values beyond which the life of the device may be impaired.

Note 2: The inputs are protected by back-to-back diodes. If the differential input voltage exceeds 0.7V, the input current should be limited to less than 10mA.

Note 3: A heat sink may be required to keep the junction temperature below absolute maximum.

Note 4: The LT1884C/LT1885C and LT1884I/LT1885I are guaranteed functional over the operating temperature range of –40°C to 85°C.

Note 5: The LT1884C/LT1885C are designed, characterized and expected to meet specified performance from –40°C to 85°C but are not tested or QA sampled at these temperatures. LT1884I is guaranteed to meet specified performance from –40°C to 85°C.

Note 6: This parameter is not 100% tested.

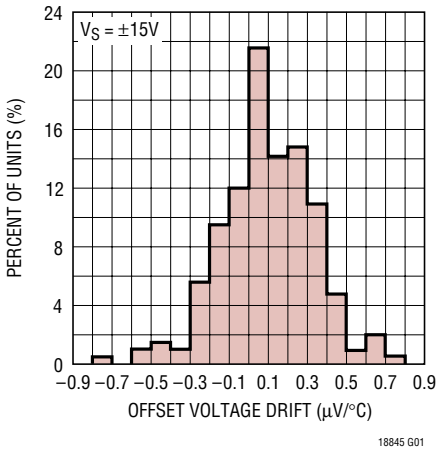
Note 7: Matching parameters are the difference between amplifiers A and B in the LT1884 and between amplifiers A and D and B and C in the LT1885.

Note 8: This parameter is the difference between the two noninverting input bias currents.

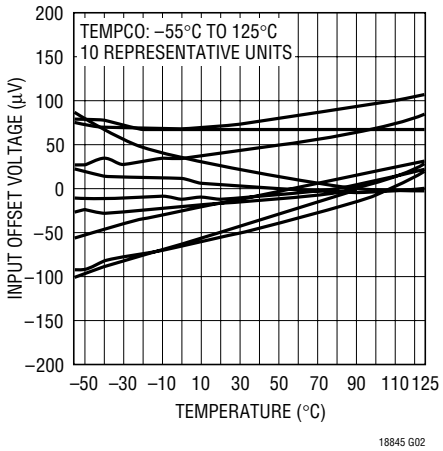
Note 9: ΔCMRR and ΔPSRR are defined as follows: CMRR and PSRR are measured in μV/V on each amplifier. The difference is calculated in μV/V and then converted to dB.

TYPICAL PERFORMANCE CHARACTERISTICS

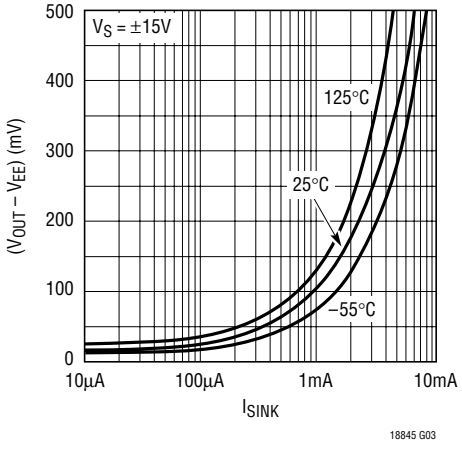
Distribution of Offset Voltage Drift



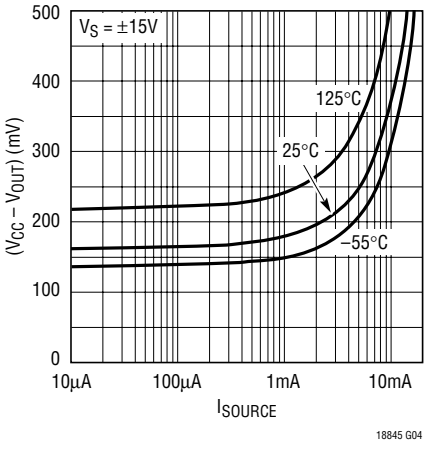
Input Offset Voltage vs Temperature



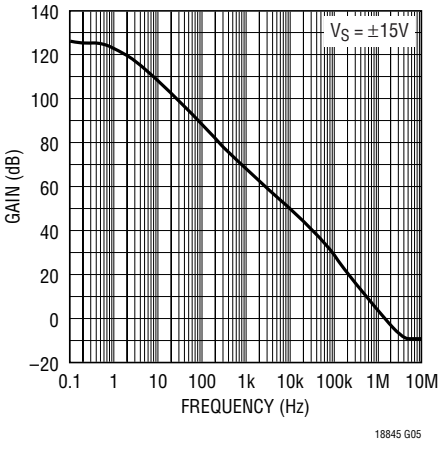
V_{OUT} vs I_{SINK}



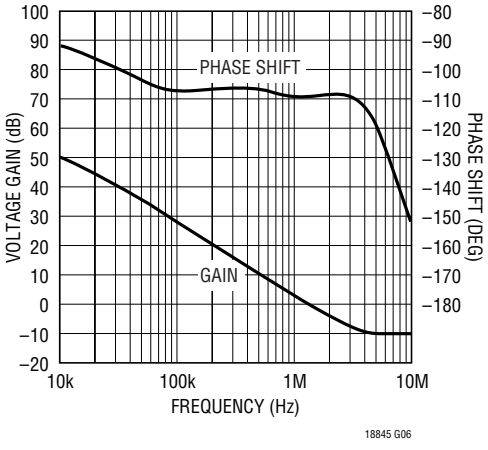
V_{OUT} vs I_{SOURCE}



Gain vs Frequency

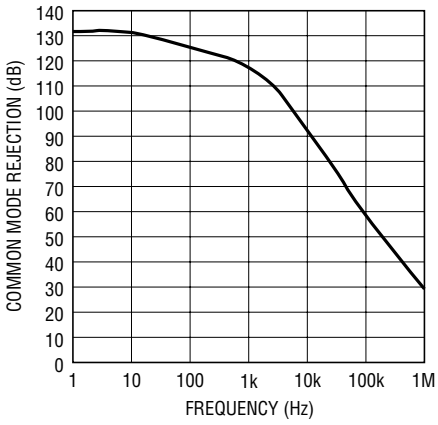


Gain, Phase Shift vs Frequency



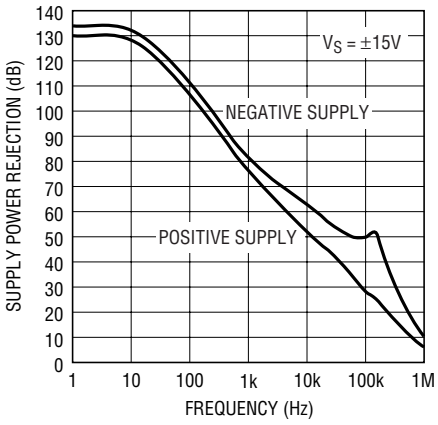
TYPICAL PERFORMANCE CHARACTERISTICS

CMRR vs Frequency



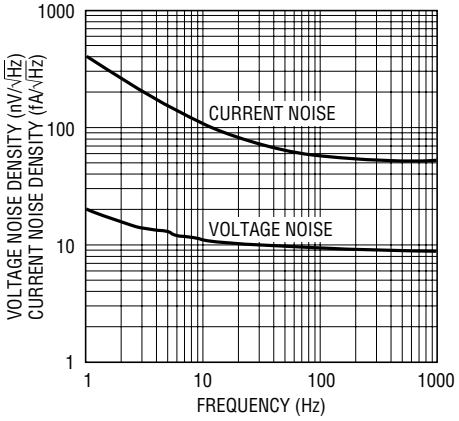
18845 G07

PSRR vs Frequency



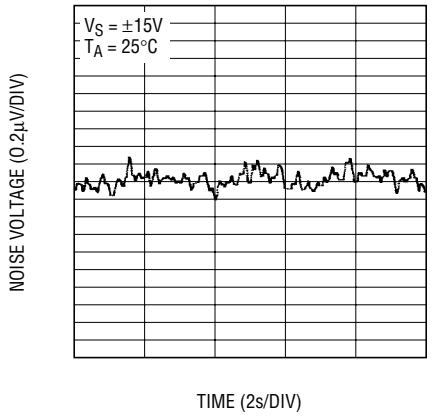
18845 G08

V_n, I_n vs Frequency



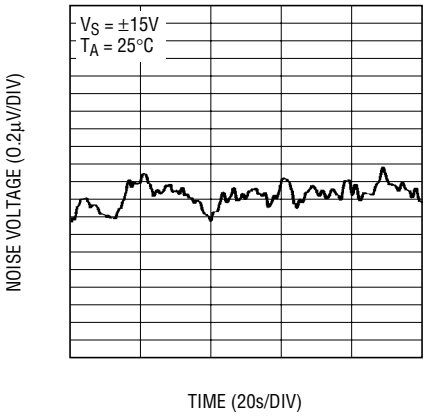
18845 G09

0.1Hz to 10Hz Noise



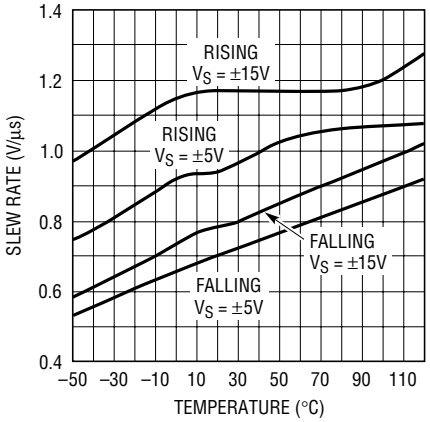
18845 G10

0.01Hz to 1Hz Noise



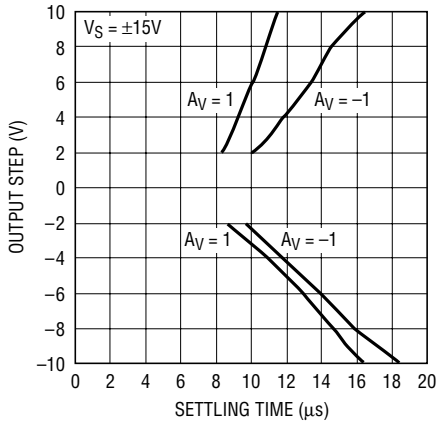
18845 G11

Slew Rate vs Temperature



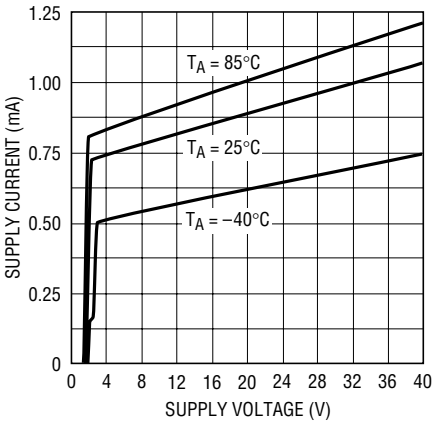
18845 G12

Settling Time to 0.01% vs Output Step



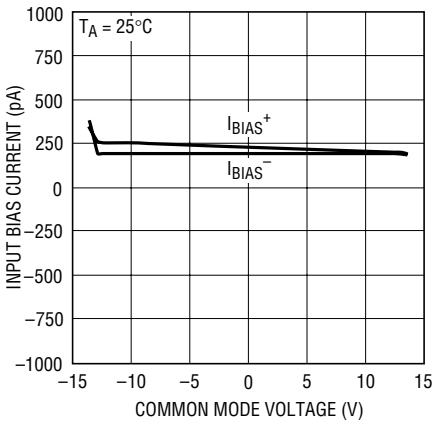
18845 G13

Supply Current per Amplifier vs Supply Voltage



18845 G14

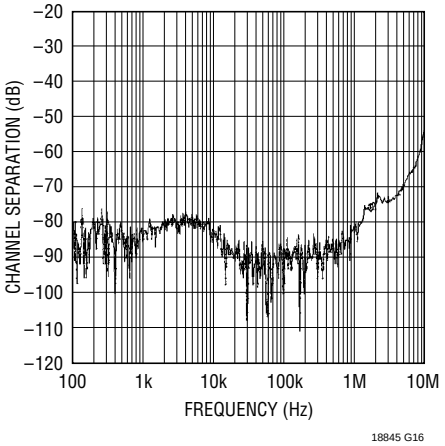
Input Bias Current vs Common Mode Voltage



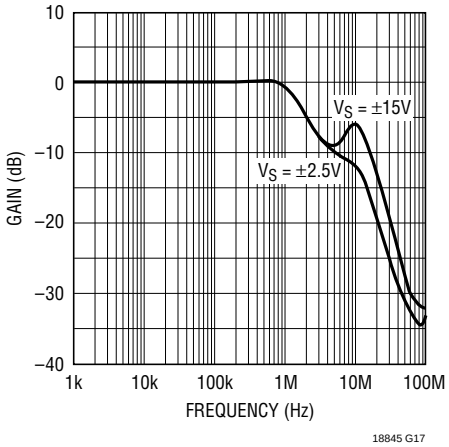
LTXXXX • TPCXX

TYPICAL PERFORMANCE CHARACTERISTICS

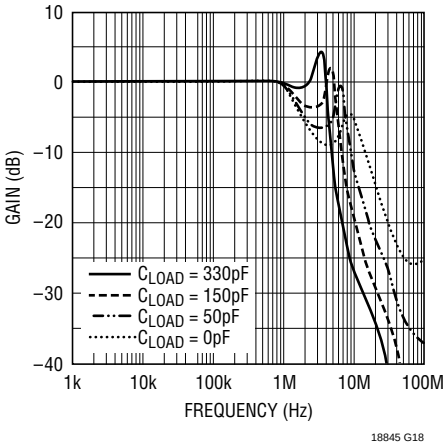
Channel Separation vs Frequency



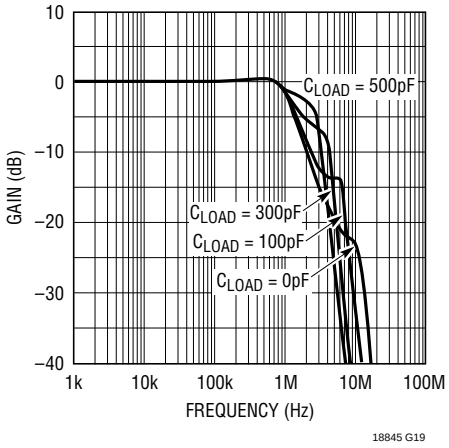
Gain vs Frequency (A_V = 1)



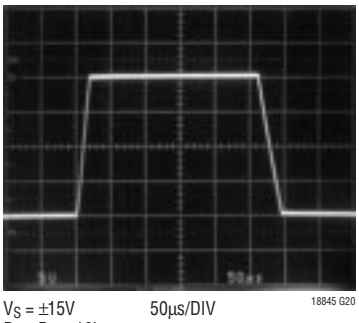
Gain vs Frequency vs C_{LOAD} (A_V = 1)



Gain vs Frequency vs C_{LOAD} (A_V = –1)

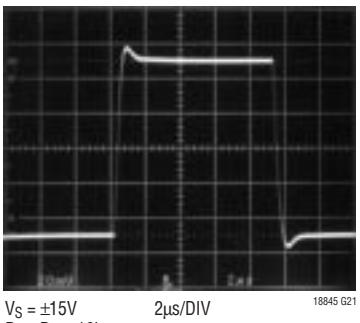


Large-Signal Response



V_S = ±15V 50µs/DIV
$R_F = R_G$ = 10k
A_V = –1

Small-Signal Response



V_S = ±15V 2µs/DIV
$R_F = R_G$ = 10k
A_V = –1

APPLICATIONS INFORMATION

The LT1884/LT1885 dual op amp features exceptional input precision with rail-to-rail output swing. Slew rate and small-signal bandwidth are superior to other amplifiers with comparable input precision. These characteristics make the LT1884/LT1885 a convenient choice for precision low voltage systems and for improved AC performance in higher voltage precision systems. Maintaining the advantage of the precision inherent in the amplifier depends upon proper applications circuit design and board layout.

Preserving Input Precision

Preserving the input voltage accuracy of the LT1884/LT1885 requires that the applications circuit and PC board layout do not introduce errors comparable to or greater than the 30μV offset. Temperature differentials across the input connections can generate thermocouple voltages of 10s of microvolts. PC board layouts should keep connections to the amplifier's input pins close together and away from heat dissipating components. Air currents across the board can also generate temperature differentials.

The extremely low input bias currents, 100pA, allow high accuracy to be maintained with high impedance sources and feedback networks. The LT1884/LT1885's low input bias currents are obtained by using a cancellation circuit on-chip. This causes the resulting I_{BIAS}^+ and I_{BIAS}^- to be uncorrelated, as implied by the I_{OS} specification being comparable to the I_{BIAS}. The user should not try to balance the input resistances in each input lead, as is commonly recommended with most amplifiers. The impedance at either input should be kept as small as possible to minimize total circuit error.

PC board layout is important to ensure that leakage currents do not corrupt the low I_{BIAS} of the amplifier. In high precision, high impedance circuits, the input pins should be surrounded by a guard ring of PC board interconnect, with the guard driven to the same common mode voltage as the amplifier inputs.

Input Common Mode Range

The LT1884/LT1885 output is able to swing close to each power supply rail, but the input stage is limited to operating between V_{EE} + 0.8V and V_{CC} – 0.9V. Exceeding this common mode range will cause the gain to drop to zero; however, no gain reversal will occur.

Input Protection

The inverting and noninverting input pins of the LT1884/LT1885 have limited on-chip protection. ESD protection is provided to prevent damage during handling. The input transistors have voltage clamping and limiting resistors to protect against input differentials up to 10V. Short transients above this level will also be tolerated. If the input pins may be subject to a sustained differential voltage above 10V, external limiting resistors should be used to prevent damage to the amplifier. A 1k resistor in each input lead will provide protection against a 30V differential voltage.

Capacitive Loads

The LT1884/LT1885 can drive capacitive loads up to 300pF when configured for unity gain. The capacitive load driving capability increases as the amplifier is used in higher gain configurations. Capacitive load driving may also be increased by decoupling the capacitance from the output with a small resistance.

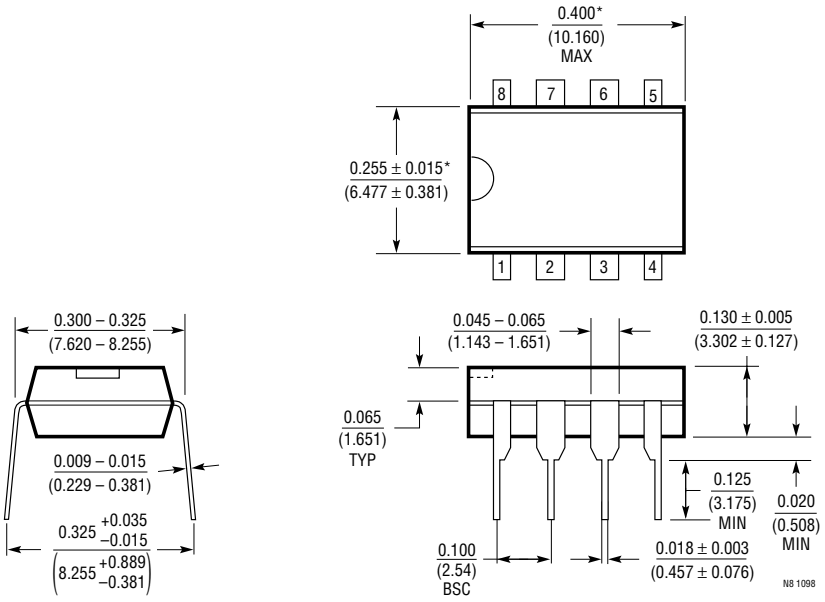
Input Bias Currents

While it may be tempting to seek out a JFET amplifier for low input bias current, remember that bipolar devices improve with temperature while JFETs degrade.

PACKAGE DESCRIPTION

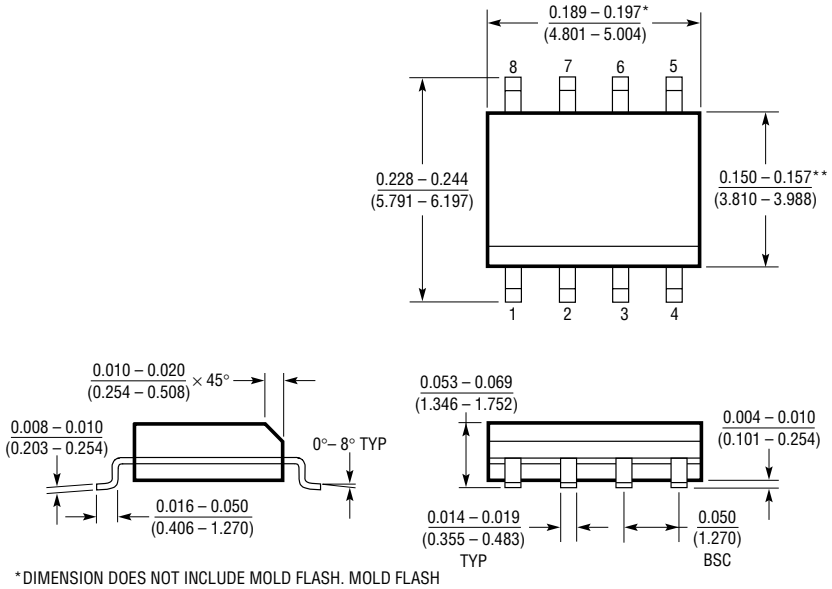
Dimensions in inches (millimeters) unless otherwise noted.

N8 Package
8-Lead PDIP (Narrow 0.300)
(LTC DWG # 05-08-1510)



*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.010 INCH (0.254mm)

S8 Package
8-Lead Plastic Small Outline (Narrow 0.150)
(LTC DWG # 05-08-1610)



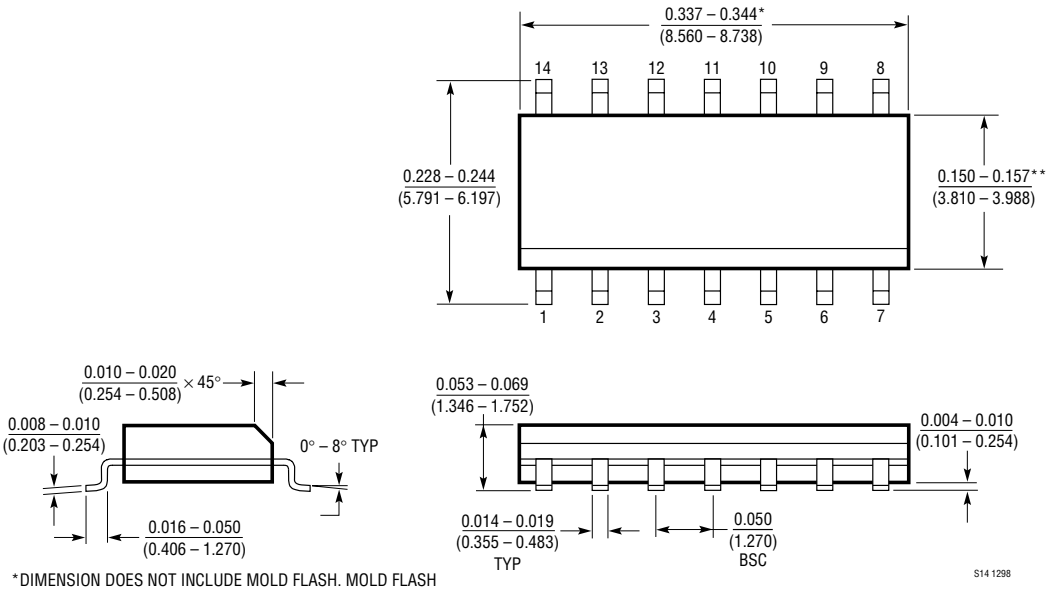
*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

S Package
14-Lead Plastic Small Outline (Narrow 0.150)
(LTC DWG # 05-08-1610)

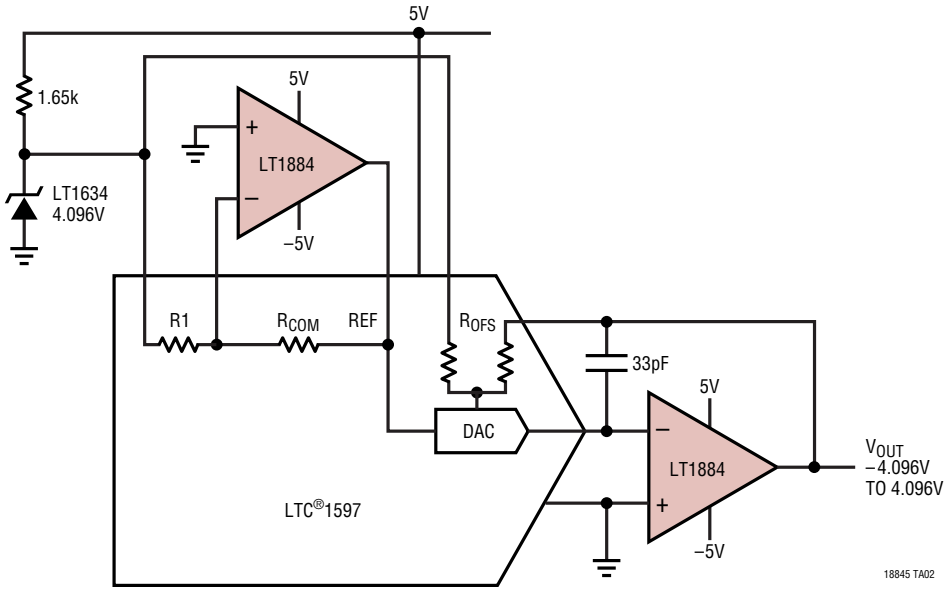


*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

TYPICAL APPLICATION

16-Bit Voltage Output DAC on ±5V Supply



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1112	Dual Picoamp Input Op Amp	V_{OS} = 60µV Max
LT1114	Quad Picoamp Input Op Amp	V_{OS} = 60µV Max
LT1167	Gain Programmable Instrumentation Amp	Gain Error = 0.08% Max
LT1490	Micropower Rail-to-Rail Input and Output Op Amp	Over-The-Top™ Common Mode Range
LT1793	Low Noise JFET Op Amp	I_B = 10pA Max
LT1881/LT1882	Picoamp Input Rail-to-Rail Output Op Amp	Lower Input Bias Currents Than LT1884/LT1885
LTC2050	Zero Drift Op Amp in SOT-23	V_{OS} = 3µV Max, Rail-to-Rail Output

Over-The-Top is a trademark of Linear Technology Corporation.

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