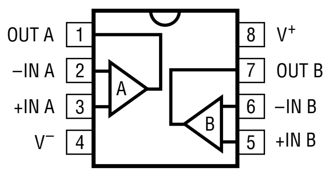
ABSOLUTE MAXIMUM RATINGS (Note 1)

Total Supply Voltage (V^+ to V^-) 36V
Differential Input Voltage
(Transient Only, Note 2) .... ±10V
Input Voltage .... $\pm V_S$
Output Short-Circuit Duration (Note 3) .... Indefinite
Operating Temperature Range (Note 8) ...–40°C to 85°C
Specified Temperature Range (Note 9) ....–40°C to 85°C
Maximum Junction Temperature (See Below)
Plastic Package .... 150°C
Storage Temperature Range ....–65°C to 150°C
Lead Temperature (Soldering, 10 sec).................. 300°C

PACKAGE/ORDER INFORMATION

TOP VIEW

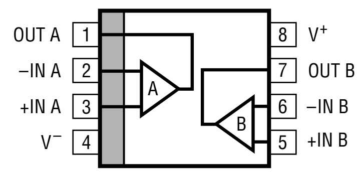


N8 PACKAGE
8-LEAD PDIP
T_{JMAX} = 150°C, θ_{JA} = 130°C/W

ORDER PART NUMBER

LT1364CN8

TOP VIEW



S8 PACKAGE
8-LEAD PLASTIC SO
T_{JMAX} = 150°C, θ_{JA} = 190°C/W

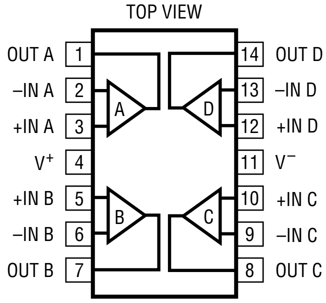
ORDER PART NUMBER

LT1364CS8

S8 PART MARKING

1364

TOP VIEW



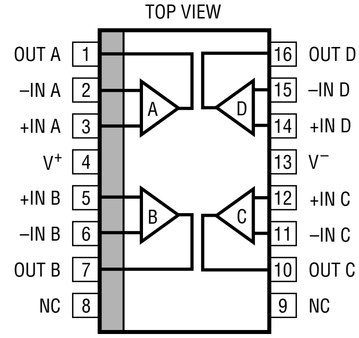
N PACKAGE
14-LEAD PDIP

T_{JMAX} = 150°C, θ_{JA} = 110°C/W

ORDER PART NUMBER

LT1365CN

TOP VIEW



S PACKAGE
16-LEAD PLASTIC SO
T_{JMAX} = 150°C, θ_{JA} = 150°C/W

ORDER PART NUMBER

LT1365CS

Consult factory for Industrial and Military grade parts.

ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CM} = 0V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	V_{SUPPLY}	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	(Note 4)	±15V ±5V ±2.5V		0.5 0.5 0.7	1.5 1.5 1.8	mV mV mV
I_{OS}	Input Offset Current		±2.5V to ±15V		120	350	nA
I_B	Input Bias Current		±2.5V to ±15V		0.6	2.0	µA
e_n	Input Noise Voltage	f = 10kHz	±2.5V to ±15V		9		$nV/\sqrt{Hz}$
i_n	Input Noise Current	f = 10kHz	±2.5V to ±15V		1		$pA/\sqrt{Hz}$
R_{IN}	Input Resistance	V_{CM} = ±12V	±15V	12	50		MΩ
	Input Resistance	Differential	±15V		5		MΩ
C_{IN}	Input Capacitance		±15V		3		pF

ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CM} = 0V$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	V_{SUPPLY}	MIN	TYP	MAX	UNITS
	Input Voltage Range $^+$		±15V	12.0	13.4		V
			±5V	2.5	3.4		V
			±2.5V	0.5	1.1		V
	Input Voltage Range $^-$		±15V		−13.2	−12.0	V
			±5V		−3.2	−2.5	V
			±2.5V		−0.9	−0.5	V
CMRR	Common Mode Rejection Ratio	V_{CM} = ±12V	±15V	84	90		dB
		V_{CM} = ±2.5V	±5V	76	81		dB
		V_{CM} = ±0.5V	±2.5V	66	71		dB
PSRR	Power Supply Rejection Ratio	V_S = ±2.5V to ±15V		90	100		dB
A_{VOL}	Large-Signal Voltage Gain	V_{OUT} = ±12V, R_L = 1k	±15V	4.5	9.0		V/mV
		V_{OUT} = ±10V, R_L = 500Ω	±15V	3.0	6.5		V/mV
		V_{OUT} = ±7.5V, R_L = 150Ω	±15V	2.0	3.8		V/mV
		V_{OUT} = ±2.5V, R_L = 500Ω	±5V	3.0	6.4		V/mV
		V_{OUT} = ±2.5V, R_L = 150Ω	±5V	2.0	5.6		V/mV
		V_{OUT} = ±1V, R_L = 500Ω	±2.5V	2.5	5.2		V/mV
V_{OUT}	Output Swing	R_L = 1k, V_{IN} = ±40mV	±15V	13.5	14.0		±V
		R_L = 500Ω, V_{IN} = ±40mV	±15V	13.0	13.7		±V
		R_L = 500Ω, V_{IN} = ±40mV	±5V	3.5	4.1		±V
		R_L = 150Ω, V_{IN} = ±40mV	±5V	3.4	3.8		±V
		R_L = 500Ω, V_{IN} = ±40mV	±2.5V	1.3	1.7		±V
I_{OUT}	Output Current	V_{OUT} = ±7.5V	±15V	50	60		mA
		V_{OUT} = ±3.4V	±5V	23	29		mA
I_{SC}	Short-Circuit Current	V_{OUT} = 0V, V_{IN} = ±3V	±15V	70	105		mA
SR	Slew Rate	A_V = −2, (Note 5)	±15V	750	1000		V/µs
			±5V	300	450		V/µs
	Full Power Bandwidth	10V Peak, (Note 6)	±15V		15.9		MHz
		3V Peak, (Note 6)	±5V		23.9		MHz
GBW	Gain Bandwidth	f = 200kHz	±15V	50	70		MHz
			±5V	35	50		MHz
			±2.5V		40		MHz
t_r, t_f	Rise Time, Fall Time	A_V = 1, 10%-90%, 0.1V	±15V		2.6		ns
			±5V		3.6		ns
	Overshoot	A_V = 1, 0.1V	±15V		36		%
			±5V		23		%
	Propagation Delay	50% V_{IN} to 50% V_{OUT}, 0.1V	±15V		4.6		ns
			±5V		5.6		ns
t_s	Settling Time	10V Step, 0.1%, A_V = −1	±15V		50		ns
		10V Step, 0.01%, A_V = −1	±15V		80		ns
		5V Step, 0.1%, A_V = −1	±5V		55		ns
	Differential Gain	f = 3.58MHz, A_V = 2, R_L = 150Ω	±15V		0.03		%
			±5V		0.06		%
		f = 3.58MHz, A_V = 2, R_L = 1k	±15V		0.01		%
			±5V		0.01		%
	Differential Phase	f = 3.58MHz, A_V = 2, R_L = 150Ω	±15V		0.10		Deg
			±5V		0.04		Deg
		f = 3.58MHz, A_V = 2, R_L = 1k	±15V		0.05		Deg
			±5V		0.25		Deg
R_O	Output Resistance	A_V = 1, f = 1MHz	±15V		0.7		Ω
	Channel Separation	V_{OUT} = ±10V, R_L = 500Ω	±15V	100	113		dB
I_S	Supply Current	Each Amplifier	±15V		6.3	7.5	mA
		Each Amplifier	±5V		6.0	7.2	mA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the temperature range $0°C \leq T_A \leq 70°C$, $V_{CM} = 0V$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	V_{SUPPLY}		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	(Note 4)	±15V ±5V ±2.5V	● ● ●			2.0 2.0 2.2	mV mV mV
	Input V_{OS} Drift	(Note 7)	±2.5V to ±15V	●		10	13	µV/°C
I_{OS}	Input Offset Current		±2.5V to ±15V	●			500	nA
I_B	Input Bias Current		±2.5V to ±15V	●			3	µA
CMRR	Common Mode Rejection Ratio	$V_{CM} = ±12V$ $V_{CM} = ±2.5V$ $V_{CM} = ±0.5V$	±15V ±5V ±2.5V	● ● ●	82 74 64			dB dB dB
PSRR	Power Supply Rejection Ratio	$V_S = ±2.5V$ to $±15V$		●	88			dB
A_{VOL}	Large-Signal Voltage Gain	$V_{OUT} = ±12V$, $R_L = 1k$ $V_{OUT} = ±10V$, $R_L = 500Ω$ $V_{OUT} = ±2.5V$, $R_L = 500Ω$ $V_{OUT} = ±2.5V$, $R_L = 150Ω$ $V_{OUT} = ±1V$, $R_L = 500Ω$	±15V ±15V ±5V ±5V ±2.5V	● ● ● ● ●	3.6 2.4 2.4 1.5 2.0			V/mV V/mV V/mV V/mV V/mV
V_{OUT}	Output Swing	$R_L = 1k$, $V_{IN} = ±40mV$ $R_L = 500Ω$, $V_{IN} = ±40mV$ $R_L = 500Ω$, $V_{IN} = ±40mV$ $R_L = 150Ω$, $V_{IN} = ±40mV$ $R_L = 500Ω$, $V_{IN} = ±40mV$	±15V ±15V ±5V ±5V ±2.5V	● ● ● ● ●	13.4 12.8 3.4 3.3 1.2			±V ±V ±V ±V ±V
I_{OUT}	Output Current	$V_{OUT} = ±12.8V$ $V_{OUT} = ±3.3V$	±15V ±5V	● ●	25 22			mA mA
I_{SC}	Short-Circuit Current	$V_{OUT} = 0V$, $V_{IN} = ±3V$	±15V	●	55			mA
SR	Slew Rate	$A_V = -2$, (Note 5)	±15V ±5V	● ●	600 225			V/µs V/µs
GBW	Gain Bandwidth	f = 200kHz	±15V ±5V	● ●	44 31			MHz MHz
	Channel Separation	$V_{OUT} = ±10V$, $R_L = 500Ω$	±15V	●	98			dB
I_S	Supply Current	Each Amplifier Each Amplifier	±15V ±5V	● ●			8.7 8.4	mA mA

The ● denotes the specifications which apply over the temperature range $-40°C \leq T_A \leq 85°C$, $V_{CM} = 0V$ unless otherwise noted. (Note 9)

SYMBOL	PARAMETER	CONDITIONS	V_{SUPPLY}		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	(Note 4)	±15V ±5V ±2.5V	● ● ●			2.5 2.5 2.7	mV mV mV
	Input V_{OS} Drift	(Note 7)	±2.5V to ±15V	●		10	13	µV/°C
I_{OS}	Input Offset Current		±2.5V to ±15V	●			600	nA
I_B	Input Bias Current		±2.5V to ±15V	●			3.6	µA
CMRR	Common Mode Rejection Ratio	$V_{CM} = ±12V$ $V_{CM} = ±2.5V$ $V_{CM} = ±0.5V$	±15V ±5V ±2.5V	● ● ●	82 74 64			dB dB dB
PSRR	Power Supply Rejection Ratio	$V_S = ±2.5V$ to $±15V$		●	87			dB
A_{VOL}	Large-Signal Voltage Gain	$V_{OUT} = ±12V$, $R_L = 1k$ $V_{OUT} = ±10V$, $R_L = 500Ω$ $V_{OUT} = ±2.5V$, $R_L = 500Ω$ $V_{OUT} = ±2.5V$, $R_L = 150Ω$ $V_{OUT} = ±1V$, $R_L = 500Ω$	±15V ±15V ±5V ±5V ±2.5V	● ● ● ● ●	2.5 1.5 1.5 1.0 1.3			V/mV V/mV V/mV V/mV V/mV

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the temperature range $-40°C \le T_A \le 85°C$, V_{CM} = 0V unless otherwise noted. (Note 9)

SYMBOL	PARAMETER	CONDITIONS	V_{SUPPLY}		MIN	TYP	MAX	UNITS
V_{OUT}	Output Swing	R_L = 1k, V_{IN} = ±40mV	±15V	●	13.4			±V
		R_L = 500Ω, V_{IN} = ±40mV	±15V	●	12.7			±V
		R_L = 500Ω, V_{IN} = ±40mV	±5V	●	3.4			±V
		R_L = 150Ω, V_{IN} = ±40mV	±5V	●	3.2			±V
		R_L = 500Ω, V_{IN} = ±40mV	±2.5V	●	1.2			±V
I_{OUT}	Output Current	V_{OUT} = ±12.7V	±15V	●	25			mA
		V_{OUT} = ±3.2V	±5V	●	21			mA
I_{SC}	Short-Circuit Current	V_{OUT} = 0V, V_{IN} = ±3V	±15V	●	50			mA
SR	Slew Rate	A_V = –2, (Note 5)	±15V	●	550			V/µs
			±5V	●	180			V/µs
GBW	Gain Bandwidth	f = 200kHz	±15V	●	43			MHz
			±5V	●	30			MHz
	Channel Separation	V_{OUT} = ±10V, R_L = 500Ω	±15V	●	98			dB
I_S	Supply Current	Each Amplifier	±15V	●			9.0	mA
		Each Amplifier	±5V	●			8.7	mA

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: Differential inputs of ±10V are appropriate for transient operation only, such as during slewing. Large, sustained differential inputs will cause excessive power dissipation and may damage the part. See Input Considerations in the Applications Information section of this data sheet for more details.

Note 3: A heat sink may be required to keep the junction temperature below absolute maximum when the output is shorted indefinitely.

Note 4: Input offset voltage is pulse tested and is exclusive of warm-up drift.

Note 5: Slew rate is measured between ±10V on the output with ±6V input for ±15V supplies and ±1V on the output with ±1.75V input for ±5V supplies.

Note 6: Full power bandwidth is calculated from the slew rate measurement: FPBW = $SR/2\pi V_P$.

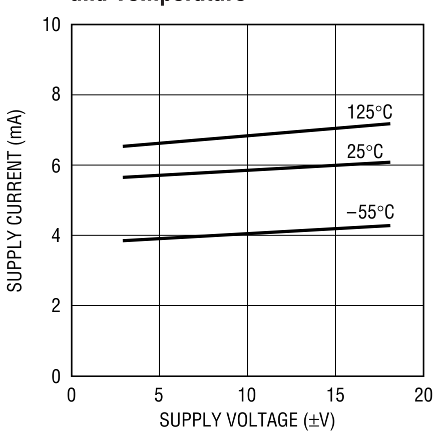
Note 7: This parameter is not 100% tested.

Note 8: The LT1364C/LT1365C are guaranteed functional over the operating temperature range of –40°C to 85°C.

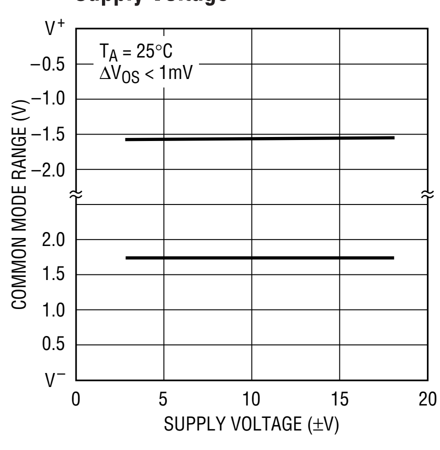
Note 9: The LT1364C/LT1365C are guaranteed to meet specified performance from 0°C to 70°C. The LT1364C/LT1365C are designed, characterized and expected to meet specified performance from –40°C to 85°C, but are not tested or QA sampled at these temperatures. For guaranteed I-grade parts, consult the factory.

TYPICAL PERFORMANCE CHARACTERISTICS

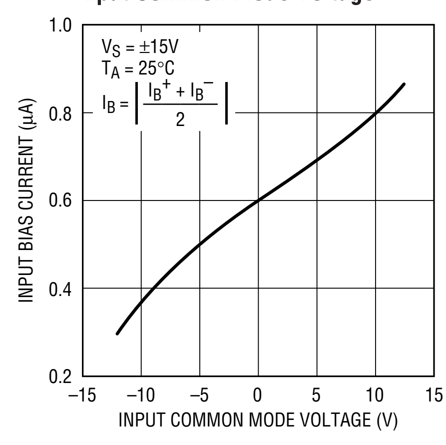
Supply Current vs Supply Voltage and Temperature



Input Common Mode Range vs Supply Voltage

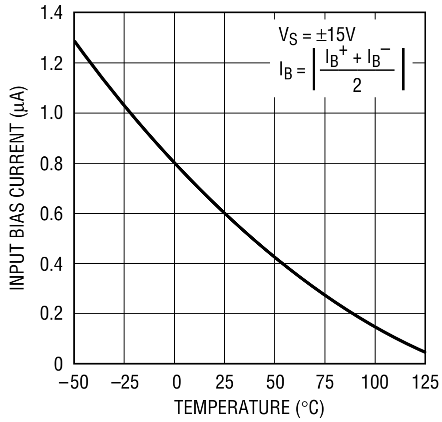


Input Bias Current vs Input Common Mode Voltage



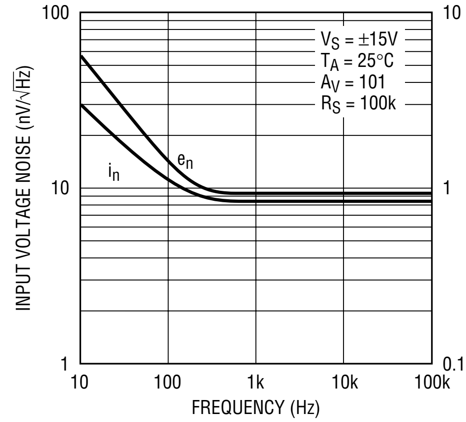
TYPICAL PERFORMANCE CHARACTERISTICS

Input Bias Current vs Temperature



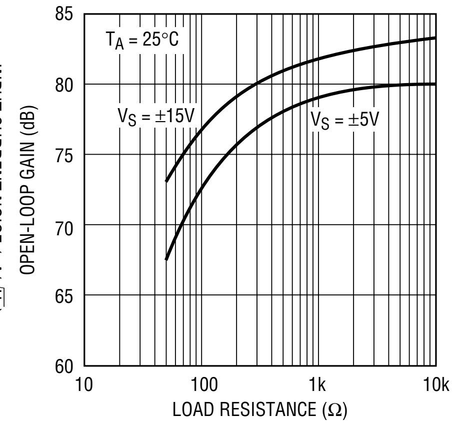
1364/1365 G04

Input Noise Spectral Density



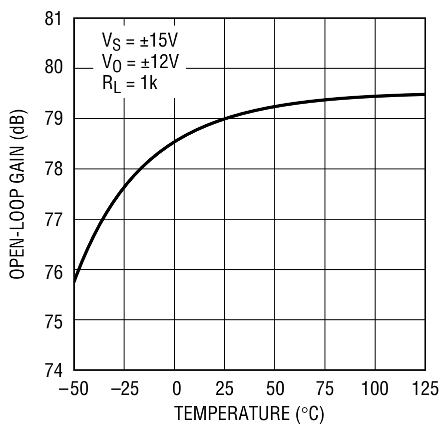
1364/1365 G05

Open-Loop Gain vs Resistive Load



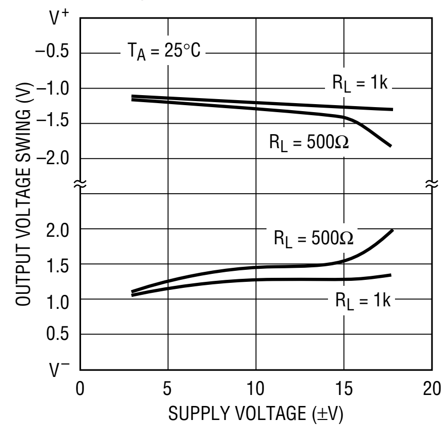
1364/1365 G06

Open-Loop Gain vs Temperature



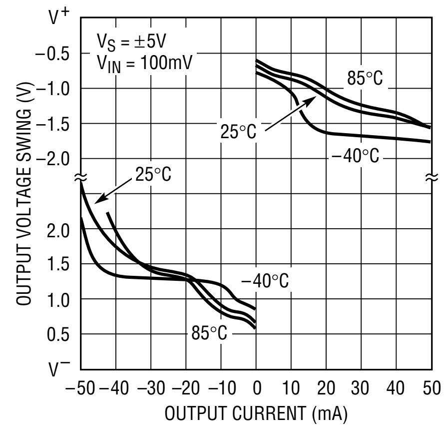
1364/1365 G07

Output Voltage Swing vs Supply Voltage



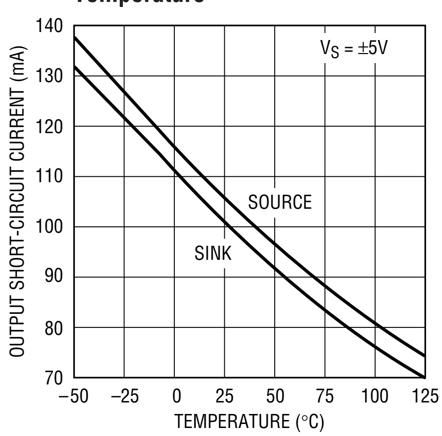
1364/1365 G08

Output Voltage Swing vs Load Current



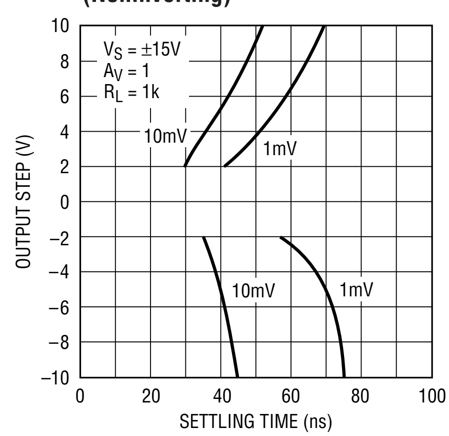
1364/1365 G09

Output Short-Circuit Current vs Temperature



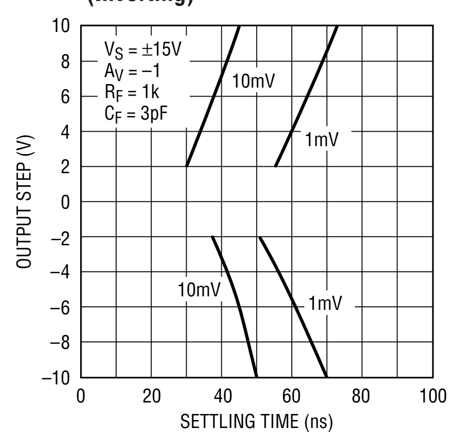
1364/1365 G10

Settling Time vs Output Step (Noninverting)



1364/1365 G11

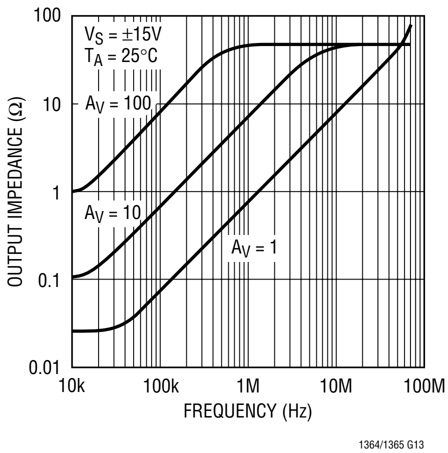
Settling Time vs Output Step (Inverting)



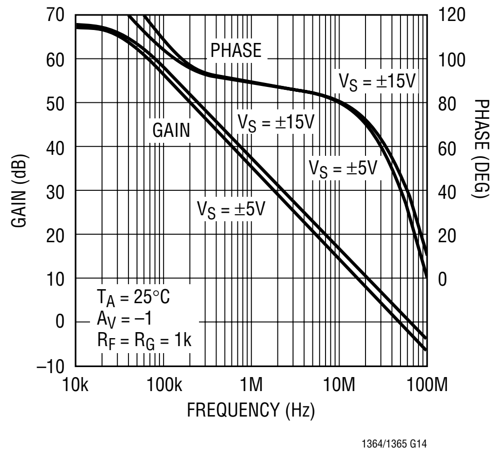
1364/1365 G12

TYPICAL PERFORMANCE CHARACTERISTICS

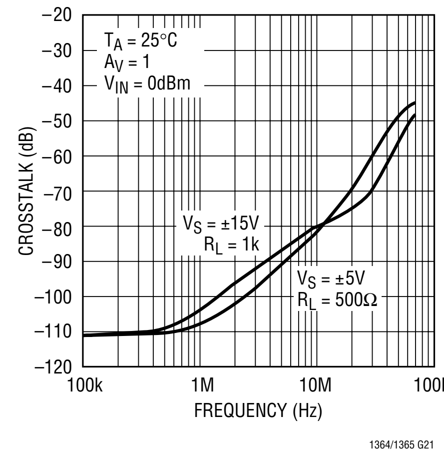
Output Impedance vs Frequency



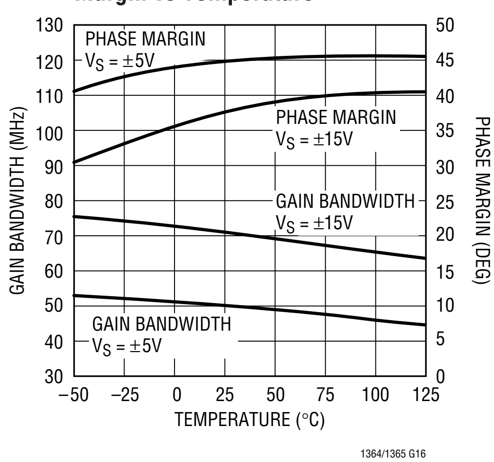
Gain and Phase vs Frequency



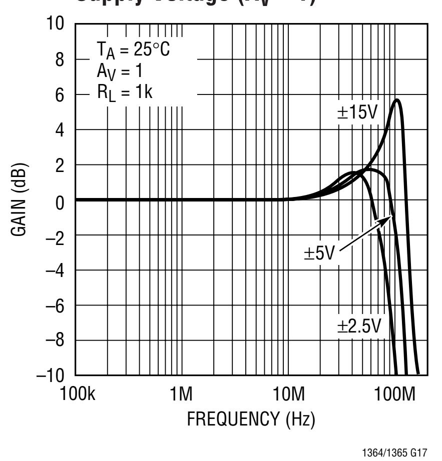
Crosstalk vs Frequency



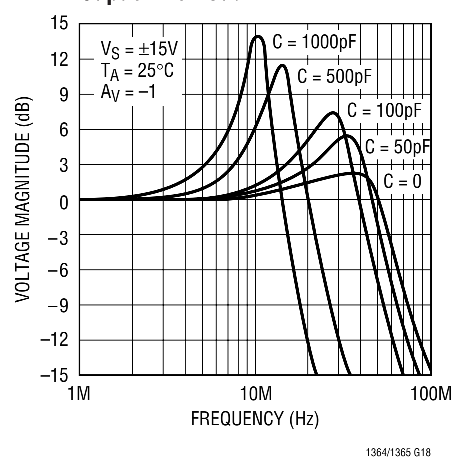
Gain Bandwidth and Phase Margin vs Temperature



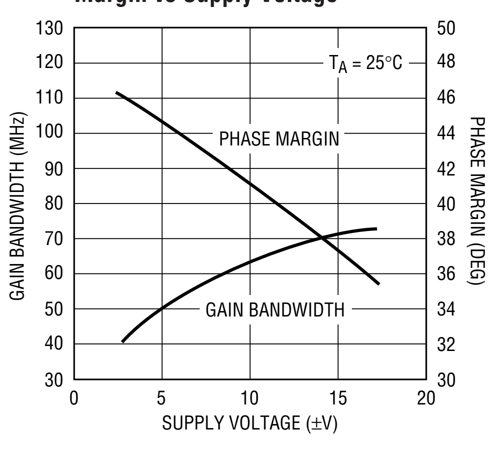
Frequency Response vs Supply Voltage (A_V = 1)



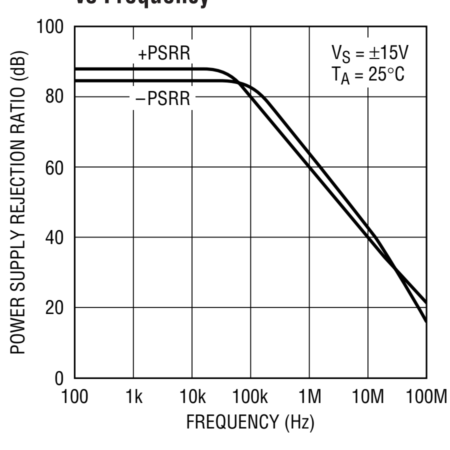
Frequency Response vs Capacitive Load



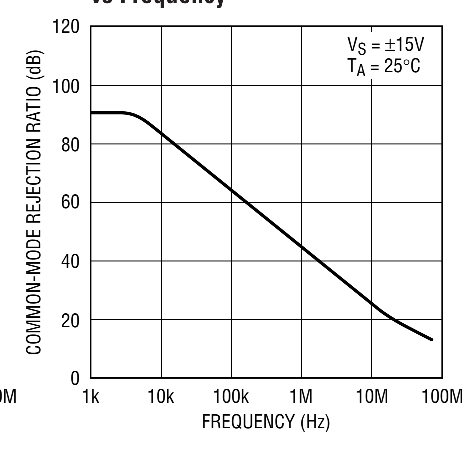
Gain Bandwidth and Phase Margin vs Supply Voltage



Power Supply Rejection Ratio vs Frequency

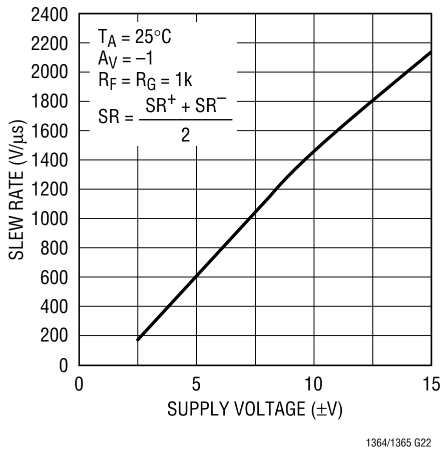


Common Mode Rejection Ratio vs Frequency

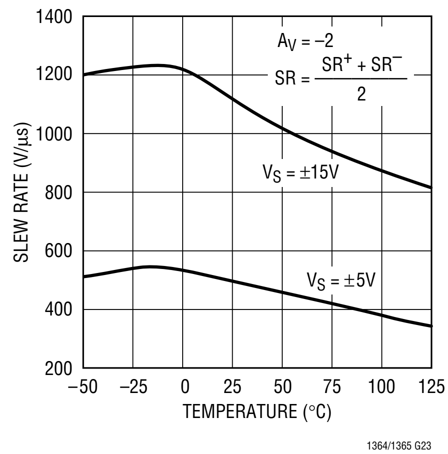


TYPICAL PERFORMANCE CHARACTERISTICS

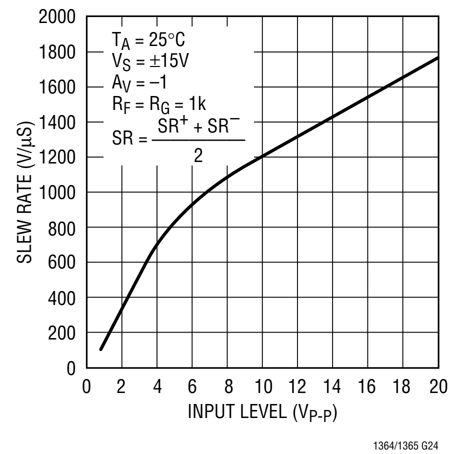
Slew Rate vs Supply Voltage



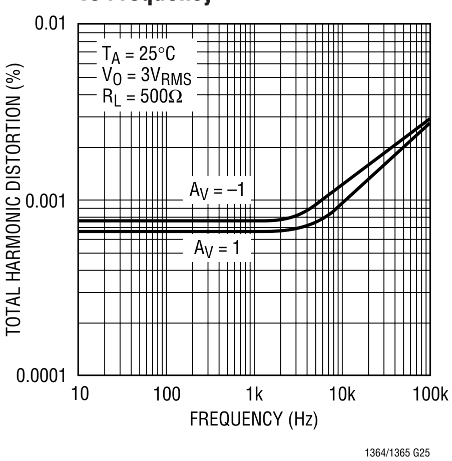
Slew Rate vs Temperature



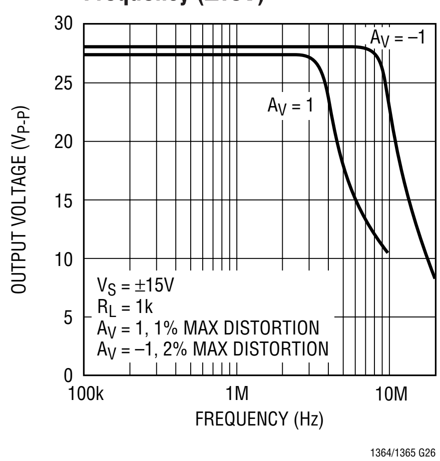
Slew Rate vs Input Level



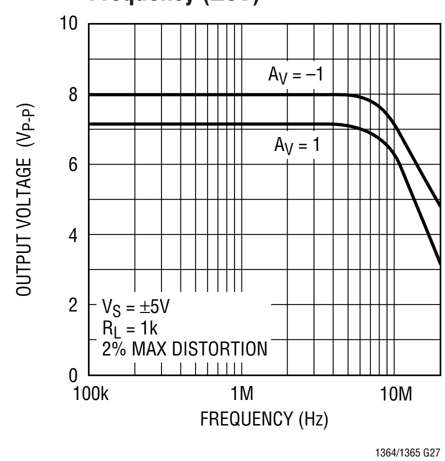
Total Harmonic Distortion vs Frequency



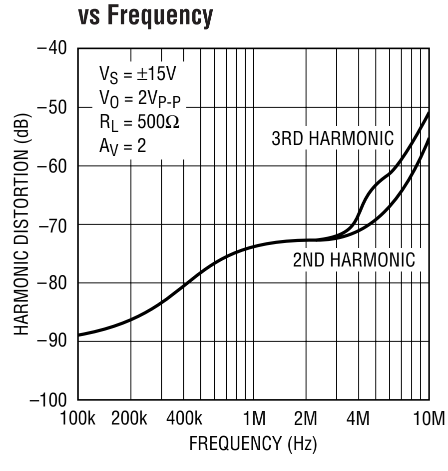
Undistorted Output Swing vs Frequency (±15V)



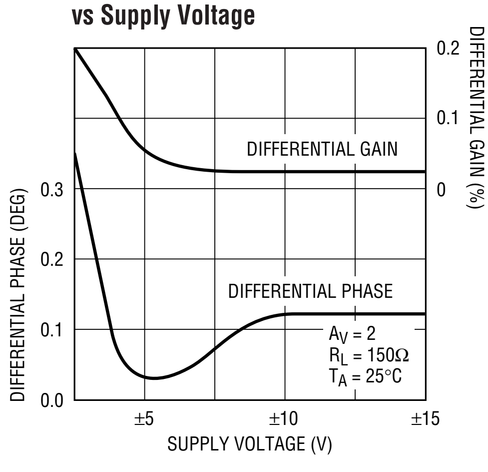
Undistorted Output Swing vs Frequency (±5V)



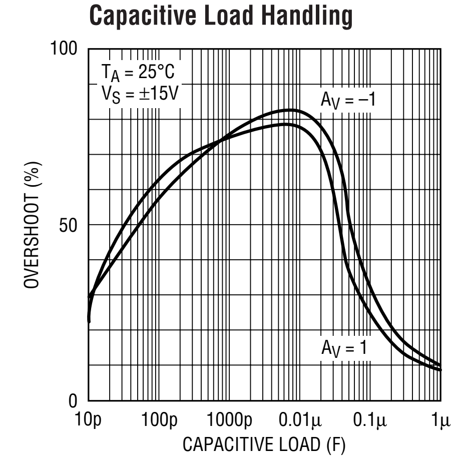
2nd and 3rd Harmonic Distortion vs Frequency



Differential Gain and Phase vs Supply Voltage

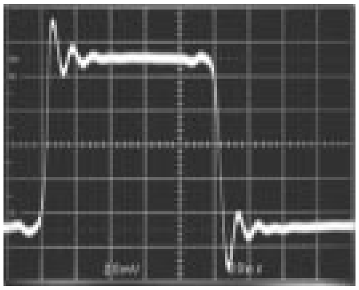


Capacitive Load Handling



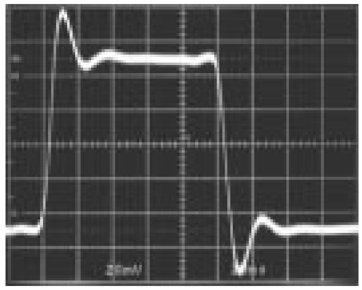
TYPICAL PERFORMANCE CHARACTERISTICS

Small-Signal Transient (A_V = 1)



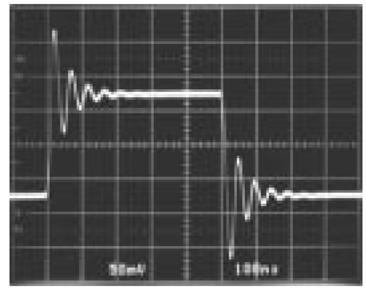
1364/1365 TA31

Small-Signal Transient (A_V = –1)



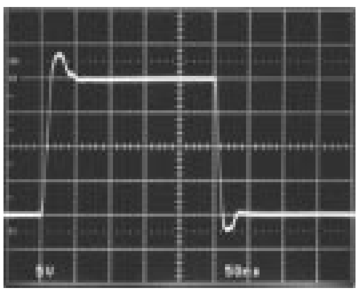
1364/1365 TA32

Small-Signal Transient (A_V = –1, C_L = 200pF)



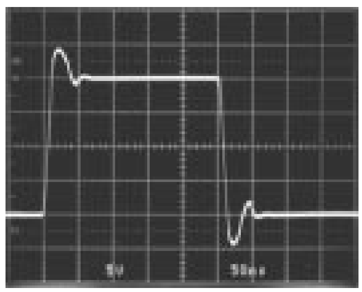
1364/1365 TA33

Large-Signal Transient (A_V = 1)



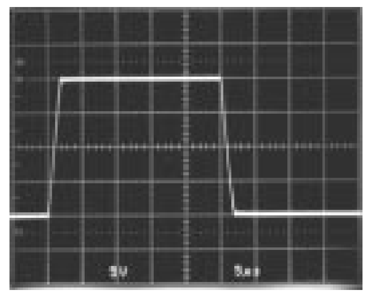
1364/1365 TA34

Large-Signal Transient (A_V = –1)



1364/1365 TA35

Large-Signal Transient (A_V = 1, C_L = 10,000pF)



1364/1365 TA36

APPLICATIONS INFORMATION

Layout and Passive Components

The LT1364/LT1365 amplifiers are easy to use and tolerant of less than ideal layouts. For maximum performance (for example, fast 0.01% settling) use a ground plane, short lead lengths, and RF-quality bypass capacitors (0.01µF to 0.1µF). For high drive current applications use low ESR bypass capacitors (1µF to 10µF tantalum).

The parallel combination of the feedback resistor and gain setting resistor on the inverting input combine with the input capacitance to form a pole which can cause peaking or oscillations. If feedback resistors greater than 5kΩ are used, a parallel capacitor of value

$$C_F > R_G \times C_{IN}/R_F$$

should be used to cancel the input pole and optimize dynamic performance. For unity-gain applications where a large feedback resistor is used, C_F should be greater than or equal to C_{IN}.

Input Considerations

Each of the LT1364/LT1365 inputs is the base of an NPN and a PNP transistor whose base currents are of opposite polarity and provide first-order bias current cancellation. Because of variation in the matching of NPN and PNP beta, the polarity of the input bias current can be positive or negative. The offset current does not depend on NPN/PNP beta matching and is well controlled. The use of balanced source resistance at each input is recommended for applications where DC accuracy must be maximized.

The inputs can withstand transient differential input voltages up to 10V without damage and need no clamping or source resistance for protection. Differential inputs, however, generate large supply currents (tens of mA) as required for high slew rates. If the device is used with sustained differential inputs, the average supply current will increase, excessive power dissipation will result and the part may be damaged. **The part should not be used as**

APPLICATIONS INFORMATION

a comparator, peak detector or other open-loop application with large, sustained differential inputs. Under normal, closed-loop operation, an increase of power dissipation is only noticeable in applications with large slewing outputs and is proportional to the magnitude of the differential input voltage and the percent of the time that the inputs are apart. Measure the average supply current for the application in order to calculate the power dissipation.

Capacitive Loading

The LT1364/LT1365 are stable with any capacitive load. This is accomplished by sensing the load induced output pole and adding compensation at the amplifier gain node. As the capacitive load increases, both the bandwidth and phase margin decrease so there will be peaking in the frequency domain and in the transient response as shown in the typical performance curves. The photo of the small signal response with 200pF load shows 62% peaking. The large signal response shows the output slew rate being limited to 10V/μs by the short-circuit current. Coaxial cable can be driven directly, but for best pulse fidelity a resistor of value equal to the characteristic impedance of the cable (i.e., 75Ω) should be placed in series with the output. The other end of the cable should be terminated with the same value resistor to ground.

Circuit Operation

The LT1364/LT1365 circuit topology is a true voltage feedback amplifier that has the slewing behavior of a current feedback amplifier. The operation of the circuit can be understood by referring to the simplified schematic. The inputs are buffered by complementary NPN and PNP emitter followers which drive a 500Ω resistor. The input voltage appears across the resistor generating currents which are mirrored into the high impedance node. Complementary followers form an output stage which buffers the gain node from the load. The bandwidth is set by the input resistor and the capacitance on the high impedance node. The slew rate is determined by the current available to charge the gain node capacitance. This current is the differential input voltage divided by R1, so the slew rate is proportional to the input. Highest slew rates are therefore seen in the lowest gain configurations. For example, a 10V output step in a gain of 10 has only a 1V input step, whereas the same output step in unity gain has a 10 times greater input step. The curve of Slew Rate vs Input Level illustrates this relationship. The LT1364/LT1365 are tested for slew rate in a gain of –2 so higher slew rates can be expected in gains of 1 and –1, and lower slew rates in higher gain configurations.

The RC network across the output stage is bootstrapped when the amplifier is driving a light or moderate load and has no effect under normal operation. When driving a capacitive load (or a low value resistive load) the network is incompletely bootstrapped and adds to the compensation at the high impedance node. The added capacitance slows down the amplifier which improves the phase margin by moving the unity-gain frequency away from the pole formed by the output impedance and the capacitive load. The zero created by the RC combination adds phase to ensure that even for very large load capacitances, the total phase lag can never exceed 180 degrees (zero phase margin) and the amplifier remains stable.

Power Dissipation

The LT1364/LT1365 combine high speed and large output drive in small packages. Because of the wide supply voltage range, it is possible to exceed the maximum junction temperature under certain conditions. Maximum junction temperature (T_J) is calculated from the ambient temperature (T_A) and power dissipation (P_D) as follows:

LT1364CN8: $T_J = T_A + (P_D \times 130°C/W)$
LT1364CS8: $T_J = T_A + (P_D \times 190°C/W)$
LT1365CN: $T_J = T_A + (P_D \times 110°C/W)$
LT1365CS: $T_J = T_A + (P_D \times 150°C/W)$

Worst case power dissipation occurs at the maximum supply current and when the output voltage is at 1/2 of either supply voltage (or the maximum swing if less than 1/2 supply voltage). For each amplifier P_{DMAX} is:

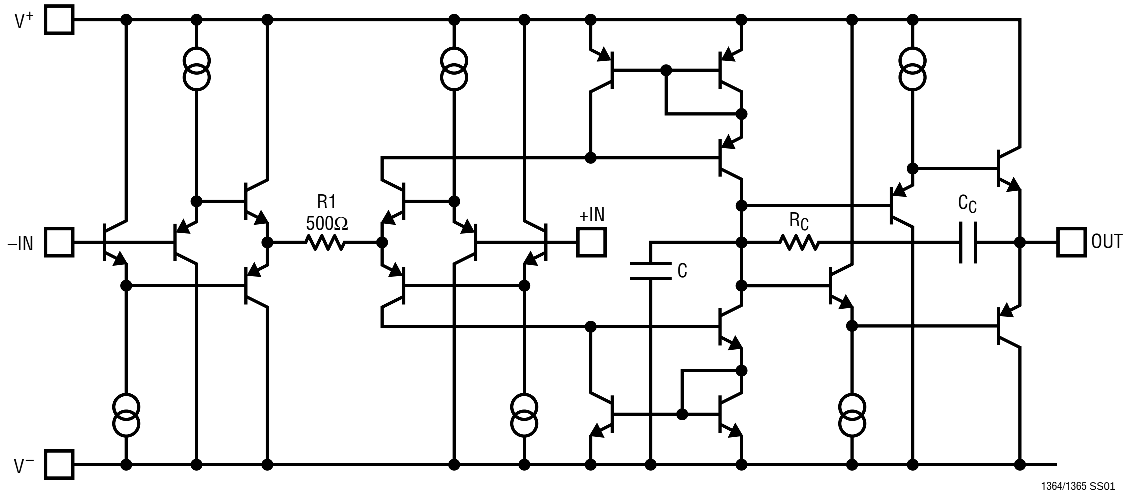
$$P_{DMAX} = (V^+ - V^-)(I_{SMAX}) + (V^+/2)^2/R_L$$

Example: LT1365 in S16 at 70°C, $V_S = \pm5V$, $R_L = 150W$

$$P_{DMAX} = (10V)(8.4mA) + (2.5V)^2/150\Omega = 126mW$$

$$T_{JMAX} = 70°C + (4 \times 126mW)(150°C/W) = 145°C$$

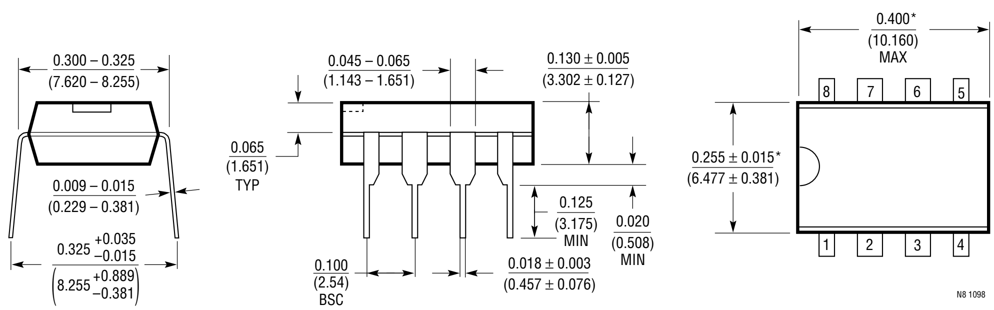
SIMPLIFIED SCHEMATIC



PACKAGE DESCRIPTION

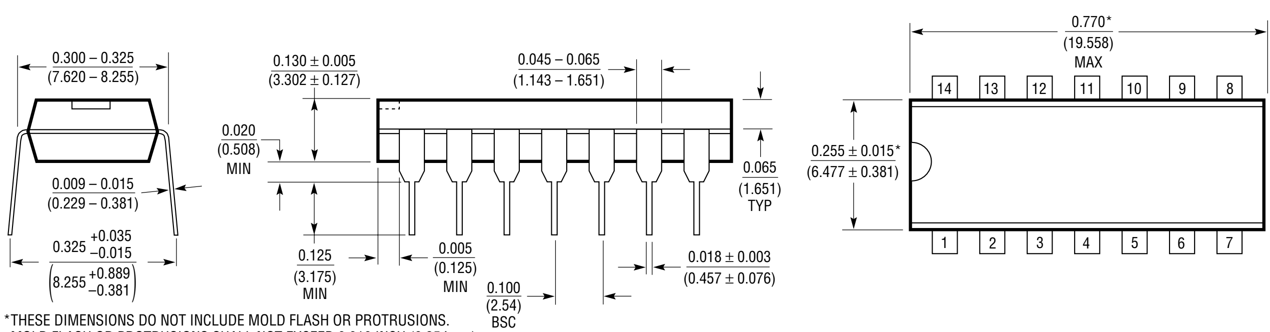
Dimension in inches (millimeters) unless otherwise noted.

N8 Package
8-Lead PDIP (Narrow 0.300)
(LTC DWG # 05-08-1510)



*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.010 INCH (0.254mm)

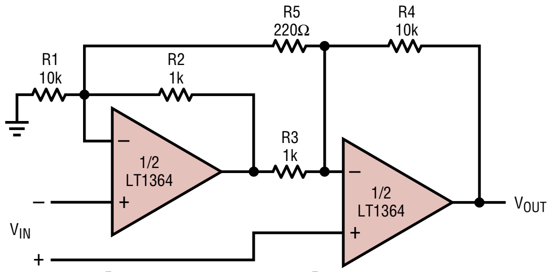
N Package
14-Lead PDIP (Narrow 0.300)
(LTC DWG # 05-08-1510)



*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.010 INCH (0.254mm)

TYPICAL APPLICATIONS

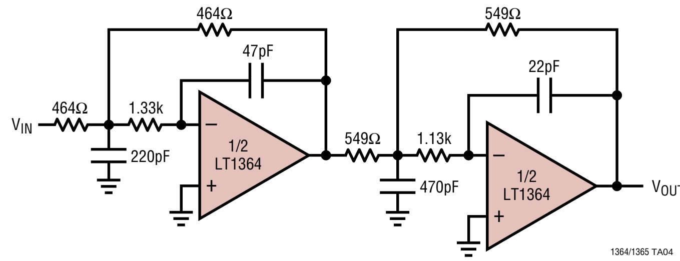
Two Op Amp Instrumentation Amplifier



$$GAIN = \left[\frac{R4}{R3}\right]\left[1 + \left(\frac{1}{2}\right)\left(\frac{R2}{R1} + \frac{R3}{R4}\right) + \frac{(R2 + R3)}{R5}\right] = 102$$

TRIM R5 FOR GAIN
TRIM R1 FOR COMMON-MODE REJECTION
BW = 700kHz

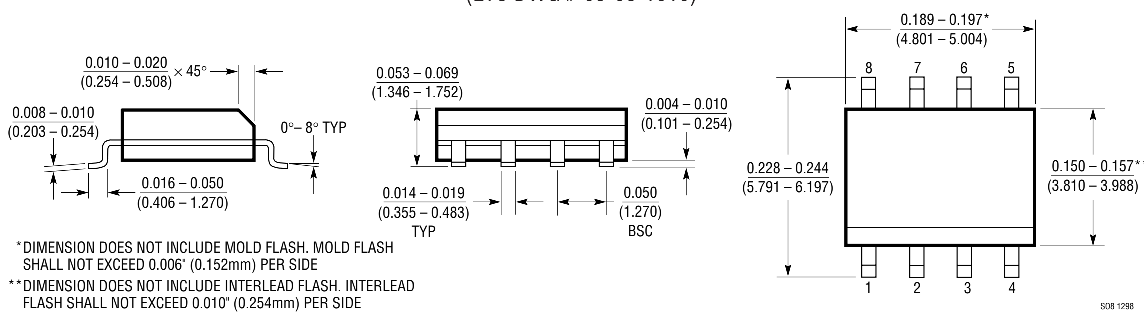
2MHz, 4th Order Butterworth Filter



PACKAGE DESCRIPTION

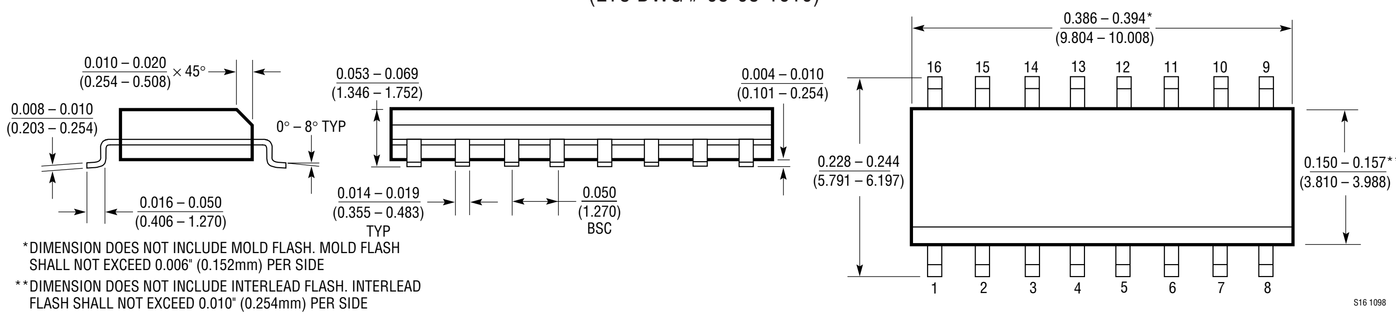
Dimension in inches (millimeters) unless otherwise noted.

S8 Package
8-Lead Plastic Small Outline (Narrow 0.150)
(LTC DWG # 05-08-1610)



*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE
**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

S Package
16-Lead Plastic Small Outline (Narrow 0.150)
(LTC DWG # 05-08-1610)



*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE
**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1363	70MHz, 1000V/µs Op Amp	Single Version of LT1364/LT1365
LT1361/LT1362	Dual and Quad 50MHz, 800V/µs Op Amps	Lower Power Version of LT1364/LT1365, V_{OS} = 1mV, 4mA/Amplifier
LT1358/LT1359	Dual and Quad 25MHz, 600V/µs Op Amps	Lower Power Version of LT1364/LT1365, V_{OS} = 0.6mV, 2mA/Amplifier
LT1813	Dual 100MHz, 700V/µs Op Amps	Low Voltage, Low Power LT1364/LT1365, 3mA/Amplifier

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