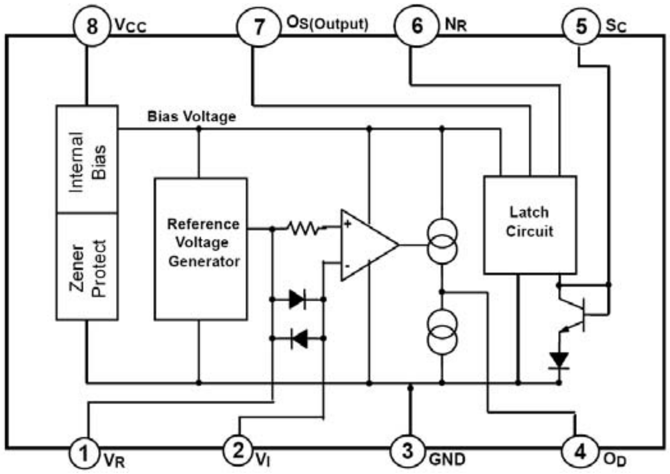


Figure 1. Block Diagram

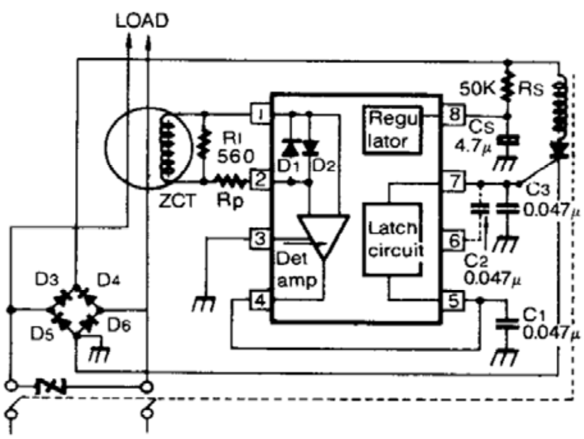


Figure 2. Full–Wave Application Circuit

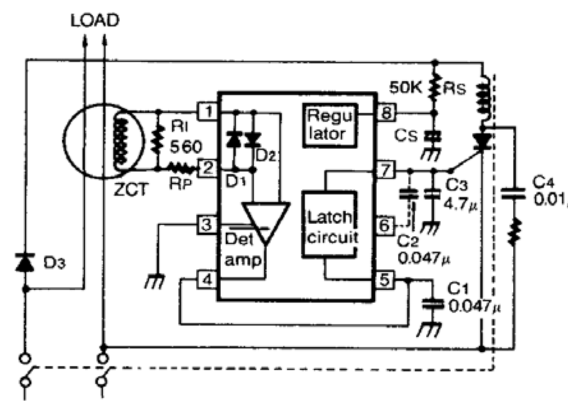


Figure 3. Half–Wave Application Circuit

Application Information

(Refer to full–wave application circuit in Figure 2)

Figure 2 shows the KA2803B connected in a typical leakage current detector system. The power is applied to the V_{CC} terminal (Pin 8) directly from the power line. The resistor R_S and capacitor C_S are chosen so that Pin 8 voltage is at least 12 V. The value of C_S is recommended above 1 μF.

If the leakage current is at the load, it is detected by the zero current transformer (ZCT). The output voltage signal of ZCT is amplified by the differential amplifier of the KA2803B internal circuit and appears as a half–cycle sine wave signal referred to input signal at the output of the amplifier. The amplifier closed–loop gain is fixed about 1000 times with internal feedback resistor to compensate for zero current transformer (ZCT) variations. The resistor R_L should be selected so that the breaker satisfies the required sensing current. The protection resistor R_P is not usually used when high current is injected at the breaker; this resistor should be used to protect the earth leakage detector IC (KA2803B). The range of R_P is from several hundred ∧ to several k∧.

Capacitor C_1 is for the noise canceller and a standard value of C_1 is 0.047 μF. Capacitor C2 is also a noise canceller capacitance, but it is not usually used.

When high noise is present, a 0.047 μF capacitor may be connected between Pins 6 and 7. The amplified signal finally appears at the Pin 7 with pulse signal through the internal latch circuit of the KA2803B. This signal drives the gate of the external SCR, which energizes the trip coil, which opens the circuit breaker. The trip time of the breaker is determined by capacitor C_3 and the mechanism breaker. This capacitor should be selected under 1 μF to satisfy the required trip time. The full–wave bridge supplies power to the KA2803B during both the positive and negative half cycles of the line voltage. This allows the hot and neutral lines to be interchanged.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply Voltage		20	V
I_{CC}	Supply Current		8	mA
P_D	Power Dissipation		300	mW
T_L	Lead Temperature, Soldering 10 Seconds		260	°C
T_A	Operation Temperature Range	−25	+80	°C
T_{STG}	Storage Temperature Range	−65	+150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

PACKAGE MARKING AND ORDERING INFORMATION

Part Number	Operating Temperature Range	Package	Packing Method
KA2803B	−25 to +80°C	8−Lead, Dual Inline Package (DIP)	Tube
KA2803BD	−25 to +80°C	8−Lead, Small Outline Package (SOP)	Tape and Reel

ELECTRICAL CHARACTERISTICS (T_A = −25°C to + 80°C unless otherwise noted)

Symbol	Parameter	Conditions		Test Circuit	Min.	Typ.	Max.	Units
I_{CC}	Supply Current 1	V_{CC} = 12V V_R = OPEN V_I = 2 V	T_A = −25°C	Figure 4			580	μA
			T_A = +25°C		300	400	530	
			T_A = +80°C				480	
V_T	Trip Voltage	V_{CC} = 16 V, V_R = 2 V~2.02 V, V_I = 2		Figure 5	14	16	18	mV (ms)
		Note 1			12.5	14.2	17.0	
$I_{O(D)}$	Differential Amplifier Current 1	V_{CC} = 16 V, V_R~V_I = 30 mV, V_{OD} = 1.2 V		Figure 7	−12	20	−30	μA
	Differential Amplifier Current 2	V_{CC} = 16 V, V_{OD} = 0.8 V,V_R, V_I Short = V_P		Figure 8	17	27	37	
I_O	Output Current	V_{SC} = 1.4 V, V_{OS} = 0.8 V, V_{CC} = 16.0 V	T_A= −25°C	Figure 9	200	400	800	μA
			T_A= +25°C		200	400	800	
			T_A= +80°C		100	300	600	
V_{SCON}	Latch−On Voltage	V_{CC} = 16 V		Figure 10	0.7	1.0	1.4	V
I_{SCON}	Latch Input Current	V_{CC} = 16 V		Figure 11	−13	−7	−1	μA
I_{OSL}	Output Low Current	V_{CC} = 12 V, V_{OSL} = 0.2 V		Figure 12	200	800	1400	μA
V_{IDC}	Differential Input Clamp Voltage	V_{CC} = 16 V, I_{DC} = 100 mA		Figure 13	0.4	1.2	2.0	V
V_{SM}	Maximum Current Voltage	I_{SM} = 7 mA		Figure 14	20	24	28	V
I_{S2}	Supply Current 2	V_{CC} = 12.0 V, V_{OSL} = 0.6 V		Figure 15	200	400	900	μA
V_{SOFF}	Latch−Off Supply Voltage	V_{OS} = 12.0 V		Figure 16	7	8	9	V
		V_{SC} = 1.8 V						
		I_{IDC} = 100.0 mA						
t_{ON}	Response Time	V_{CC} = 16 V, V_R−V_I = 0.3 V, 1 V<V_X<5 V		Figure 17	2	3	4	ms

1. Guaranteed by design, not tested in production.

TEST CIRCUITS

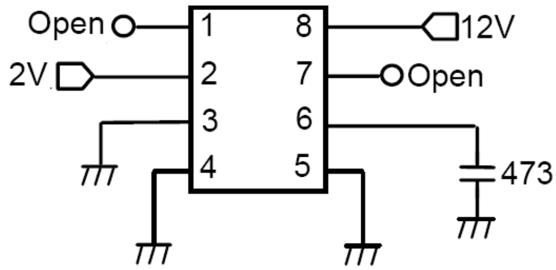


Figure 4. Supply Current 1

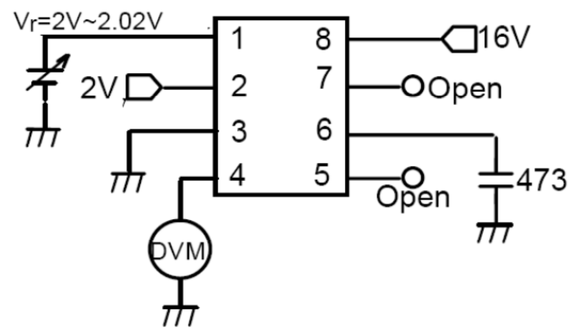
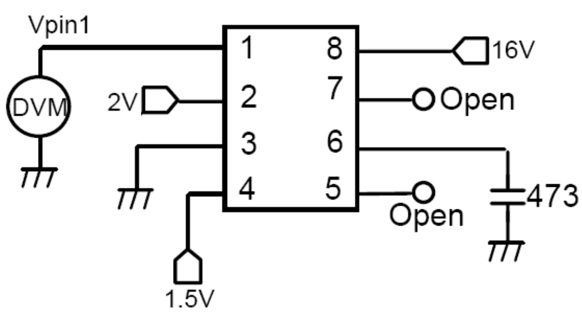


Figure 5. Trip Voltage



* V_p=Vpin1-0.03V

Figure 6. V_{PN1} for V_P Measurement

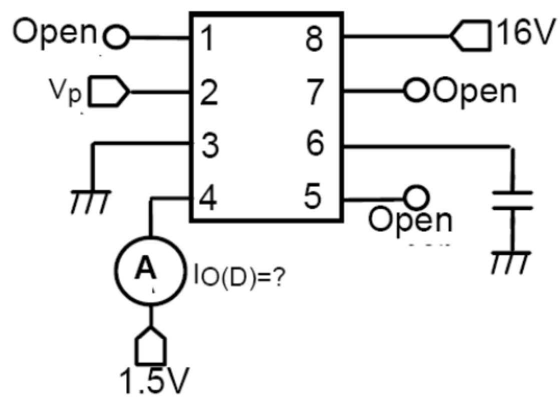


Figure 7. Differential Amplifier Output Current 1

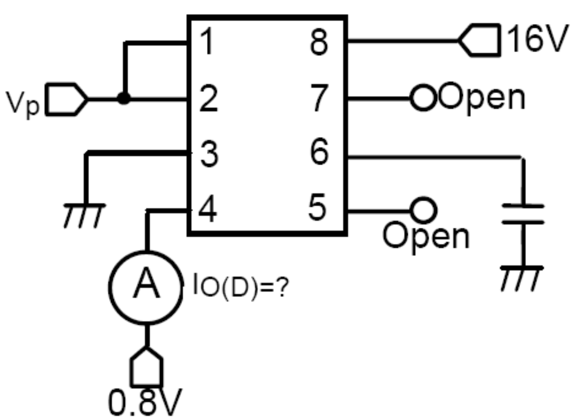


Figure 8. Differential Amplifier Output Current 2

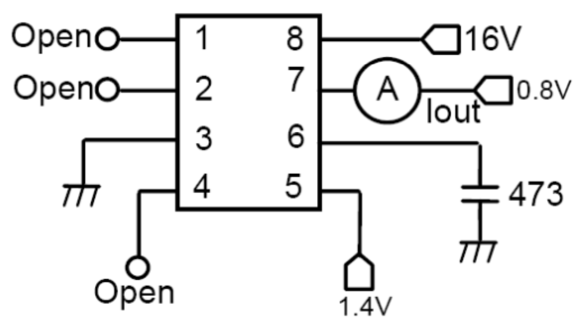


Figure 9. Output Current

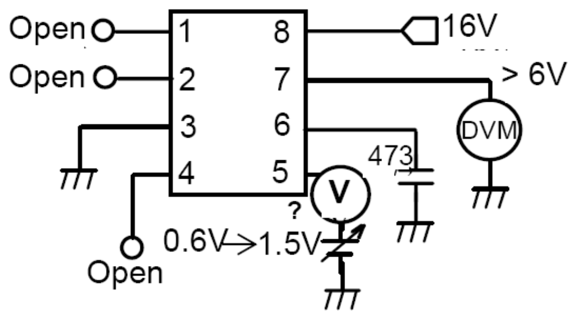


Figure 10. Latch−On Voltage

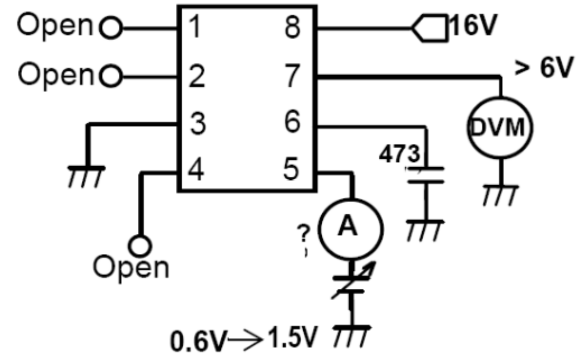


Figure 11. Latch Input Current

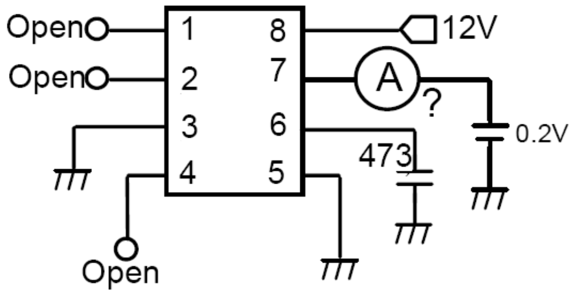


Figure 12. Output Low Current

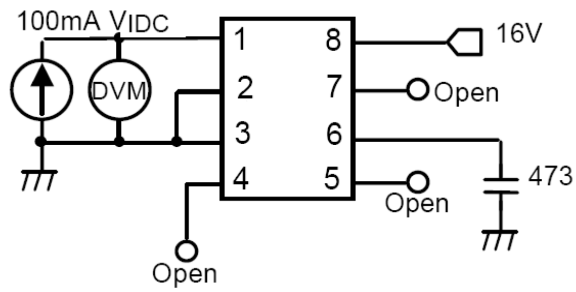


Figure 13. Differential Input Clamp Voltage

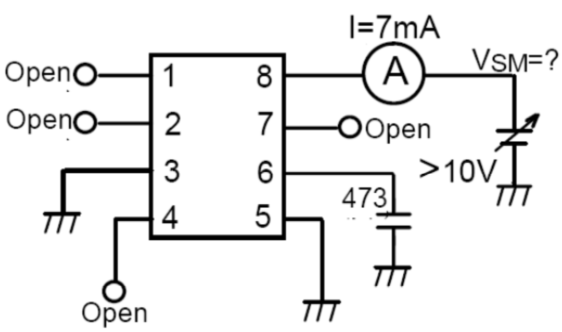


Figure 14. Maximum Current Voltage

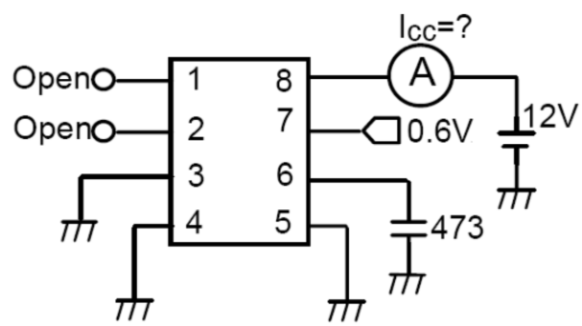


Figure 15. Supply Current 2

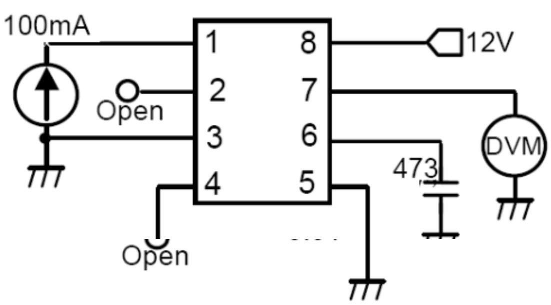


Figure 16. Latch−Off Supply Voltage

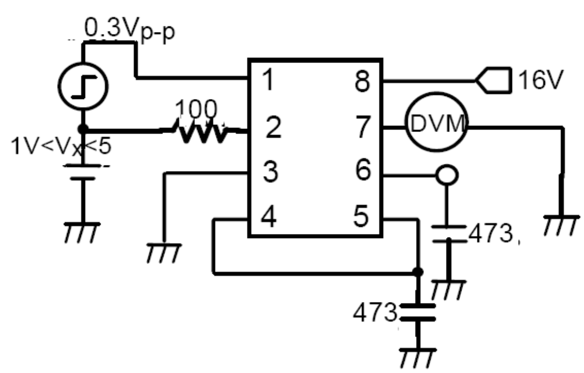


Figure 17. Response Time

TYPICAL PERFORMANCE CHARACTERISTICS

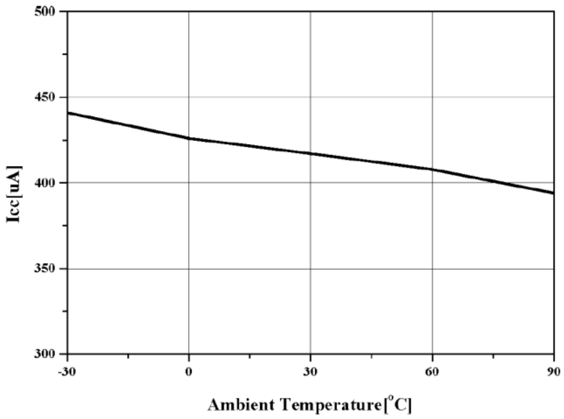


Figure 18. Supply Current

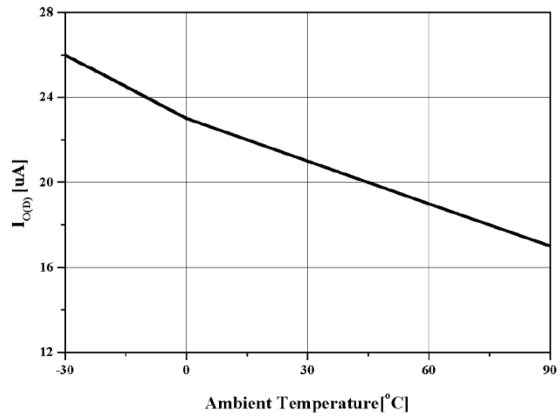


Figure 19. Differential Amplifier Output Current (V_R – V_I = 30 mV, V_{OD} = 1.2 V)

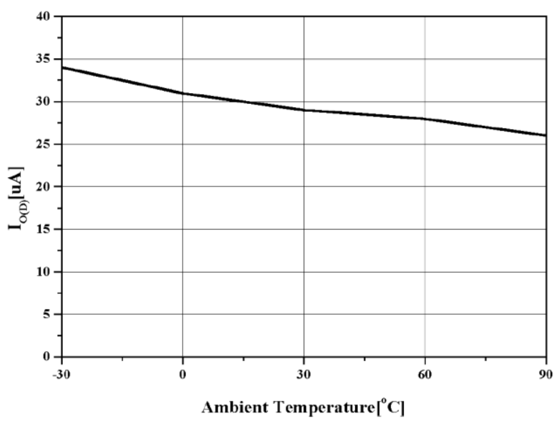


Figure 20. Differential Amplifier Output Current (V_R, V_I = V_P, V_{OD} = 0.8 V)

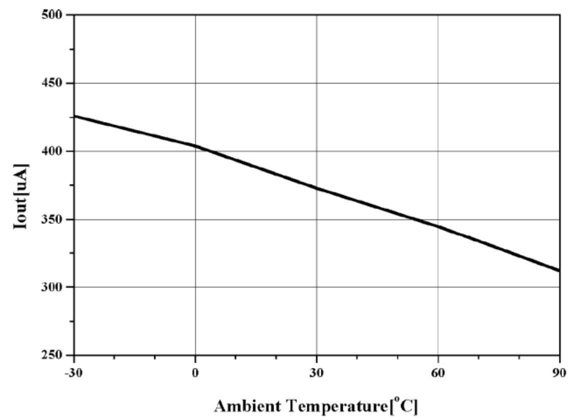


Figure 21. Output Current

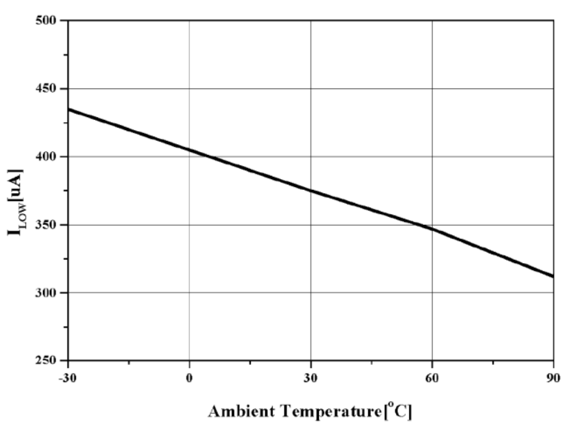


Figure 22. Output Low Current

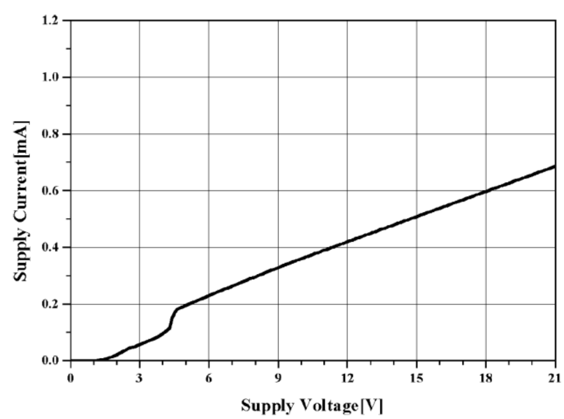


Figure 23. V_{CC} Voltage vs. Supply Current 1

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

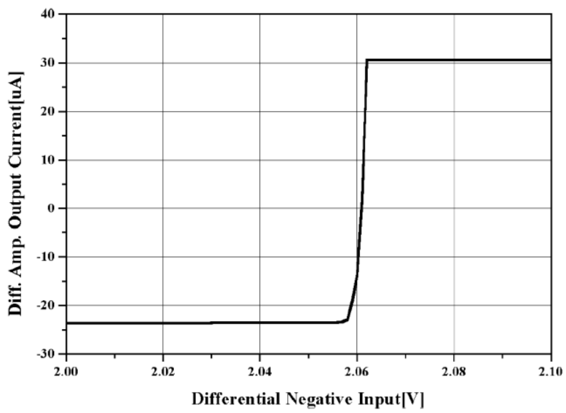


Figure 24. Differential Amplifier Output Current 1

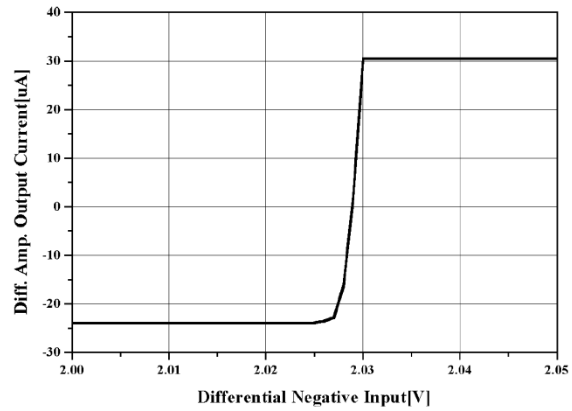


Figure 25. Differential Amplifier Output

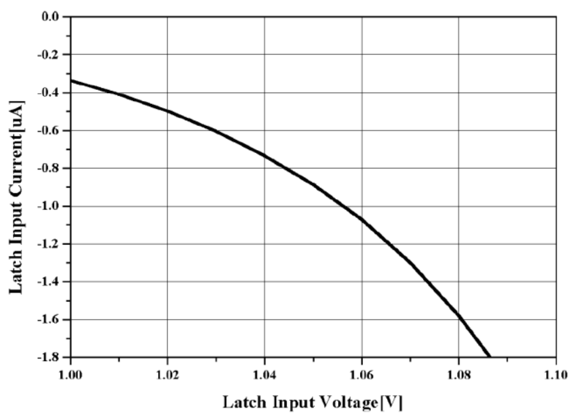


Figure 26. Latch Input Current

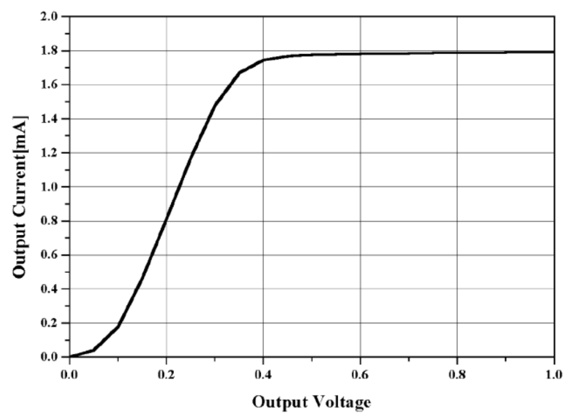


Figure 27. Output Low Current

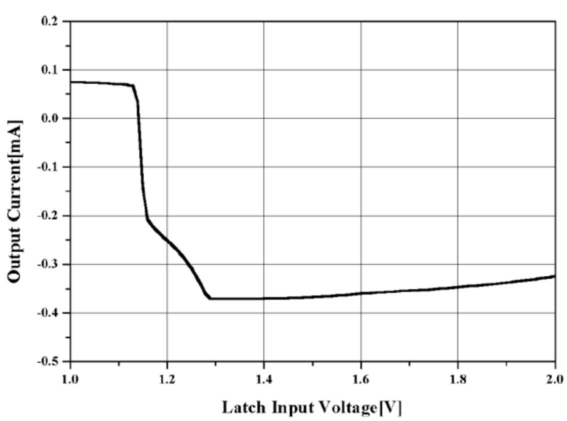


Figure 28. Output Current

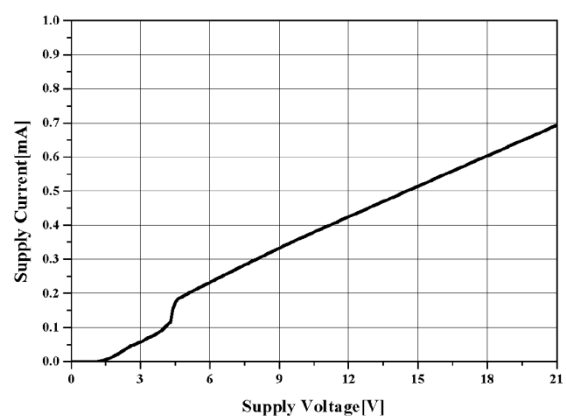


Figure 29. V_{CC} Voltage vs. Supply Current 2

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

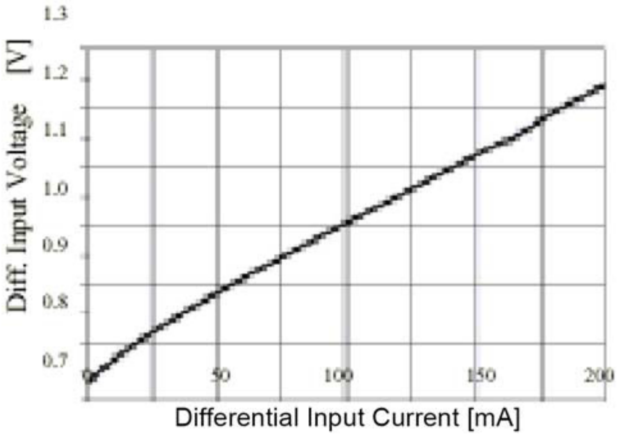


Figure 30. Differential Input Clamp Voltage

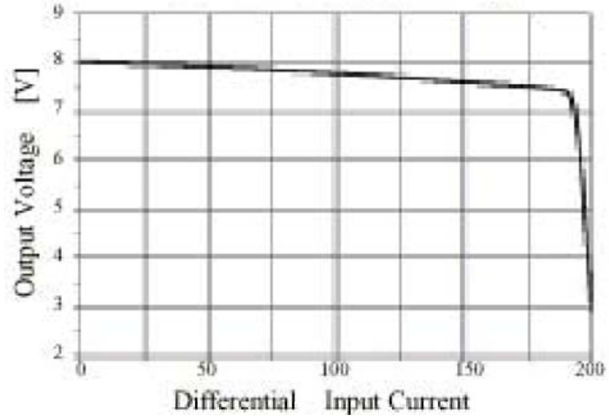


Figure 31. Latch−Off Supply Voltage

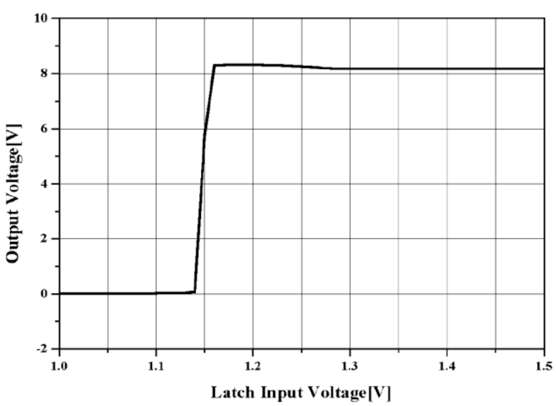


Figure 32. Latch−On Input Voltage

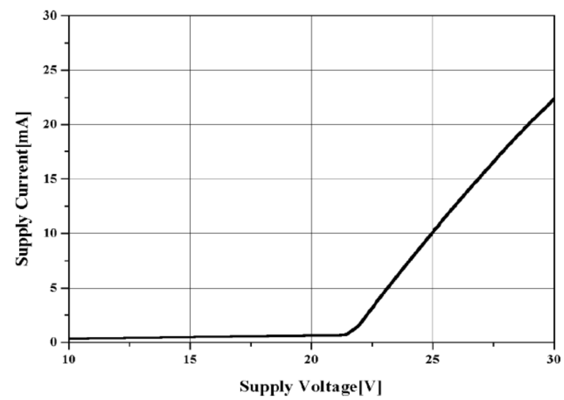


Figure 33. Maximum Supply

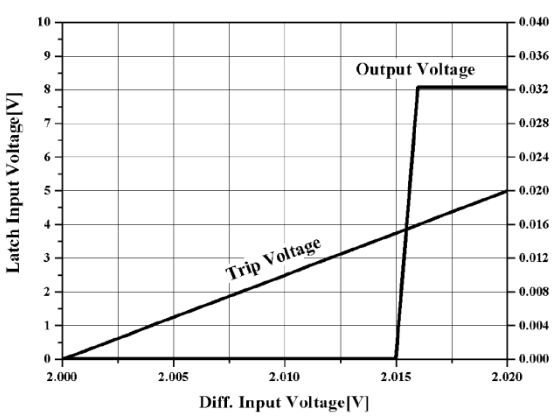


Figure 34. Trip and Output

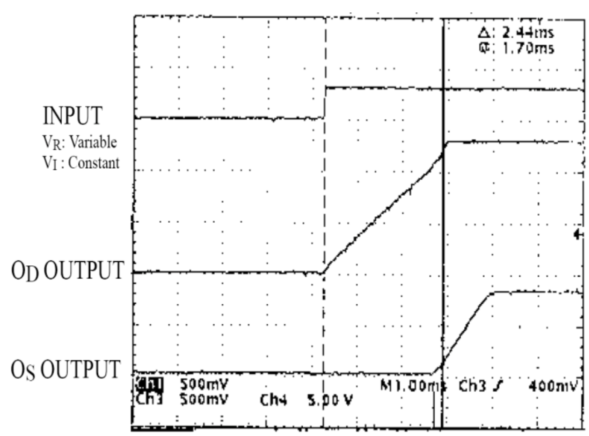
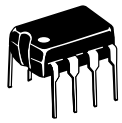


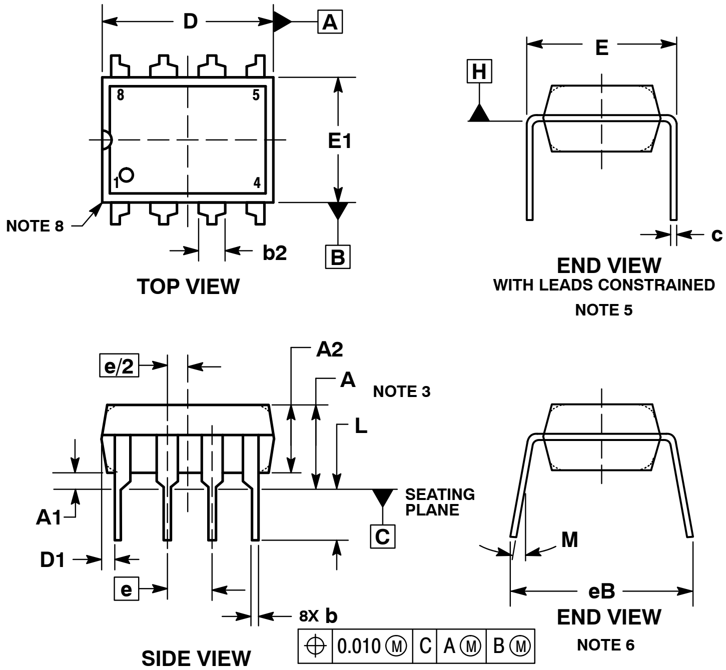
Figure 35. Output Response Time



SCALE 1:1

PDIP−8
CASE 626−05
ISSUE P

DATE 22 APR 2015

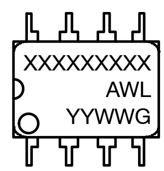


NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSIONS A, A1 AND L ARE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS−3.
4. DIMENSIONS D, D1 AND E1 DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS ARE NOT TO EXCEED 0.10 INCH.
5. DIMENSION E IS MEASURED AT A POINT 0.015 BELOW DATUM PLANE H WITH THE LEADS CONSTRAINED PERPENDICULAR TO DATUM C.
6. DIMENSION eB IS MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
7. DATUM PLANE H IS COINCIDENT WITH THE BOTTOM OF THE LEADS, WHERE THE LEADS EXIT THE BODY.
8. PACKAGE CONTOUR IS OPTIONAL (ROUNDED OR SQUARE CORNERS).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	----	0.210	---	5.33
A1	0.015	----	0.38	---
A2	0.115	0.195	2.92	4.95
b	0.014	0.022	0.35	0.56
b2	0.060 TYP		1.52 TYP	
C	0.008	0.014	0.20	0.36
D	0.355	0.400	9.02	10.16
D1	0.005	----	0.13	---
E	0.300	0.325	7.62	8.26
E1	0.240	0.280	6.10	7.11
e	0.100 BSC		2.54 BSC	
eB	----	0.430	---	10.92
L	0.115	0.150	2.92	3.81
M	----	10°	---	10°

STYLE 1:
PIN 1. AC IN
2. DC + IN
3. DC − IN
4. AC IN
5. GROUND
6. OUTPUT
7. AUXILIARY
8. V_{CC}

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

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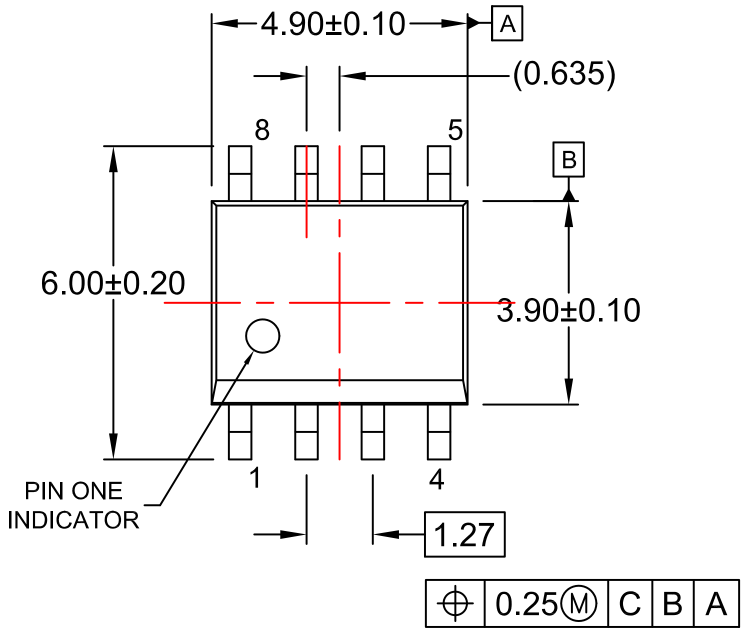
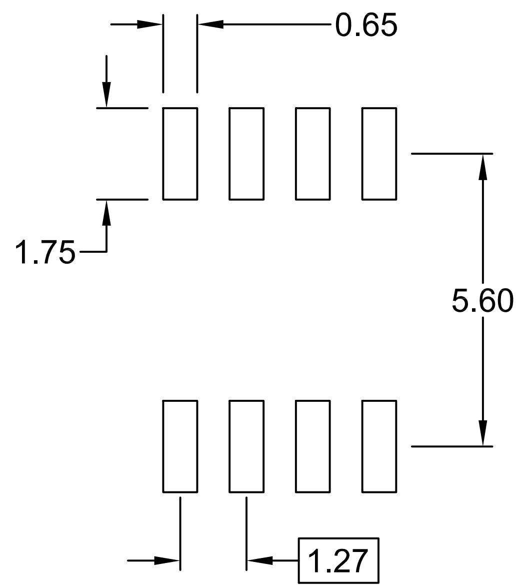
DESCRIPTION:	PDIP−8	PAGE 1 OF 1

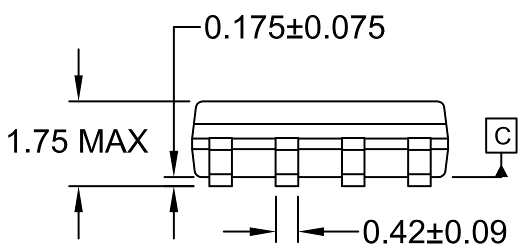
SOIC8
CASE 751EB
ISSUE A

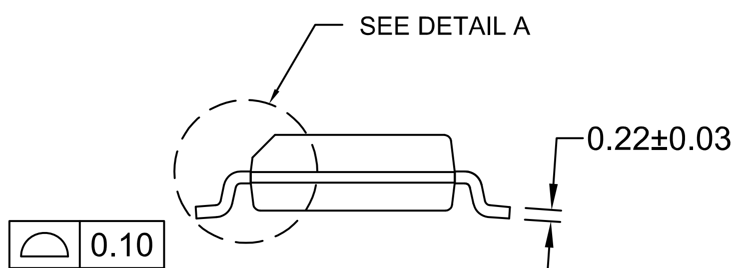
DATE 24 AUG 2017



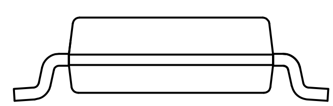


LAND PATTERN RECOMMENDATION

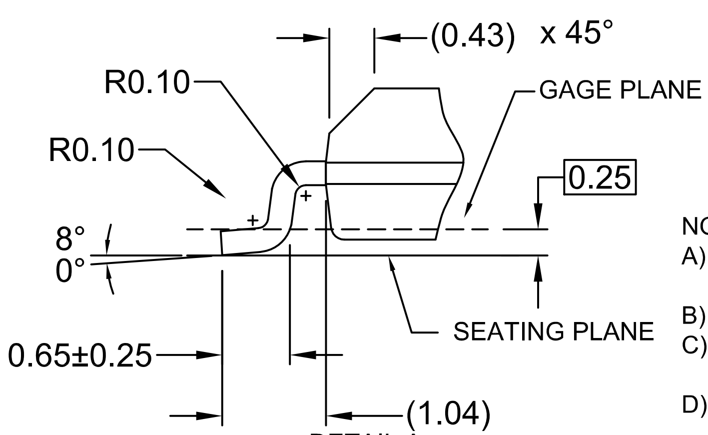




OPTION A - BEVEL EDGE



OPTION B - NO BEVEL EDGE



DETAIL A
SCALE: 2:1

NOTES:
A) THIS PACKAGE CONFORMS TO JEDEC MS-012, VARIATION AA.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.
D) LANDPATTERN STANDARD: SOIC127P600X175-8M

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PUBLICATION ORDERING INFORMATION

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Phone: 011 421 33 790 2910

Europe, Middle East and Africa Technical Support:
Phone: 00421 33 790 2910
For additional information, please contact your local Sales Representative

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