

Description (Continued)

found in each I/O cell. Each output has individual, programmable I/O tri-state control (OE), output latch clock (CLK), clock enable (CLKEN), and two multiplexer control (MUX0 and MUX1) inputs. Polarity for these signals is programmable for each I/O cell. The MUX0 and MUX1 inputs control a fast 4:1 MUX, allowing dynamic selection of up to four signal sources for a given output. A wider 16:1 MUX can be implemented with the MUX expander feature of each I/O and a propagation delay increase of 2.0ns. OE, CLK, CLKEN, and MUX0 and MUX1 inputs can be driven directly from selected sets of I/O pins. Optional dedicated clock input pins give minimum clock-to-output delays. CLK and CLKEN share the same set of I/O pins. CLKEN disables the register clock when CLKEN = 0.

Through in-system programming, connections between I/O pins and architectural features (latched or registered inputs or outputs, output enable control, etc.) can be defined. In keeping with its data path application focus, the ispGDXVA devices contain no programmable logic arrays. All input pins include Schmitt trigger buffers for noise immunity. These connections are programmed into the device using non-volatile E²CMOS technology. Non-volatile technology means the device configuration is saved even when the power is removed from the device.

In addition, there are no pin-to-pin routing constraints for 1:1 or 1:n signal routing. That is, *any* I/O pin configured as an input can drive one or more I/O pins configured as outputs.

The device pins also have the ability to set outputs to fixed HIGH or LOW logic levels (Jumper or DIP Switch mode). Device outputs are specified for 24mA sink and 12mA source current (at JEDEC LVTTTL levels) and can be tied together in parallel for greater drive. On the ispGDXVA, each I/O pin is individually programmable for 3.3V or 2.5V output levels as described later. Programmable output slew rate control can be defined independently for each I/O pin to reduce overall ground bounce and switching noise.

All I/O pins are equipped with IEEE1149.1-compliant Boundary Scan Test circuitry for enhanced testability. In addition, in-system programming is supported through the Test Access Port via a special set of private commands.

The ispGDXVA I/Os are designed to withstand “live insertion” system environments. The I/O buffers are disabled during power-up and power-down cycles. When designing for “live insertion,” absolute maximum rating conditions for the Vcc and I/O pins must still be met.

Table 1. ispGDXVA Family Members

	ispGDXV/VA Device		
	ispGDX80VA	ispGDX160V/VA	ispGDX240VA
I/O Pins	80	160	240
I/O-OE Inputs*	20	40	60
I/O-CLK / CLKEN Inputs*	20	40	60
I/O-MUXsel1 Inputs*	20	40	60
I/O-MUXsel2 Inputs*	20	40	60
Dedicated Clock Pins**	2	4	4
EPEN	1	1	1
TOE	1	1	1
BSCAN Interface	4	4	4
RESET	1	1	1
Pin Count/Package	100-Pin TQFP	208-Pin PQFP 208-Ball fpBGA 272-Ball BGA	388-Ball fpBGA

* The CLK/CLK_EN, OE, MUX0 and MUX1 terminals on each I/O cell can each be assigned to 25% of the I/Os.

** Global clock pins Y0, Y1, Y2 and Y3 are multiplexed with CLKEN0, CLKEN1, CLKEN2 and CLKEN3 respectively in all devices.

Architecture

The ispGDXVA architecture is different from traditional PLD architectures, in keeping with its unique application focus. The block diagram is shown below. The programmable interconnect consists of a single Global Routing Pool (GRP). Unlike ispLSI® devices, there are no programmable logic arrays on the device. Control signals for OEs, Clocks/Clock Enables and MUX Controls must come from designated sets of I/O pins. The polarity of these signals can be independently programmed in each I/O cell.

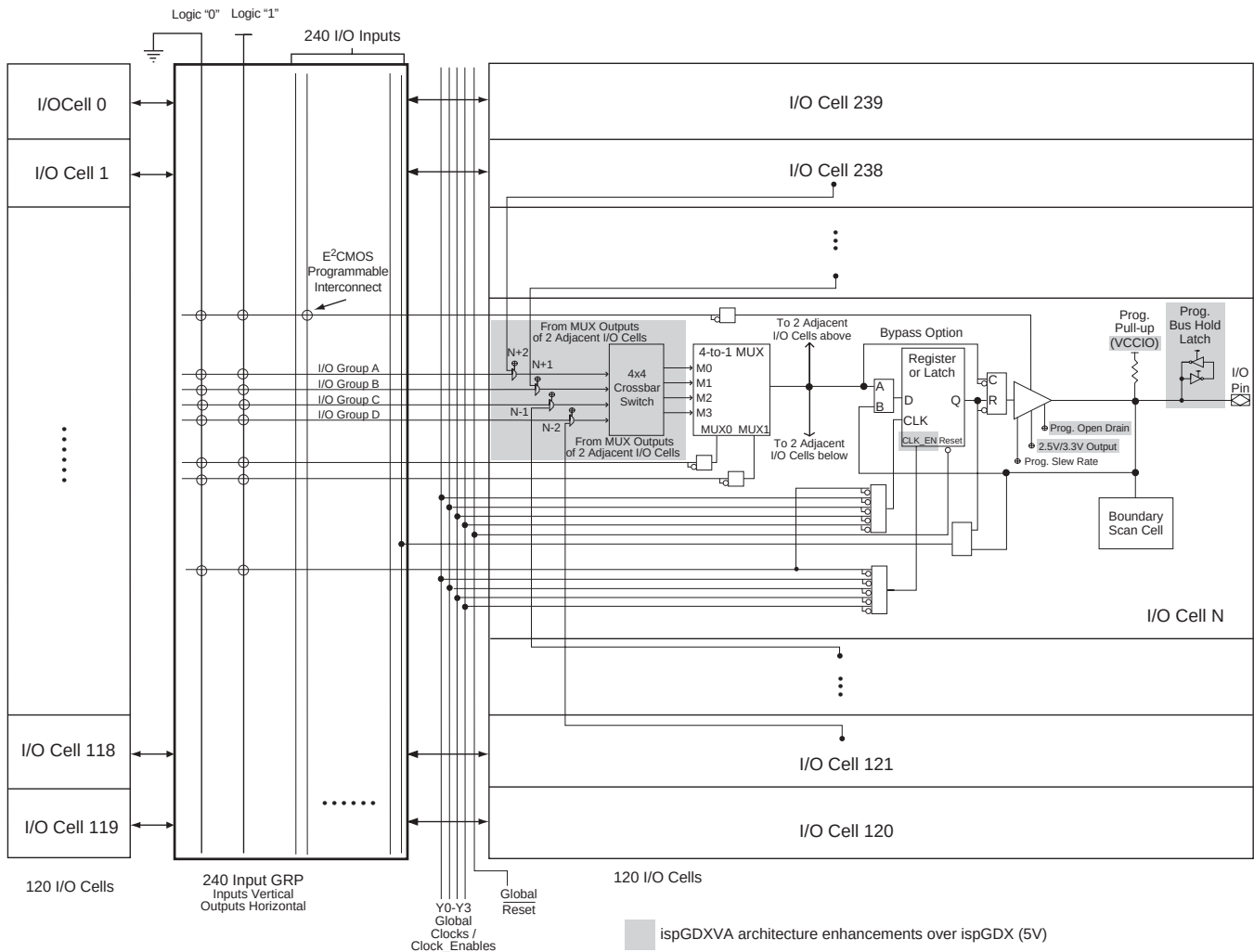
Each I/O cell drives a unique pin. The OE control for each I/O pin is independent and may be driven via the GRP by one of the designated I/O pins (I/O-OE set). The I/O-OE set consists of 25% of the total I/O pins. Boundary Scan test is supported by dedicated registers at each I/O pin. In-system programming is accomplished through the standard Boundary Scan protocol.

The various I/O pin sets are also shown in the block diagram below. The A, B, C, and D I/O pins are grouped together with one group per side.

I/O Architecture

Each I/O cell contains a 4:1 dynamic MUX controlled by two select lines as well as a 4x4 crossbar switch controlled by software for increased routing flexibility (Figure 1). The four data inputs to the MUX (called M0, M1, M2, and M3) come from I/O signals in the GRP and/or adjacent I/O cells. Each MUX data input can access one quarter of the total I/Os. For example, in a 240-I/O ispGDXVA, each data input can connect to one of 60 I/O pins. MUX0 and MUX1 can be driven by designated I/O pins called MUXsel1 and MUXsel2. Each MUXsel input covers 25% of the total I/O pins (e.g. 60 out of 240). MUX0 and MUX1 can be driven from either MUXsel1 or MUXsel2.

Figure 1. ispGDXVA I/O Cell and GRP Detail (240 I/O Device)



I/O MUX Operation

MUX1	MUX0	Data Input Selected
0	0	M0
0	1	M1
1	1	M2
1	0	M3

Flexible mapping of MUXsel_x to MUX_x allows the user to change the MUX select assignment after the ispGDXVA device has been soldered to the board. Figure 1 shows that the I/O cell can accept (by programming the appropriate fuses) inputs from the MUX outputs of four adjacent I/O cells, two above and two below. This enables cascading of the MUXes to enable wider (up to 16:1) MUX implementations.

The I/O cell also includes a programmable flow-through latch or register that can be placed in the input or output path and bypassed for combinatorial outputs. As shown in Figure 1, when the input control MUX of the register/latch selects the “A” path, the register/latch gets its inputs from the 4:1 MUX and drives the I/O output. When selecting the “B” path, the register/latch is directly driven by the I/O input while its output feeds the GRP. The programmable polarity Clock to the latch or register can be connected to any I/O in the I/O-CLK/CLKEN set (one-quarter of total I/Os) or to one of the dedicated clock input pins (Y_x). The programmable polarity Clock Enable input to the register can be programmed to connect to any of the I/O-CLK/CLKEN input pin set or to the global clock enable inputs (CLKEN_x). Use of the dedicated clock inputs gives minimum clock-to-output delays and minimizes delay variation with fanout. Combinatorial output mode may be implemented by a dedicated architecture bit and bypass MUX. I/O cell output polarity can be programmed as active high or active low.

MUX Expander Using Adjacent I/O Cells

The ispGDXVA allows adjacent I/O cell MUXes to be cascaded to form wider input MUXes (up to 16 x 1) without incurring an additional full Tpd penalty. However, there are certain dependencies on the locality of the adjacent MUXes when used along with direct MUX inputs.

Adjacent I/O Cells

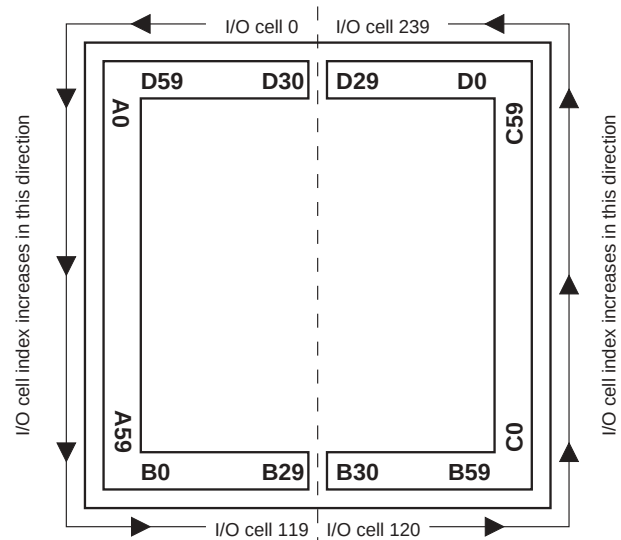
Expansion inputs MUXOUT[n-2], MUXOUT[n-1], MUXOUT[n+1], and MUXOUT[n+2] are fuse-selectable for each I/O cell MUX. These expansion inputs share the same path as the standard A, B, C and D MUX inputs, and

allow adjacent I/O cell outputs to be directly connected without passing through the global routing pool. The relationship between the [N+i] adjacent cells and A, B, C and D inputs will vary depending on where the I/O cell is located on the physical die. The I/O cells can be grouped into “normal” and “reflected” I/O cells or I/O “hemispheres.” These are defined as:

Device	Normal I/O Cells	Reflected I/O Cells
ispGDX80VA	TBA	TBA
ispGDX160V/VA	B19-B0, A39-A20, A19-A0, D39-D20	B20-B39, C0-C19, C20-C39, D0-D19
ispGDX240VA	TBA	TBA

Table 2 shows the relationship between adjacent I/O cells as well as their relationship to direct MUX inputs. Note that the MUX expansion is circular and that I/O cell B30, for example, draws on I/Os B29 and B28, as well as B31 and B32, even though they are in different hemispheres of the physical die. Table 2 shows some typical cases and all boundary cases. All other cells can be extrapolated from the pattern shown in the table.

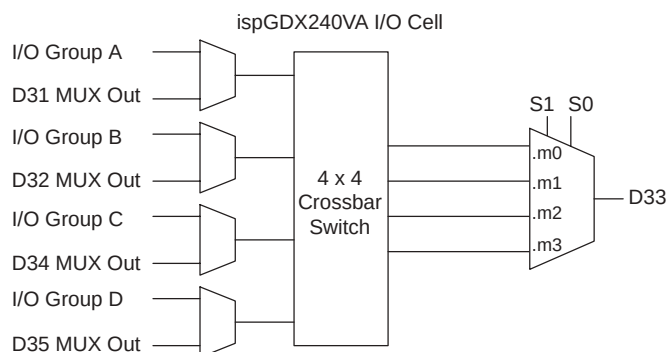
Figure 2. I/O Hemisphere Configuration of ispGDX240VA



Direct and Expander Input Routing

Table 2 also illustrates the routing of MUX direct inputs that are accessible when using adjacent I/O cells as inputs. Take I/O cell D33 as an example, which is also shown in Figure 3.

Figure 3. Adjacent I/O Cells vs. Direct Input Path for ispGD_X240VA, I/O D33



It can be seen from Figure 3 that if the D31 adjacent I/O cell is used, the I/O group “A” input is no longer available as a direct MUX input.

The ispGD_XVA can implement MUXes up to 16 bits wide in a single level of logic, but care must be taken when combining adjacent I/O cell outputs with direct MUX inputs. Any particular combination of adjacent I/O cells as MUX inputs will dictate what I/O groups (A, B, C or D) can be routed to the remaining inputs. By properly choosing the adjacent I/O cells, all of the MUX inputs can be utilized.

Table 2. Adjacent I/O Cells (Mapping of ispGD_X240VA)

		Data A/ MUXOUT	Data B/ MUXOUT	Data C/ MUXOUT	Data D/ MUXOUT
Reflected I/O Cells	B30	B32	B31	B29	B28
	B31	B33	B32	B30	B29
	B32	B34	B33	B31	B30
	B33	B35	B34	B32	B31
	D26	D28	D27	D25	D24
	D27	D29	D28	D26	D25
	D28	D30	D29	D27	D26
	D29	D31	D30	D28	D27
Normal I/O Cells	D30	D28	D29	D31	D32
	D31	D29	D30	D32	D33
	D32	D30	D31	D33	D34
	D33	D31	D32	D34	D35
	B26	B24	B25	B27	B28
	B27	B25	B26	B28	B29
	B28	B26	B27	B29	B30
	B29	B27	B28	B30	B31

Special Features

Slew Rate Control

All output buffers contain a programmable slew rate control that provides software-selectable slew rate options.

Open Drain Control

All output buffers provide a programmable Open-Drain option which allows the user to drive system level reset, interrupt and enable/disable lines directly without the need for an off-chip Open-Drain or Open-Collector buffer. Wire-OR logic functions can be performed at the printed circuit board level.

Pull-up Resistor

All pins have a programmable active pull-up. A typical resistor value for the pull-up ranges from 50kΩ to 80kΩ.

Output Latch (Bus Hold)

All pins have a programmable circuit that weakly holds the previously driven state when all drivers connected to the pin (including the pin's output driver as well as any other devices connected to the pin by external bus) are tristated.

User-Programmable I/Os

The ispGD_X240VA features user-programmable I/Os supporting either 3.3V or 2.5V output voltage level options. The ispGD_X240VA uses a VCCIO pin to provide the 2.5V reference voltage when used.

PCI Compatible Drive Capability

The ispGD_X240VA supports PCI compatible drive capability for all I/Os.

Applications

The ispGDXVA Family architecture has been developed to deliver an in-system programmable signal routing solution with high speed and high flexibility. The devices are targeted for three similar but distinct classes of end-system applications:

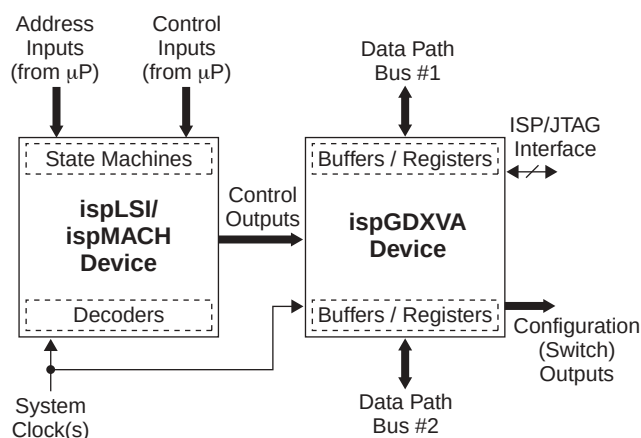
Programmable, Random Signal Interconnect (PRSI)

This class includes PCB-level programmable signal routing and may be used to provide arbitrary signal swapping between chips. It opens up the possibilities of programmable system hardware. It is characterized by the need to provide a large number of 1:1 pin connections which are statically configured, i.e., the pin-to-pin paths do not need to change dynamically in response to control inputs.

Programmable Data Path (PDP)

This application area includes system data path transceiver, MUX and latch functions. With today's 32- and 64-bit microprocessor buses, but standard data path glue components still relegated primarily to eight bits, PCBs are frequently crammed with a dozen or more data path glue chips that use valuable real estate. Many of these applications consist of "on-board" bus and memory interfaces that do not require the very high drive of standard glue functions but can benefit from higher integration. Therefore, there is a need for a flexible means to integrate these on-board data path functions in an analogous way to programmable logic's solution to control logic integration. Lattice's CPLDs make an ideal control logic complement to the ispGDXVA in-system programmable data path devices as shown below.

Figure 4. ispGDXVA Complements Lattice CPLDs



Programmable Switch Replacement (PSR)

Includes solid-state replacement and integration of mechanical DIP Switch and jumper functions. Through in-system programming, pins of the ispGDXVA devices can be driven to HIGH or LOW logic levels to emulate the traditional device outputs. PSR functions do not require any input pin connections.

These applications actually require somewhat different silicon features. PRSI functions require that the device support arbitrary signal routing on-chip between any two pins with no routing restrictions. The routing connections are static (determined at programming time) and each input-to-output path operates independently. As a result, there is little need for dynamic signal controls (OE, clocks, etc.). Because the ispGDXVA device will interface with control logic outputs from other components (such as ispLSI or ispMACH™) on the board (which frequently change late in the design process as control logic is finalized), there must be no restrictions on pin-to-pin signal routing for this type of application.

PDP functions, on the other hand, require the ability to dynamically switch signal routing (MUXing) as well as latch and tri-state output signals. As a result, the programmable interconnect is used to define *possible* signal routes that are then selected dynamically by control signals from an external MPU or control logic. These functions are usually formulated early in the conceptual design of a product. The data path requirements are driven by the microprocessor, bus and memory architecture defined for the system. This part of the design is the earliest portion of the system design frozen, and will not usually change late in the design because the result would be total system and PCB redesign. As a result, the ability to accommodate *arbitrary* any pin-to-any pin re-routing is not a strong requirement as long as the designer has the ability to define his functions with a reasonable degree of freedom initially.

As a result, the ispGDXVA architecture has been defined to support PSR and PRSI applications (including bidirectional paths) with no restrictions, while PDP applications (using dynamic MUXing) are supported with a minimal number of restrictions as described below. In this way, speed and cost can be optimized and the devices can still support the system designer's needs.

The following diagrams illustrate several ispGDXVA applications.

Applications (Continued)

Figure 5. Address Demultiplex/Data Buffering

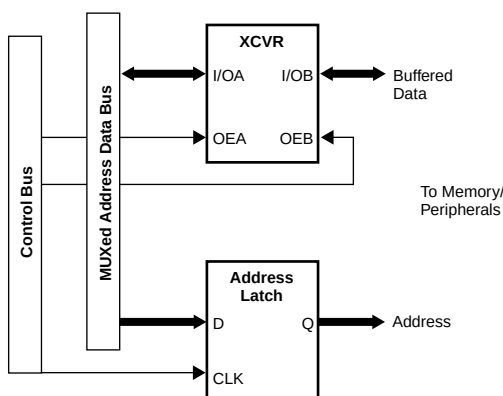


Figure 6. Data Bus Byte Swapper

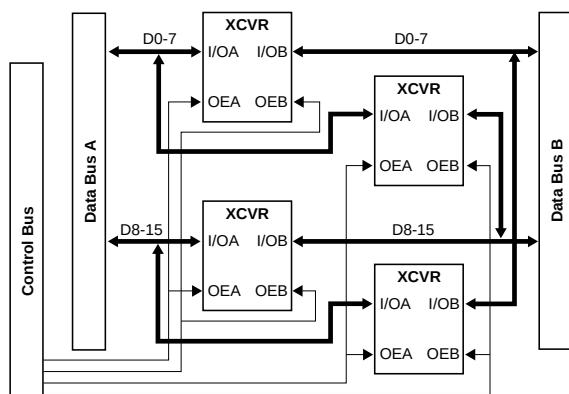
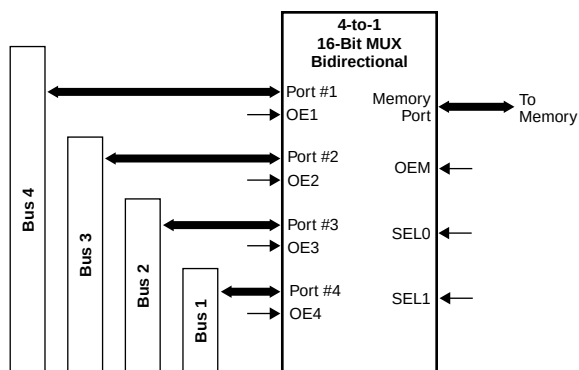


Figure 7. Four-Port Memory Interface



Note: All OE and SEL lines driven by external arbiter logic (not shown).

Designing with the ispGDXVA

As mentioned earlier, this architecture satisfies the PRSI class of applications without restrictions: any I/O pin as a single input or bidirectional can drive any other I/O pin as output.

For the case of PDP applications, the designer does have to take into consideration the limitations on pins that can be used as control (MUX0, MUX1, OE, CLK) or data (MUXA-D) inputs. The restrictions on control inputs are not likely to cause any major design issues because the input possibilities span 25% of the total pins.

The MUXA-D input partitioning requires that designers consciously assign pinouts so that MUX inputs are in the appropriate, disjoint groups. For example, since the MUXA group includes I/O A0-39 (240 I/O device), it is not possible to use I/O A0 and I/O A9 in the same MUX function. As previously discussed, data path functions will be assigned early in the design process and these restrictions are reasonable in order to optimize speed and cost.

User Electronic Signature

The ispGDXVA Family includes dedicated User Electronic Signature (UES) E²CMOS storage to allow users to code design-specific information into the devices to identify particular manufacturing dates, code revisions, or the like. The UES information is accessible through the boundary scan programming port via a specific command. This information can be read even when the security cell is programmed.

Security

The ispGDXVA Family includes a security feature that prevents reading the device program once set. Even when set, it does not inhibit reading the UES or device ID code. It can be erased only via a device bulk erase.

Absolute Maximum Ratings ^{1,2}

Supply Voltage V_{CC} -0.5 to +5.4V
 Input Voltage Applied -0.5 to +5.6V
 Off-State Output Voltage Applied -0.5 to +5.6V
 Storage Temperature -65 to 150°C
 Case Temp. with Power Applied -55 to 125°C
 Max. Junction Temp. (T_J) with Power Applied ... 150°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).
2. Compliance with the Thermal Management section of the Lattice Semiconductor Data Book or CD-ROM is a requirement.

DC Recommended Operating Conditions

SYMBOL	PARAMETER		MIN.	MAX.	UNITS
V _{CC}	Supply Voltage	Commercial T _A = 0°C to +70°C	3.00	3.60	V
		Industrial T _A = -40°C to +85°C	3.00	3.60	V
V _{CCIO}	I/O Reference Voltage		2.3	3.60	V

Table 2-0005/gdxva

Capacitance ($T_A = 25^\circ\text{C}$, $f = 1.0\text{ MHz}$)

SYMBOL	PARAMETER	PACKAGE TYPE	TYPICAL	UNITS	TEST CONDITIONS
C_1	I/O Capacitance	TQFP	7	pf	$V_{CC} = 3.3\text{V}$, $V_{I/O} = 2.0\text{V}$
C_2	Dedicated Clock Capacitance	TQFP	8	pf	$V_{CC} = 3.3\text{V}$, $V_Y = 2.0\text{V}$

Table 2-0006/gdxva

Erase/Reprogram Specifications

PARAMETER	MINIMUM	MAXIMUM	UNITS
Erase/Reprogram Cycles	10,000	—	Cycles

Switching Test Conditions

Input Pulse Levels	GND to VCCIO(MIN)
Input Rise and Fall Time	$\leq 1.5\text{ns}$ 10% to 90%
Input Timing Reference Levels	VCCIO(MIN)/2
Output Timing Reference Levels	VCCIO(MIN)/2
Output Load	See Figure 8

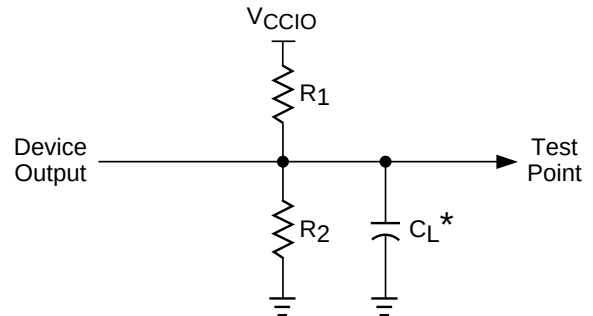
3-state levels are measured 0.5V from steady-state active level.

Output Load Conditions (See Figure 8)

		3.3V		2.5V		
TEST CONDITION		R1	R2	R1	R2	CL
A		153Ω	134Ω	156Ω	144Ω	35pF
B	Active High	∞	134Ω	∞	144Ω	35pF
	Active Low	153Ω	∞	156Ω	∞	35pF
C	Active High to Z at V _{OH} -0.5V	∞	134Ω	∞	144Ω	5pF
	Active Low to Z at V _{OL} +0.5V	153Ω	∞	156Ω	∞	5pF
D	Slow Slew	∞	∞	∞	∞	35pF

Table 2-0004A/gdxva

Figure 8. Test Load



*C_L includes Test Fixture and Probe Capacitance.

0213D

DC Electrical Characteristics for 3.3V Range

Over Recommended Operating Conditions

SYMBOL	PARAMETER	CONDITION	MIN.	TYP. ¹	MAX.	UNITS
VCCIO	I/O Reference Voltage	—	3.0	—	3.6	V
VIL	Input Low Voltage	V _{OH} ≤ V _{OUT} or V _{OUT} ≤ V _{OL} (MAX)	-0.3	—	0.8	V
VIH	Input High Voltage	V _{OH} ≤ V _{OUT} or V _{OUT} ≤ V _{OL} (MAX)	2.0	—	5.25	V
VOL	Output Low Voltage	V _{CC} = V _{CC} (MIN)	I _{OL} = +100μA	—	0.2	V
			I _{OL} = +24mA	—	0.55	V
VOH	Output High Voltage	V _{CC} = V _{CC} (MIN)	I _{OH} = -100μA	—	—	V
			I _{OH} = -12mA	—	—	V

1. Typical values are at V_{CC} = 3.3V and T_A = 25°C.

Table 2-0007/gdxva

DC Electrical Characteristics for 2.5V Range

Over Recommended Operating Conditions

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNITS
V _{CCIO}	I/O Reference Voltage	—	2.3	—	2.7	V
V _{IL}	Input Low Voltage	$V_{OH(MIN)} \leq V_{OUT}$ or $V_{OUT} \leq V_{OL(MAX)}$	-0.3	—	0.7	V
V _{IH}	Input High Voltage	$V_{OH(MIN)} \leq V_{OUT}$ or $V_{OUT} \leq V_{OL(MAX)}$	1.7	—	5.25	V
V _{OL}	Output Low Voltage	V _{CCIO} =MIN, I _{OL} = 100μA	—	—	0.2	V
		V _{CCIO} =MIN, I _{OL} = 8mA	—	—	0.6	V
V _{OH}	Output High Voltage	V _{CCIO} =MIN, I _{OH} = -100μA	2.1	—	—	V
		V _{CCIO} =MIN, I _{OH} = -8mA	1.8	—	—	V

2.5V/gdxva

DC Electrical Characteristics

Over Recommended Operating Conditions

SYMBOL	PARAMETER	CONDITION	MIN.	TYP. ²	MAX.	UNITS
I _{IL}	Input or I/O Low Leakage Current	$0V \leq V_{IN} \leq V_{IL(MAX)}$	—	—	-10	μA
I _{IH}	Input or I/O High Leakage Current	$(V_{CCIO}-0.2) \leq V_{IN} \leq V_{CCIO}$	—	—	10	μA
		$V_{CCIO} \leq V_{IN} \leq 5.25V$	—	—	50	μA
I _{PU}	I/O Active Pullup Current	$0V \leq V_{IN} \leq V_{IL(MAX)}$	—	—	-200	μA
I _{BHLS}	Bus Hold Low Sustaining Current	$V_{IN} = V_{IL(MAX)}$	40	—	—	μA
I _{BHHS}	Bus Hold High Sustaining Current	$V_{IN} = V_{IH(MIN)}$	-40	—	—	μA
I _{BHLO}	Bus Hold Low Overdrive Current	$0V \leq V_{IN} \leq V_{CCIO}$	—	—	550	μA
I _{BHHO}	Bus Hold High Overdrive Current	$0V \leq V_{IN} \leq V_{CCIO}$	—	—	-550	μA
I _{BHT}	Bus Hold Trip Points		V _{IL}	—	V _{IH}	V
I _{OS} ¹	Output Short Circuit Current	V _{CC} = 3.3V, V _{OUT} = 0.5V, T _A = 25°C	—	—	-250	mA
I _{CCQ} ⁴	Quiescent Power Supply Current	V _{IL} = 0.5V, V _{IH} = V _{CC}	—	20	—	mA
I _{CC}	Dynamic Power Supply Current per Input Switching	One input toggling at 50% duty cycle, outputs open.	—	See Note 3	—	mA/MHz
I _{CONT} ⁵	Maximum Continuous I/O Pin Sink Current Through Any GND Pin	—	—	—	135	mA

DC Char_gdxva

- One output at a time for a maximum of one second. V_{OUT} = 0.5V was selected to avoid test problems by tester ground degradation. Characterized, but not 100% tested.
- Typical values are at V_{CC} = 3.3V and T_A = 25°C.
- I_{CC} / MHz = (0.0025 x I/O cell fanout) + 0.042.
e.g. An input driving four I/O cells at 40MHz results in a dynamic I_{CC} of approximately ((0.0025 x 4) + 0.042) x 40 = 2.08mA.
- For a typical application with 50% of I/O pins used as inputs, 50% used as outputs or bi-directionals.
- This parameter limits the total current sinking of I/O pins surrounding the nearest GND pin.

External Timing Parameters

Over Recommended Operating Conditions

PARAMETER	TEST ¹ COND.	#	DESCRIPTION	-4		-7		-10		UNITS
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{pd}^2	A	1	Data Prop. Delay from Any I/O Pin to Any I/O Pin (4:1 MUX)	–	4.5	–	7.0	–	10.0	ns
t_{sel}^2	A	2	Data Prop. Delay from MUXsel Inputs to Any Output (4:1 MUX)	–	4.5	–	7.0	–	10.0	ns
f_{max} (Tog.)	–	3	Clk. Frequency, Max. Toggle	200.0	–	100.0	–	71.0	–	MHz
f_{max} (Ext.)	–	4	Clk. Frequency with External Feedback ($\frac{1}{t_{su3}+t_{gco1}}$)	153.8	–	80.0	–	56.0	–	MHz
t_{su1}	–	5	Input Latch or Reg. Setup Time Before Y_x	2.5	–	5.5	–	8.0	–	ns
t_{su2}	–	6	Input Latch or Reg. Setup Time Before I/O Clk.	1.5	–	4.5	–	6.5	–	ns
t_{su3}	–	7	Output Latch or Reg. Setup Time Before Y_x	2.5	–	5.5	–	8.0	–	ns
t_{su4}	–	8	Output Latch or Reg. Setup Time Before I/O Clk.	1.5	–	4.5	–	6.5	–	ns
t_{suce1}	–	9	Global Clock Enable Setup Time Before Y_x	2.5	–	3.5	–	5.0	–	ns
t_{suce2}	–	10	Global Clock Enable Setup Time Before I/O Clock	1.5	–	2.5	–	3.5	–	ns
t_{suce3}	–	11	I/O Clock Enable Setup Time Before Y_x	3.0	–	6.5	–	9.0	–	ns
t_{h1}	–	12	Input Latch or Reg. Hold Time (Y_x)	0.0	–	0.0	–	0.0	–	ns
t_{h2}	–	13	Input Latch or Reg. Hold Time (I/O Clock)	1.0	–	2.5	–	3.5	–	ns
t_{h3}	–	14	Output Latch or Reg. Hold Time (Y_x)	0.0	–	0.0	–	0.0	–	ns
t_{h4}	–	15	Output Latch or Reg. Hold Time (I/O Clock)	1.0	–	2.5	–	3.5	–	ns
t_{hce1}	–	16	Global Clock Enable Hold Time (Y_x)	0.0	–	0.0	–	0.0	–	ns
t_{hce2}	–	17	Global Clock Enable Hold Time (I/O Clock)	1.0	–	2.5	–	3.5	–	ns
t_{hce3}	–	18	I/O Clock Enable Hold Time (Y_x)	0.0	–	0.0	–	0.0	–	ns
t_{gco1}^2	A	19	Output Latch or Reg. Clk (from Y_x) to Output Delay	–	4.0	–	7.0	–	10.0	ns
t_{gco2}^2	A	20	Input Latch or Register Clk (from Y_x) to Output Delay	–	7.0	–	11.0	–	15.5	ns
t_{co1}^2	A	21	Output Latch or Reg. Clk. (from I/O pin) to Output Delay	–	5.0	–	9.0	–	12.5	ns
t_{co2}^2	A	22	Input Latch or Reg. Clk. (from I/O pin) to Output Delay	–	8.0	–	13.0	–	18.0	ns
t_{en}^2	B	23	Input to Output Enable	–	5.0	–	8.5	–	12.0	ns
t_{dis}^2	C	24	Input to Output Disable	–	5.0	–	8.5	–	12.0	ns
t_{toen}^2	B	25	Test OE Output Enable	–	6.5	–	8.5	–	12.0	ns
t_{toedis}^2	C	26	Test OE Output Disable	–	6.5	–	8.5	–	12.0	ns
t_{wh}	–	27	Clk. Pulse Duration, High	2.5	–	5.0	–	7.0	–	ns
t_{wl}	–	28	Clk. Pulse Duration, Low	2.5	–	5.0	–	7.0	–	ns
t_{rst}	–	29	Reg. Reset Delay from RESET Low	–	12.0	–	18.0	–	25.0	ns
t_{rw}	–	30	Reset Pulse Width	7.5	–	14.0	–	18.0	–	ns
t_{sl}	D	31	Output Delay Adder for Output Timings Using Slow Slew Rate	–	4.0	–	4.0	–	4.0	ns
t_{sk}	A	32	Output Skew (t_{gco1} Across Chip)	–	0.5	–	0.5	–	1.0	ns

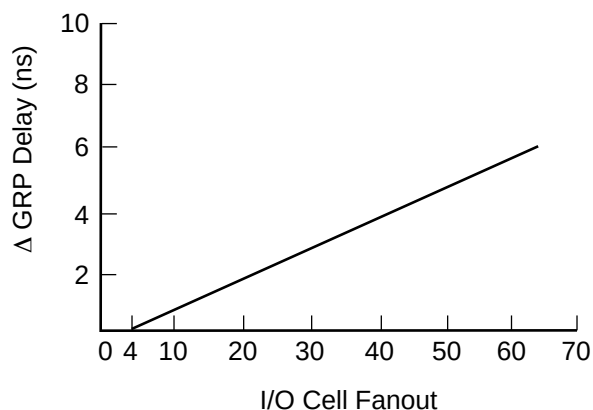
Timing ver. 2.8

1. All timings measured with one output switching, fast output slew rate setting, except t_{sl} .
2. The delay parameters are measured with V_{cc} as I/O voltage reference. An additional 0.5ns delay is incurred when V_{ccio} is used as I/O voltage reference.

External Timing Parameters (Continued)

ispGD_X240VA timings are specified with a GRP load (fanout) of four I/O cells. The figure below shows the Δ GRP Delay with increased GRP loads. These deltas apply to any signal path traversing the GRP (MUXA-D, OE, CLK/CLKEN, MUXsel0-1). Global Clock signals which do not use the GRP have no fanout delay adder.

ispGD_X240VA Maximum Δ GRP Delay vs. I/O Cell Fanout



Internal Timing Parameters¹

Over Recommended Operating Conditions

PARAMETER	#	DESCRIPTION ¹	-4		-7		-10		UNITS
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Inputs									
t _{io}	32	Input Buffer Delay	—	0.8	—	1.4	—	2.1	ns
GRP									
t _{grp}	33	GRP Delay	—	1.1	—	1.1	—	1.1	ns
MUX									
t _{muxd}	34	I/O Cell MUX A/B/C/D Data Delay	—	1.3	—	2.0	—	2.8	ns
t _{muxexp}	35	I/O Cell MUX A/B/C/D Expander Delay	—	1.8	—	2.5	—	3.3	ns
t _{muxs}	36	I/O Cell Data Select	—	1.3	—	2.0	—	2.8	ns
t _{muxsio}	37	I/O Cell Data Select (I/O Clock)	—	2.3	—	4.5	—	6.0	ns
t _{muxsg}	38	I/O Cell Data Select (Yx Clock)	—	2.3	—	2.5	—	5.0	ns
t _{muxselexp}	39	I/O Cell MUX Data Select Expander Delay	—	1.8	—	2.5	—	3.3	ns
Register									
t _{iolat}	40	I/O Latch Delay	—	1.0	—	1.0	—	1.0	ns
t _{iosu}	41	I/O Register Setup Time Before Clock	—	0.3	—	3.2	—	5.0	ns
t _{ioh}	42	I/O Register Hold Time After Clock	—	2.2	—	2.3	—	2.5	ns
t _{ioco}	43	I/O Register Clock to Output Delay	—	0.5	—	0.5	—	0.4	ns
t _{ior}	44	I/O Reset to Output Delay	—	1.5	—	1.5	—	1.5	ns
t _{cesu}	45	I/O Clock Enable Setup Time Before Clock	—	2.0	—	2.5	—	2.0	ns
t _{ceh}	46	I/O Clock Enable Hold Time After Clock	—	0.0	—	1.0	—	3.0	ns
Data Path									
t _{fdbk}	47	I/O Register Feedback Delay	—	0.8	—	1.2	—	1.5	ns
t _{iobp}	48	I/O Register Bypass Delay	—	0.0	—	0.3	—	0.8	ns
t _{iobb}	49	I/O Register Output Buffer Delay	—	0.2	—	0.6	—	0.7	ns
t _{muxcg}	50	I/O Register A/B/C/D Data Input MUX Delay (Yx Clock)	—	2.3	—	2.5	—	5.0	ns
t _{muxcio}	51	I/O Register A/B/C/D Data Input MUX Delay (I/O Clock)	—	2.3	—	4.5	—	6.0	ns
t _{iodg}	52	I/O Register I/O MUX Delay (Yx Clock)	—	4.2	—	5.0	—	8.7	ns
t _{iodio}	53	I/O Register I/O MUX Delay (I/O Clock)	—	4.2	—	7.0	—	9.7	ns
Outputs									
t _{ob}	54	Output Buffer Delay	—	1.3	—	2.2	—	3.2	ns
t _{obs}	55	Output Buffer Delay (Slow Slew Option)	—	5.3	—	6.2	—	7.2	ns
t _{oen}	56	I/O Cell OE to Output Enable	—	3.1	—	6.0	—	8.2	ns
t _{oedis}	57	I/O Cell OE to Output Disable	—	3.1	—	6.0	—	8.2	ns
t _{goe}	58	GRP Output Enable and Disable Delay	—	0.0	—	0.0	—	0.6	ns
t _{toe}	59	Test OE Enable and Disable Delay	—	3.4	—	2.5	—	3.8	ns
Clocks									
t _{ioclk}	60	I/O Clock Delay	—	1.1	—	3.2	—	5.0	ns
t _{gclk}	61	Global Clock Delay	—	2.0	—	2.7	—	5.7	ns
t _{gclkeng}	62	Global Clock Enable (Yx Clock)	—	2.0	—	3.7	—	8.7	ns
t _{gclkenio}	63	Global Clock Enable (I/O Clock)	—	2.0	—	5.7	—	9.7	ns
t _{ioclkeng}	64	I/O Clock Enable (Yx Clock)	—	1.1	—	4.2	—	8.0	ns
Global Reset									
t _{gr}	65	Global Reset to I/O Register Latch	—	9.0	—	13.7	—	19.6	ns

1. Internal Timing Parameters are not tested and are for reference only.

Timing ver. 2.8

2. Refer to the Timing Model in this data sheet for further details.

MUXSEL (I/O INPUT)

DATA (I/O INPUT)

COMBINATORIAL I/O OUTPUT

VALID INPUT

VALID INPUT

t_{sel}

t_{pd}

CLK (I/O INPUT)

The diagram shows a square wave signal. The high pulse width is labeled t_{wh} and the low pulse width is labeled t_{wl} .

DATA (I/O INPUT)

VALID INPUT

t_{su} t_h

CLK

t_{gco} t_{co}

REGISTERED I/O OUTPUT

$1/f_{max}$ (external fdbk)

Timing diagram for the RESET pin. The diagram shows the relationship between the RESET signal and the REGISTERED I/O OUTPUT. The RESET signal is active-low. The output is updated on the falling edge of RESET. The time from the falling edge of RESET to the output becoming valid is labeled t_{trst} . The time from the rising edge of RESET to the output becoming invalid is labeled t_{trw} .

ispGDXVA Timing Model



ispLEVER Development System

The ispLEVER Development System supports ispGDX design using a VHDL or Verilog language syntax. From creation to in-system programming, the ispLEVER system is an easy-to-use, self-contained design tool.

Features

- VHDL and Verilog Synthesis Support Available
- ispGDX Design Compiler
 - Design Rule Checker
 - I/O Connectivity Checker
 - Automatic Compiler Function
- Industry Standard JEDEC File for Programming
- Min/Max Timing Report
- Interfaces To Popular Timing Simulators
- User Electronic Signature (UES) Support
- Detailed Log and Report Files For Easy Design Debug
- On-line Help
- Windows[®] XP, Windows 2000, Windows 98 and Windows NT[®] Compatible
- Solaris[®] and HP-UX Versions Available

In-System Programmability

All necessary programming of the ispGDXVA is done via four TTL level logic interface signals. These four signals

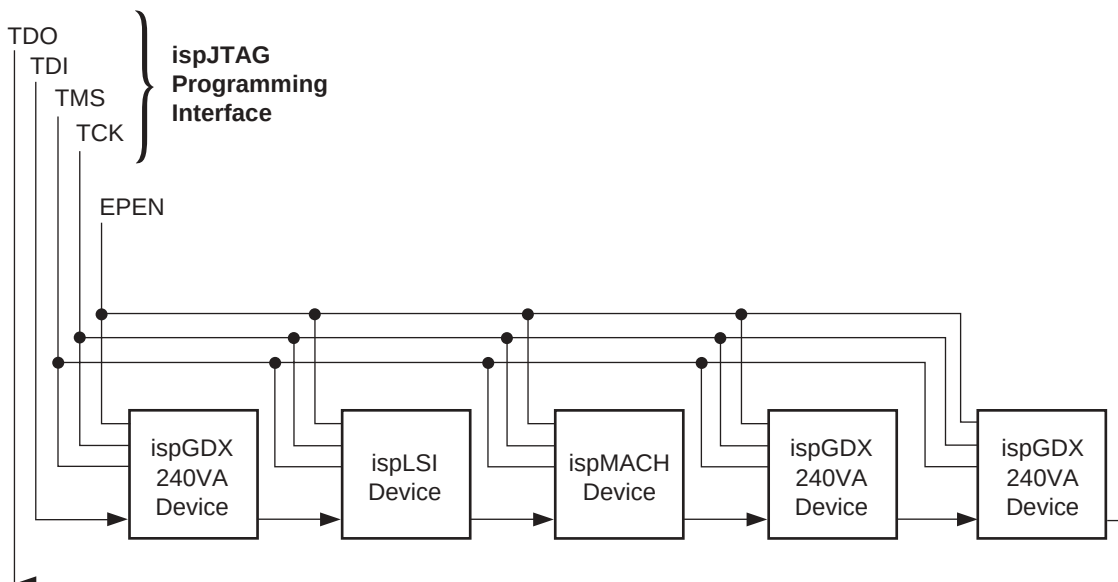
are fed into the on-chip programming circuitry where a state machine controls the programming.

On-chip programming can be accomplished using an IEEE 1149.1 boundary scan protocol. The IEEE 1149.1-compliant interface signals are Test Data In (TDI), Test Data Out (TDO), Test Clock (TCK) and Test Mode Select (TMS) control. The EPEN pin is also used to enable or disable the JTAG port.

The embedded controller port enable pin (EPEN) is used to enable the JTAG tap controller and in that regard has similar functionality to a TRST pin. When the pin is driven high, the JTAG TAP controller is enabled. This is also true when the pin is left unconnected, in which case the pin is pulled high by the permanent internal pullup. This allows ISP programming and BSCAN testing to take place as specified by the Instruction Table.

When the pin is driven low, the JTAG TAP controller is driven to a reset state asynchronously. It stays there while the pin is held low. After pulling the pin high the JTAG controller becomes active. The intent of this feature is to allow the JTAG interface to be directly controlled by the data bus of an embedded controller (hence the name Embedded Port Enable). The EPEN signal is used as a "device select" to prevent spurious programming and/or testing from occurring due to random bit patterns on the data bus. Figure 5 illustrates the block diagram for the ispJTAG[™] interface.

Figure 5. ispJTAG Device Programming Interface



Boundary Scan

The ispGDXVA devices provide IEEE1149.1a test capability and ISP programming through a standard Boundary Scan Test Access Port (TAP) interface.

The boundary scan circuitry on the ispGDXVA Family operates independently of the programmed pattern. This allows customers using boundary scan test to have full test capability with only a single BSDL file.

The ispGDXVA devices are identified by the 32-bit JTAG IDCODE register. The device ID assignments are listed in Table 3.

The ispJTAG programming is accomplished by executing Lattice private instructions under the Boundary Scan State Machine.

Contact Lattice Applications to obtain more detailed programming information.

Table 2. I/O Shift Register Order

DEVICE	I/O SHIFT REGISTER ORDER
ispGDX240VA	TDI, TOE, Y2, Y3, <u>RESET</u> , Y1, Y0, I/O B30 .. B59, I/O C0 .. C59, I/O D0 .. D29, I/O B29 .. B0, I/O A59.. A0, I/O D59 .. D30, TDO

I/O Shift Reg Order/ispGDX240

Table 3. ispGDX240VA Device ID Codes

DEVICE	32-BIT BOUNDARY SCAN ID CODE
ispGDX240VA	0001, 0000, 0011, 0101, 0100, 0000, 0100, 0011

ID Code/GDX240VA

Figure 7. Boundary Scan I/O Register Cell

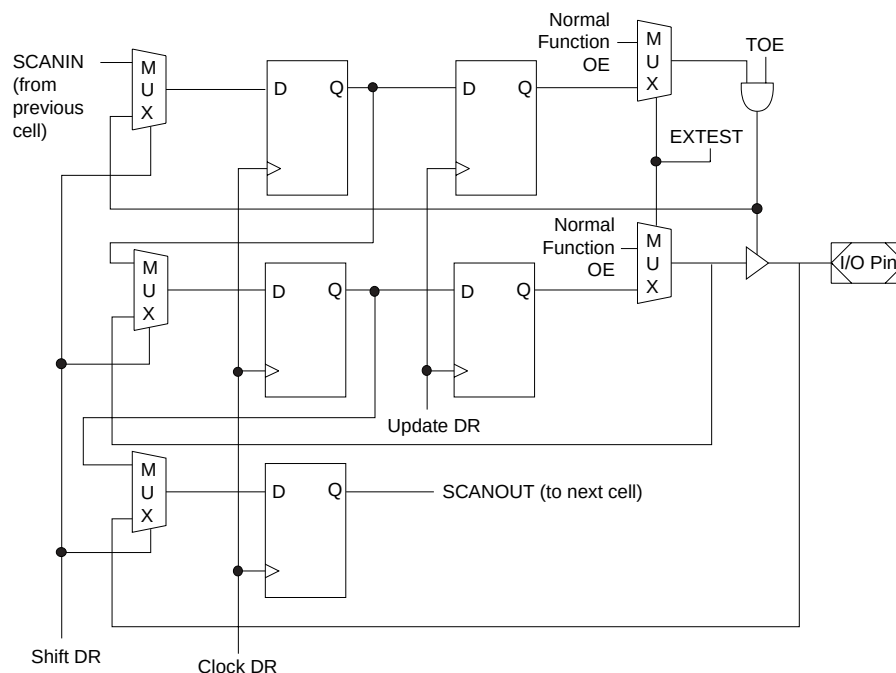
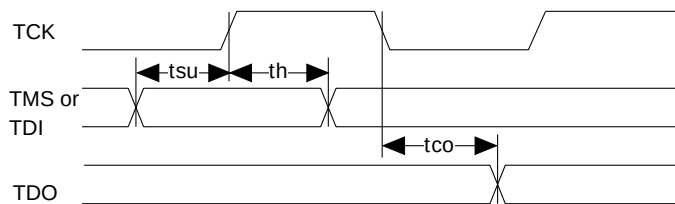
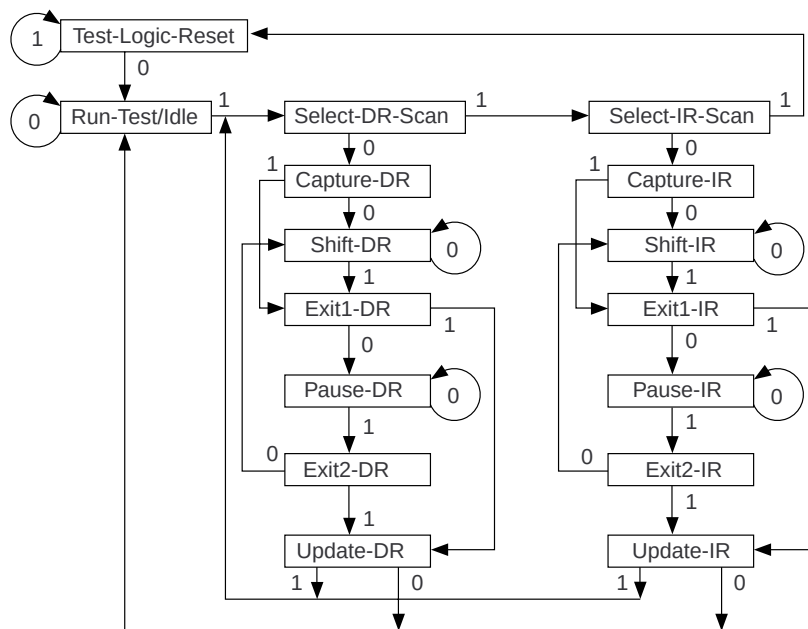


Figure 8. Boundary Scan State Machine



tsu = 0.1μs (min.) th = 0.1μs (min.) tco = 0.1μs (min.)

Signal Descriptions

Signal Name	Description
I/O	Input/Output Pins – These are the general purpose bidirectional data pins. When used as outputs, each may be independently latched, registered or tristated. They can also each assume one other control function (OE, CLK/CLKEN, and MUXsel as described in the text).
TOE	Test Output Enable Pin – This pin tristates all I/O pins when a logic low is driven.
RESET	Active LOW Input Pin – Resets all I/O register outputs when LOW.
Yx/CLKENx	Input Pins –These can be either Global Clocks or Clock Enables.
EPEN	Input Pin – JTAG TAP Controller Enable Pin. When high, JTAG operation is enabled. When low, JTAG TAP controller is driven to reset.
TDI	Input Pin – Serial data input during ISP programming or Boundary Scan mode.
TCK	Input Pin – Serial data clock during ISP programming or Boundary Scan mode.
TMS	Input Pin – Control input during ISP programming or Boundary Scan mode.
TDO	Output Pin – Serial data output during ISP programming or Boundary Scan mode.
GND	Ground (GND)
VCC	Vcc – Supply voltage (3.3V).
VCCIO	Input – This pin is used if optional 2.5V output is to be used. Every I/O can independently select either 3.3V or the optional voltage as its output level. If the optional output voltage is not required, this pin must be connected to the VCC supply. Programmable pull-up resistors and bus-hold latches only draw current from this supply.
NC ¹	No Connect.

1. NC pins are not to be connected to any active signals, VCC or GND.

Signal Locations: ispGDX240VA

Signal	388-Ball fpBGA
TOE	L22
RESET	L21
Y0/CLKEN0	M4
Y1/CLKEN1	L3
Y2/CLKEN2	M20
Y3/CLKEN3	M21
EPEN	A11
TDI	M1
TCK	L1
TMS	L2
TDO	AB12
GND	A1, A22, B2, B21, C3, C20, D4, D19, H9, H10, H11, H12, H13, H14, J8, J9, J10, J11, J12, J13, J14, J15, K8, K9, K10, K11, K12, K13, K14, K15, L8, L9, L10, L11, L12, L13, L14, L15, M8, M9, M10, M11, M12, M13, M14, M15, N8, N9, N10, N11, N12, N13, N14, N15, P8, P9, P10, P11, P12, P13, P14, P15, R9, R10, R11, R12, R13, R14, W4, W19, Y3, Y20, AA2, AA21, AB1, AB22
VCC	D6, D9, D12, D14, D17, F4, F19, G7, G8, G15, G16, H7, H16, J4, J19, L4, M19, P4, P19, R7, R16, T7, T8, T15, T16, U4, U19, W6, W9, W11, W14, W17
VCCIO	M22
NC ¹	G9, G10, G11, G12, G13, G14, H8, H15, J7, J16, K7, K16, L7, L16, M7. M16, N7, N16, P7, P16, R8, R15, T9, T10, T11, T12, T13, T14

1. NC pins are not to be connected to any active signals, VCC or GND.

388-Ball BGA I/O Locations (Sorted by I/O)

I/O #	Control Signal	Ball	I/O #	Control Signal	Ball	I/O #	Control Signal	Ball	I/O #	Control Signal	Ball
VCC			I/O A49	OE	V1	I/O B39	MUXsel2	Y14	I/O C29	OE	N22
I/O A0	CLK/CLKEN	A2	I/O A50	MUXsel1	V2	I/O B40	CLK/CLKEN	AB15	GND		
I/O A1	OE	B1	I/O A51	MUXsel2	V4	I/O B41	OE	AA15	I/O C30	MUXsel1	L20
I/O A2	MUXsel1	C2	I/O A52	CLK/CLKEN	V3	I/O B42	MUXsel1	Y15	I/O C31	MUXsel2	K22
I/O A3	MUXsel2	D3	GND			GND			I/O C32	CLK/CLKEN	K19
I/O A4	CLK/CLKEN	C1	I/O A53	OE	W1	I/O B43	MUXsel2	AB16	I/O C33	OE	K21
I/O A5	OE	D2	I/O A54	MUXsel1	W2	I/O B44	CLK/CLKEN	AA16	I/O C34	MUXsel1	K20
I/O A6	MUXsel1	D1	I/O A55	MUXsel2	Y1	I/O B45	OE	W15	I/O C35	MUXsel2	J22
GND			I/O A56	CLK/CLKEN	W3	I/O B46	MUXsel1	Y16	VCC		
I/O A7	MUXsel2	E3	I/O A57	OE	Y2	I/O B47	MUXsel2	AB17	I/O C36	CLK/CLKEN	J21
I/O A8	CLK/CLKEN	E4	I/O A58	MUXsel1	AA1	VCC			I/O C37	OE	J20
I/O A9	OE	E2	I/O A59	MUXsel2	AB2	I/O B48	CLK/CLKEN	AA17	GND		
I/O A10	MUXsel1	E1	GND			I/O B49	OE	Y17	I/O C38	MUXsel1	H22
I/O A11	MUXsel2	F3	VCC			I/O B50	MUXsel1	AB18	I/O C39	MUXsel2	H21
VCC			I/O B0	CLK/CLKEN	AA3	GND			I/O C40	CLK/CLKEN	H19
I/O A12	CLK/CLKEN	F2	I/O B1	OE	W5	I/O B51	MUXsel2	W16	I/O C41	OE	H20
I/O A13	OE	F1	I/O B2	MUXsel1	AB3	I/O B52	CLK/CLKEN	Y18	I/O C42	MUXsel1	G22
I/O A14	MUXsel1	G3	I/O B3	MUXsel2	Y4	I/O B53	OE	AA18	I/O C43	MUXsel2	G21
GND			I/O B4	CLK/CLKEN	AB4	I/O B54	MUXsel1	AB19	I/O C44	CLK/CLKEN	G19
I/O A15	MUXsel2	G4	I/O B5	OE	AA4	I/O B55	MUXsel2	W18	GND		
I/O A16	CLK/CLKEN	G2	I/O B6	MUXsel1	AA5	I/O B56	CLK/CLKEN	AA20	I/O C45	OE	G20
I/O A17	OE	G1	I/O B7	MUXsel2	Y5	I/O B57	OE	AB20	I/O C46	MUXsel1	F22
I/O A18	MUXsel1	H3	I/O B8	CLK/CLKEN	W7	I/O B58	MUXsel1	Y19	I/O C47	MUXsel2	F21
I/O A19	MUXsel2	H4	GND			I/O B59	MUXsel2	AA19	VCC		
I/O A20	CLK/CLKEN	H2	I/O B9	OE	AB5	GND			I/O C48	CLK/CLKEN	F20
I/O A21	OE	H1	I/O B10	MUXsel1	Y6	VCC			I/O C49	OE	E22
GND			I/O B11	MUXsel2	AA6	I/O C0	CLK/CLKEN	AB21	I/O C50	MUXsel1	E21
I/O A22	MUXsel1	J3	VCC			I/O C1	OE	AA22	I/O C51	MUXsel2	E19
I/O A23	MUXsel2	J2	I/O B12	CLK/CLKEN	AB6	I/O C2	MUXsel1	Y21	I/O C52	CLK/CLKEN	E20
VCC			I/O B13	OE	Y7	I/O C3	MUXsel2	W20	GND		
I/O A24	CLK/CLKEN	J1	I/O B14	MUXsel1	W8	I/O C4	CLK/CLKEN	Y22	I/O C53	OE	D22
I/O A25	OE	K3	I/O B15	MUXsel2	AA7	I/O C5	OE	W21	I/O C54	MUXsel1	D21
I/O A26	MUXsel1	K2	I/O B16	CLK/CLKEN	AB7	I/O C6	MUXsel1	W22	I/O C55	MUXsel2	C22
I/O A27	MUXsel2	K4	GND			GND			I/O C56	CLK/CLKEN	D20
I/O A28	CLK/CLKEN	K1	I/O B17	OE	Y8	I/O C7	MUXsel2	V20	I/O C57	OE	C21
GND			I/O B18	MUXsel1	AA8	I/O C8	CLK/CLKEN	V19	I/O C58	MUXsel1	B22
I/O A29	OE	M2	I/O B19	MUXsel2	AB8	I/O C9	OE	V21	I/O C59	MUXsel2	A21
I/O A30	MUXsel1	M3	I/O B20	CLK/CLKEN	Y9	I/O C10	MUXsel1	V22	GND		
I/O A31	MUXsel2	N1	I/O B21	OE	AA9	I/O C11	MUXsel2	U20	VCC		
I/O A32	CLK/CLKEN	N4	I/O B22	MUXsel1	AB9	VCC			I/O D0	CLK/CLKEN	B20
I/O A33	OE	N2	I/O B23	MUXsel2	W10	I/O C12	CLK/CLKEN	U21	I/O D1	OE	D18
I/O A34	MUXsel1	N3	VCC			I/O C13	OE	U22	I/O D2	MUXsel1	A20
I/O A35	MUXsel2	P1	I/O B24	CLK/CLKEN	Y10	I/O C14	MUXsel1	T20	I/O D3	MUXsel2	C19
VCC			GND			GND			I/O D4	CLK/CLKEN	A19
I/O A36	CLK/CLKEN	P2	I/O B25	OE	AA10	I/O C15	MUXsel2	T19	I/O D5	OE	B19
I/O A37	OE	P3	I/O B26	MUXsel1	AB10	I/O C16	CLK/CLKEN	T21	I/O D6	MUXsel1	B18
GND			I/O B27	MUXsel2	W12	I/O C17	OE	T22	I/O D7	MUXsel2	C18
I/O A38	MUXsel1	R1	I/O B28	CLK/CLKEN	Y11	I/O C18	MUXsel1	R20	I/O D8	CLK/CLKEN	D16
I/O A39	MUXsel2	R2	I/O B29	OE	AA11	I/O C19	MUXsel2	R19	GND		
I/O A40	CLK/CLKEN	R4	I/O B30	MUXsel1	AB11	I/O C20	CLK/CLKEN	R21	I/O D9	OE	A18
I/O A41	OE	R3	I/O B31	MUXsel2	AA12	I/O C21	OE	R22	I/O D10	MUXsel1	C17
I/O A42	MUXsel1	T1	I/O B32	CLK/CLKEN	Y12	GND			I/O D11	MUXsel2	B17
I/O A43	MUXsel2	T2	I/O B33	OE	AB13	I/O C22	MUXsel1	P20	VCC		
I/O A44	CLK/CLKEN	T4	I/O B34	MUXsel1	AA13	I/O C23	MUXsel2	P21	I/O D12	CLK/CLKEN	A17
GND			GND			VCC			I/O D13	OE	C16
I/O A45	OE	T3	I/O B35	MUXsel2	Y13	I/O C24	CLK/CLKEN	P22	I/O D14	MUXsel1	D15
I/O A46	MUXsel1	U1	VCC			I/O C25	OE	N20	I/O D15	MUXsel2	B16
I/O A47	MUXsel2	U2	I/O B36	CLK/CLKEN	AB14	I/O C26	MUXsel1	N21	I/O D16	CLK/CLKEN	A16
VCC			I/O B37	OE	AA14	I/O C27	MUXsel2	N19	GND		
I/O A48	CLK/CLKEN	U3	I/O B38	MUXsel1	W13	I/O C28	CLK/CLKEN	L19	I/O D17	OE	C15

388-Ball BGA I/O Locations (Sorted by I/O), continued

I/O #	Control Signal	Ball	I/O #	Control Signal	Ball	I/O #	Control Signal	Ball	I/O #	Control Signal	Ball
I/O D18	MUXsel1	B15	I/O D29	OE	B12	I/O D40	CLK/CLKEN	A8	GND		
I/O D19	MUXsel2	A15	I/O D30	MUXsel1	A12	I/O D41	OE	B8	I/O D51	MUXsel2	D7
I/O D20	CLK/CLKEN	C14	I/O D31	MUXsel2	B11	I/O D42	MUXsel1	C8	I/O D52	CLK/CLKEN	C5
I/O D21	OE	B14	I/O D32	CLK/CLKEN	C11	GND			I/O D53	OE	B5
I/O D22	MUXsel1	A14	I/O D33	OE	A10	I/O D43	MUXsel2	A7	I/O D54	MUXsel1	B4
I/O D23	MUXsel2	D13	I/O D34	MUXsel1	B10	I/O D44	CLK/CLKEN	B7	I/O D55	MUXsel2	A4
VCC			GND			I/O D45	OE	D8	I/O D56	CLK/CLKEN	C4
I/O D24	CLK/CLKEN	C13	I/O D35	MUXsel2	C10	I/O D46	MUXsel1	C7	I/O D57	OE	A3
GND			VCC			I/O D47	MUXsel2	A6	I/O D58	MUXsel1	D5
I/O D25	OE	B13	I/O D36	CLK/CLKEN	A9	VCC			I/O D59	MUXsel2	B3
I/O D26	MUXsel1	A13	I/O D37	OE	B9	I/O D48	CLK/CLKEN	B6	GND		
I/O D27	MUXsel2	D11	I/O D38	MUXsel1	D10	I/O D49	OE	C6			
I/O D28	CLK/CLKEN	C12	I/O D39	MUXsel2	C9	I/O D50	MUXsel1	A5			

388-Ball BGA I/O Locations (Sorted by Ball)

I/O #	Control Signal	Ball	I/O #	Control Signal	Ball	I/O #	Control Signal	Ball	I/O #	Control Signal	Ball
I/O A0	CLK/CLKEN	A2	I/O A5	OE	D2	I/O A29	OE	M2	I/O C6	MUXsel1	W22
I/O D57	OE	A3	I/O A3	MUXsel2	D3	I/O A30	MUXsel1	M3	I/O A55	MUXsel2	Y1
I/O D55	MUXsel2	A4	I/O D58	MUXsel1	D5	I/O A31	MUXsel2	N1	I/O A57	OE	Y2
I/O D50	MUXsel1	A5	I/O D51	MUXsel2	D7	I/O A33	OE	N2	I/O B3	MUXsel2	Y4
I/O D47	MUXsel2	A6	I/O D45	OE	D8	I/O A34	MUXsel1	N3	I/O B7	MUXsel2	Y5
I/O D43	MUXsel2	A7	I/O D38	MUXsel1	D10	I/O A32	CLK/CLKEN	N4	I/O B10	MUXsel1	Y6
I/O D40	CLK/CLKEN	A8	I/O D27	MUXsel2	D11	I/O C27	MUXsel2	N19	I/O B13	OE	Y7
I/O D36	CLK/CLKEN	A9	I/O D23	MUXsel2	D13	I/O C25	OE	N20	I/O B17	OE	Y8
I/O D33	OE	A10	I/O D14	MUXsel1	D15	I/O C26	MUXsel1	N21	I/O B20	CLK/CLKEN	Y9
I/O D30	MUXsel1	A12	I/O D8	CLK/CLKEN	D16	I/O C29	OE	N22	I/O B24	CLK/CLKEN	Y10
I/O D26	MUXsel1	A13	I/O D1	OE	D18	I/O A35	MUXsel2	P1	I/O B28	CLK/CLKEN	Y11
I/O D22	MUXsel1	A14	I/O C56	CLK/CLKEN	D20	I/O A36	CLK/CLKEN	P2	I/O B32	CLK/CLKEN	Y12
I/O D19	MUXsel2	A15	I/O C54	MUXsel1	D21	I/O A37	OE	P3	I/O B35	MUXsel2	Y13
I/O D16	CLK/CLKEN	A16	I/O C53	OE	D22	I/O C22	MUXsel1	P20	I/O B39	MUXsel2	Y14
I/O D12	CLK/CLKEN	A17	I/O A10	MUXsel1	E1	I/O C23	MUXsel2	P21	I/O B42	MUXsel1	Y15
I/O D9	OE	A18	I/O A9	OE	E2	I/O C24	CLK/CLKEN	P22	I/O B46	MUXsel1	Y16
I/O D4	CLK/CLKEN	A19	I/O A7	MUXsel2	E3	I/O A38	MUXsel1	R1	I/O B49	OE	Y17
I/O D2	MUXsel1	A20	I/O A8	CLK/CLKEN	E4	I/O A39	MUXsel2	R2	I/O B52	CLK/CLKEN	Y18
I/O C59	MUXsel2	A21	I/O C51	MUXsel2	E19	I/O A41	OE	R3	I/O B58	MUXsel1	Y19
I/O A1	OE	B1	I/O C52	CLK/CLKEN	E20	I/O A40	CLK/CLKEN	R4	I/O C2	MUXsel1	Y21
I/O D59	MUXsel2	B3	I/O C50	MUXsel1	E21	I/O C19	MUXsel2	R19	I/O C4	CLK/CLKEN	Y22
I/O D54	MUXsel1	B4	I/O C49	OE	E22	I/O C18	MUXsel1	R20	I/O A58	MUXsel1	AA1
I/O D53	OE	B5	I/O A13	OE	F1	I/O C20	CLK/CLKEN	R21	I/O B0	CLK/CLKEN	AA3
I/O D48	CLK/CLKEN	B6	I/O A12	CLK/CLKEN	F2	I/O C21	OE	R22	I/O B5	OE	AA4
I/O D44	CLK/CLKEN	B7	I/O A11	MUXsel2	F3	I/O A42	MUXsel1	T1	I/O B6	MUXsel1	AA5
I/O D41	OE	B8	I/O C48	CLK/CLKEN	F20	I/O A43	MUXsel2	T2	I/O B11	MUXsel2	AA6
I/O D37	OE	B9	I/O C47	MUXsel2	F21	I/O A45	OE	T3	I/O B15	MUXsel2	AA7
I/O D34	MUXsel1	B10	I/O C46	MUXsel1	F22	I/O A44	CLK/CLKEN	T4	I/O B18	MUXsel1	AA8
I/O D31	MUXsel2	B11	I/O A17	OE	G1	I/O C15	MUXsel2	T19	I/O B21	OE	AA9
I/O D29	OE	B12	I/O A16	CLK/CLKEN	G2	I/O C14	MUXsel1	T20	I/O B25	OE	AA10
I/O D25	OE	B13	I/O A14	MUXsel1	G3	I/O C16	CLK/CLKEN	T21	I/O B29	OE	AA11
I/O D21	OE	B14	I/O A15	MUXsel2	G4	I/O C17	OE	T22	I/O B31	MUXsel2	AA12
I/O D18	MUXsel1	B15	I/O C44	CLK/CLKEN	G19	I/O A46	MUXsel1	U1	I/O B34	MUXsel1	AA13
I/O D15	MUXsel2	B16	I/O C45	OE	G20	I/O A47	MUXsel2	U2	I/O B37	OE	AA14
I/O D11	MUXsel2	B17	I/O C43	MUXsel2	G21	I/O A48	CLK/CLKEN	U3	I/O B41	OE	AA15
I/O D6	MUXsel1	B18	I/O C42	MUXsel1	G22	I/O C11	MUXsel2	U20	I/O B44	CLK/CLKEN	AA16
I/O D5	OE	B19	I/O A21	OE	H1	I/O C12	CLK/CLKEN	U21	I/O B48	CLK/CLKEN	AA17
I/O D0	CLK/CLKEN	B20	I/O A20	CLK/CLKEN	H2	I/O C13	OE	U22	I/O B53	OE	AA18
I/O C58	MUXsel1	B22	I/O A18	MUXsel1	H3	I/O A49	OE	V1	I/O B59	MUXsel2	AA19
I/O A4	CLK/CLKEN	C1	I/O A19	MUXsel2	H4	I/O A50	MUXsel1	V2	I/O B56	CLK/CLKEN	AA20
I/O A2	MUXsel1	C2	I/O C40	CLK/CLKEN	H19	I/O A52	CLK/CLKEN	V3	I/O C1	OE	AA22
I/O D56	CLK/CLKEN	C4	I/O C41	OE	H20	I/O A51	MUXsel2	V4	I/O A59	MUXsel2	AB2
I/O D52	CLK/CLKEN	C5	I/O C39	MUXsel2	H21	I/O C8	CLK/CLKEN	V19	I/O B2	MUXsel1	AB3
I/O D49	OE	C6	I/O C38	MUXsel1	H22	I/O C7	MUXsel2	V20	I/O B4	CLK/CLKEN	AB4
I/O D46	MUXsel1	C7	I/O A24	CLK/CLKEN	J1	I/O C9	OE	V21	I/O B9	OE	AB5
I/O D42	MUXsel1	C8	I/O A23	MUXsel2	J2	I/O C10	MUXsel1	V22	I/O B12	CLK/CLKEN	AB6
I/O D39	MUXsel2	C9	I/O A22	MUXsel1	J3	I/O A53	OE	W1	I/O B16	CLK/CLKEN	AB7
I/O D35	MUXsel2	C10	I/O C37	OE	J20	I/O A54	MUXsel1	W2	I/O B19	MUXsel2	AB8
I/O D32	CLK/CLKEN	C11	I/O C36	CLK/CLKEN	J21	I/O A56	CLK/CLKEN	W3	I/O B22	MUXsel1	AB9
I/O D28	CLK/CLKEN	C12	I/O C35	MUXsel2	J22	I/O B1	OE	W5	I/O B26	MUXsel1	AB10
I/O D24	CLK/CLKEN	C13	I/O A28	CLK/CLKEN	K1	I/O B8	CLK/CLKEN	W7	I/O B30	MUXsel1	AB11
I/O D20	CLK/CLKEN	C14	I/O A26	MUXsel1	K2	I/O B14	MUXsel1	W8	I/O B33	OE	AB13
I/O D17	OE	C15	I/O A25	OE	K3	I/O B23	MUXsel2	W10	I/O B36	CLK/CLKEN	AB14
I/O D13	OE	C16	I/O A27	MUXsel2	K4	I/O B27	MUXsel2	W12	I/O B40	CLK/CLKEN	AB15
I/O D10	MUXsel1	C17	I/O C32	CLK/CLKEN	K19	I/O B38	MUXsel1	W13	I/O B43	MUXsel2	AB16
I/O D7	MUXsel2	C18	I/O C34	MUXsel1	K20	I/O B45	OE	W15	I/O B47	MUXsel2	AB17
I/O D3	MUXsel2	C19	I/O C33	OE	K21	I/O B51	MUXsel2	W16	I/O B50	MUXsel1	AB18
I/O C57	OE	C21	I/O C31	MUXsel2	K22	I/O B55	MUXsel2	W18	I/O B54	MUXsel1	AB19
I/O C55	MUXsel2	C22	I/O C28	CLK/CLKEN	L19	I/O C3	MUXsel2	W20	I/O B57	OE	AB20
I/O A6	MUXsel1	D1	I/O C30	MUXsel1	L20	I/O C5	OE	W21	I/O C0	CLK/CLKEN	AB21

NOTE: VCC and GND Pads Shown for Reference

Signal Configuration: ispGDX240VA

ispGDX240VA 388-Ball fpBGA (1.0mm Ball Pitch / 23.0mm x 23.0mm Body Size)

	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
A	GND	I/O C59	I/O D2	I/O D4	I/O D9	I/O D12	I/O D16	I/O D19	I/O D22	I/O D26	I/O D30	EPEN	I/O D33	I/O D36	I/O D40	I/O D43	I/O D47	I/O D50	I/O D55	I/O D57	I/O A0	GND	A
B	I/O C58	GND	I/O D0	I/O D5	I/O D6	I/O D11	I/O D15	I/O D18	I/O D21	I/O D25	I/O D29	I/O D31	I/O D34	I/O D37	I/O D41	I/O D44	I/O D48	I/O D53	I/O D54	I/O D59	GND	I/O A1	B
C	I/O C55	I/O C57	GND	I/O D3	I/O D7	I/O D10	I/O D13	I/O D17	I/O D20	I/O D24	I/O D28	I/O D32	I/O D35	I/O D39	I/O D42	I/O D46	I/O D49	I/O D52	I/O D56	GND	I/O A2	I/O A4	C
D	I/O C53	I/O C54	I/O C56	GND	I/O D1	VCC	I/O D8	I/O D14	VCC	I/O D23	VCC	I/O D27	I/O D38	VCC	I/O D45	I/O D51	VCC	I/O D58	GND	I/O A3	I/O A5	I/O A6	D
E	I/O C49	I/O C50	I/O C52	I/O C51															I/O A8	I/O A7	I/O A9	I/O A10	E
F	I/O C46	I/O C47	I/O C48	VCC															VCC	I/O A11	I/O A12	I/O A13	F
G	I/O C42	I/O C43	I/O C45	I/O C44															I/O A15	I/O A14	I/O A16	I/O A17	G
H	I/O C38	I/O C39	I/O C41	I/O C40															I/O A19	I/O A18	I/O A20	I/O A21	H
J	I/O C35	I/O C36	I/O C37	VCC															VCC	I/O A22	I/O A23	I/O A24	J
K	I/O C31	I/O C33	I/O C34	I/O C32															I/O A27	I/O A25	I/O A26	I/O A28	K
L	TOE	RESET	I/O C30	I/O C28															VCC	Y1	TMS	TCK	L
M	VCCIO	Y3	Y2	VCC															Y0	I/O A30	I/O A29	TDI	M
N	I/O C29	I/O C26	I/O C25	I/O C27															I/O A32	I/O A34	I/O A33	I/O A31	N
P	I/O C24	I/O C23	I/O C22	VCC															VCC	I/O A37	I/O A36	I/O A35	P
R	I/O C21	I/O C20	I/O C18	I/O C19															I/O A40	I/O A41	I/O A39	I/O A38	R
T	I/O C17	I/O C16	I/O C14	I/O C15															I/O A44	I/O A45	I/O A43	I/O A42	T
U	I/O C13	I/O C12	I/O C11	VCC															VCC	I/O A48	I/O A47	I/O A46	U
V	I/O C10	I/O C9	I/O C7	I/O C8															I/O A51	I/O A52	I/O A50	I/O A49	V
W	I/O C6	I/O C5	I/O C3	GND	I/O B55	VCC	I/O B51	I/O B45	VCC	I/O B38	I/O B27	VCC	I/O B23	VCC	I/O B14	I/O B8	VCC	I/O B1	GND	I/O A56	I/O A54	I/O A53	W
Y	I/O C4	I/O C2	GND	I/O B58	I/O B52	I/O B49	I/O B46	I/O B42	I/O B39	I/O B35	I/O B32	I/O B28	I/O B24	I/O B20	I/O B17	I/O B13	I/O B10	I/O B7	I/O B3	GND	I/O A57	I/O A55	Y
AA	I/O C1	GND	I/O B56	I/O B59	I/O B53	I/O B48	I/O B44	I/O B41	I/O B37	I/O B34	I/O B31	I/O B29	I/O B25	I/O B21	I/O B18	I/O B15	I/O B11	I/O B6	I/O B5	I/O B0	GND	I/O A58	AA
AB	GND	I/O C0	I/O B57	I/O B54	I/O B50	I/O B47	I/O B43	I/O B40	I/O B36	I/O B33	TD0	I/O B30	I/O B26	I/O B22	I/O B19	I/O B16	I/O B12	I/O B9	I/O B4	I/O B2	I/O A59	GND	AB
	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	

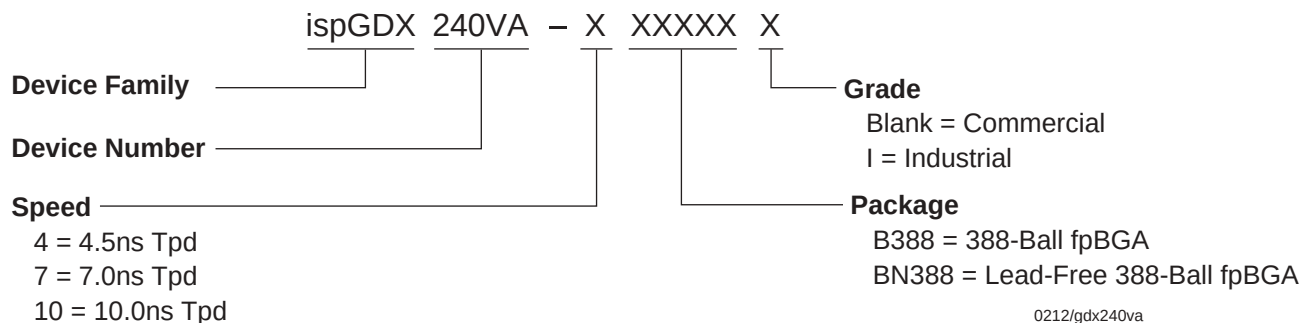
ispGDX240VA

Bottom View

1. NCs are not to be connected to any active signals, VCC or GND.

Note: Ball A1 indicator dot on top side of package.

Part Number Description



Ordering Information

Conventional Packaging

COMMERCIAL

FAMILY	tpd (ns)	ORDERING NUMBER	PACKAGE
ispGDXVA	4.5	ispGDX240VA-4B388	388-Ball fpBGA
	7	ispGDX240VA-7B388	388-Ball fpBGA

Table 2-0041A/gdx240va

INDUSTRIAL

FAMILY	tpd (ns)	ORDERING NUMBER	PACKAGE
ispGDXVA	7	ispGDX240VA-7B388I	388-Ball fpBGA
	10	ispGDX240VA-10B388I	388-Ball fpBGA

Note: The ispGDX240VA devices are dual-marked with both Commercial and Industrial grades.
The Commercial speed grade is faster, e.g. ispGDX240VA-4B388-7I.

Table 2-0041A/gdx240va

Lead-Free Packaging

COMMERCIAL

FAMILY	tpd (ns)	ORDERING NUMBER	PACKAGE
ispGDXVA	4.5	ispGDX240VA-4BN388	Lead-Free 388-Ball fpBGA
	7	ispGDX240VA-7BN388	Lead-Free 388-Ball fpBGA

INDUSTRIAL

FAMILY	tpd (ns)	ORDERING NUMBER	PACKAGE
ispGDXVA	7	ispGDX240VA-7BN388I	Lead-Free 388-Ball fpBGA
	10	ispGDX240VA-10BN388I	Lead-Free 388-Ball fpBGA

Note: The ispGDX240VA devices are dual-marked with both Commercial and Industrial grades.
The Commercial speed grade is faster, e.g. ispGDX240VA-4B388-7I.