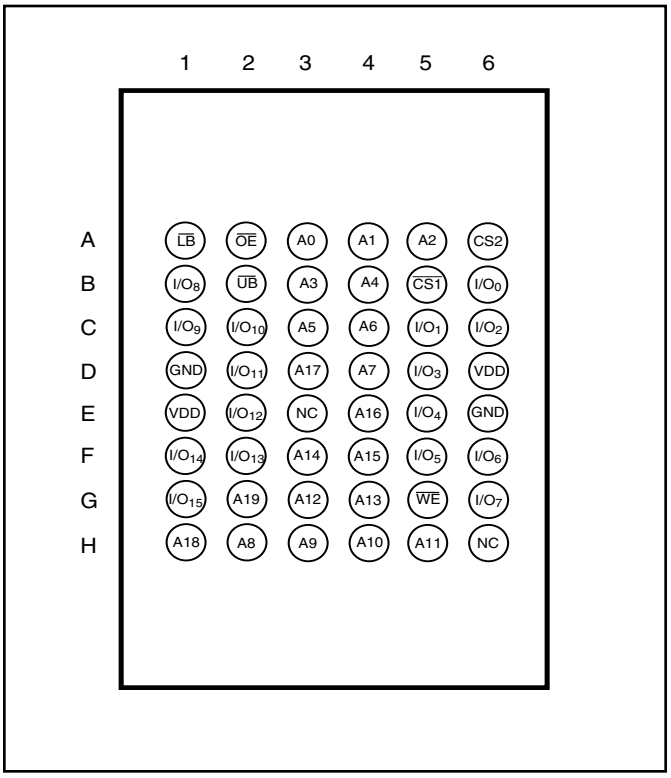
1Mx16 LOW POWER PIN CONFIGURATIONS

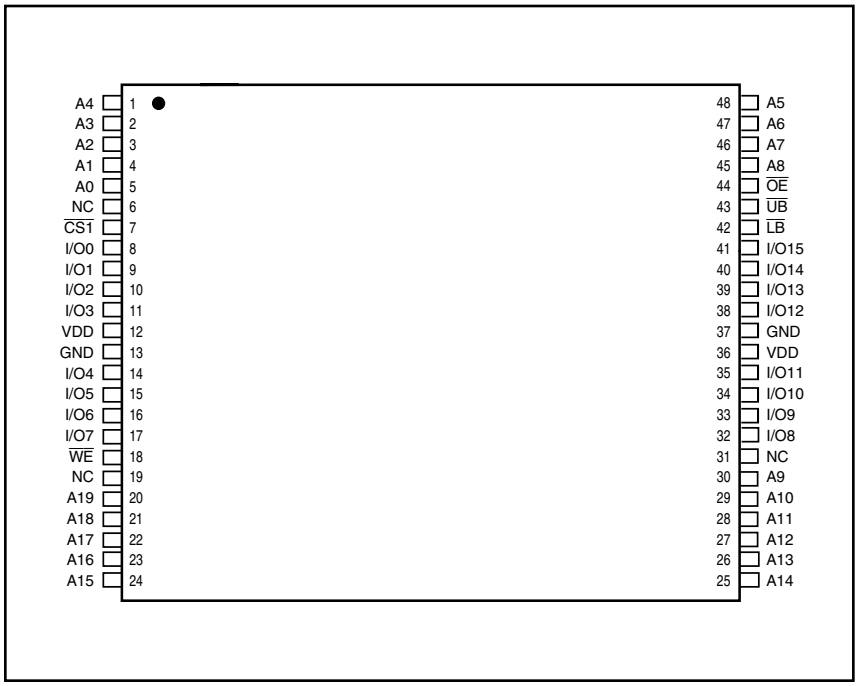
48-Pin mini BGA (9mmx11mm)



PIN DESCRIPTIONS

A0-A19	Address Inputs
I/O0-I/O15	Data Inputs/Outputs
$\overline{CS1}$, CS2	Chip Enable Input
$\overline{OE}$	Output Enable Input
$\overline{WE}$	Write Enable Input
$\overline{LB}$	Lower-byte Control (I/O0-I/O7)
$\overline{UB}$	Upper-byte Control (I/O8-I/O15)
NC	No Connection
V_{DD}	Power
GND	Ground

48-pin TSOP-I (12mm x 20mm)



PIN DESCRIPTIONS

A0-A19	Address Inputs
I/O0-I/O15	Data Inputs/Outputs
$\overline{CS1}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
$\overline{WE}$	Write Enable Input
$\overline{LB}$	Lower-byte Control (I/O0-I/O7)
$\overline{UB}$	Upper-byte Control (I/O8-I/O15)
NC	No Connection
V_{DD}	Power
GND	Ground

TRUTH TABLE

Mode	$\overline{WE}$	$\overline{CS1}$	CS2	$\overline{OE}$	$\overline{LB}$	$\overline{UB}$	I/O PIN I/O0-I/O7	I/O PIN I/O8-I/O15	V_{DD} Current
Not Selected	X	H	X	X	X	X	High-Z	High-Z	I_{SB1}, I_{SB2}
	X	X	L	X	X	X	High-Z	High-Z	I_{SB1}, I_{SB2}
	X	X	X	X	H	H	High-Z	High-Z	I_{SB1}, I_{SB2}
Output Disabled	H	L	H	H	L	X	High-Z	High-Z	I_{CC}
	H	L	H	H	X	L	High-Z	High-Z	I_{CC}
Read	H	L	H	L	L	H	D_{OUT}	High-Z	I_{CC}
	H	L	H	L	H	L	High-Z	D_{OUT}	
	H	L	H	L	L	L	D_{OUT}	D_{OUT}	
Write	L	L	H	X	L	H	D_{IN}	High-Z	I_{CC}
	L	L	H	X	H	L	High-Z	D_{IN}	
	L	L	H	X	L	L	D_{IN}	D_{IN}	

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Parameter	Value	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to V_{DD} + 0.5	V
V_{DD}	V_{DD} Relates to GND	–0.3 to 4.0	V
T_{STG}	Storage Temperature	–65 to +150	°C
P_T	Power Dissipation	1.0	W

Notes:
1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE(1,2)

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF
$C_{I/O}$	Input/Output Capacitance	V_{OUT} = 0V	8	pF

Notes:
1. Tested initially and after any design or process changes that may affect these parameters.
2. Test conditions: T_A = 25°C, f = 1 MHz, V_{DD} = 3.3V.

OPERATING RANGE (V_{DD}) (IS62WV102416ALL)

Range	Ambient Temperature	V_{DD} (35 ns)
Commercial	0°C to +70°C	1.65V-2.2V
Industrial	–40°C to +85°C	1.65V-2.2V
Automotive	–40°C to +125°C	1.65V-2.2V

OPERATING RANGE (V_{DD}) (IS62WV102416BLL)[1]

Range	Ambient Temperature	V_{DD} (25 ns)
Commercial	0°C to +70°C	2.4V-3.6V
Industrial	–40°C to +85°C	2.4V-3.6V

Note:
1. When operated in the range of 2.4V-3.6V, the device meets 10ns.

OPERATING RANGE (V_{DD}) (IS65WV102416BLL)

Range	Ambient Temperature	V_{DD} (25 ns)
Automotive	–40°C to +125°C	2.4V-3.6V

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

V_{DD} = 2.4V-3.6V

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{DD} = Min., I_{OH} = –1.0 mA	1.8	—	V
V_{OL}	Output LOW Voltage	V_{DD} = Min., I_{OL} = 1.0 mA	—	0.4	V
V_{IH}	Input HIGH Voltage		2.0	V_{DD} + 0.3	V
V_{IL}	Input LOW Voltage[1]		–0.3	0.8	V
I_{LI}	Input Leakage	GND ≤ V_{IN} ≤ V_{DD}	–1	1	µA
I_{LO}	Output Leakage	GND ≤ V_{OUT} ≤ V_{DD}, Outputs Disabled	–1	1	µA

Note:
1. V_{IL} (min.) = –0.3V DC; V_{IL} (min.) = –2.0V AC (pulse width < 10 ns). Not 100% tested.
   V_{IH} (max.) = V_{DD} + 0.3V DC; V_{IH} (max.) = V_{DD} + 2.0V AC (pulse width < 10 ns). Not 100% tested.

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

V_{DD} = 1.65V-2.2V

Symbol	Parameter	Test Conditions	V_{DD}	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = -0.1 mA	1.65-2.2V	Vcc – 0.4V	—	V
V_{OL}	Output LOW Voltage	I_{OL} = 0.1 mA	1.65-2.2V	—	0.2	V
V_{IH}	Input HIGH Voltage		1.65-2.2V	1.4	V_{DD} + 0.2	V
V_{IL}[1]	Input LOW Voltage		1.65-2.2V	–0.2	0.4	V
I_{LI}	Input Leakage	GND ≤ V_{IN} ≤ V_{DD}		–1	1	µA
I_{LO}	Output Leakage	GND ≤ V_{OUT} ≤ V_{DD}, Outputs Disabled		–1	1	µA

Notes:
1. V_{IL} (min.) = –0.3V DC; V_{IL} (min.) = –2.0V AC (pulse width < 10ns). Not 100% tested.
   V_{IH} (max.) = V_{DD} + 0.3V DC; V_{IH} (max.) = V_{DD} + 2.0V AC (pulse width < 10ns). Not 100% tested.

AC TEST CONDITIONS (HIGH SPEED)

Parameter	Unit (2.4V-3.6V)	Unit (1.65V-2.2V)
Input Pulse Level	0.4V to V_{DD}-0.3V	0.4V to V_{DD}-0.2V
Input Rise and Fall Times	1.5ns	1.5ns
Input and Output Timing and Reference Level (V_{Ref})	$V_{DD}/2$	$V_{DD}/2$
Output Load	See Figures 1 and 2	See Figures 1 and 2

AC TEST LOADS

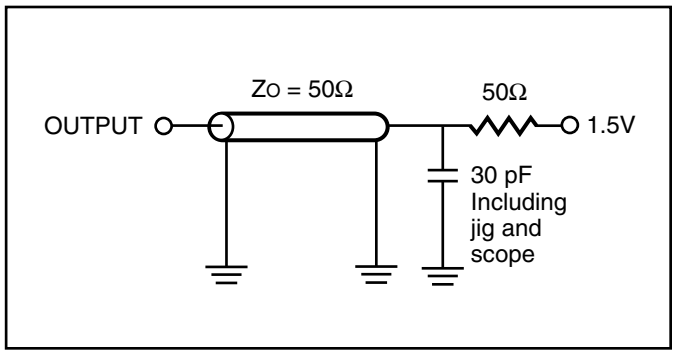


Figure 1.

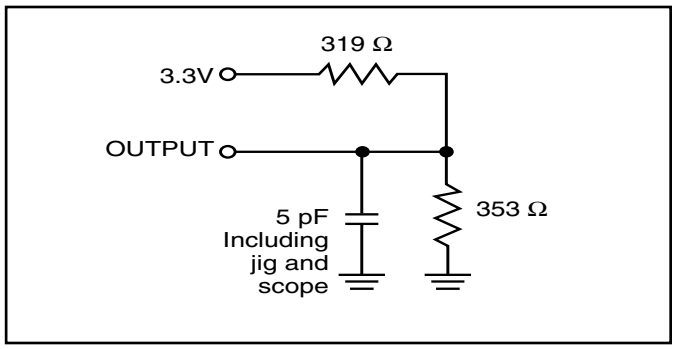


Figure 2.

POWER SUPPLY CHARACTERISTICS[1] (Over Operating Range)

Symbol	Parameter	Test Conditions		-25 Min.	-25 Max.	-35 Min.	-35 Max.	Unit
I_{CC}	V_{DD} Dynamic Operating Supply Current	V_{DD} = Max., I_{OUT} = 0 mA, f = f_{MAX} V_{IN} = 0.4V or V_{DD} –0.3V	Com.	—	30	—	25	mA
			Ind.	—	35	—	30	
			Auto.	—	60	—	60	
			typ.[2]	25				
I_{CC1}	Operating Supply Current	V_{DD} = Max., I_{OUT} = 0 mA, f = 0 V_{IN} = 0.4V or V_{DD} –0.3V	Com.	—	20	—	20	mA
			Ind.	—	30	—	30	
			Auto.	—	50	—	50	
I_{SB1}	TTL Standby Current (TTL Inputs)	V_{DD} = Max., V_{IN} = V_{IH} or V_{IL} $\overline{CS1} \geq V_{IH}$, f = 0	Com.	—	15	—	15	mA
			Ind.	—	20	—	20	
			Auto.	—	40	—	40	
I_{SB2}	CMOS Standby Current (CMOS Inputs)	V_{DD} = Max., $\overline{CS1} \geq V_{DD}$ – 0.2V, $V_{IN} \geq V_{DD}$ – 0.2V, or $V_{IN} \leq$ 0.2V, f = 0	Com.	—	0.8	—	0.8	mA
			Ind.	—	1.2	—	1.2	
			Auto.	—	2	—	2	
			typ.[2]	0.1				

Note:

1. At f = f_{MAX}, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.
2. Typical values are measured at V_{DD} = 3.0V, T_A = 25°C and not 100% tested.

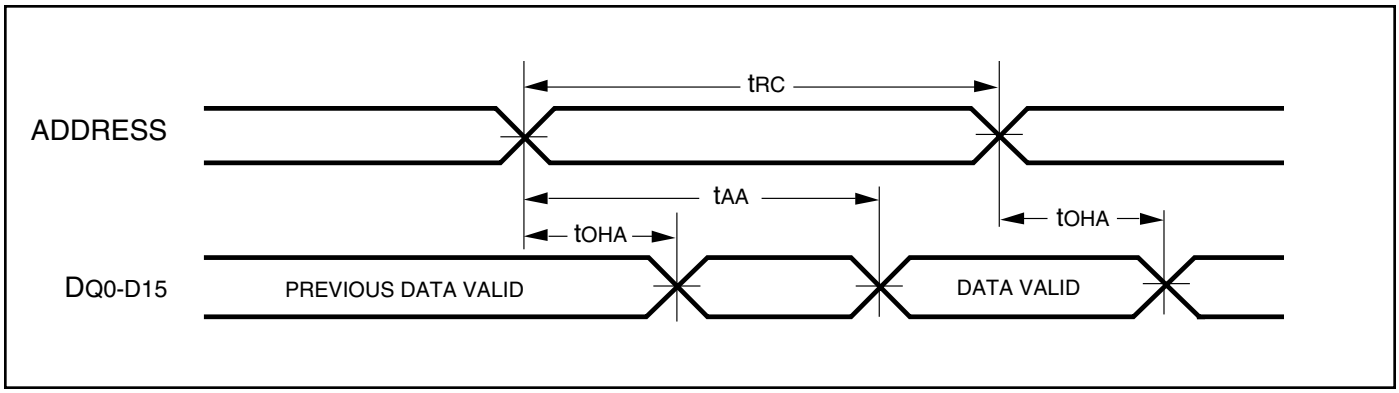
READ CYCLE SWITCHING CHARACTERISTICS[1] (Over Operating Range)

Symbol	Parameter	25 ns Min.	25 ns Max.	35 ns Min.	35 ns Max.	Unit
t_{RC}	Read Cycle Time	25	—	35	—	ns
t_{AA}	Address Access Time	—	25	—	35	ns
t_{OHA}	Output Hold Time	3	—	3	—	ns
t_{ACS1}/t_{ACS2}	$\overline{CS1}$/CS2 Access Time	—	25	—	35	ns
t_{DOE}	$\overline{OE}$ Access Time	—	12	—	15	ns
t_{HZOE}[2]	$\overline{OE}$ to High-Z Output	—	8	—	10	ns
t_{LZOE}[2]	$\overline{OE}$ to Low-Z Output	5	—	5	—	ns
t_{HZCS1}/t_{HZCS2}[2]	$\overline{CS1}$/CS2 to High-Z Output	0	8	0	10	ns
t_{LZCS1}/t_{LZCS2}[2]	$\overline{CS1}$/CS2 to Low-Z Output	10	—	10	—	ns
t_{BA}	$\overline{LB}$, $\overline{UB}$ Access Time	—	25	—	35	ns
t_{HZB}	$\overline{LB}$, $\overline{UB}$ to High-Z Output	0	8	0	10	ns
t_{LZB}	$\overline{LB}$, $\overline{UB}$ to Low-Z Output	0	—	0	—	ns

Notes:
1. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 0.9V/1.5V, input pulse levels of 0.4 to V_{DD}-0.2V/0.4V to V_{DD}-0.3V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.

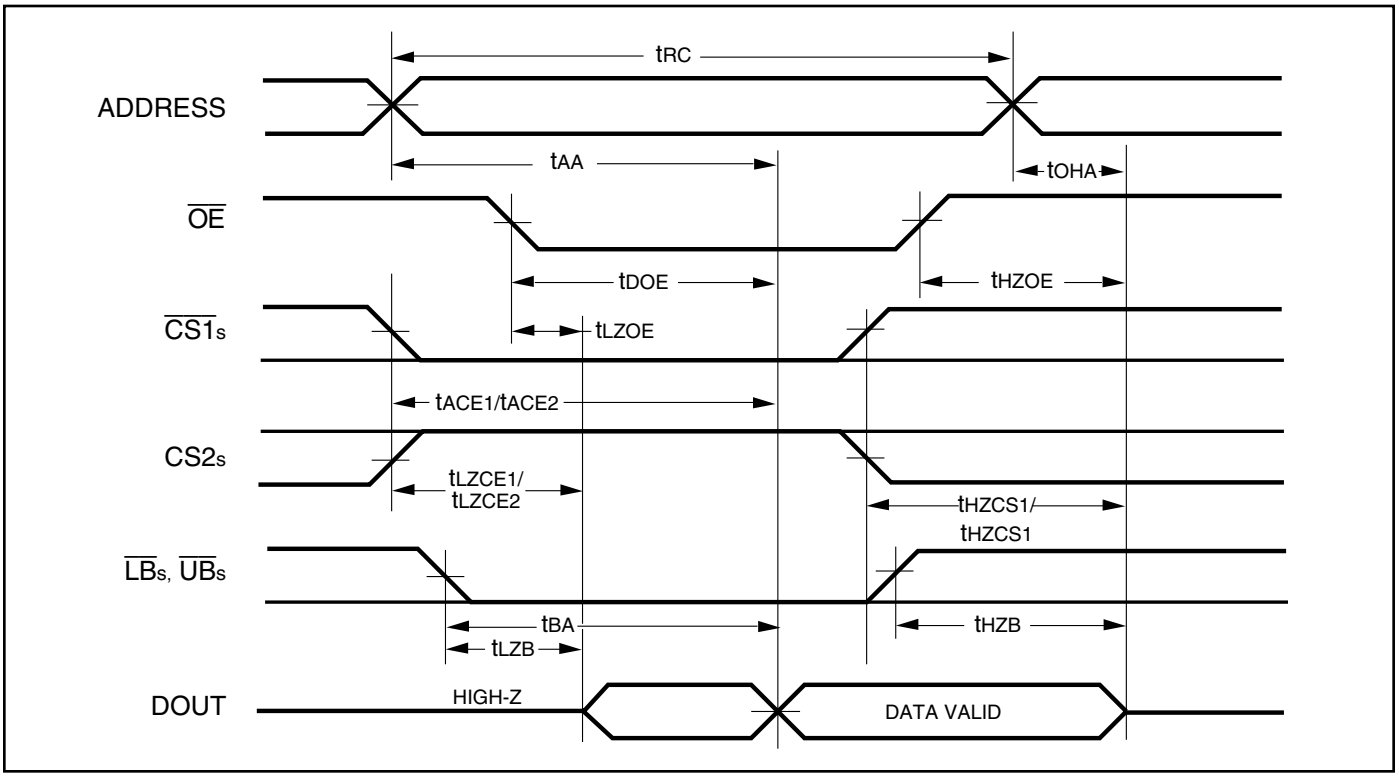
AC WAVEFORMS

READ CYCLE NO. 1[1,2] (Address Controlled) ($\overline{CS1}$ = $\overline{OE}$ = V_{IL}, CS2 = $\overline{WE}$ = V_{IH}, $\overline{UB}$ or $\overline{LB}$ = V_{IL})



AC WAVEFORMS

READ CYCLE NO. 2[1,3] ($\overline{CS1}$, CS2, $\overline{OE}$, AND $\overline{UB}$/$\overline{LB}$ Controlled)



Notes:
1. $\overline{WE}$ is HIGH for a Read Cycle.
2. The device is continuously selected. $\overline{OE}$, $\overline{CS1}$, $\overline{UB}$, or $\overline{LB}$ = V_{IL}. CS2=$\overline{WE}$=V_{IH}.
3. Address is valid prior to or coincident with $\overline{CS1}$ LOW transition.

WRITE CYCLE SWITCHING CHARACTERISTICS[1,2] (Over Operating Range)

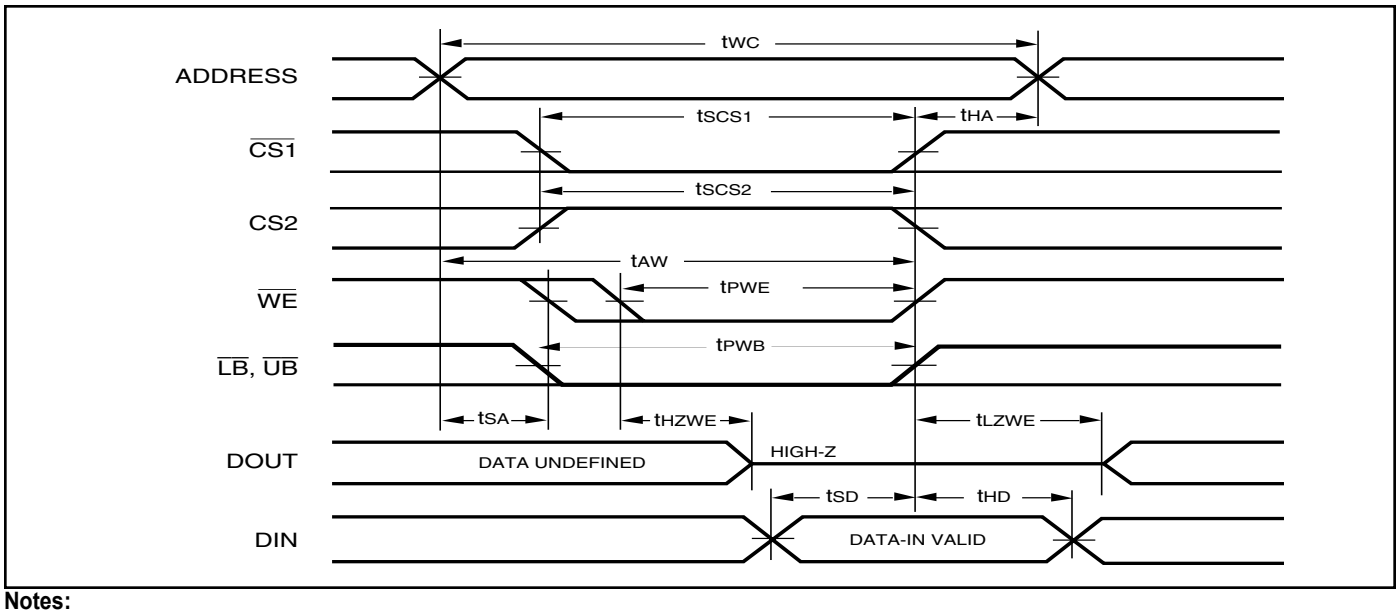
Symbol	Parameter	25ns Min.	25ns Max.	35 ns Min.	35 ns Max.	Unit
t_{WC}	Write Cycle Time	25	—	35	—	ns
t_{SCS1}/t_{SCS2}	$\overline{CS1}$/CS2 to Write End	18	—	25	—	ns
t_{AW}	Address Setup Time to Write End	15	—	25	—	ns
t_{HA}	Address Hold from Write End	0	—	0	—	ns
t_{SA}	Address Setup Time	0	—	0	—	ns
t_{PWB}	$\overline{LB}$, $\overline{UB}$ Valid to End of Write	18	—	25	—	ns
t_{PWE}[4]	$\overline{WE}$ Pulse Width	18	—	30	—	ns
t_{SD}	Data Setup to Write End	12	—	15	—	ns
t_{HD}	Data Hold from Write End	0	—	0	—	ns
t_{HZWE}[3]	$\overline{WE}$ LOW to High-Z Output	—	12	—	20	ns
t_{LZWE}[3]	$\overline{WE}$ HIGH to Low-Z Output	5	—	5	—	ns

Notes:

1. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 0.9V/1.5V, input pulse levels of 0.4 to V_{DD}-0.2V/0.4V to V_{DD}-0.3V and output loading specified in Figure 1.
2. The internal write time is defined by the overlap of $\overline{CS1}$ LOW, CS2 HIGH and $\overline{UB}$ or $\overline{LB}$, and $\overline{WE}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write.
3. Tested with the load in Figure 2. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.
4. $t_{PWE} > t_{HZWE} + t_{SD}$ when $\overline{OE}$ is LOW.

AC WAVEFORMS

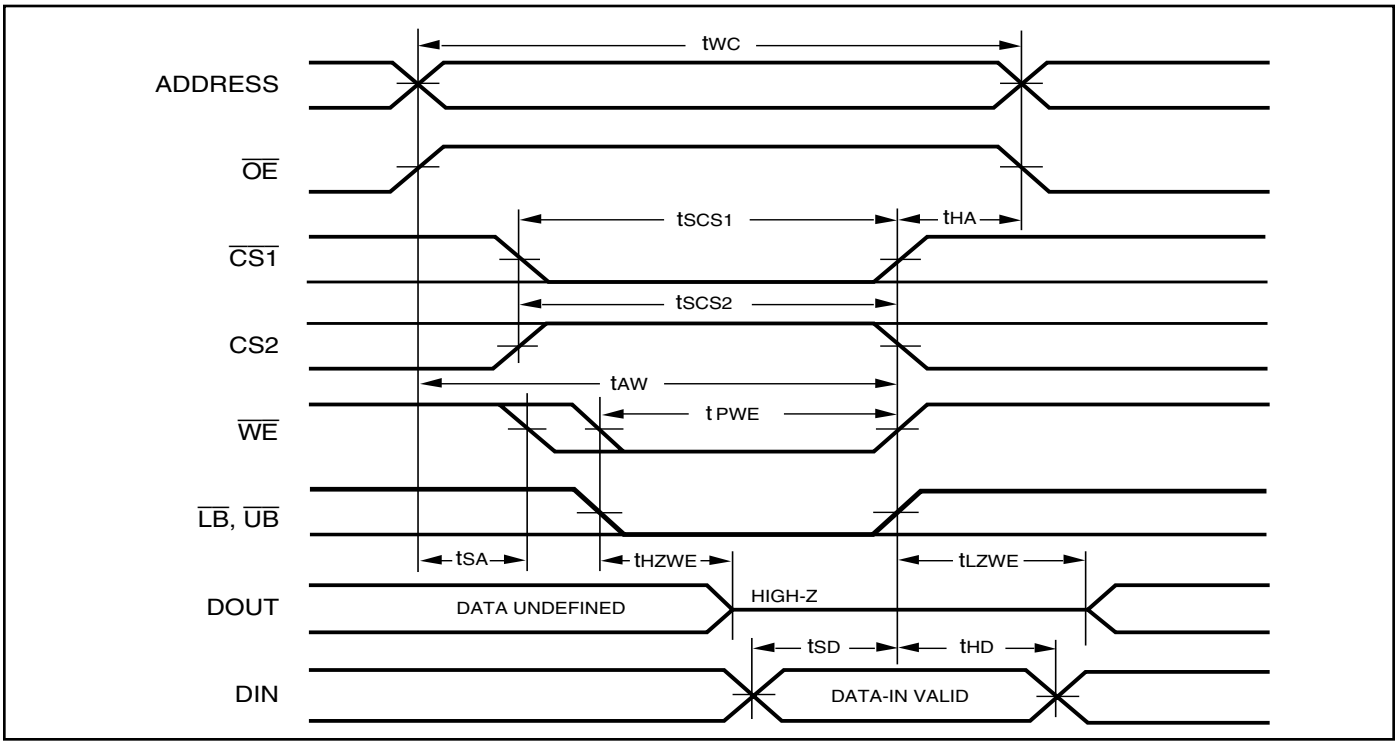
WRITE CYCLE NO. 1[1,2] ($\overline{CS1}$ Controlled, $\overline{OE}$ = HIGH or LOW)



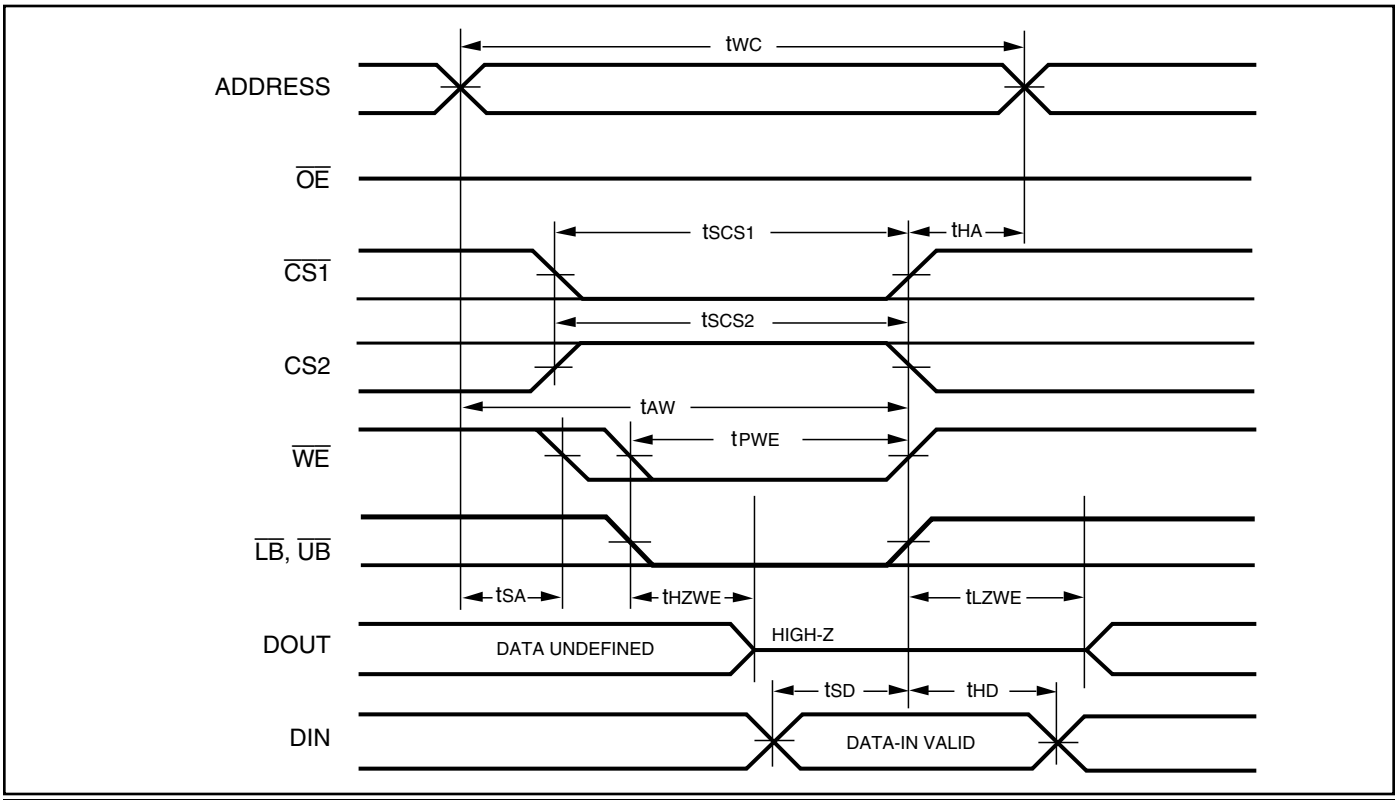
Notes:

1. WRITE is an internally generated signal asserted during an overlap of the LOW states on the $\overline{CS1}$, CS2 and $\overline{WE}$ inputs and at least one of the $\overline{LB}$ and $\overline{UB}$ inputs being in the LOW state.
2. WRITE = ($\overline{CS1}$) [($\overline{LB}$) = ($\overline{UB}$)] ($\overline{WE}$).

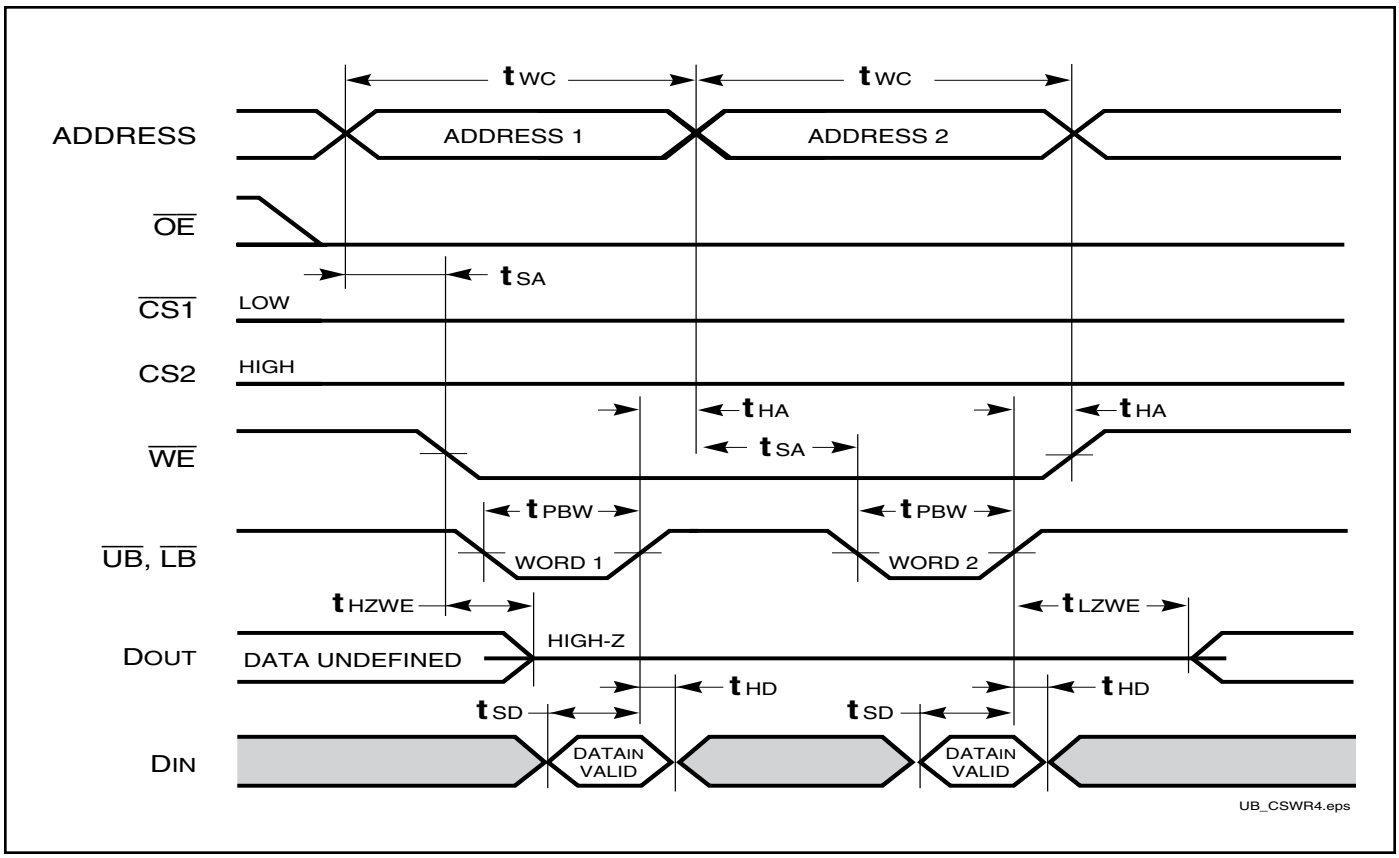
WRITE CYCLE NO. 2 ($\overline{WE}$ Controlled: $\overline{OE}$ is HIGH During Write Cycle)



WRITE CYCLE NO. 3 ($\overline{WE}$ Controlled: $\overline{OE}$ is LOW During Write Cycle)



WRITE CYCLE NO. 4 ($\overline{UB}$/$\overline{LB}$ Controlled)

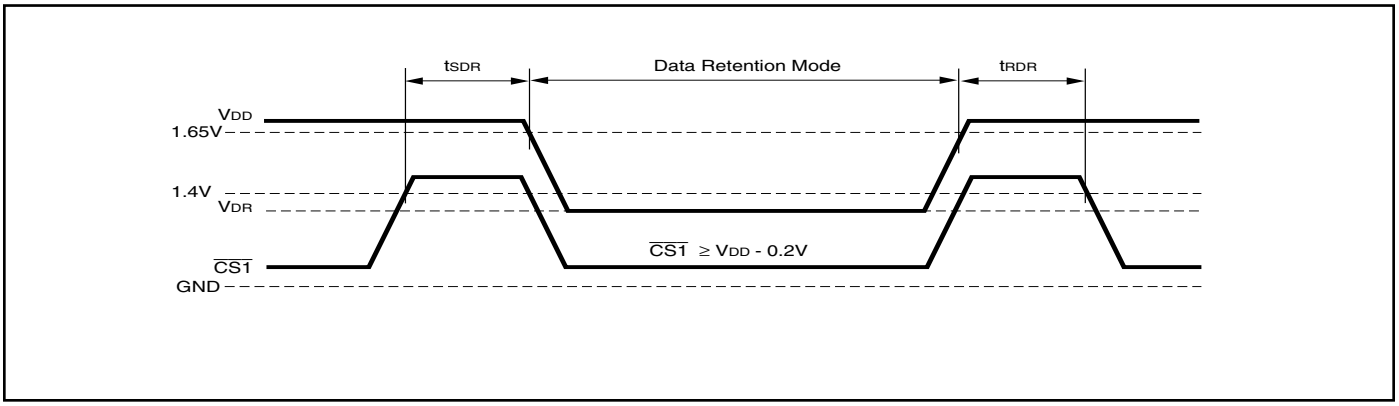


DATA RETENTION SWITCHING CHARACTERISTICS

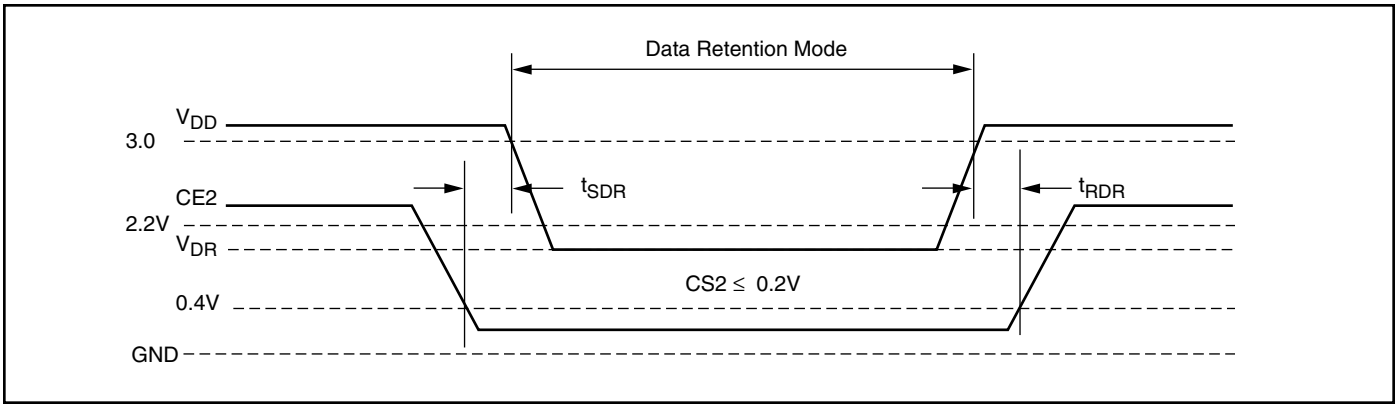
Symbol	Parameter	Test Condition		Min.	Typ.(1)	Max.	Unit
V_{DR}	V_{DD} for Data Retention	See Data Retention Waveform		1.2		3.6	V
I_{DR}	Data Retention Current	V_{DD} = 1.2V, $\overline{CS1} \geq V_{DD} - 0.2V$	Com.	—	0.1	0.8	mA
			Ind.	—	0.1	1.2	
			Auto.	—	0.1	2	
t_{SDR}	Data Retention Setup Time	See Data Retention Waveform		0		—	ns
t_{RDR}	Recovery Time	See Data Retention Waveform		t_{RC}		—	ns

Note:
1. Typical values are measured at V_{DD} = 3.0V, T_A = 25°C and not 100% tested.

DATA RETENTION WAVEFORM ($\overline{CS1}$ Controlled)



DATA RETENTION WAVEFORM (CS2 Controlled)



ORDERING INFORMATION

Industrial Range: -40°C to +85°C

Voltage Range: 2.4V to 3.6V

Speed (ns)	Order Part No.	Package
25	IS62WV102416BLL-25MI	48 mini BGA (9mm x 11mm)
	IS62WV102416BLL-25MLI	48 mini BGA (9mm x 11mm), Lead-free
	IS62WV102416BLL-25TI	TSOP (Type I)
	IS62WV102416BLL-25TLI	TSOP (Type I), Lead-free

Industrial Range: -40°C to +85°C

Voltage Range: 1.65V to 2.2V

Speed (ns)	Order Part No.	Package
35	IS62WV102416ALL-35MI	48 mini BGA (9mm x 11mm)
	IS62WV102416ALL-35MLI	48 mini BGA (9mm x 11mm), Lead-free
	IS62WV102416ALL-35TI	TSOP (Type I)
	IS62WV102416ALL-35TLI	TSOP (Type I), Lead-free

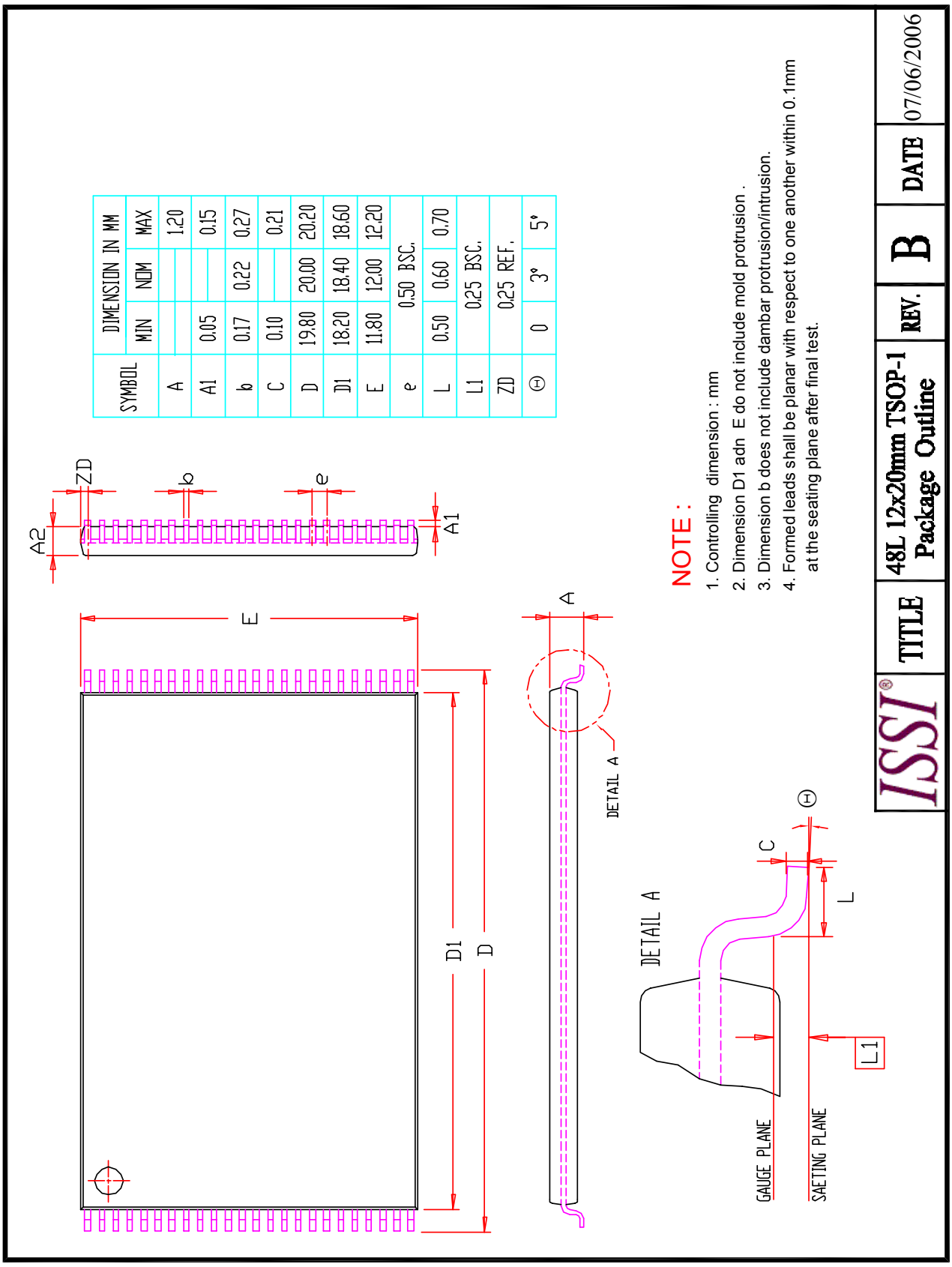
Automotive Range: -40°C to +125°C

Voltage Range: 2.4V to 3.6V

Speed (ns)	Order Part No.	Package
25	IS65WV102416BLL-25MA3	48 mini BGA (9mm x 11mm)
	IS65WV102416BLL-25MLA3	48 mini BGA (9mm x 11mm), Lead-free
	IS65WV102416BLL-25CTA3	TSOP (Type I)
	IS65WV102416BLL-25CTLA3	TSOP (Type I), Lead-free

PACKAGE INFORMATION

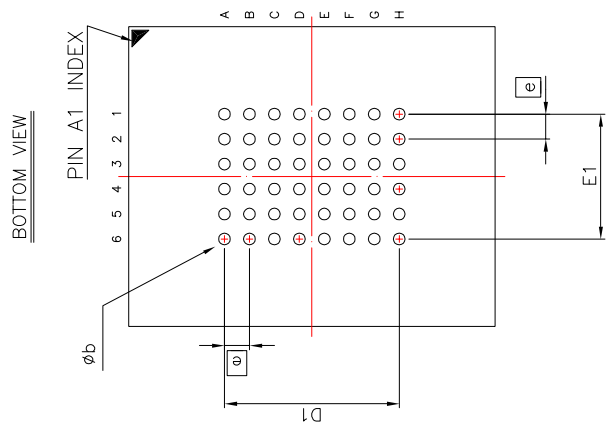
SYMBOL	DIMENSION IN MM		
	MIN	NOM	MAX
A			1.20
A1	0.05		0.15
b	0.17	0.22	0.27
C	0.10		0.21
D	19.80	20.00	20.20
D1	18.20	18.40	18.60
E	11.80	12.00	12.20
e		0.50 BSC.	
L	0.50	0.60	0.70
L1		0.25 BSC.	
ZD		0.25 REF.	
θ	0	3°	5°

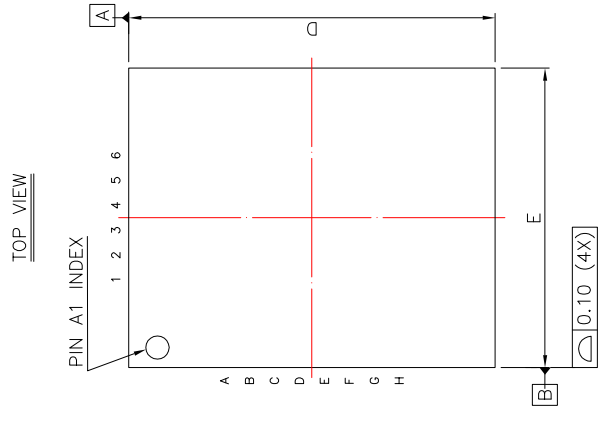


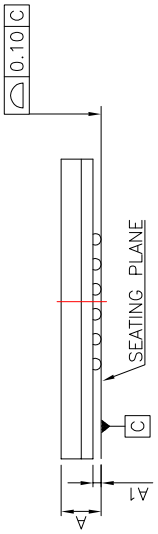
SYM.	DIMENSION (mm)			DIMENSION (INCH)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.20	—	—	0.047
A1	0.20	—	0.30	0.008	—	0.012
b	0.30	0.35	0.40	0.012	0.014	0.016
D	10.90	11.00	11.10	0.429	0.433	0.437
D1	5.25 BSC			0.207 BSC		
E	8.90	9.00	9.10	0.350	0.354	0.358
E1	3.75 BSC			0.148 BSC		
e	0.75 BSC			0.030 BSC		

NOTE :

1. CONTROLLING DIMENSION : MM .
2. Reference document : JEDEC MO-207







ISSI	TITLE	48L 9x11mm TF-BGA Package Outline	REV.	B	DATE	08/21/2008