FUNCTIONAL DESCRIPTION

RECEIVER

Figure 1 shows the general architecture of the ARINC 429 receiver. The receiver operates off the VCC supply only. The inputs RINA and RINB each require 140KΩ of resistance between the ARINC bus and comparator. This resistance is completely on-chip for the HI-8591. In contrast, the HI-8591-40 has 100 KΩ on-chip and requires an external 40KΩ, ¼ watt resistor on each of the ARINC 429 input pins. The HI-8591-40 device is typically chosen for applications where lightning protection is a requirement.

After level translation, the inputs are buffered and become inputs to a differential amplifier. The amplitude of the differential signal is compared to levels derived from a divider between VCC and Ground. The nominal settings correspond to a One/Zero amplitude of 6.0V and a Null amplitude of 3.3V.

The status of the ARINC receiver input is latched. A Null input resets the latches and a One or Zero input sets the latches.

The logic at the output is controlled by the test signal which is generated by the logical OR of the TESTA and TESTB pins. If TESTA and TESTB are both One, the HI-8591 outputs are pulled low. This allows the digital outputs of a transmitter to be connected to the test inputs through control logic for system self-test purposes.

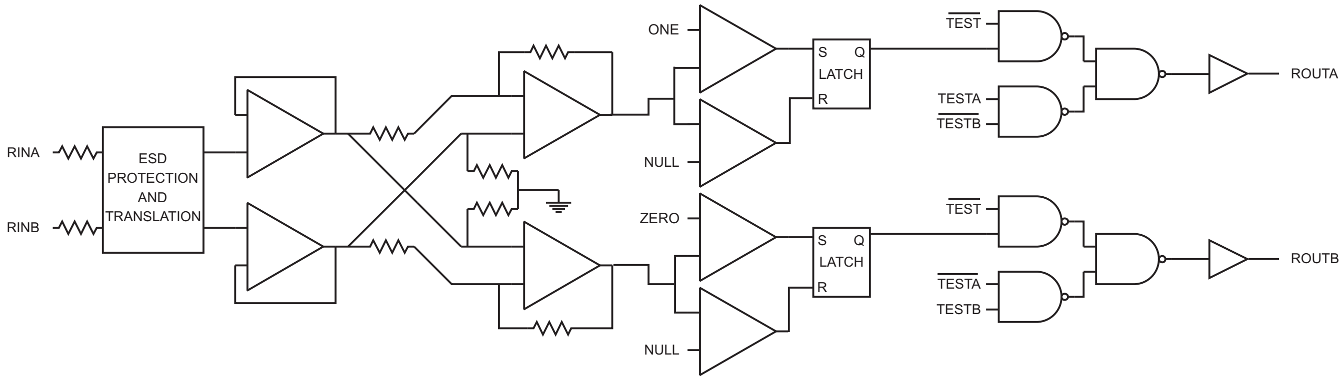


FIGURE 1 - RECEIVER BLOCK DIAGRAM

APPLICATION INFORMATION

Figure 2 shows a possible application of the HI-8591 interfacing an ARINC 429 bus input to a 3.3V ASIC or FPGA. In this example a HI-8586 ARINC 429 line driver is used to take 3.3V logic outputs and generate the necessary 10V differential signal for driving an ARINC 429 bus.

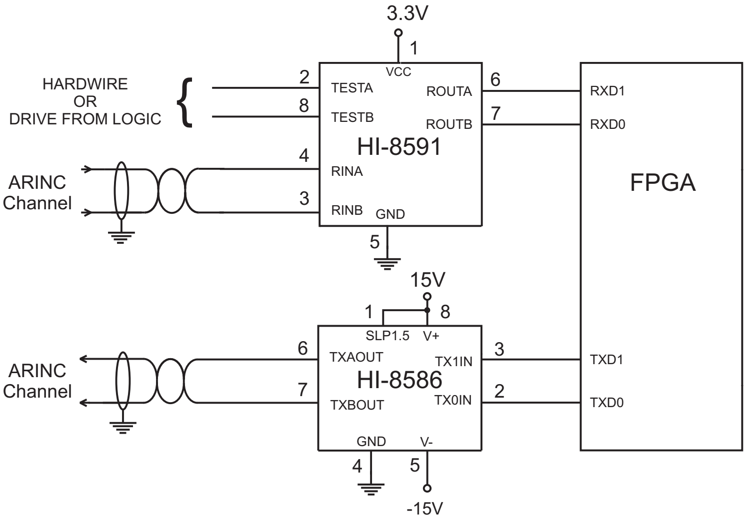


FIGURE 2 - APPLICATION DIAGRAM

ABSOLUTE MAXIMUM RATINGS

Voltages referenced to Ground

Supply voltages
VCC.....................................-0.3V to +7V

ARINC input - pins 3 & 4
Voltage at either pin.........+120V to -120V

DC current per input pin.................... ±10mA

Power dissipation at 25°C
plastic DIP............0.7W
ceramic DIP..........0.5W

Solder Temperature (Reflow) 260°C

Storage Temperature........-65°C to +150°C

RECOMMENDED OPERATING CONDITIONS

Supply Voltages
VCC..............................3.3V to 5V ± 10%

Operating Temperature Range
Industrial .... -40°C to +85°C
Hi-Temp .... -55°C to +125°C

NOTE: Stresses above absolute maximum ratings or outside recommended operating conditions may cause permanent damage to the device. These are stress ratings only. Operation at the limits is not recommended.

DC ELECTRICAL CHARACTERISTICS

OPERATING TEMPERATURE RANGE, VCC = 3.3V ± 10% or 5.0V ± 10% UNLESS OTHERWISE STATED

PARAMETERS	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
ARINC input voltage						
one or zero	V_{DIN}	Differential volt., pins 3 & 4	6.5	10	13	volts
null	V_{NIN}	" " "	-	-	2.5	volts
common mode	V_{COM}	with respect to ground	-30.0	-	+30.0	volts
logic input voltage						
high	V_{IH}		75% VCC	-	-	volts
low	V_{IL}		-	-	25% VCC	volts
ARINC input resistance		Includes external 40KΩ for HI-8591-40				
RINA to RINB	R_{DIFF}	Supplies floating	-	300	-	KΩ
RINA or RINB to GND	R_{GND}	" "	-	150	-	KΩ
RINA or RINB to VCC	R_{VCC}	" "	-	150	-	KΩ
logic input current						
source	I_{IH}	V_{IN} = 2.0V	-	-	20.0	µA
sink	I_{IL}	V_{IN} = 0.8V	-	-	20.0	µA
logic output drive voltage						
one	V_{OH1}	VCC = 5V ± 10% I_{OH} = 5mA	2.4	-	-	V
	V_{OH2}	VCC= 3.3V ± 10% I_{OH} = 1.5mA	2.4	-	-	V
zero	V_{OL1}	VCC = 5V ± 10% I_{OH} = 5mA	-	-	0.5	V
	V_{OL2}	VCC = 3.3V ± 10% I_{OH} = 1.5mA	-	-	0.4	V
Current drain						
operating	I_{CC1}	pins 2, 8 = 0V; pins 3, 4 open	-	1.5	5.0	mA

AC ELECTRICAL CHARACTERISTICS

OPERATING TEMPERATURE RANGE, VCC = 3.3V ± 10% or 5.0V ± 10% UNLESS OTHERWISE STATED

PARAMETERS	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Receiver propagation delay		defined in Figure 3, C_L= 50pF				
Output high to low	t_{phlr}	VCC = 3.3V ± 10%	-	600	1000	ns
		VCC = 5.0V ± 10%	-	600	900	ns
Output low to high	t_{plhr}	VCC = 3.3V ± 10%	-	600	1000	ns
		VCC = 5.0V ± 10%	-	600	900	ns
TEST pin propagation delay		defined in Figure 4, C_L= 50pF				
Output high to low	t_{pth}	VCC = 3.3V ± 10%	-	-	100	ns
		VCC = 5.0V ± 10%	-	-	60	ns
Output low to high	t_{ptl}	VCC = 3.3V ± 10%	-	-	100	ns
		VCC = 5.0V ± 10%	-	-	60	ns
Receiver output transition times		VCC = 3.3V or 5.0V ± 10%				
Output high to low	t_{fr}		-	15	50	ns
Output low to high	t_{rr}		-	15	50	ns
Input capacitance (1)						
ARINC differential	C_{AD}		-	5	10	pF
ARINC single ended to Ground	C_{AS}		-	-	10	pF
Logic	C_{IN}		-	-	10	pF

Notes: 1. Guaranteed but not tested

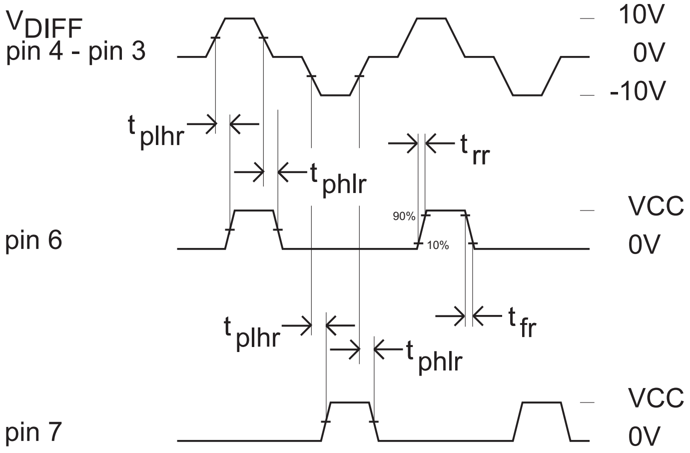


FIGURE 3 - RECEIVER TIMING

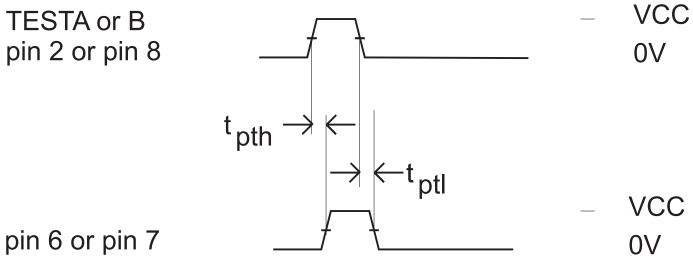


FIGURE 4 - TEST PIN TIMING

HEAT SINK - CHIP-SCALE PACKAGE ONLY

The HI-8591PCI and HI-8591PCT use a 16-pin plastic chip-scale (QFN) package. This package has a metal heat sink pad on its bottom surface. This heat sink should be soldered down to the printed circuit board for optimum thermal dissipation. The heat sink is electrically isolated from the chip and can be soldered to any ground or power plane. However, since the chip's substrate is at V+, connecting the heat sink to this power plane is recommended to avoid coupling noise into the circuit.

ORDERING INFORMATION

HI - 8591 xx x x - xx

PART NUMBER	INPUT SERIES RESISTANCE	
	BUILT-IN	REQUIRED EXTERNALLY
No dash number	140 Kohm	0
-40	100 Kohm	40 Kohm

PART NUMBER	LEAD FINISH
Blank	Tin / Lead (Sn / Pb) Solder
F	100% Matte Tin (Pb-free, RoHS compliant)

PART NUMBER	TEMPERATURE RANGE	FLOW	BURN IN
I	-40°C TO +85°C	I	NO
T	-55°C TO +125°C	T	NO
M	-55°C TO +125°C	M	YES

PART NUMBER	PACKAGE DESCRIPTION
PC	16 PIN PLASTIC 4 x 4 mm CHIP SCALE (16PCS) not available with "M" flow
PD	8 PIN PLASTIC DIP (8P) not available with "M" flow
PS	8 PIN PLASTIC NARROW BODY SOIC (8HN)
CR	8 PIN CERDIP (8D) not available Pb-free

REVISION HISTORY

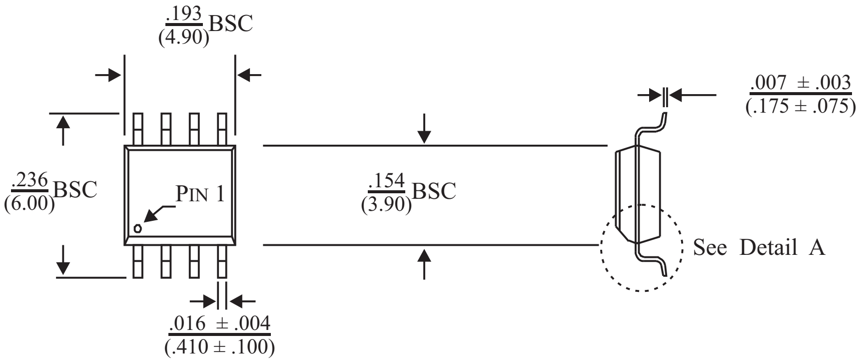
P/N	Rev	Date	Description of Change
DS8591	F	06/21/11	Updated pad & heat-sink dimensions on 16-pin plastic chip-scale (QFN) package to reflect current package vendor's dimensions.
	G	08/03/12	Updated VIL/VIH specification, Solder Temperature, and package dimensions (8PS, 16PC).
	H	03/13/13	Clarify ARINC input resistance and correct error in RDIFF. Clarify solder temperature in Absolute Maximum Ratings. Clarify operating temperature range in Recommended Operating Conditions.

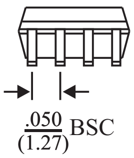
HI-8591 PACKAGE DIMENSIONS

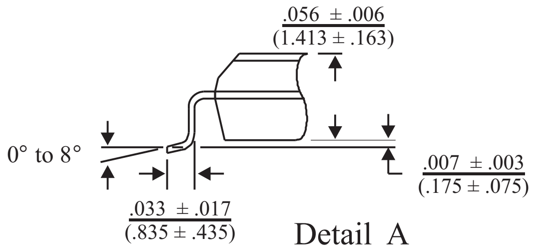
8-PIN PLASTIC SMALL OUTLINE (SOIC) - NB
(Narrow Body)

inches (millimeters)

Package Type: 8HN





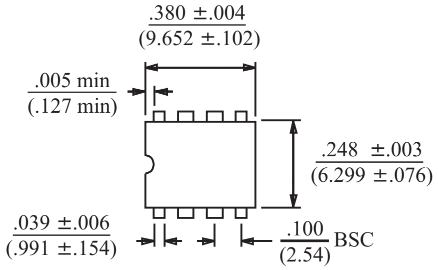


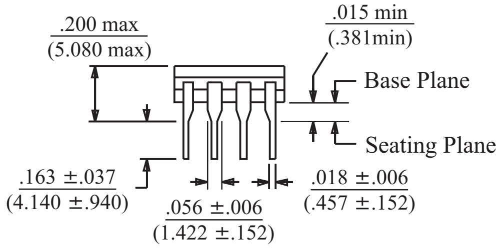
BSC = "Basic Spacing between Centers" is theoretical true position dimension and has no tolerance. (JEDEC Standard 95)

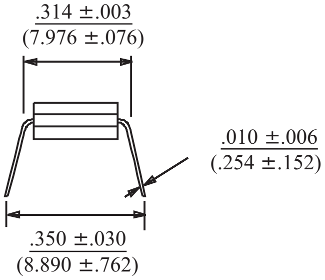
8-PIN CERDIP

inches (millimeters)

Package Type: 8D







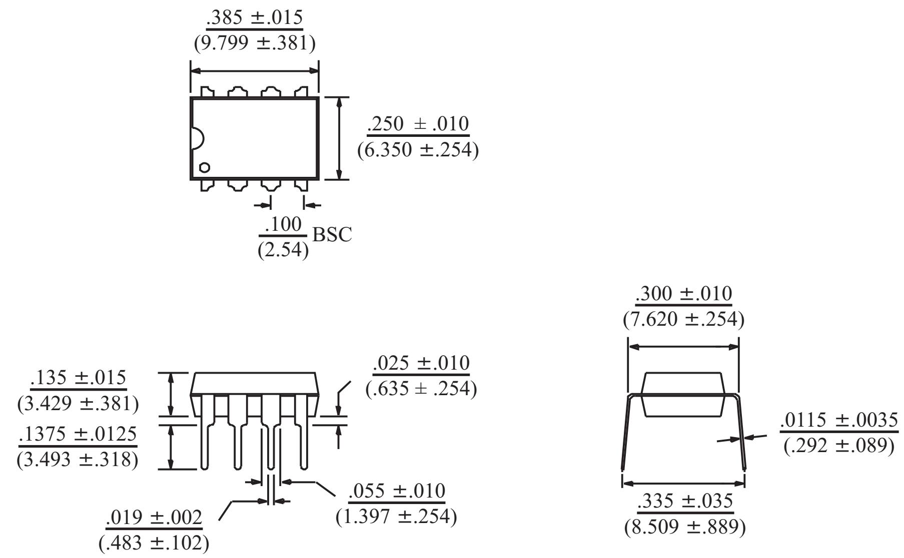
BSC = "Basic Spacing between Centers" is theoretical true position dimension and has no tolerance. (JEDEC Standard 95)

HI-8591 PACKAGE DIMENSIONS

8-PIN PLASTIC DIP

inches (millimeters)

Package Type: 8P

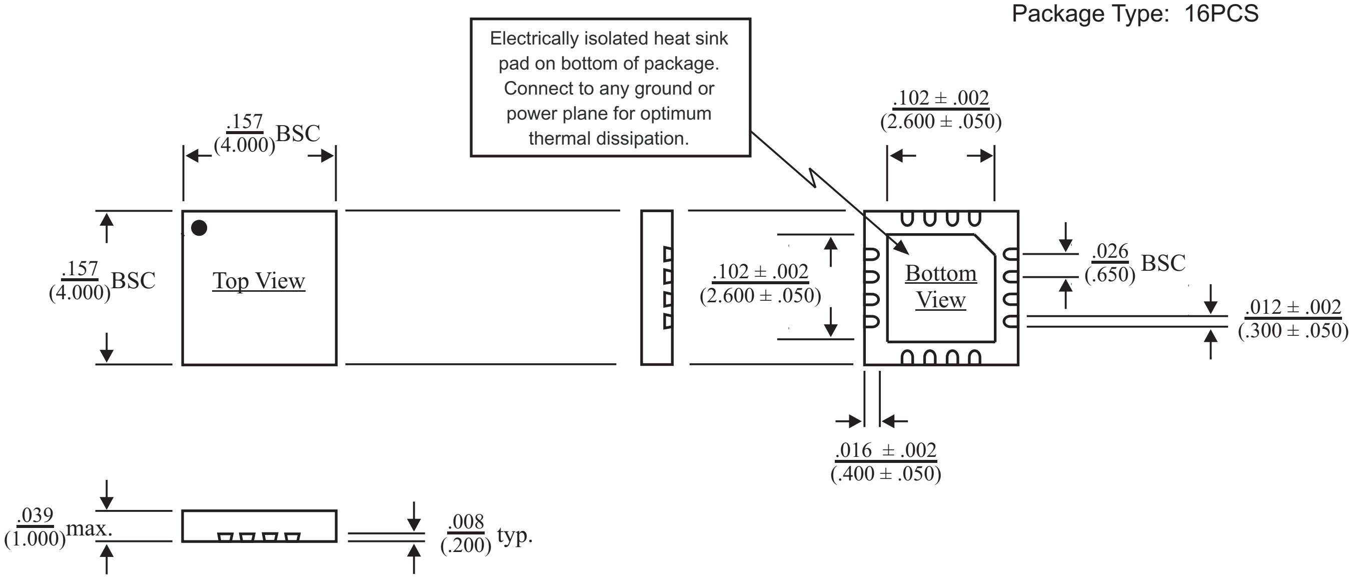


BSC = "Basic Spacing between Centers" is theoretical true position dimension and has no tolerance. (JEDEC Standard 95)

16-PIN PLASTIC CHIP-SCALE PACKAGE

inches (millimeters)

Package Type: 16PCS


Electrically isolated heat sink pad on bottom of package. Connect to any ground or power plane for optimum thermal dissipation.

BSC = "Basic Spacing between Centers" is theoretical true position dimension and has no tolerance. (JEDEC Standard 95)