

ORDERING INFORMATION

Part Number	Package Markings	T _J Rating	Package Description
EP5388QI	ABXX	-40°C to +125°C	16-pin (3mm x 3mm x 1.1mm) QFN
EP5388QI-E		QFN Evaluation Board	

Packing and Marking Information: www.intel.com/support/reliability/packing/rel-packing-and-marking.html

PIN FUNCTIONS

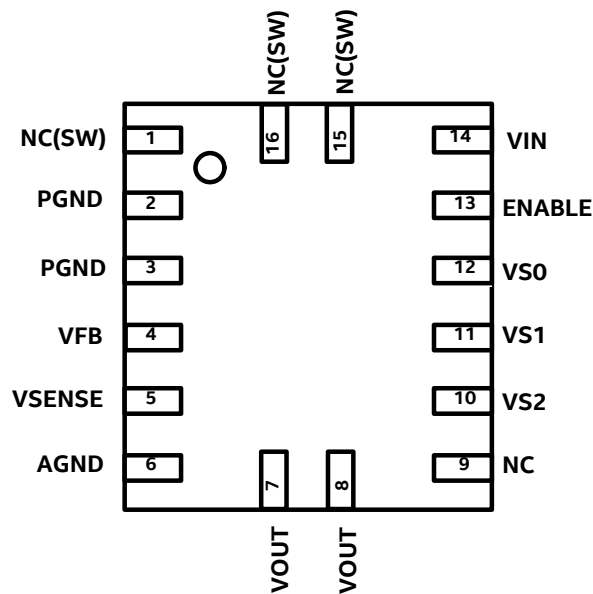


Figure 3. EP5388QI Pin Out Diagram (Top View)

NOTE A: NC pins are not to be electrically connected to each other or to any external signal, ground or voltage. However, they must be soldered to the PCB. Failure to follow this guideline may result in part malfunction or damage.

NOTE B: White 'dot' on top left is pin 1 indicator on top of the device package.

PIN DESCRIPTIONS

PIN	NAME	TYPE	FUNCTION
1, 15, 16	NC(SW)	-	NO CONNECT – These pins are internally connected to the common drain output of the internal MOSFETs. NC(SW) pins are not to be electrically connected to any external signal, ground, or voltage. However, they must be soldered to the PCB. Failure to follow this guideline may result in part malfunction or damage.
2, 3	PGND	Ground	Power Ground
4	VFB	Analog	Feedback pin for external divider option. When using the external divider option (VS0=VS1=VS2= high) connect this pin to the center of the external divider. Set the divider such that VFB = 0.6V. The “ground” side of the external divider should be connected to AGND. This pin may be left unconnected when using Voltage Select pins (VS0-VS2) to set the output voltage.
5	VSENSE	Analog	Sense pin for output voltage regulation. Refer to application section for proper configuration.
6	AGND	Ground	Analog ground. This is the quiet ground for the internal control circuitry
7, 8	VOUT	Power	Regulated Output Voltage. Refer to application section for proper layout and decoupling.
9	NC	Analog	NO CONNECT – This pin should not be electrically connected to any external signal, voltage, or ground. This pin may be connected internally. However, this pin must be soldered to the PCB.
10, 11, 12	VS0,VS1,VS2	Analog	Output voltage select. VS2=pin10 VS1=pin11, VS0=pin12. Selects one of seven preset output voltages or choose external divider by connecting pins to logic high or low. Refer to section on output voltage select for more detail.
13	ENABLE	Analog	Output enable. Enable = logic high, disable = logic low.
14	VIN	Power	Input voltage pin. Refer to application section for proper layout and decoupling.

ABSOLUTE MAXIMUM RATINGS

CAUTION: Absolute Maximum ratings are stress ratings only. Functional operation beyond the recommended operating conditions is not implied. Stress beyond the absolute maximum ratings may impair device life. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

Absolute Maximum Pin Ratings

PARAMETER	SYMBOL	MIN	MAX	UNITS
Input Supply Voltage	V_{IN}	-0.3	7.0	V
ENABLE, V_{SENSE} , $V_{SO} - V_{S2}$		-0.3	$V_{IN}+0.3$	V
V_{FB}		-0.3	2.7	V

Absolute Maximum Thermal Ratings

PARAMETER	CONDITION	MIN	MAX	UNITS
Storage Temperature Range		-65	+150	°C
Reflow Peak Body Temperature	(10 Sec) MSL3 JEDEC J-STD-020A		+260	°C

Absolute Maximum ESD Ratings

PARAMETER	CONDITION	MIN	MAX	UNITS
HBM (Human Body Model)		±2000		V

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	MAX	UNITS
Input Voltage Range	V_{IN}	2.4	5.5	V
Output Voltage Range	V_{OUT}	0.603	$V_{IN}-0.5$	V
Operating Ambient Temperature Range	T_A	-40	+85	°C
Operating Junction Temperature	T_J	-40	+125	°C

THERMAL CHARACTERISTICS

PARAMETER	SYMBOL	TYPICAL	UNITS
Thermal Resistance: Junction to Ambient –0 LFM ⁽¹⁾	θ_{JA}	100	°C/W
Thermal Overload Trip Point	T_{J-TP}	+150	°C
Thermal Overload Trip Point Hysteresis		15	°C

⁽¹⁾ Based on 2oz. external copper layers and proper thermal design in line with EIJ/JEDEC JESD51-7 standard for high thermal conductivity boards.

ELECTRICAL CHARACTERISTICS

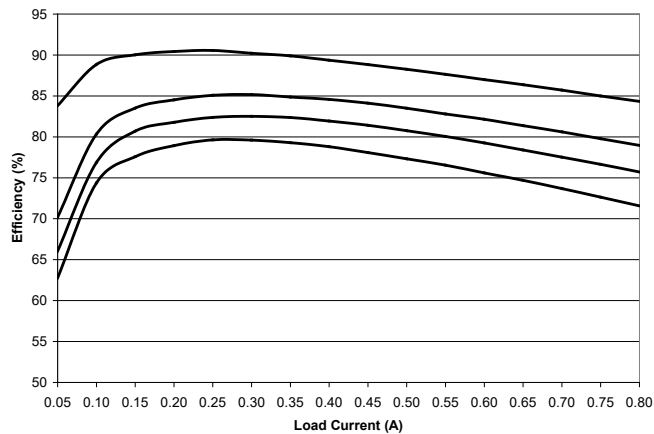
NOTE: $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ unless otherwise noted. Typical values are at $T_A = 25^{\circ}\text{C}$, $V_{IN} = 3.6\text{V}$

$C_{IN} = 4.7\mu\text{F}$ 0603 MLCC, $C_{OUT} = 47\mu\text{F}$ 0805 MLCC

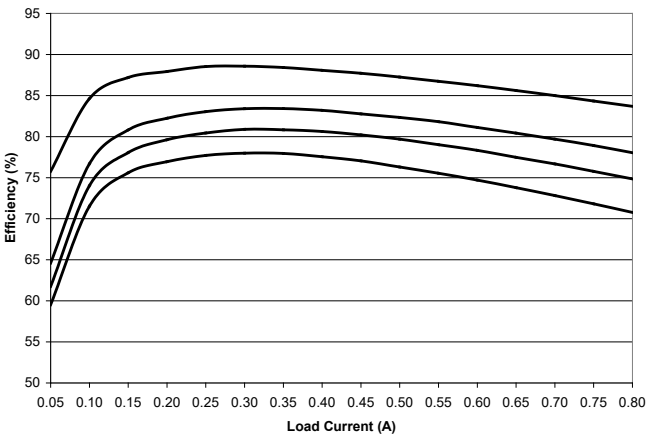
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
VOUT Initial Accuracy (VID Preset Mode)	ΔV_{OUT_initl}	$T_A = 25^{\circ}\text{C}$, $2.4\text{V} \leq V_{IN} \leq 5.5\text{V}$	-2%		+2%	
Line Regulation	ΔV_{OUT_linel}	$2.4\text{V} \leq V_{IN} \leq 5.5\text{V}$		0.0566		%/V
Load Regulation	ΔV_{OUT_load}	$0\text{A} \leq I_{LOAD} \leq 800\text{mA}$		0.0003		%/mA
Temperature Variation	ΔV_{OUT_templ}	$-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$		0.0078		%/ $^{\circ}\text{C}$
Overall V_{OUT} Accuracy (Line, Load, and Temperature combined)	ΔV_{OUT_all}	$2.4\text{V} \leq V_{IN} \leq 5.5\text{V}$ $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ $0\text{A} \leq I_{LOAD} \leq 800\text{mA}$	-3%		+3%	
Dropout Resistance	$R_{DROPOUT}$			400	500	$\text{m}\Omega$
Dynamic Voltage Slew Rate	V_{slew}		0.975	1.5	2.025	V/ms
Continuous Output Current	I_{OUT}	$-20^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$	800 750			mA
Shut-Down Current	I_{SD}	Enable = Low		0.75		μA
PFET OCP Threshold	I_{LIM}			1000		mA
Feedback Pin Voltage	V_{FB}			0.603		V
Feedback Pin Input Current	I_{FB}				100	nA
VS0-VS1, Enable Voltage Threshold	V_{TH}	Pin = Low Pin = High	0.0 1.4		0.4 V_{IN}	
VS0-VS2 Pin Input Current	I_{VSX}			1		nA
Operating Frequency	F_{OSC}			4		MHz
PFET On Resistance	$R_{DS(ON)}$			340		$\text{m}\Omega$
NFET On Resistance	$R_{DS(ON)}$			270		$\text{m}\Omega$
Soft-Start Slew Rate	V_{SS}	VID programming mode	0.975	1.5	2.025	V/ms
V_{OUT} Rise Time	T_{SS}	VFB programming mode	0.784	1.2	1.628	ms

(2) $V_{DO} = I_{OUT} \times R_{DO}$

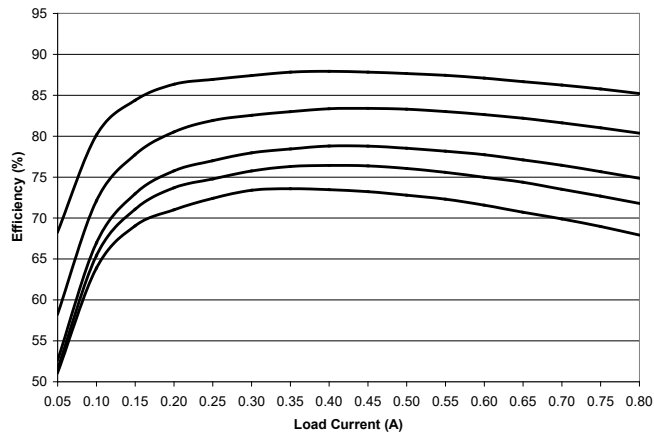
TYPICAL PERFORMANCE CURVES



Efficiency Versus Load; $V_{IN} = 3.3V$,
 V_{OUT} (from top to bottom) 2.5V, 1.8V, 1.5V, 1.2V

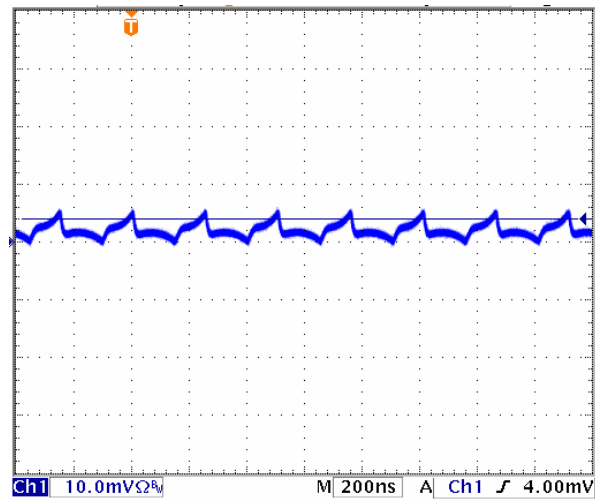


Efficiency Versus Load; $V_{IN} = 3.7V$,
 V_{OUT} (from top to bottom) 2.5V, 1.8V, 1.5V, 1.2V

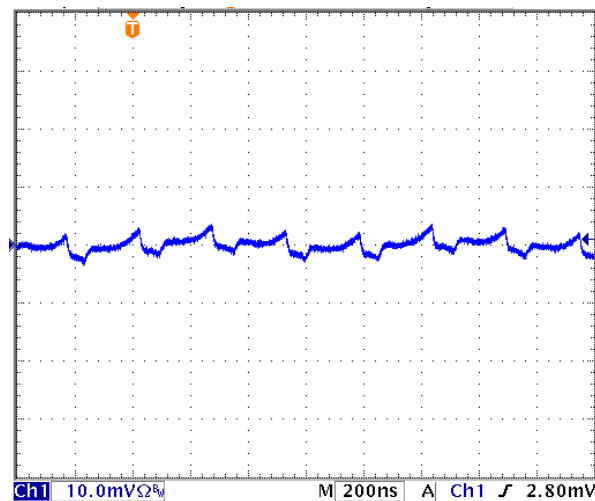
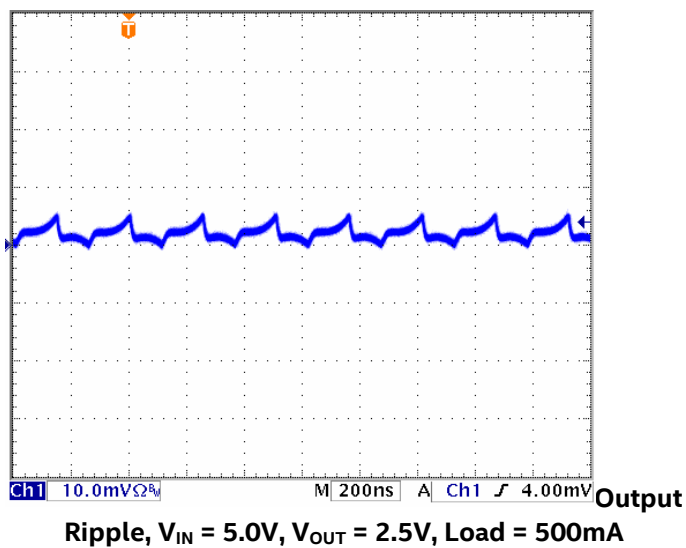


Efficiency Versus Load; $V_{IN} = 5V$,
 V_{OUT} (from top to bottom) 3.3V, 2.5V, 1.8V, 1.5V, 1.2V

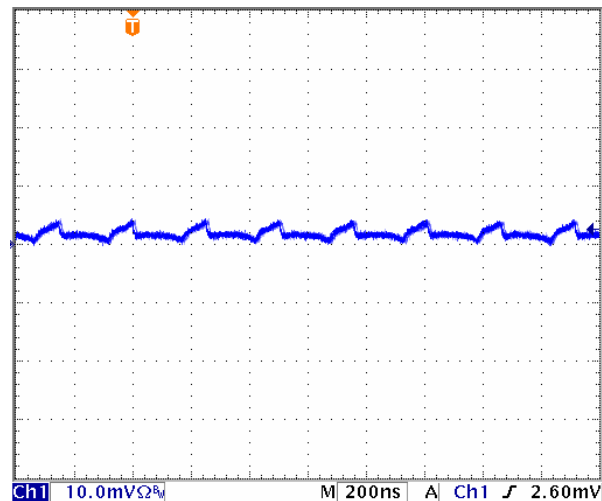
TYPICAL PERFORMANCE CHARACTERISTICS



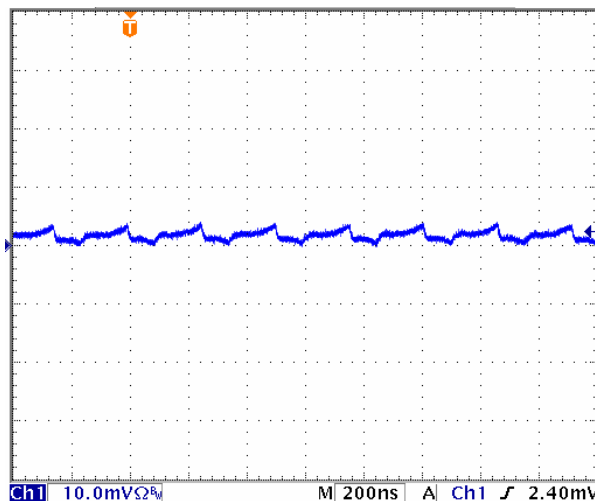
Output Ripple, $V_{IN} = 5.0V$, $V_{OUT} = 1.8V$, Load = 500mA



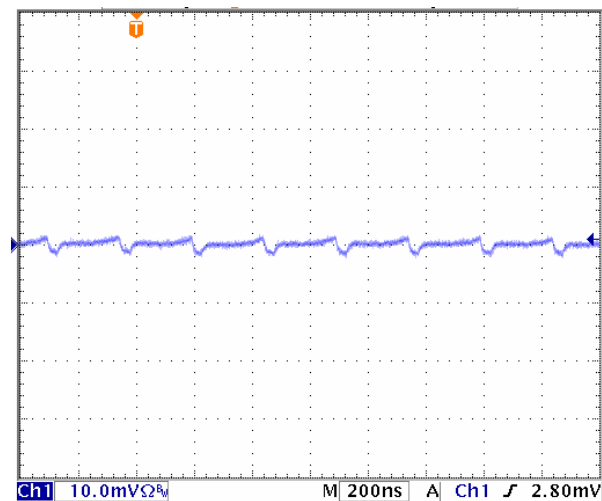
Output Ripple, $V_{IN} = 5.0V$, $V_{OUT} = 3.3V$, Load = 500mA



Output Ripple, $V_{IN} = 3.3V$, $V_{OUT} = 1.2V$, Load = 500mA

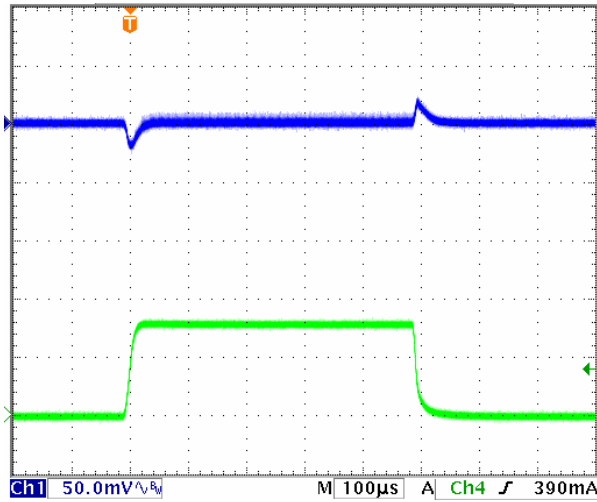


Output Ripple, $V_{IN} = 3.3V$, $V_{OUT} = 1.8V$, Load = 500mA

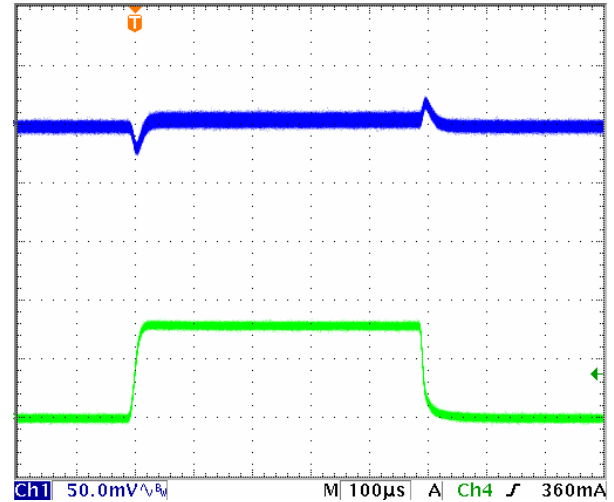


Output Ripple, $V_{IN} = 3.3V$, $V_{OUT} = 2.5V$, Load = 500mA

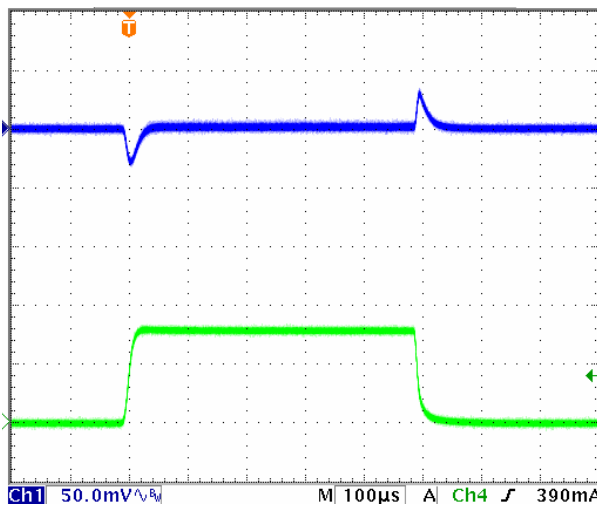
TYPICAL PERFORMANCE CHARACTERISTICS (CONTINUED)



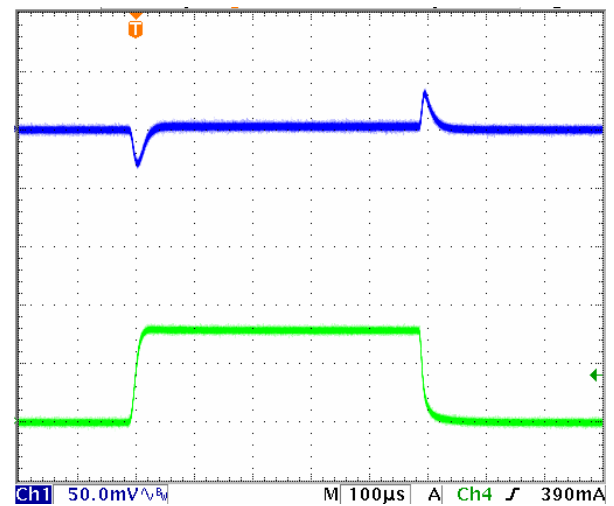
Transient, $V_{IN} = 5.0V$, $V_{OUT} = 1.2V$, Load = 0-800mA



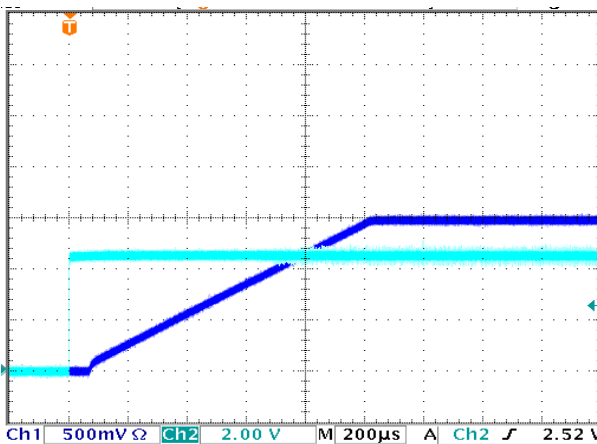
Transient, $V_{IN} = 5.0V$, $V_{OUT} = 3.3V$, Load = 0-800mA



Transient, $V_{IN} = 3.3V$, $V_{OUT} = 1.2V$, Load = 0-800mA

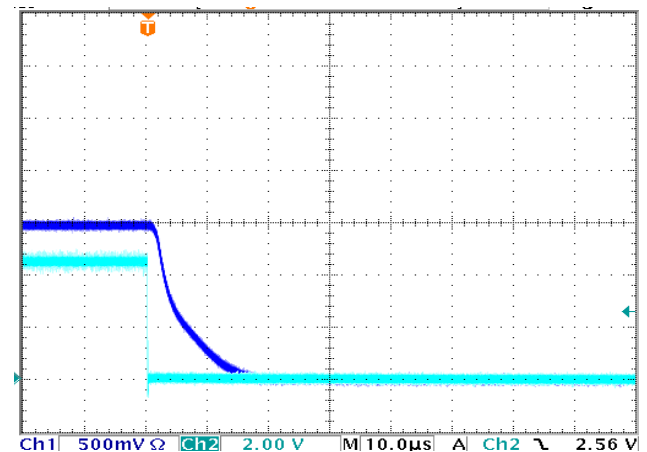


Transient, $V_{IN} = 3.3V$, $V_{OUT} = 1.8V$, Load = 0-800mA



Startup, $V_{IN} = 3.6V$, $V_{OUT} = 1.5V$, Load = 500mA.

Enable in light blue; Vout in Dark blue.



Shutdown, $V_{IN} = 3.6V$, $V_{OUT} = 1.5V$, Load = 500mA.

Enable in light blue; Vout in Dark blue.



FUNCTIONAL DESCRIPTION

Synchronous DC-DC Step-Down PowerSoC

The EP5388QI is a complete DC-DC converter solution requiring only two low cost MLCC capacitors. MOSFET switches, PWM controller, Gate-drive, compensation, and inductor are integrated into the tiny 3mm x 3mm x 1.1mm package to provide the smallest footprint possible while maintaining high efficiency, low ripple, and high performance. The converter uses voltage mode control to provide the simplest implementation and high noise immunity. The device operates at a 4MHz switching frequency. The high switching frequency allows for a wide control loop bandwidth providing excellent transient performance. The high switching frequency further enables the use of very small components making possible this unprecedented level of integration.

Intel Enprion's proprietary power MOSFET technology provides very low switching loss at frequencies of 4 MHz and higher, allowing for the use of very small internal components, and high performance. Integration of the magnetics virtually eliminates the design/layout issues normally associated with switch-mode DC-DC converters. All of this enables much easier and faster incorporation into various applications to meet demanding EMI requirements.

Output voltage is chosen from seven preset values via a three pin VID voltage select scheme. An external divider option enables the selection of any voltage in V_{IN} to 0.6V range. This reduces the number of components that must be qualified and reduces inventory burden. The VID pins can be toggled on the fly to implement glitch free dynamic voltage scaling.

Protection features include under-voltage lock-out (UVLO), over-current protection (OCP), short circuit protection, and thermal overload protection.

Integrated Inductor

Intel Enpirion has introduced the world's first product family featuring integrated inductors. The EP5388QI utilizes a proprietary low loss integrated inductor. The use of an internal inductor localizes the noises associated with the output loop currents. The inherent shielding and compact construction of the integrated inductor reduces the radiated noise that couples into the traces of the circuit board. Further, the package layout is optimized to reduce the electrical path length for the AC ripple currents that are a major source of radiated emissions from DC-DC converters. The integrated inductor significantly reduces parasitic effects that can harm loop stability, and makes layout very simple.

Stable Over Wide Range of Operating Conditions

The EP5388QI utilizes an internal type III compensation network and is designed to provide a high degree of stability over a wide range of operating conditions. The device operates over the entire input and output voltage range with no external modifications required. The very high switching frequency allows for a very wide control loop bandwidth.

Soft Start

Internal soft start circuits limit in-rush current when the device starts up from a power down condition or when the "ENABLE" pin is asserted "high". Digital control circuitry limits the V_{OUT} ramp rate to levels that are safe for the Power MOSFETS and the integrated inductor.

The EP5388QI has two soft start operating modes. When V_{OUT} is programmed using a preset voltage in VID mode, the device has a constant slew rate. When the EP5388QI is configured in external resistor divider mode, the device has a constant V_{OUT} ramp time. Output voltage slew rate and ramp time is given in the Electrical Characteristics Table.

Excess bulk capacitance on the output of the device can cause an over-current condition at startup. Maximum allowable output capacitance depends on the device's minimum current limit, the output current at startup, the minimum soft-start time and the output voltage (all are listed in the Electrical Characteristics Table). The total maximum capacitance on the output rail is estimated by the equation below:

$$C_{OUT_MAX} = 0.7 * (I_{LIMIT} - I_{OUT}) * t_{SS} / V_{OUT}$$

C_{OUT_MAX} = maximum allowable output capacitance

I_{LIMIT} = minimum current limit = 0.8A

I_{OUT} = output current at startup

V_{OUT} = output voltage

0.7 = margin factor

$t_{SS(VFB)}$ = min soft-start time

= 0.784ms ← External feedback setting

$t_{SS(VID)}$ = $V_{OUT} [V] / 2.025 [V/ms]$ ← VID setting

The soft-start time in VID setting is different than External Feedback (VFB) setting, so be sure to use the correct value when calculating the maximum allowable output capacitance.

NOTE: Do not use excessive output capacitance since it may affect device stability. The EP5388QI has high loop bandwidth and 80μF is all that is needed for transient response optimization.

Over Current/Short Circuit Protection

The current limit function is achieved by sensing the current flowing through a sense P-MOSFET which is compared to a reference current. When this level is exceeded the P-FET is turned off and the N-FET is turned on, pulling V_{OUT} low. This condition is maintained for a period of 1ms and then a normal soft start is initiated. If the over current condition still persists, this cycle will repeat in a "hiccup" mode.

Under Voltage Lockout

During initial power up an under voltage lockout circuit will hold-off the switching circuitry until the input voltage reaches a sufficient level to insure proper operation. If the voltage drops below the UVLO threshold the lockout circuitry will again disable the switching. Hysteresis is included to prevent chattering between states.

Enable

The ENABLE pin provides a means to shut down the converter or enable normal operation. A logic low will disable the converter and cause it to shut down. A logic high will enable the converter into normal operation. In shutdown mode, the device quiescent current will be less than 1μA. At extremely cold conditions below -30°C, the controller may not be properly powered if ENABLE is tied directly to AVIN during startup. It is recommended to use an external RC circuit to delay the ENABLE voltage rise so that the internal controller has time to startup into regulation (see circuit below). The RC circuit may be adjusted so that AVIN and PVIN are above UVLO before ENABLE is high. The startup time will be delayed by the extra time it takes for the capacitor voltage to reach the ENABLE threshold.

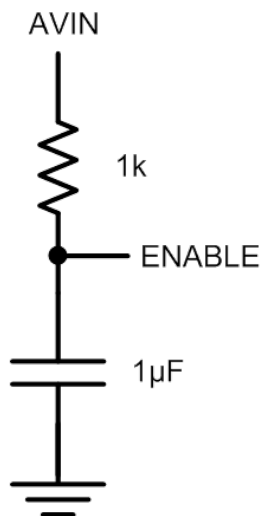


Figure 5. ENABLE Delay Circuit

NOTE: This pin must not be left floating

Thermal Shutdown

When excessive power is dissipated in the chip, the junction temperature rises. Once the junction temperature exceeds the thermal shutdown temperature the thermal shutdown circuit turns off the converter output voltage thus allowing the device to cool. When the junction temperature decreases to a safe operating level, the device will go through the normal startup process. The specific thermal shutdown junction temperature and hysteresis values can be found in the thermal characteristics table.

APPLICATION INFORMATION

Output Voltage Programming

To provide the highest degree of flexibility in choosing output voltage, the EP5388QI uses a 3 pin VID, or Voltage ID, output voltage select arrangement. This allows the designer to choose one of seven preset voltages, or to use an external voltage divider. Internally, the output of the VID multiplexer sets the value for the voltage reference DAC, which in turn is connected to the non-inverting input of the error amplifier. This allows the use of a single feedback divider with constant loop gain and optimum compensation, independent of the output voltage selected.

shows the various VS0-VS2 pin logic states and the associated output voltage levels. A logic “1” indicates a connection to VIN or to a “high” logic voltage level. A logic “0” indicates a connection to ground or to a “low” logic voltage level. These pins can be either hardwired to VIN or GND or alternatively can be driven by standard logic levels. Logic low is defined as $V_{LOW} \leq 0.4V$. Logic high is defined as $V_{HIGH} \geq 1.4V$. Any level between these two values is indeterminate. These pins must not be left floating.

Table 1: VID Voltage Select Settings

VS2	VS1	VS0	V _{OUT}
0	0	0	3.3V
0	0	1	2.5V
0	1	0	1.8V
0	1	1	1.5V
1	0	0	1.25V
1	0	1	1.2V
1	1	0	0.8V
1	1	1	User Selectable

External Voltage Divider

As described above, the external voltage divider option is chosen by connecting the VS0, VS1, and VS2 pins to VIN or logic “high”. The EP5388QI uses a separate feedback pin, VFB, when using the external divider. VSENSE must be connected to VOUT as indicated in Figure 6.

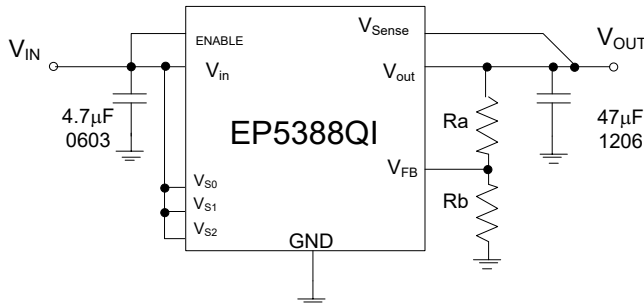


Figure 6. External Divider Application Circuit

The output voltage is selected by the following formula:

$$V_{OUT} = 0.603V \left(1 + \frac{R_a}{R_b}\right)$$

R_a must be chosen as 200k Ω to maintain loop gain. Then R_b is given as:

$$R_b = \frac{1.206 \times 10^5}{V_{OUT} - 0.603} \Omega$$

V_{OUT} can be programmed over the range of 0.6V to $V_{IN}-0.5V$.

Dynamically Adjustable Output

The EP5388QI is designed to allow for dynamic switching between the predefined VID voltage levels. The inter-voltage slew rate is optimized to prevent excess undershoot or overshoot as the output voltage levels transition. The slew rate is identical to the soft-start slew rate of 1.5V/mS.

Dynamic transitioning between internal VID settings and the external divider is not allowed.

Input and Output Capacitors

The **input** capacitance requirement is 4.7 μ F 0603 MLCC. Intel Enpirion recommends that a low ESR MLCC capacitor be used. The input capacitor must use a X5R or X7R or equivalent dielectric formulation. Y5V or equivalent dielectric formulations lose capacitance with frequency, bias, and with temperature, and are not suitable for switch-mode DC-DC converter input filter applications.

A variety of **output** capacitor configurations are possible depending on footprint and ripple requirements. For applications where V_{IN} range is up to 5.5V, it is recommended to use a single 47 μ F 1206 MLCC capacitor. Ripple performance can be improved by using 2 x 22 μ F 0805 MLCC capacitors.

A single 10 μ F 0805 MLCC can be used if V_{OUT} programming is accomplished using an external divider, with the addition of a 10pF phase lead capacitor as shown in Figure 7. Note that in this configuration, V_{SENSE} should NOT be connected to V_{OUT} . This modification is necessary to ensure proper operation of the compensation network over the range of operating conditions.

As described in the Soft Start section, there is a limitation on the maximum bulk capacitance that can be placed on the output of this device. Please refer to the section on Soft Start for more details.

The output capacitor must use a X5R or X7R or equivalent dielectric formulation. Y5V or equivalent dielectric formulations lose capacitance with frequency, bias, and temperature and are not suitable for switch-mode DC-DC converter output filter applications.

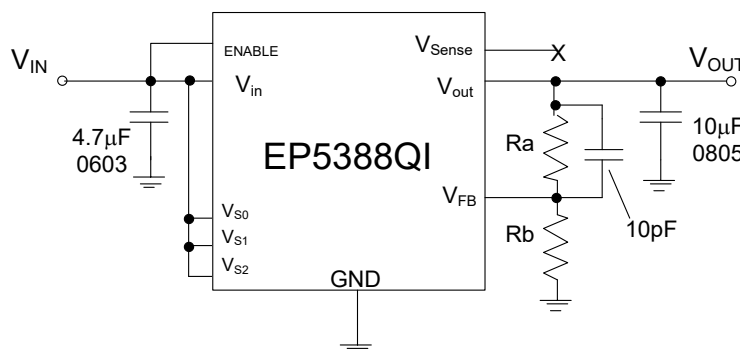


Figure 7. Applications circuit for $C_{OUT} = 1 \times 10\mu F$ 0805

Power-Up/Down Sequencing

During power-up, ENABLE should not be asserted before VIN. During power down, the VIN should not be powered down before the ENABLE. Tying PVIN and ENABLE together during power-up or power-down meets this requirement.

Pre-Bias Start-up

The EP5388QI does not support startup into a pre-biased condition. Be sure the output capacitors are not charged or the output of the EP5388QI is not pre-biased when the EP5388QI is first enabled.

LAYOUT RECOMMENDATIONS

Figure 8 shows critical components and layer 1 traces of a recommended minimum footprint EP5388QI layout. ENABLE configurations and other small signal pins need to be connected and routed according to specific customer application. Please see the Gerber files on the Intel website www.intel.com/enpirion for exact dimensions and other layers. Please refer to Figure 8 while reading the layout recommendations in this section.

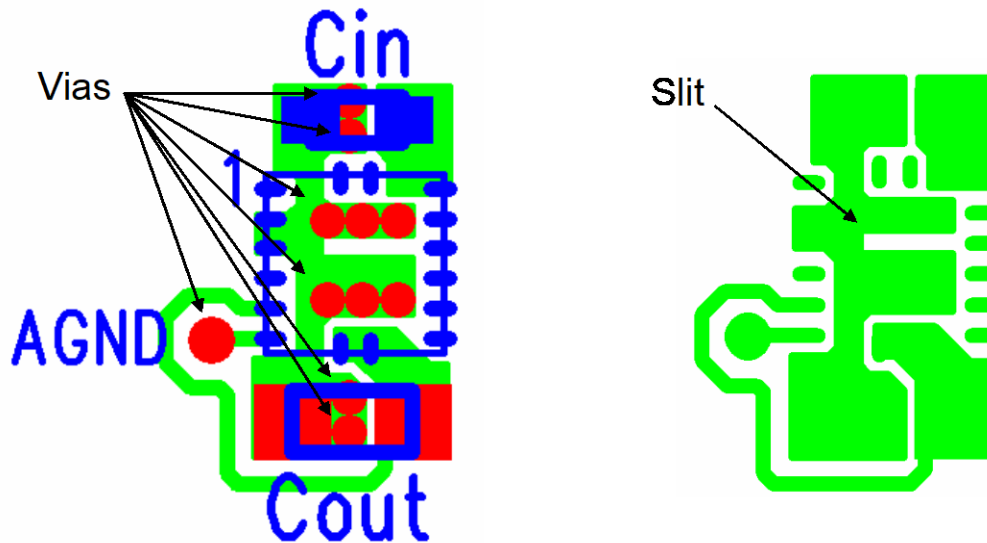


Figure 8: PCB Layer Critical Components and Copper for Minimum Footprint

Recommendation 1: The input and output filter capacitors should be placed as close to the EP5388QI as possible to reduce EMI from input and output loop AC currents. This reduces the physical area of these AC current loops.

Recommendation 2: The system ground plane should be the first layer immediately below the surface layer (PCB layer 2). If it is not possible to make PCB layer 2 the system ground plane, a local ground island should be created on PCB layer 2 under the Altera Enpirion device and including the area under the input and output filter capacitors. This ground plane, or ground island, should be continuous and uninterrupted underneath the Altera Enpirion device and the input and output filter capacitors.

Recommendation 3: The surface layer ground pour should include a “slit” as shown in Figure 8 to separate the input and output AC loop currents. This will help reduce noise coupling from the input current loop to the output current loop.

Recommendation 4: Multiple small vias (approximately 0.25mm finished diameter) should be used to connect the ground terminals of the input and output capacitors, and the surface ground pour under the device, to the system ground plane. If a local ground island is used on PCB layer 2, the vias should connect to the ground island and continue down to the PCB system ground plane.

Recommendation 5: The AGND pin should be connected to the system ground plane using a via as described in recommendation 4. AGND must NOT be connected to the surface layer ground pour.

Recommendation 6: As with any switch-mode DC-DC converter, do not run any sensitive signal or control lines under the converter package.

RECOMMENDED PCB FOOTPRIN

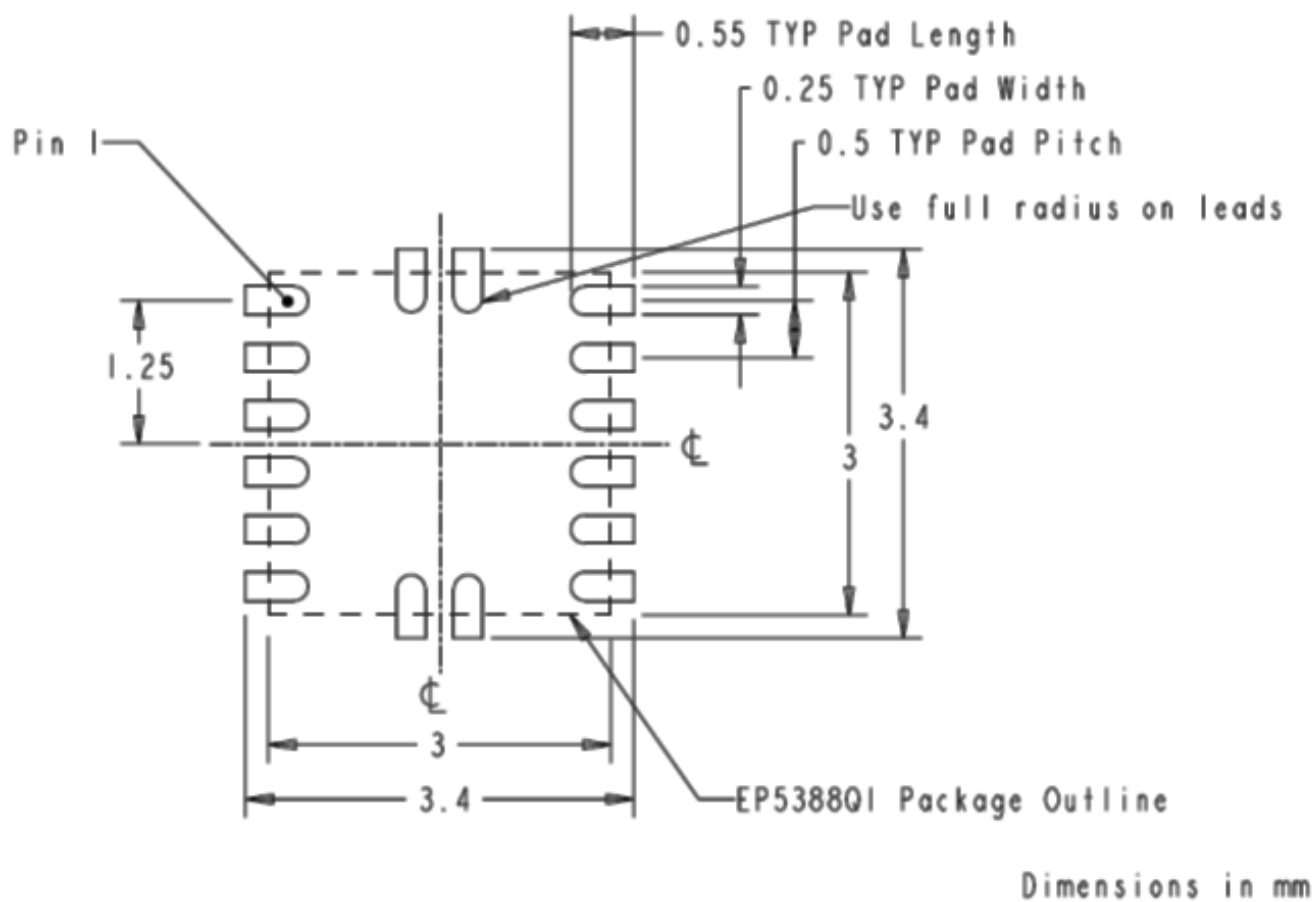


Figure 9: EP5388QI PCB Footprint (Top View)

PACKAGE DIMENSIONS

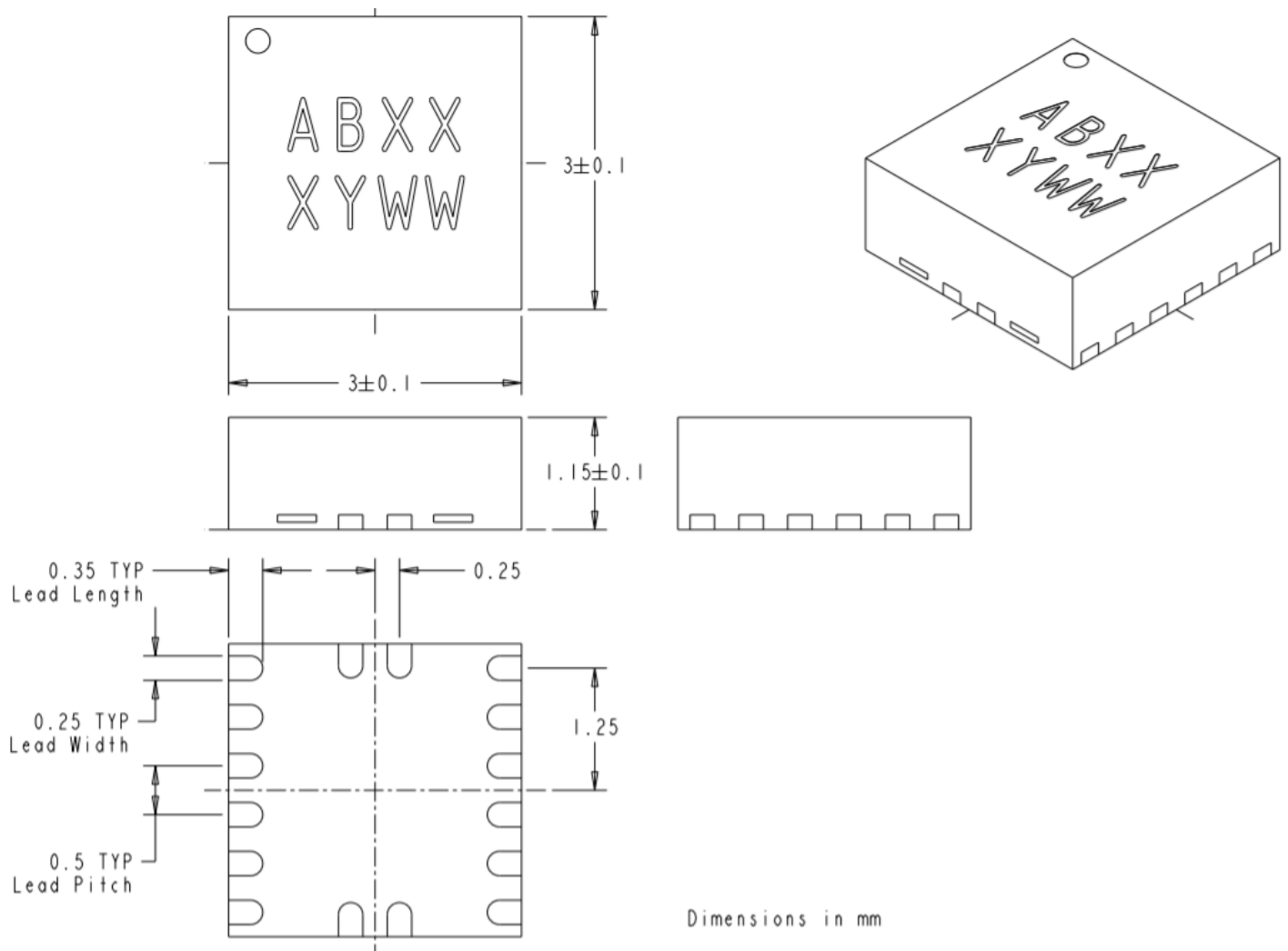


Figure 10: EP5388QI Package Dimensions

Packing and Marking Information: <https://www.intel.com/support/quality-and-reliability/packing.html>

REVISION HISTORY

Rev	Date	Change(s)
F	June, 2017	Max Bulk Cap (C_{OUT_MAX}) equation updated to reflect loading and startup time (with margin added)
G	Dec, 2017	Revision History added
H	Dec, 2018	Changed datasheet into Intel format.

WHERE TO GET MORE INFORMATION

For more information about Intel® and Enpirion® PowerSoCs, visit:

www.intel.com/enpirion