Driver Output Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
C_{out}	Output Capacitance		2500		pF
R_{out}	Output Resistance		.8		Ω
L_{out}	Output Inductance		3		nH
F_{MAX}	Operating Frequency CL = 3000nF + 50Ω	30			MHz
F_{MAX}	Operating Frequency RL = 50Ω	50			

Driver Thermal Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
$R_{\theta JC}$	Thermal Resistance Junction to Case		1.5		°C/W
$R_{\theta JHS}$	Thermal Resistance Junction to Heat Sink		2.5		
T_{JSTG}	Storage Temperature		-55 to 150		°C
P_{DJHS}	Maximum Power Dissipation @ T_{SINK} = 25°C		60		W
P_{DJC}	Total Power Dissipation @ T_C = 25°C		100		

MOSFET Absolutes Maximum Ratings (Per-Section)

Symbol	Parameter	Min	Typ	Max	Unit
BV_{DSS}	Drain Source Voltage	1000			V
I_D	Continuous Drain Current T_{HS} = 25°C			15	A
$R_{DS(on)}$	Drain-Source On State Resistance		1		Ω
T_{jmax}	Operating Temperature			175	°C

MOSFET Dynamic Characteristics (Per-Section)

Symbol	Parameter	Min	Typ	Max	Unit
C_{iss}	Input Capacitance		1800		pF
C_{oss}	Output Capacitance		335		
C_{rss}	Reverse Transfer Capacitance		75		

MOSFET Thermal Characteristics (Total Package)

Symbol	Parameter	Min	Type	Max	Unit
$R_{\theta JC}$	Junction to Case Thermal Resistance		.06		°C/W
$R_{\theta JHS}$	Junction to Heat Sink Thermal Resistance		.14		
T_{JSTG}	Storage Junction Temperature		-55 to 150		°C
P_{DHS}	Maximum Power Dissipation @ T_{SINK} = 25°C		1.07		KW
P_{DC}	Total Power Dissipation @ T_C = 25°C		2.5		

Section A and B Output Switching Performance

Symbol	Characteristic	Min	Typ	Max	Unit
T_{ON}	Leading Edge 10% to 90%	2	3	4	ns
T_{OFF}	Trailing Edge 10% to 90%	45	TBD	49	
$T_{DLY(ON)}$	Total Throughput Delay Time, ON	45	TBD	47	
$T_{DLY(OFF)}$	Total Throughput Delay Time, OFF	49	50	51	
$\Delta T_{DLY(ON)}$	Delta T_{ON} Delay between Section A and B	-0.5	0	1.5	
$\Delta T_{DLY(OFF)}$	Delta T_{OFF} Delay between Section A and B	0	0.6	1.3	

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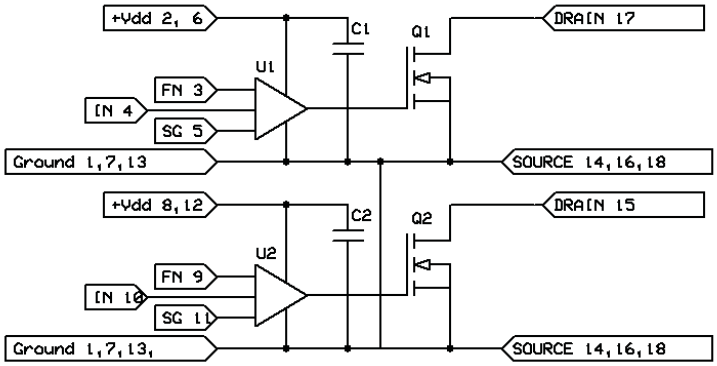

Figure 1, DRF1301 Circuit Diagram

The DRF1301 is configured as a Push Pull Hybrid incorporating two independent channels configured with a common source each consisting of a driver, a high voltage MOSFET and by-pass capacitors. The function of the by-pass capacitors C1 and C2 is to reduce the internal parasitic loop inductance. This coupled with the tight geometry of the hybrid allows optimal gate drive to the MOSFET. This low parasitic approach coupled with the Schmitt trigger input (IN), Kelvin signal ground (SG) and the Anti-Ring function; provide improved stability and control in Kilowatt to Multi-Kilowatt high frequency applications. The IN pin should be referenced to the Kelvin Ground (SG) and is applied to a Schmitt Trigger. The SG pin is a Kelvin return for the IN pin only. The signal is then applied to the intermediate drivers and level shifters; this section contains proprietary circuitry designed specifically for ring abatement. To further increase the utility of the device the driver die and the MOSFET die are adjacent die selected. This provides a very close match in the turn on and propagation delays.

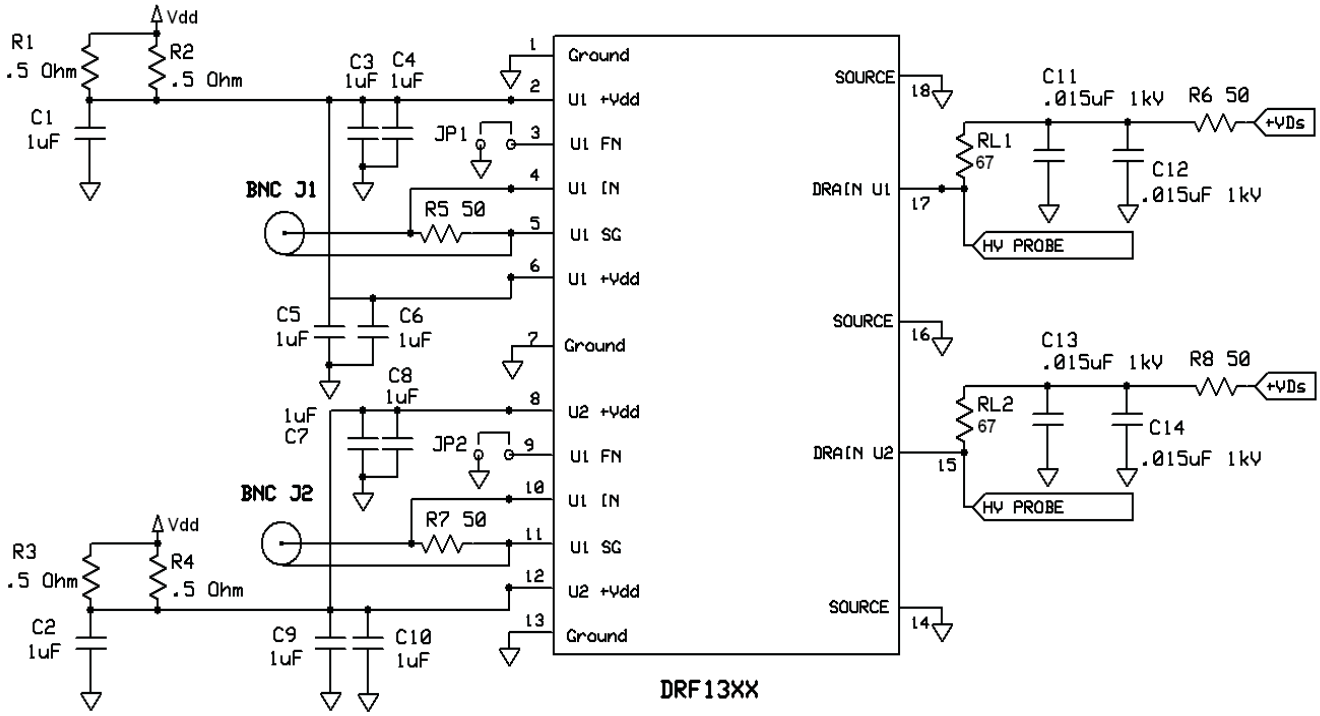

Figure 2, DRF1301 Test Circuit

The test circuit illustrated in Figure 2 was used to evaluate the DRF1301 (available as an evaluation board DRF13XX/EVALSW.) The input control signal is applied via IN and SG pins using RG188. This provides excellent noise immunity and control of the signal ground currents. The $+V_{DD}$ inputs (pins 2, 6, 8 and 12) should be heavily by-passed by 1uF capacitors as close to the pins as possible. The capacitors used for this function must be capable of supporting the RMS currents and frequency of the gate load. R_L set for I_{DM} at V_{DS} max this load is used to evaluate the output performance.

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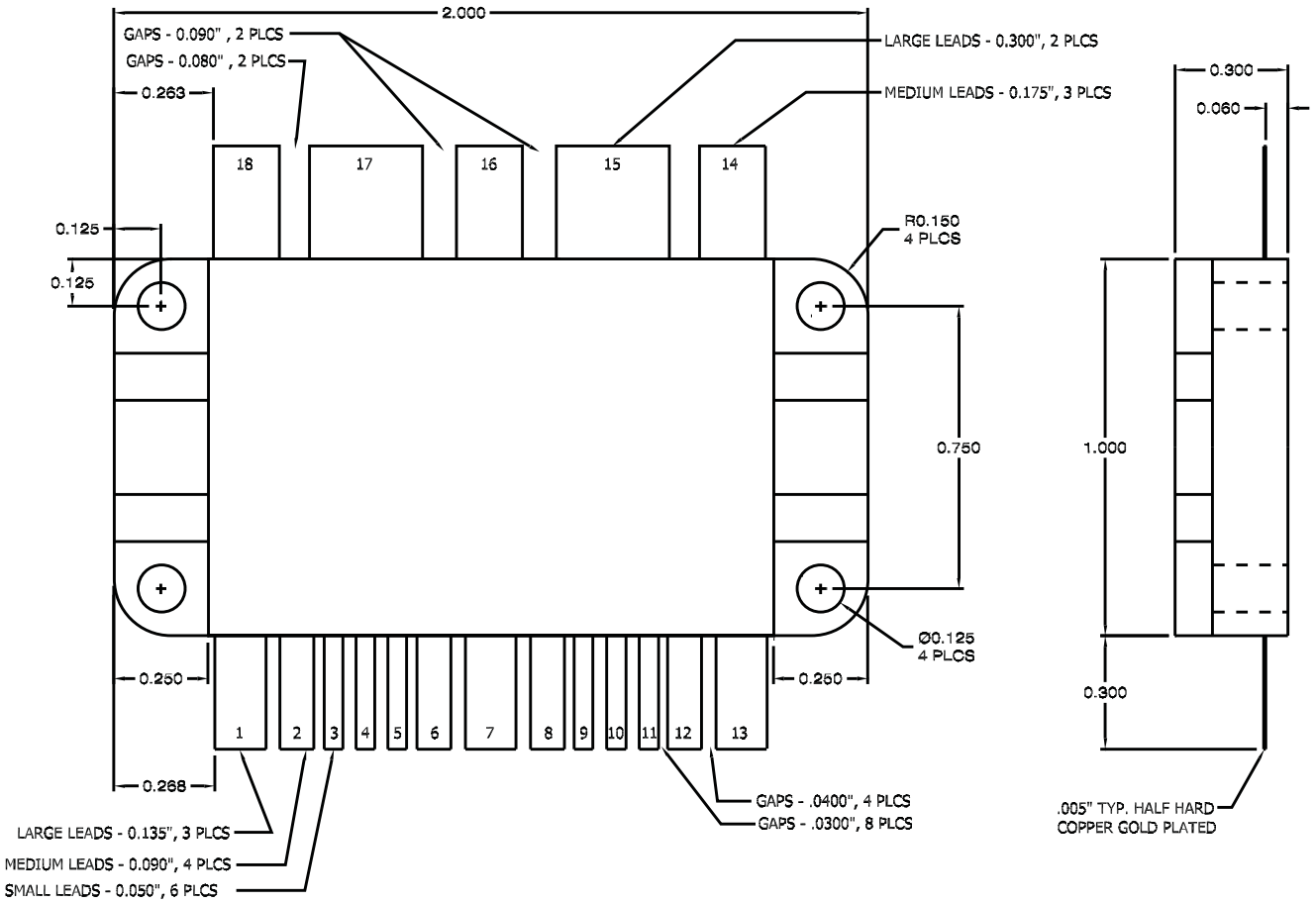
Pin Assignments	
Pin 1	Ground
Pin 2	U1 +Vdd
Pin 3	U1 FN
Pin 4	U1 IN
Pin 5	U1 SG
Pin 6	U1 +Vdd
Pin 7	Ground
Pin 8	U2 +Vdd
Pin 9	U2 FN
Pin 10	U2 IN
Pin 11	U2 SG
Pin 12	U2 +Vdd
Pin 13	Ground
Pin 14	Source
Pin 15	U2 Drain
Pin 16	Source
Pin 17	U1 Drain
Pin 18	Source

None of the inputs to U1 or U2 of the DRF1300 are isolated for direct connection to a ground referenced power supply or control circuitry. **Isolation appropriate to the application is the responsibility of the end user.** It is imperative that high output currents be restricted to the Source (14, 16, 18) and drain (15, 17) pins by design. See DRF100 for more information on Driver IC used in the device.

The Function (FN, pin 3 or pin 9) is the invert or non-invert select Pin, it is Internally held high.

Truth Table * Referenced to SG		
FN (pin 3)	**IN (pin 4)**	**MOSFET U1**
HIGH	**HIGH**	**ON**
HIGH	**LOW**	**OFF**
LOW	**HIGH**	**OFF**
LOW	**LOW**	**ON**

Truth Table * Referenced to SG		
FN (pin 9)	**IN (pin 10)**	**MOSFET U2**
HIGH	**HIGH**	**ON**
HIGH	**LOW**	**OFF**
LOW	**HIGH**	**OFF**
LOW	**LOW**	**ON**



All dimensions are ± .005

Figure 4, DRF1301 Mechanical Outline

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