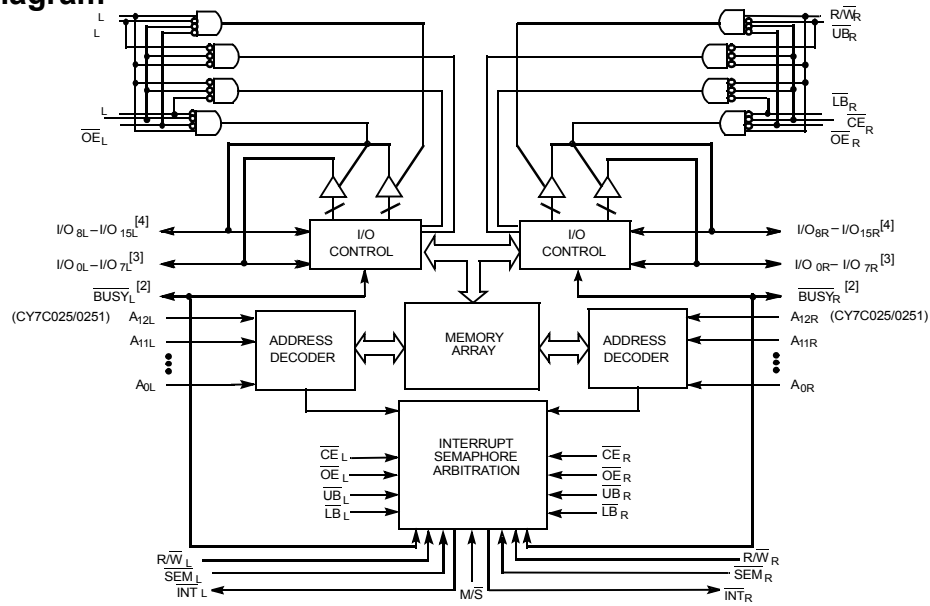
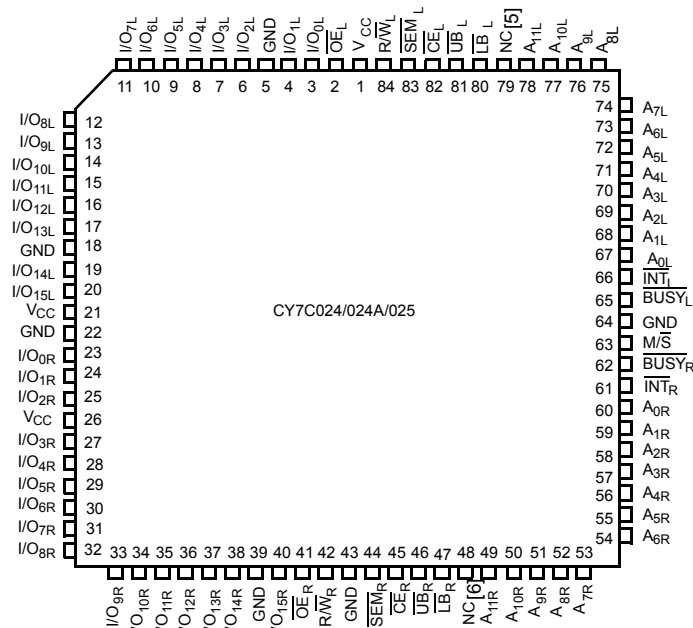


## Logic Block Diagram



## Pin Configurations

Figure 1. 84-Pin PLCC (Top View)

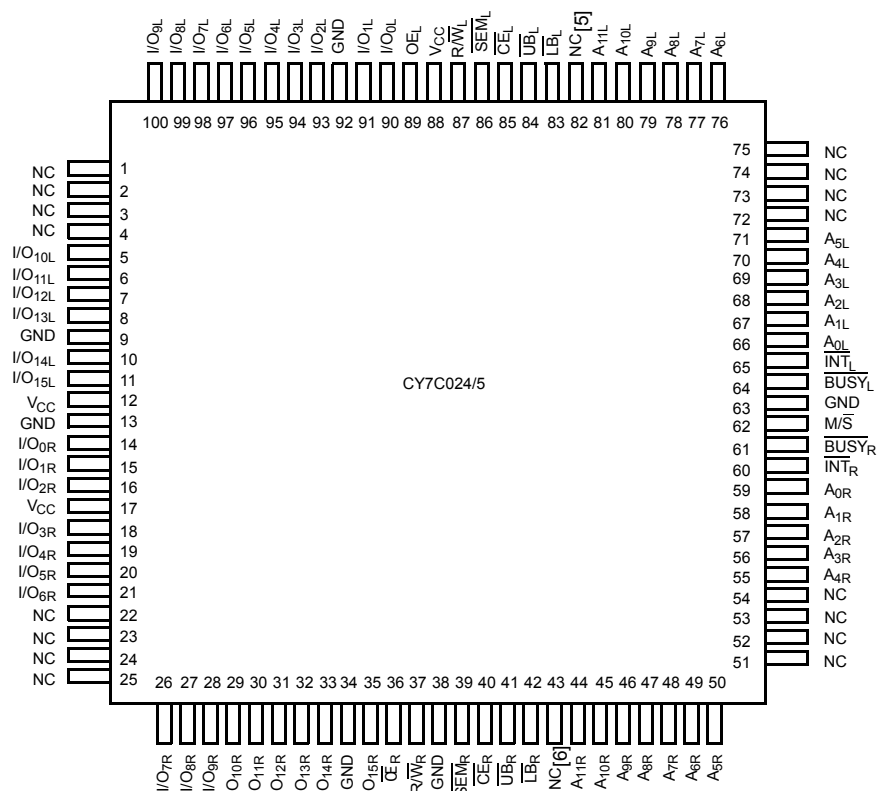


### Notes

2. BUSY is an output in master mode and an input in slave mode.
3. I/O<sub>0</sub>–I/O<sub>8</sub> on the CY7C0241/0251.
4. I/O<sub>9</sub>–I/O<sub>17</sub> on the CY7C0241/0251.
5. A<sub>12L</sub> on the CY7C025/0251.
6. A<sub>12R</sub> on the CY7C025/0251.

## Pin Configurations (continued)

**Figure 2. 100-Pin TQFP (Top View)**



## Pin Definitions

Left Port	Right Port	Description
CE <sub>L</sub>	CE <sub>R</sub>	Chip Enable
R/W <sub>L</sub>	R/W <sub>R</sub>	Read/Write Enable
OE <sub>L</sub>	OE <sub>R</sub>	Output Enable
A <sub>0L</sub> –A <sub>11/12L</sub>	A <sub>0R</sub> –A <sub>11/12R</sub>	Address
I/O <sub>0L</sub> –I/O <sub>15/17L</sub>	I/O <sub>0R</sub> –I/O <sub>15/17R</sub>	Data Bus Input/Output
SEM <sub>L</sub>	SEM <sub>R</sub>	Semaphore Enable
UB <sub>L</sub>	UB <sub>R</sub>	Upper Byte Select
LB <sub>L</sub>	LB <sub>R</sub>	Lower Byte Select
INT <sub>L</sub>	INT <sub>R</sub>	Interrupt Flag
BUSY <sub>L</sub>	BUSY <sub>R</sub>	Busy Flag
M/S		Master or Slave Select
V <sub>CC</sub>		Power
GND		Ground

## Selection Guide

Parameter	7C024/024A/0241–15 7C025/0251–15	7C024/0241–25 7C025/0251–25	7C024/0241–35 7C025/0251–35	7C024/0241–55 7C025/0251–55
Maximum Access Time (ns)	15	25	35	55
Typical Operating Current (mA)	190	170	160	150
Typical Standby Current for I <sub>SB1</sub> (mA)	50	40	30	20

## Architecture

The CY7C024/024A/0241 and CY7C025/0251 consist of an array of 4K words of 16/18 bits each and 8K words of 16/18 bits each of dual-port RAM cells, I/O and address lines, and control signals (CE, OE, R/W). These control pins permit independent access for reads or writes to any location in memory. To handle simultaneous writes/reads to the same location, a BUSY pin is provided on each port. Two interrupt (INT) pins can be used for port-to-port communication. Two semaphore (SEM) control pins are used for allocating shared resources. With the M/S pin, the CY7C024/024A/0241 and CY7C025/0251 can function as a master (BUSY pins are outputs) or as a slave (BUSY pins are inputs). The CY7C024/024A/0241 and CY7C025/0251 have an automatic power down feature controlled by  $\overline{CE}$ . Each port is provided with its own output enable control ( $\overline{OE}$ ), which allows data to be read from the device.

## Functional Description

### Write Operation

Data must be set up for a duration of  $t_{SD}$  before the rising edge of R/W to guarantee a valid write. A write operation is controlled by either the R/W pin (see Figure 7) or the CE pin (see Figure 8). Required inputs for non contention operations are summarized in Table 1.

If a location is being written to by one port and the opposite port attempts to read that location, a port-to-port flowthrough delay must occur before the data is read on the output; otherwise the data read is not deterministic. Data is valid on the port  $t_{DD}$  after the data is presented on the other port.

### Read Operation

When reading the device, the user must assert both the  $\overline{OE}$  and CE pins. Data is available  $t_{ACE}$  after CE or  $t_{DOE}$  after OE is asserted. If the user of the CY7C024/024A/0241 or CY7C025/0251 wishes to access a semaphore flag, then the SEM pin must be asserted instead of the CE pin, and OE must also be asserted.

### Interrupts

The upper two memory locations may be used for message passing. The highest memory location (FFF for the CY7C024/024A/0241, 1FFF for the CY7C025/0251) is the mailbox for the right port and the second-highest memory location (FFE for the CY7C024/024A/0241, 1FFE for the CY7C025/0251) is the mailbox for the left port. When one port writes to the other port's mailbox, an interrupt is generated to the owner. The interrupt is reset when the owner reads the contents of the mailbox. The message is user defined.

Each port can read the other port's mailbox without resetting the interrupt. The active state of the BUSY signal (to a port) prevents the port from setting the interrupt to the winning port. Also, an active BUSY to a port prevents that port from reading its own mailbox and thus resetting the interrupt to it.

If your application does not require message passing, do not connect the interrupt pin to the processor's interrupt request input pin.

The operation of the interrupts and their interaction with Busy are summarized in Table 2 on page 5.

### Busy

The CY7C024/024A/0241 and CY7C025/0251 provide on-chip arbitration to resolve simultaneous memory location access (contention). If both ports' CEs are asserted and an address match occurs within  $t_{PS}$  of each other, the busy logic determines which port has access. If  $t_{PS}$  is violated, one port definitely gains permission to the location, but which one is not predictable. BUSY is asserted  $t_{BLA}$  after an address match or  $t_{BLC}$  after CE is taken LOW.

### Master/Slave

A M/S pin is provided to expand the word width by configuring the device as either a master or a slave. The BUSY output of the master is connected to the BUSY input of the slave. This allows the device to interface to a master device with no external components. Writing to slave devices must be delayed until after the BUSY input has settled ( $t_{BLC}$  or  $t_{BLA}$ ). Otherwise, the slave chip may begin a write cycle during a contention situation. When tied HIGH, the M/S pin allows the device to be used as a master and, therefore, the BUSY line is an output. BUSY can then be used to send the arbitration outcome to a slave.

### Semaphore Operation

The CY7C024/024A/0241 and CY7C025/0251 provide eight semaphore latches, which are separate from the dual-port memory locations. Semaphores are used to reserve resources that are shared between the two ports. The state of the semaphore indicates that a resource is in use. For example, if the left port wants to request a given resource, it sets a latch by writing a zero to a semaphore location. The left port then verifies its success in setting the latch by reading it. After writing to the semaphore, SEM or OE must be deasserted for  $t_{SOP}$  before attempting to read the semaphore. The semaphore value is available  $t_{SWRD} + t_{DOE}$  after the rising edge of the semaphore write. If the left port was successful (reads a zero), it assumes control of the shared resource, otherwise (reads a one) it assumes the right port has control and continues to poll the semaphore. When the right side has relinquished control of the semaphore (by writing a one), the left side succeeds in gaining control of the semaphore. If the left side no longer requires the semaphore, a one is written to cancel its request.



Semaphores are accessed by asserting  $\overline{\text{SEM}}$  LOW. The  $\overline{\text{SEM}}$  pin functions as a chip select for the semaphore latches (CE must remain HIGH during SEM LOW). A0–2 represents the semaphore address. OE and R/W are used in the same manner as a normal memory access. When writing or reading a semaphore, the other address pins have no effect.

When writing to the semaphore, only I/O<sub>0</sub> is used. If a zero is written to the left port of an available semaphore, a one appears at the same semaphore address on the right port. That semaphore can now only be modified by the side showing zero (the left port in this case). If the left port now relinquishes control by writing a one to the semaphore, the semaphore is set to one

for both sides. However, if the right port had requested the semaphore (written a zero) while the left port had control, the right port immediately owns the semaphore as soon as the left port released it. Table 3 shows sample semaphore operations.

When reading a semaphore, all sixteen/eighteen data lines output the semaphore value. The read value is latched in an output register to prevent the semaphore from changing state during a write from the other port. If both ports attempt to access the semaphore within t<sub>SPS</sub> of each other, the semaphore is definitely obtained by one side or the other, but there is no guarantee which side controls the semaphore

**Table 1. Non-Contending Read/Write**

Inputs						Outputs		Operation
CE	R/W	OE	UB	LB	SEM	I/O <sub>0</sub> –I/O <sub>7</sub> <sup>[3]</sup>	I/O <sub>8</sub> –I/O <sub>15</sub> <sup>[4]</sup>	
H	X	X	X	X	H	High Z	High Z	Deselected: Power Down
X	X	X	H	H	H	High Z	High Z	Deselected: Power Down
L	L	X	L	H	H	High Z	Data In	Write to Upper Byte Only
L	L	X	H	L	H	Data In	High Z	Write to Lower Byte Only
L	L	X	L	L	H	Data In	Data In	Write to Both Bytes
L	H	L	L	H	H	High Z	Data Out	Read Upper Byte Only
L	H	L	H	L	H	Data Out	High Z	Read Lower Byte Only
L	H	L	L	L	H	Data Out	Data Out	Read Both Bytes
X	X	H	X	X	X	High Z	High Z	Outputs Disabled
H	H	L	X	X	L	Data Out	Data Out	Read Data in Semaphore Flag
X	H	L	H	H	L	Data Out	Data Out	Read Data in Semaphore Flag
H		X	X	X	L	Data In	Data In	Write D <sub>IN0</sub> into Semaphore Flag
X		X	H	H	L	Data In	Data In	Write D <sub>IN0</sub> into Semaphore Flag
L	X	X	L	X	L			Not Allowed
L	X	X	X	L	L			Not Allowed

**Table 2. Interrupt Operation Example (Assumes  $\overline{\text{BUSY}}_L = \overline{\text{BUSY}}_R = \text{HIGH}$ )<sup>[7]</sup>**

Function	Left Port					Right Port				
	R/W <sub>L</sub>	CE <sub>L</sub>	OE <sub>L</sub>	A <sub>0L–11L</sub>	INT <sub>L</sub>	R/W <sub>R</sub>	CE <sub>R</sub>	OE <sub>R</sub>	A <sub>0R–11R</sub>	INT <sub>R</sub>
Set Right $\overline{\text{INT}}_R$ Flag	L	L	X	(1)FFF	X	X	X	X	X	L <sup>[9]</sup>
Reset Right $\overline{\text{INT}}_R$ Flag	X	X	X	X	X	X	L	L	(1)FFF	H <sup>[8]</sup>
Set Left $\overline{\text{INT}}_L$ Flag	X	X	X	X	L <sup>[8]</sup>	L	L	X	(1)FFE	X
Reset Left $\overline{\text{INT}}_L$ Flag	X	L	L	(1)FFE	H <sup>[9]</sup>	X	X	X	X	X

**Table 3. Semaphore Operation Example**

Function	I/O <sub>0</sub> –I/O <sub>15/17</sub> Left	I/O <sub>0</sub> –I/O <sub>15/17</sub> Right	Status
No action	1	1	Semaphore-free
Left port writes 0 to semaphore	0	1	Left Port has semaphore token
Right port writes 0 to semaphore	0	1	No change. Right side has no write access to semaphore.
Left port writes 1 to semaphore	1	0	Right port obtains semaphore token
Left port writes 0 to semaphore	1	0	No change. Left port has no write access to semaphore
Right port writes 1 to semaphore	0	1	Left port obtains semaphore token
Left port writes 1 to semaphore	1	1	Semaphore-free
Right port writes 0 to semaphore	1	0	Right port has semaphore token
Right port writes 1 to semaphore	1	1	Semaphore-free
Left port writes 0 to semaphore	0	1	Left port has semaphore token
Left port writes 1 to semaphore	1	1	Semaphore-free

**Notes**

7. A<sub>0L-12L</sub> and A<sub>0R-12R</sub>, 1FFF/1FFE for the CY7C025.

8. If BUSY<sub>R</sub>=L, then no change.

9. If BUSY<sub>L</sub>=L, then no change.

## Maximum Ratings <sup>[10]</sup>

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage Temperature ..... -65°C to +150°C

Ambient Temperature with  
Power Applied ..... -55°C to +125°C

Supply Voltage to Ground Potential.....-0.3V to +7.0V

DC Voltage Applied to Outputs  
in High-Z State.....-0.5V to +7.0V

DC Input Voltage<sup>[11]</sup>.....-0.5V to +7.0V

Output Current into Outputs (LOW)..... 20 mA

Static Discharge Voltage..... > 2001V  
(per MIL-STD-883, Method 3015)

Latch Up Current ..... > 200 mA

## Operating Range

Range	Ambient Temperature	V <sub>CC</sub>
Commercial	0°C to +70°C	5V ± 10%
Industrial	-40°C to +85°C	5V ± 10%

## Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	7C024/024A/0241-15 7C025/0251-15			7C024/024A/0241-25 7C025/0251-25			Unit
			Min	Typ	Max	Min	Typ	Max	
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = Min, I <sub>OH</sub> = -4.0 mA	2.4			2.4			V
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = Min, I <sub>OL</sub> = 4.0 mA			0.4			0.4	V
V <sub>IH</sub>	Input HIGH Voltage		2.2			2.2			V
V <sub>IL</sub>	Input LOW Voltage		-0.7		0.8	-0.7		0.8	V
I <sub>IX</sub>	Input Leakage Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>	-10		+10	-10		+10	μA
I <sub>OZ</sub>	Output Leakage Current	Output Disabled, GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub>	-10		+10	-10		+10	μA
I <sub>CC</sub>	Operating Current	V <sub>CC</sub> = Max, I <sub>OUT</sub> = 0 mA, Outputs Disabled	Com'l	190	300		170	250	mA
			Ind	200	320		170	290	
I <sub>SB1</sub>	Standby Current (Both Ports TTL Levels)	CE <sub>L</sub> and CE <sub>R</sub> ≥ V <sub>IH</sub> , f = f <sub>MAX</sub> <sup>[12]</sup>	Com'l	50	70		40	60	mA
			Ind	50	70			75	
I <sub>SB2</sub>	Standby Current (One Port TTL Level)	CE <sub>L</sub> or CE <sub>R</sub> ≥ V <sub>IH</sub> , f = f <sub>MAX</sub> <sup>[12]</sup>	Com'l	120	180		100	150	mA
			Ind	120	180		100	170	
I <sub>SB3</sub>	Standby Current (Both Ports CMOS Levels)	Both Ports CE and CE <sub>R</sub> ≥ V <sub>CC</sub> - 0.2V, V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2V or V <sub>IN</sub> ≤ 0.2V, f = 0 <sup>[12]</sup>	Com'l	3	15		3	15	mA
			Ind	3	15		3	15	
I <sub>SB4</sub>	Standby Current (Both Ports CMOS Levels)	One Port CE <sub>L</sub> or CE <sub>R</sub> ≥ V <sub>CC</sub> - 0.2V, V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2V or V <sub>IN</sub> ≤ 0.2V, Active Port Outputs, f = f <sub>MAX</sub> <sup>[12]</sup>	Com'l	110	160		90	130	mA
			Ind	110	160		90	150	

## Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	7C024/024A/0241-35 7C025/0251-35			7C024/024A/0241-55 7C025/0251-55			Unit
			Min	Typ	Max	Min	Typ	Max	
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = Min, I <sub>OH</sub> = -4.0 mA	2.4			2.4			V
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = Min, I <sub>OL</sub> = 4.0 mA			0.4			0.4	V
V <sub>IH</sub>	Input HIGH Voltage		2.2			2.2			V
V <sub>IL</sub>	Input LOW Voltage		-0.7		0.8	-0.7		0.8	V
I <sub>IX</sub>	Input Leakage Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>	-10		+10	-10		+10	μA
I <sub>OZ</sub>	Output Leakage Current	Output Disabled, GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub>	-10		+10	-10		+10	μA

### Notes

10. The voltage on any input or I/O pin cannot exceed the power pin during power up

11. Pulse width < 20 ns.

12. f<sub>MAX</sub> = 1/t<sub>RC</sub> = All inputs cycling at f = 1/t<sub>RC</sub> (except output enable). f = 0 means no address or control lines change. This applies only to inputs at CMOS level standby I<sub>SB3</sub>.

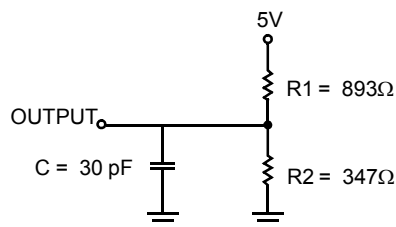
**Electrical Characteristics** Over the Operating Range (continued)

Parameter	Description	Test Conditions		7C024/024A/0241–35 7C025/0251–35			7C024/024A/0241–55 7C025/0251–55			Unit
				Min	Typ	Max	Min	Typ	Max	
$I_{CC}$	Operating Current	$V_{CC} = \text{Max}$ , $I_{OUT} = 0 \text{ mA}$ , Outputs Disabled	Com'l		160	230		150	230	mA
			Ind		160	260		150	260	
$I_{SB1}$	Standby Current (Both Ports TTL Levels)	$CE_L$ and $CE_R \geq V_{IH}$ , $f = f_{MAX}^{[12]}$	Com'l		30	50		20	50	mA
			Ind		30	65		20	65	
$I_{SB2}$	Standby Current (One Port TTL Level)	$CE_L$ or $CE_R \geq V_{IH}$ , $f = f_{MAX}^{[12]}$	Com'l		85	135		75	135	mA
			Ind		85	150		75	150	
$I_{SB3}$	Standby Current (Both Ports CMOS Levels)	Both Ports $CE$ and $CE_R \geq V_{CC} - 0.2V$ , $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$ , $f = 0^{[12]}$	Com'l		3	15		3	15	mA
			Ind		3	15		3	15	
$I_{SB4}$	Standby Current (Both Ports CMOS Levels)	One Port $CE_L$ or $CE_R \geq V_{CC} - 0.2V$ , $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$ , Active Port Outputs, $f = f_{MAX}^{[12]}$	Com'l		80	120		70	120	mA
			Ind		80	135		70	135	

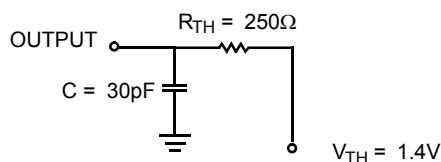
**Capacitance**<sup>[13]</sup>

Parameter	Description	Test Conditions	Max	Unit
$C_{IN}$	Input Capacitance	$T_A = 25^\circ\text{C}$ , $f = 1 \text{ MHz}$ , $V_{CC} = 5.0V$	10	pF
$C_{OUT}$	Output Capacitance		10	pF

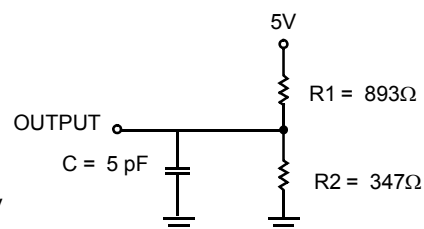
**Figure 3. AC Test Loads and Waveforms**



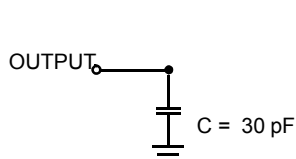
**(a) Normal Load (Load 1)**



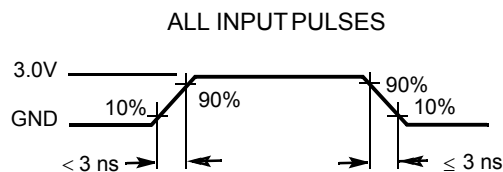
**(b) Thévenin Equivalent (Load 1)**



**(c) Three-State Delay (Load 3)**



**Load (Load 2)**



**Note**

13. Tested initially and after any design or process changes that may affect these parameters.

**Switching Characteristics** Over the Operating Range <sup>[14]</sup>

Parameter	Description	7C024/024A/0241–15 7C025/0251–15		7C024/024A/0241–25 7C025/0251–25		7C024/024A/0241–35 7C025/0251–35		7C024/024A/0241–55 7C025/0251–55		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle										
t <sub>RC</sub>	Read Cycle Time	15		25		35		55		ns
t <sub>AA</sub>	Address to Data Valid		15		25		35		55	ns
t <sub>OHA</sub>	Output Hold From Address Change	3		3		3		3		ns
t <sub>ACE</sub> <sup>[15]</sup>	CE LOW to Data Valid		15		25		35		55	ns
t <sub>DOE</sub>	OE LOW to Data Valid		10		13		20		25	ns
t <sub>LZOE</sub> <sup>[16, 17, 18]</sup>	OE Low to Low Z	3		3		3		3		ns
t <sub>HZOE</sub> <sup>[16, 17, 18]</sup>	OE HIGH to High Z		10		15		20		25	ns
t <sub>LZCE</sub> <sup>[16, 17, 18]</sup>	CE LOW to Low Z	3		3		3		3		ns
t <sub>HZCE</sub> <sup>[16, 17, 18]</sup>	CE HIGH to High Z		10		15		20		25	ns
t <sub>PU</sub> <sup>[18]</sup>	CE LOW to Power Up	0		0		0		0		ns
t <sub>PD</sub> <sup>[18]</sup>	CE HIGH to Power Down		15		25		25		55	ns
t <sub>ABE</sub> <sup>[15]</sup>	Byte Enable Access Time		15		25		35		55	ns
Write Cycle										
t <sub>WC</sub>	Write Cycle Time	15		25		35		55		ns
t <sub>SCE</sub> <sup>[15]</sup>	CE LOW to Write End	12		20		30		35		ns
t <sub>AW</sub>	Address Setup to Write End	12		20		30		35		ns
t <sub>HA</sub>	Address Hold From Write End	0		0		0		0		ns
t <sub>SA</sub> <sup>[15]</sup>	Address Setup to Write Start	0		0		0		0		ns
t <sub>PWE</sub>	Write Pulse Width	12		20		25		35		ns
t <sub>SD</sub>	Data Setup to Write End	10		15		15		20		ns
t <sub>HD</sub>	Data Hold From Write End	0		0		0		0		ns
t <sub>HZWE</sub> <sup>[17, 18]</sup>	R/W LOW to High Z		10		15		20		25	ns
t <sub>LZWE</sub> <sup>[17, 18]</sup>	R/W HIGH to Low Z	0		0		0		0		ns
t <sub>WDD</sub> <sup>[19]</sup>	Write Pulse to Data Delay		30		50		60		70	ns
t <sub>DDD</sub> <sup>[19]</sup>	Write Data Valid to Read Data Valid		25		35		35		45	ns

**Notes**

14. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified  $I_O/I_{OH}$  and 30 pF load capacitance.
15. To access RAM,  $\overline{CE}=L$ ,  $\overline{UB}=L$ ,  $\overline{SEM}=H$ . To access semaphore,  $\overline{CE}=H$  and  $\overline{SEM}=L$ . Either condition must be valid for the entire  $t_{SCE}$  time.
16. At any given temperature and voltage condition for any given device,  $t_{HZCE}$  is less than  $t_{LZCE}$  and  $t_{HZOE}$  is less than  $t_{LZOE}$ .
17. Test conditions used are Load 3.
18. This parameter is guaranteed but not tested.
19. For information on port-to-port delay through RAM cells from writing port to reading port, refer to Figure 11.



## Switching Characteristics Over the Operating Range (continued)<sup>[14]</sup>

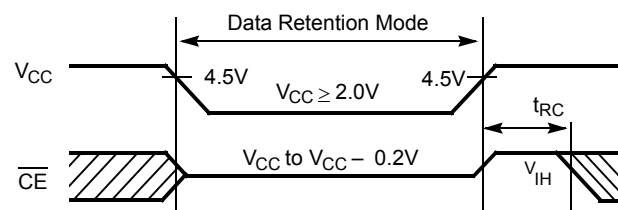
Parameter	Description	7C024/024A/0241–15 7C025/0251–15		7C024/024A/0241–25 7C025/0251–25		7C024/024A/0241–35 7C025/0251–35		7C024/024A/0241–55 7C025/0251–55		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Busy Timing <sup>[20]</sup>										
t <sub>BLA</sub>	BUSY LOW from Address Match		15		20		20		45	ns
t <sub>BHA</sub>	BUSY HIGH from Address Mismatch		15		20		20		40	ns
t <sub>BLC</sub>	BUSY LOW from CE LOW		15		20		20		40	ns
t <sub>BHC</sub>	BUSY HIGH from CE HIGH		15		20		20		35	ns
t <sub>PS</sub>	Port Setup for Priority	5		5		5		5		ns
t <sub>WB</sub>	R/W HIGH after BUSY (Slave)	0		0		0		0		ns
t <sub>WH</sub>	R/W HIGH after BUSY HIGH (Slave)	13		20		30		40		ns
t <sub>BDD</sub> <sup>[21]</sup>	BUSY HIGH to Data Valid		Note 21		Note 21		Note 21		Note 21	ns
Interrupt Timing <sup>[20]</sup>										
t <sub>INS</sub>	INT Set Time		15		20		25		30	ns
t <sub>INR</sub>	INT Reset Time		15		20		25		30	ns
Semaphore Timing										
t <sub>SOP</sub>	SEM Flag Update Pulse (OE or SEM)	10		12		15		20		ns
t <sub>SWRD</sub>	SEM Flag Write to Read Time	5		10		10		15		ns
t <sub>SPS</sub>	SEM Flag Contention Window	5		10		10		15		ns
t <sub>SAA</sub>	SEM Address Access Time		15		25		35		55	ns

## Data Retention Mode

The CY7C024/024A/0241 is designed with battery backup in mind. Data retention voltage and supply current are guaranteed over temperature. The following rules insure data retention:

1. Chip enable ( $\overline{CE}$ ) must be held HIGH during data retention, within  $V_{CC}$  to  $V_{CC} - 0.2V$ .
2.  $\overline{CE}$  must be kept between  $V_{CC} - 0.2V$  and 70% of  $V_{CC}$  during the power up and power down transitions.
3. The RAM can begin operation  $>t_{RC}$  after  $V_{CC}$  reaches the minimum operating voltage (4.5V).

## Timing



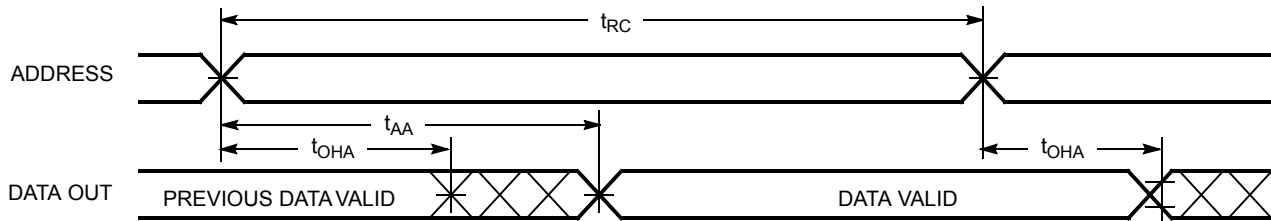
Parameter	Test Conditions <sup>[22]</sup>	Max	Unit
$I_{CCDR1}$	At $V_{CCDR} = 2V$	1.5	mA

### Notes

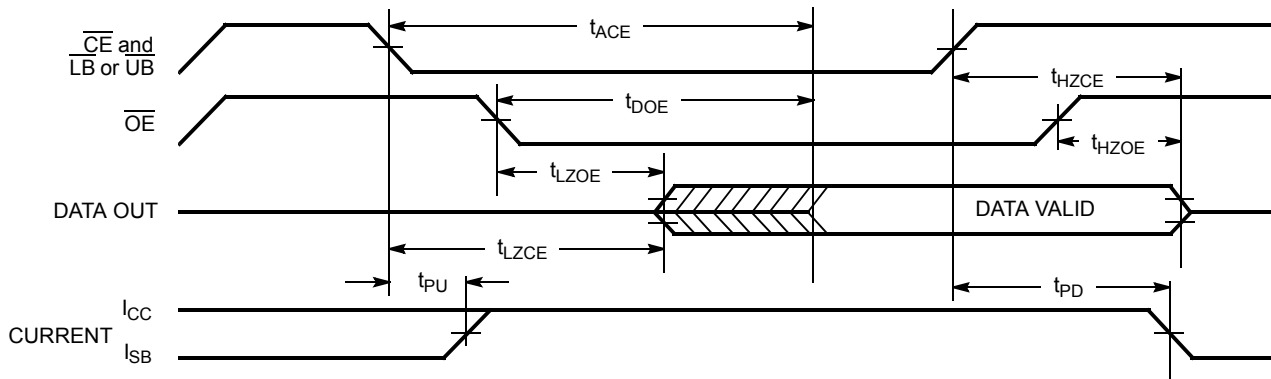
20. Test conditions used are Load 2.  
 21.  $t_{BDD}$  is a calculated parameter and is the greater of  $t_{WDD} - t_{PWE}$  (actual) or  $t_{BDD} - t_{SD}$  (actual).  
 22.  $CE = V_{CC}$ ,  $V_{in} = GND$  to  $V_{CC}$ ,  $T_A = 25^\circ C$ . This parameter is guaranteed but not tested.

## Switching Waveforms

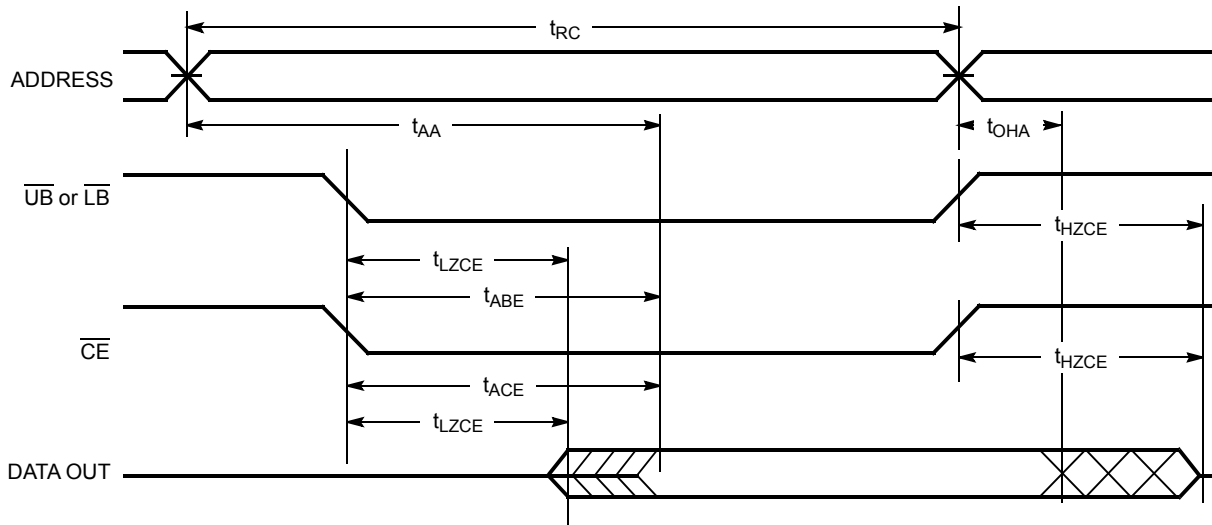
**Figure 4. Read Cycle No. 1 (Either Port Address Access)**<sup>[23, 24, 25]</sup>



**Figure 5. Read Cycle No. 2 (Either Port  $\overline{CE}/\overline{OE}$  Access)**<sup>[23, 26, 27]</sup>



**Figure 6. Read Cycle No. 3 (Either Port)**<sup>[23, 25, 26, 26, 27]</sup>

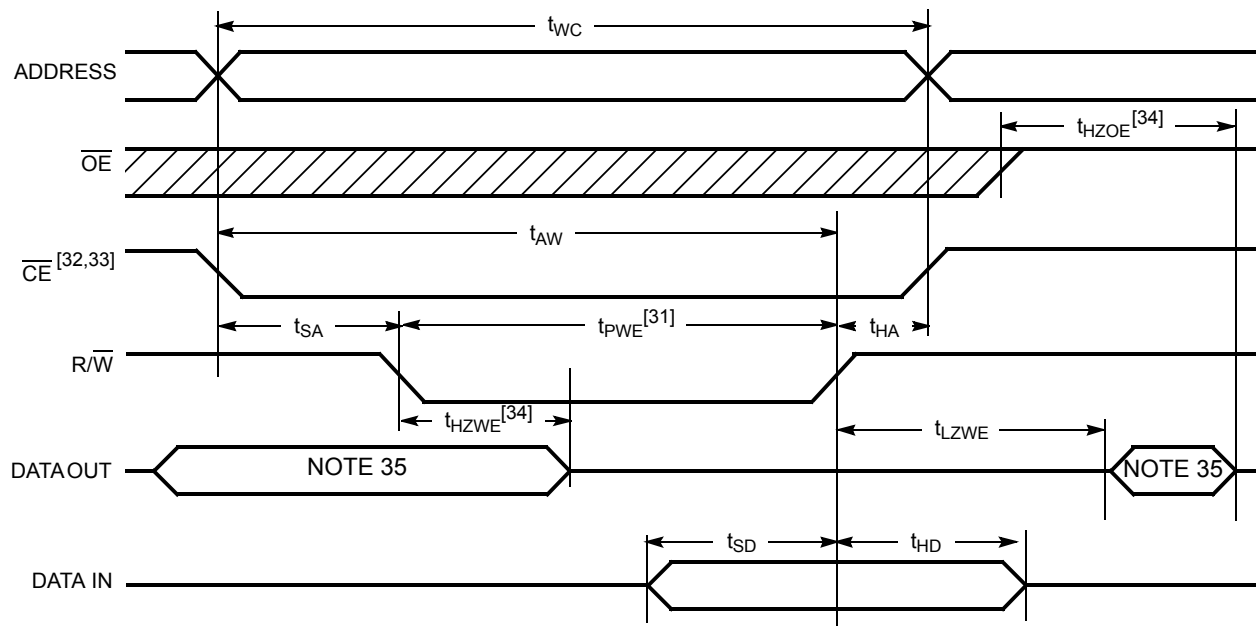


### Notes

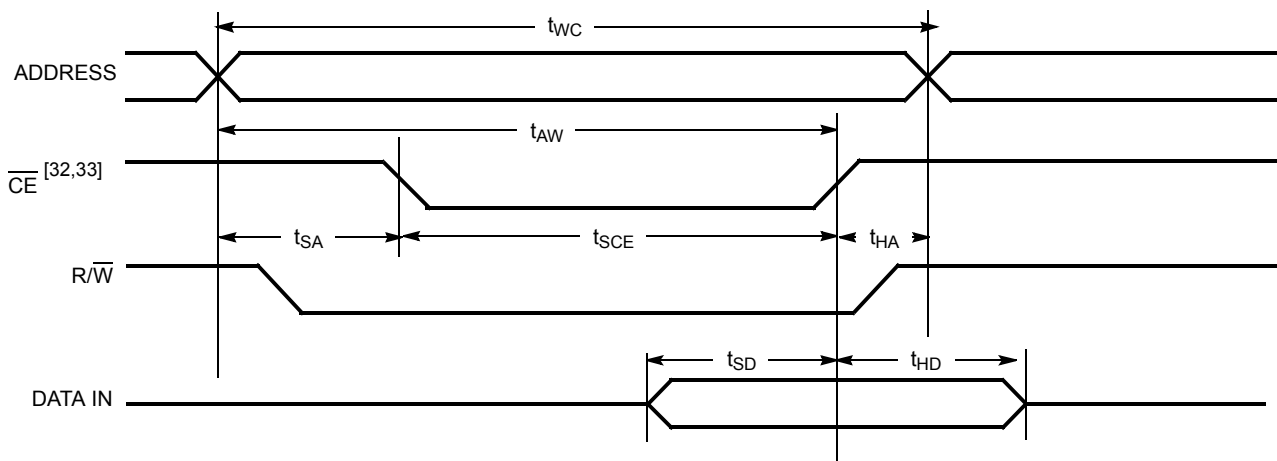
23.  $R/\overline{W}$  is HIGH for read cycles
24. Device is continuously selected  $\overline{CE} = V_{IL}$  and  $\overline{UB}$  or  $\overline{LB} = V_{IL}$ . This waveform cannot be used for semaphore reads.
25.  $\overline{OE} = V_{IL}$ .
26. Address valid prior to or coincident with  $\overline{CE}$  transition LOW.
27. To access RAM,  $\overline{CE} = V_{IL}$ ,  $\overline{UB}$  or  $\overline{LB} = V_{IL}$ ,  $\overline{SEM} = V_{IH}$ . To access semaphore,  $\overline{CE} = V_{IH}$ ,  $\overline{SEM} = V_{IL}$ .

## Switching Waveforms (continued)

**Figure 7. Write Cycle No. 1: R/W Controlled Timing** [28, 29, 30, 31]



**Figure 8. Write Cycle No. 2: CE Controlled Timing** [28, 29, 30, 36]



### Notes

28. R/W must be HIGH during all address transitions.

29. A write occurs during the overlap ( $t_{SCE}$  or  $t_{PWE}$ ) of a LOW  $\overline{CE}$  or  $\overline{SEM}$  and a LOW  $\overline{UB}$  or  $\overline{LB}$ .

30.  $t_{HA}$  is measured from the earlier of CE or R/W or ( $\overline{SEM}$  or R/W) going HIGH at the end of write cycle.

31. If OE is LOW during a R/W controlled write cycle, the write pulse width must be the larger of  $t_{PWE}$  or ( $t_{HZWE} + t_{SD}$ ) to allow the I/O drivers to turn off and data to be placed on the bus for the required  $t_{SD}$ . If OE is HIGH during an R/W controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified  $t_{PWE}$ .

32. To access RAM,  $\overline{CE} = V_{IL}$ ,  $\overline{SEM} = V_{IH}$ .

33. To access upper byte,  $\overline{CE} = V_{IL}$ ,  $\overline{UB} = V_{IL}$ ,  $\overline{SEM} = V_{IH}$ .

To access lower byte,  $\overline{CE} = V_{IL}$ ,  $\overline{LB} = V_{IL}$ ,  $\overline{SEM} = V_{IH}$ .

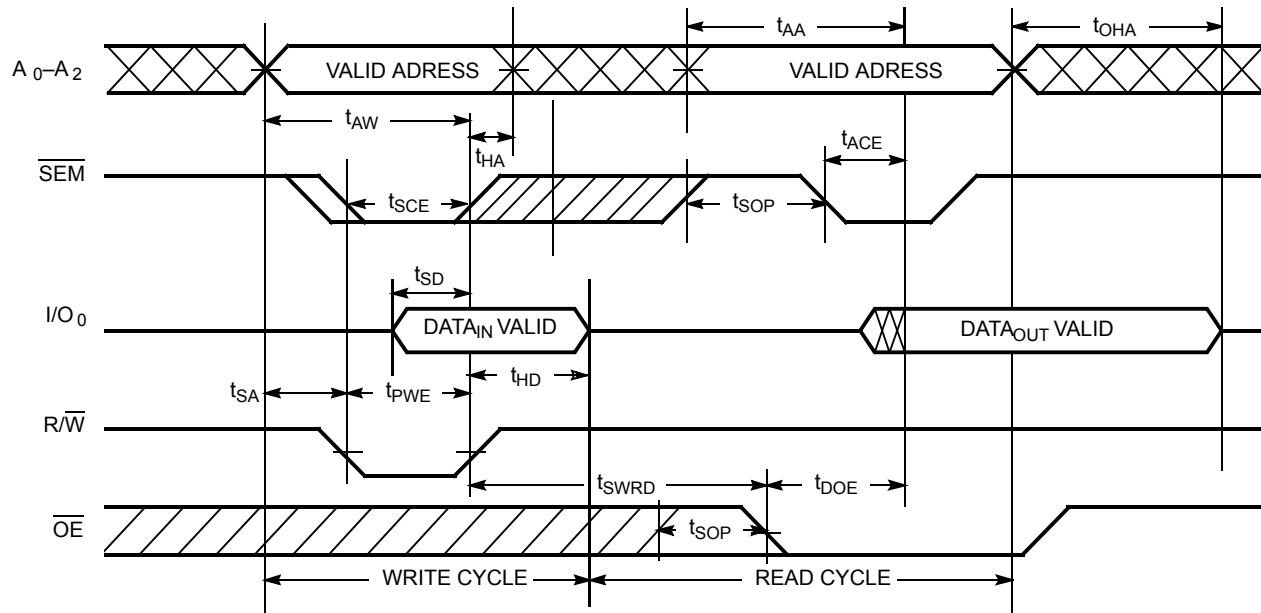
34. Transition is measured  $\pm 500$  mV from steady state with a 5 pF load (including scope and jig). This parameter is sampled and not 100% tested.

35. During this period, the I/O pins are in the output state, and input signals must not be applied.

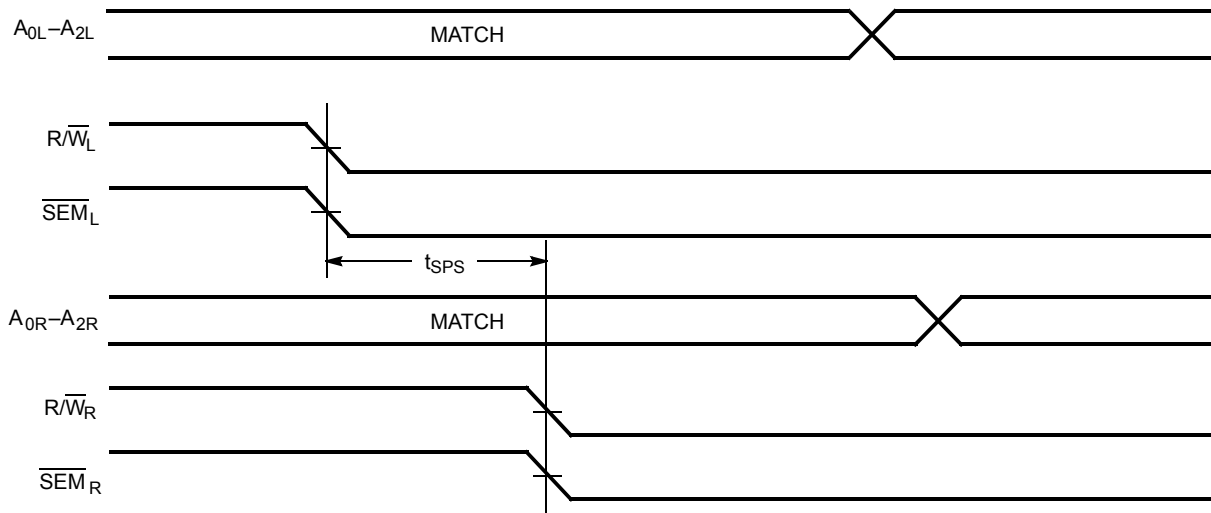
36. If the CE or SEM LOW transition occurs simultaneously with or after the R/W LOW transition, the outputs remain in the high impedance state.

## Switching Waveforms (continued)

**Figure 9. Semaphore Read After Write Timing, Either Side<sup>[37]</sup>**



**Figure 10. Timing Diagram of Semaphore Contention<sup>[38, 39, 40]</sup>**



### Notes

37. CE = HIGH for the duration of the above timing (both write and read cycle).

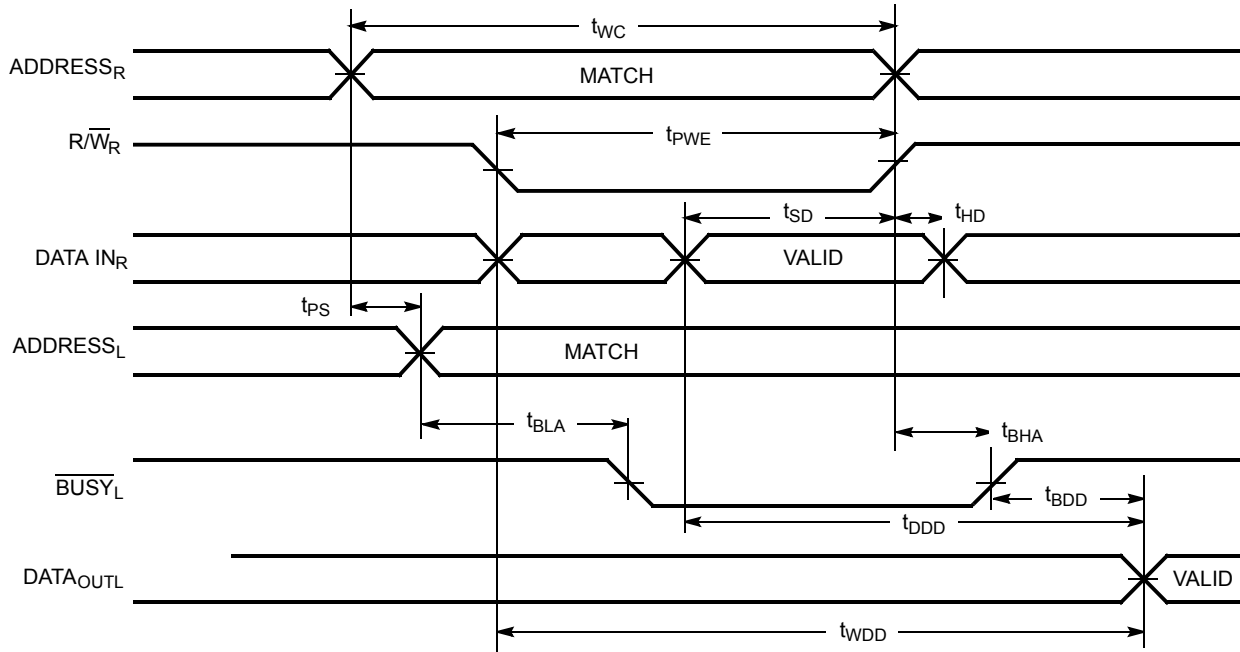
38. I/O<sub>0R</sub> = I/O<sub>0L</sub> = LOW (request semaphore); CE<sub>R</sub> = CE<sub>L</sub> = HIGH.

39. Semaphores are reset (available to both ports) at cycle start.

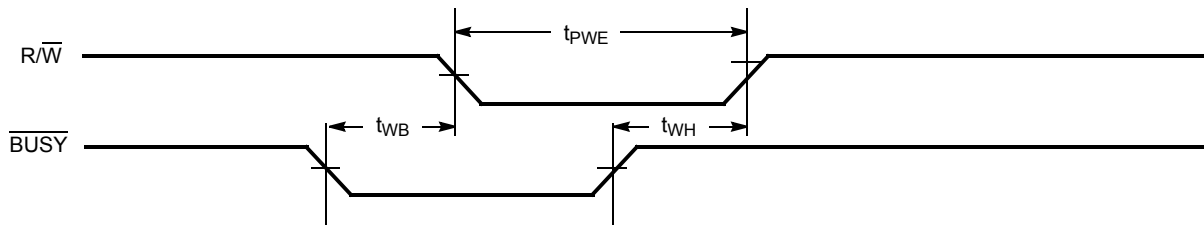
40. If t<sub>SPS</sub> is violated, the semaphore is definitely obtained by one side or the other, but which side gets the semaphore is unpredictable.

## Switching Waveforms (continued)

**Figure 11. Timing Diagram of Read with  $\overline{\text{BUSY}}$  ( $\overline{\text{M}}/\overline{\text{S}}=\text{HIGH}$ )<sup>[41]</sup>**



**Figure 12. Write Timing with Busy Input ( $\overline{\text{M}}/\overline{\text{S}}=\text{LOW}$ )**

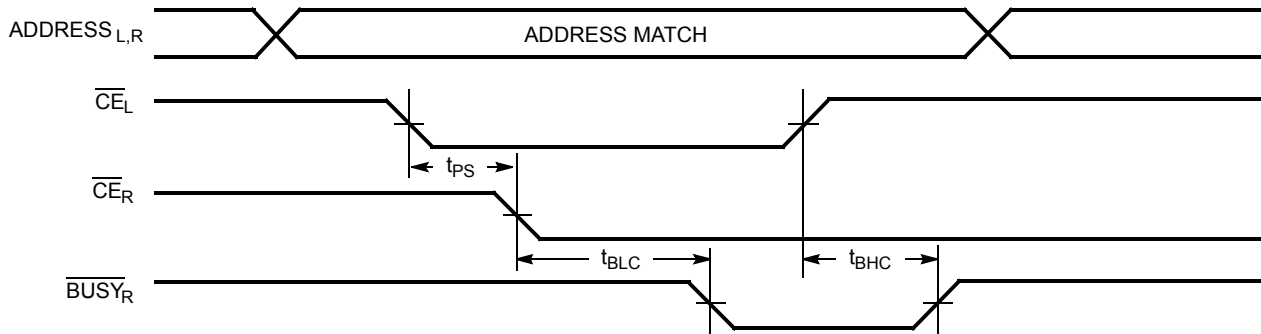


**Note**  
41.  $\overline{\text{CE}}_L = \overline{\text{CE}}_R = \text{LOW}$

## Switching Waveforms (continued)

Figure 13. Busy Timing Diagram No.1 (CE Arbitration)<sup>[42]</sup>

$\overline{CE}_L$  Valid First:



$CE_R$  Valid First:

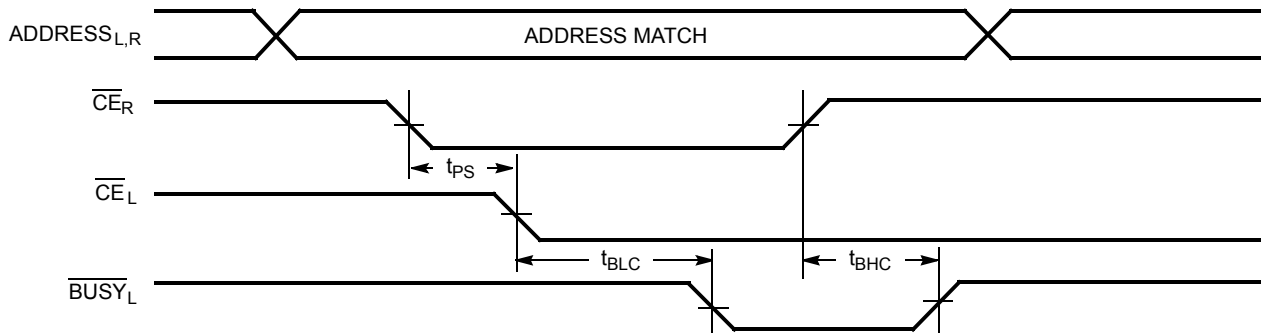
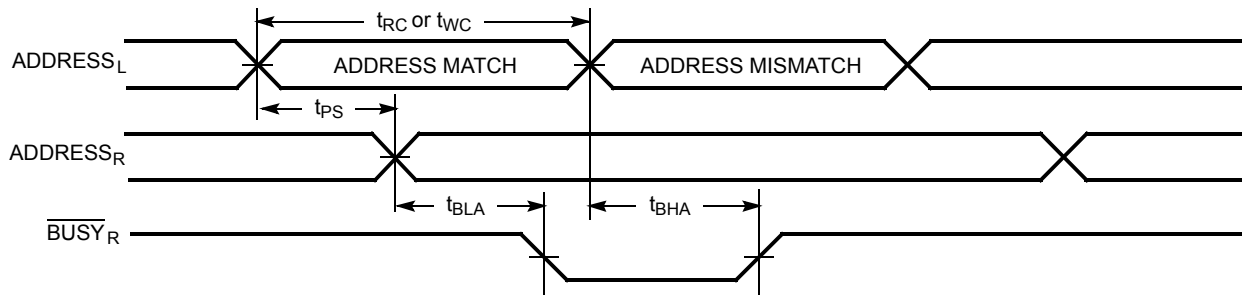
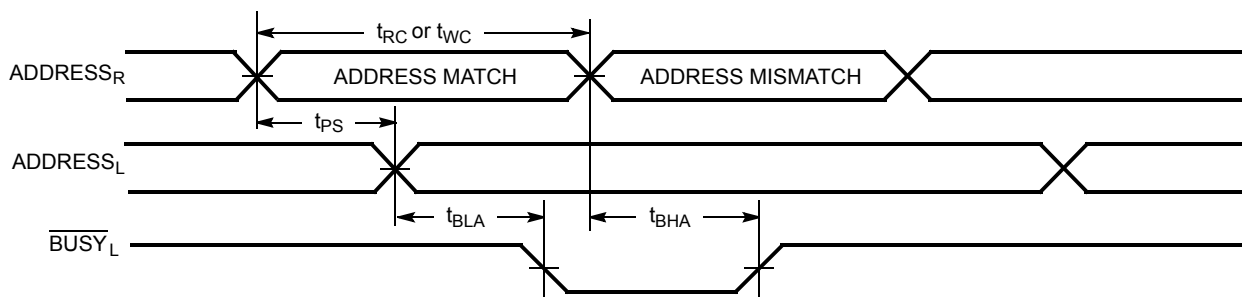


Figure 14. Busy Timing Diagram No.2 (Address Arbitration)<sup>[42]</sup>

Left Address Valid First:



Right Address Valid First:

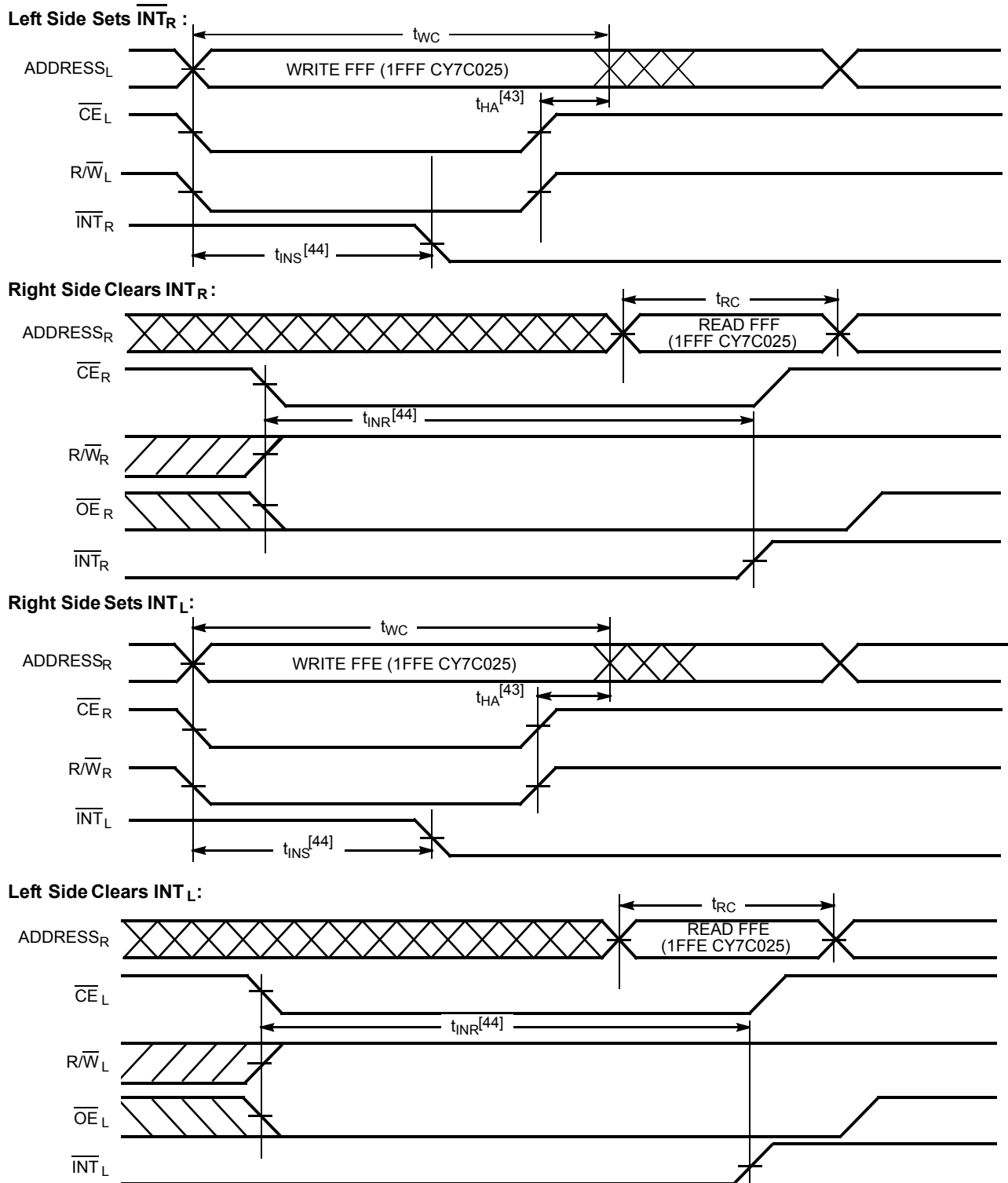


### Note

42. If  $t_{PS}$  is violated, the busy signal is asserted on one side or the other, but there is no guarantee to which side  $\overline{BUSY}$  is asserted.

## Switching Waveforms (continued)

Figure 15. Interrupt Timing Diagrams



### Notes

43.  $t_{HA}$  depends on which enable pin ( $\overline{\text{CE}}_L$  or  $\overline{\text{R}}/\overline{\text{W}}_L$ ) is deasserted first.  
44.  $t_{INS}$  or  $t_{INR}$  depends on which enable pin ( $\overline{\text{CE}}_L$  or  $\overline{\text{R}}/\overline{\text{W}}_L$ ) is asserted last.

### Ordering Information (4K x16 Dual-Port SRAM)

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7C024-15AXC	A100	100-Pin Pb Free Thin Quad Flat Pack	Commercial
25	CY7C024-25AXC	A100	100-Pin Pb Free Thin Quad Flat Pack	Commercial
	CY7C024A-25JXC	A100	84-Pin Pb Free Plastic Leaded Chip Carrier	
	CY7C024-25AXI	A100	100-Pin Pb Free Thin Quad Flat Pack	Industrial
	CY7C024-25JXI	J83	84-Pin Pb Free Plastic Leaded Chip Carrier	
55	CY7C024-55AXC	A100	100-Pin Pb Free Thin Quad Flat Pack	Commercial
	CY7C024-55JXC	J83	84-Pin Pb Free Plastic Leaded Chip Carrier	

### Ordering Information (8K x 16 Dual-Port SRAM)

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
25	CY7C025-25AXC	A100	100-Pin Pb Free Thin Quad Flat Pack	Commercial
	CY7C025-25AXI	A100	100-Pin Pb Free Thin Quad Flat Pack	Industrial
	CY7C025-25JXI	J83	84-Pin Pb Free Plastic Leaded Chip Carrier	
55	CY7C025-55AXC	A100	100-Pin Pb Free Thin Quad Flat Pack	Commercial

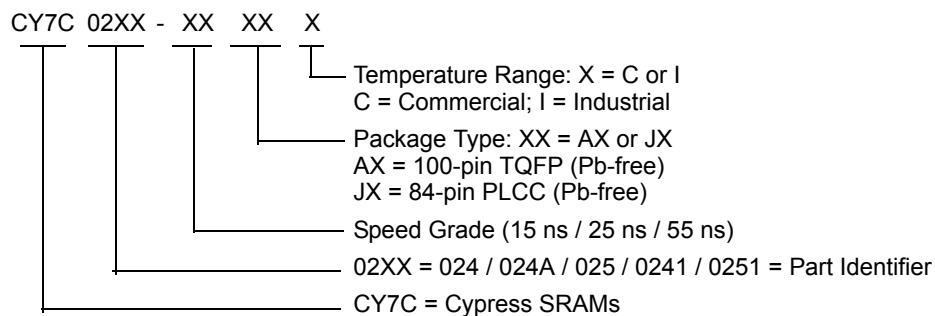
### Ordering Information (4K x 18 Dual-Port SRAM)

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7C0241-15AXI	A100	100-Pin Pb Free Thin Quad Flat Pack	Industrial
25	CY7C0241-25AXC	A100	100-Pin Pb Free Thin Quad Flat Pack	Commercial

### Ordering Information (8K x 18 Dual-Port SRAM)

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7C0251-15AXC	A100	100-Pin Pb Free Thin Quad Flat Pack	Commercial

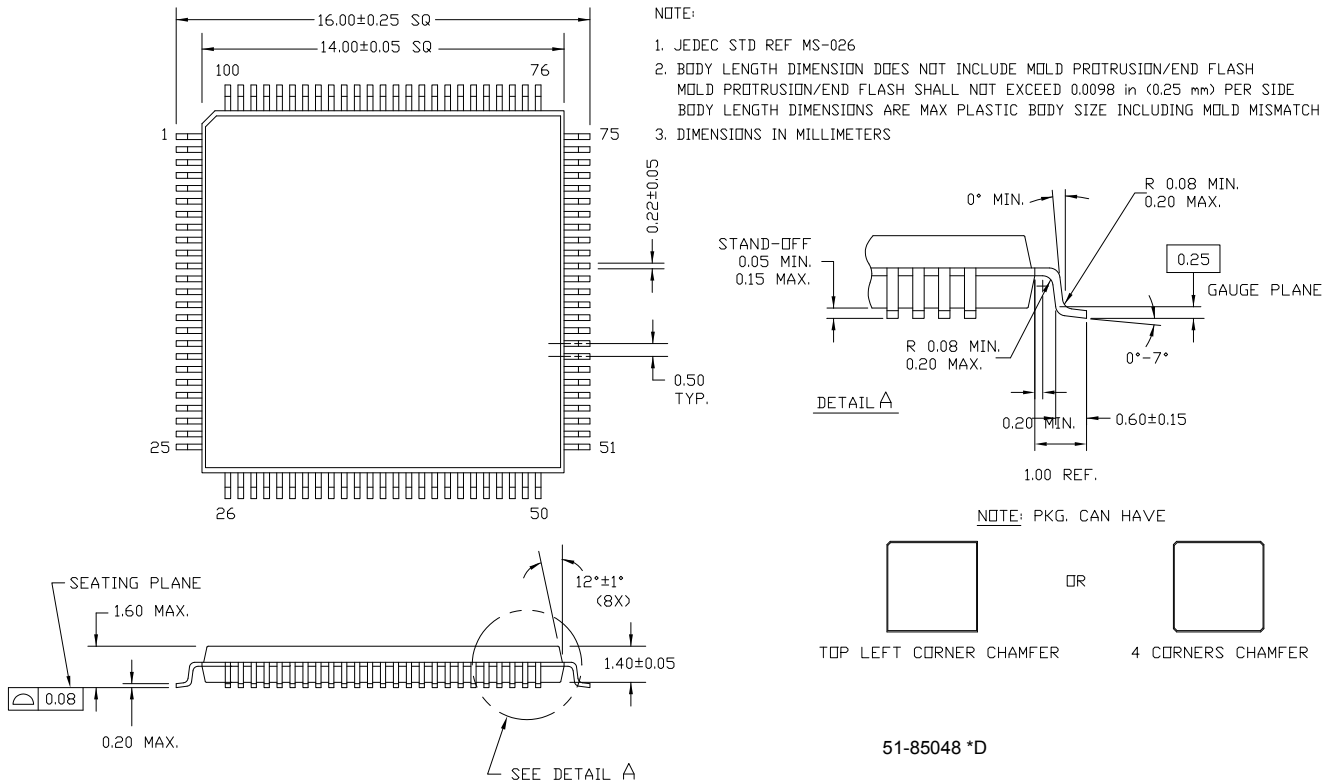
### Ordering Code Definitions



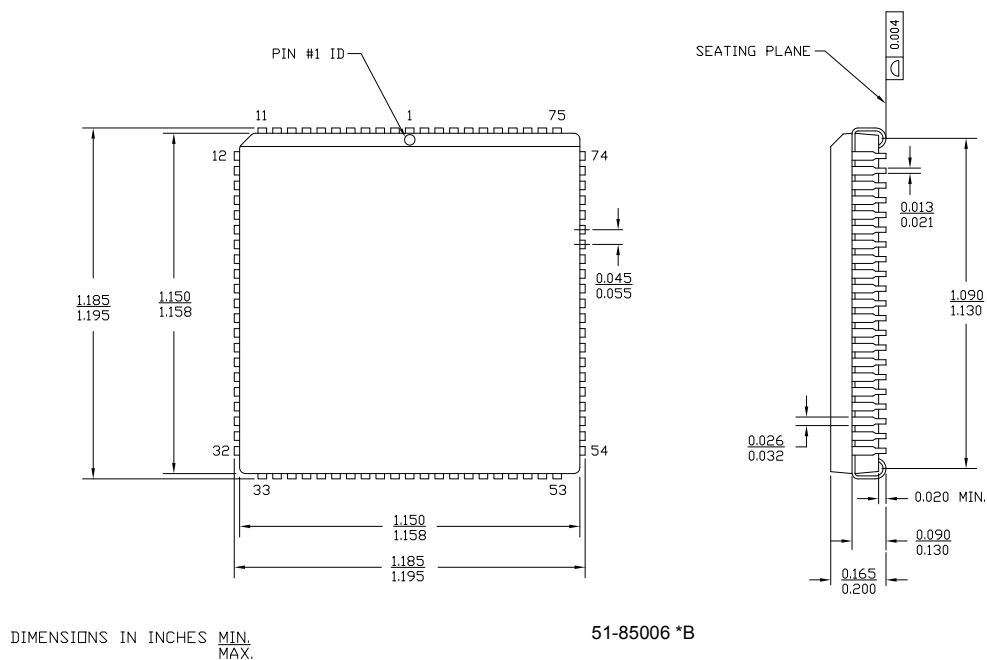


## Package Diagrams

**Figure 16. 100-Pin Pb-Free Thin Plastic Quad Flat Pack (TQFP) A100**



**Figure 17. 84-Pin Pb Free Plastic Leaded Chip Carrier J83**



## Document History Page

Document Title: CY7C024/024A/0241, CY7C025/0251 4K x 16/18 and 8K x 16/18 Dual-Port Static RAM with Sem, Int, Busy Document Number: 38-06035				
Rev.	ECN No.	Orig. of Change	Submission Date	Description of Change
**	110177	SZV	09/29/01	Change from Spec number: 38-00255 to 38-06035
*A	122286	RBI	12/27/02	Power up requirements added to Maximum Ratings Information
*B	236754	YDT	See ECN	Removed cross information from features section
*C	279132	RUY	See ECN	Added Lead (Pb)-Free packaging information
*D	2623540	VKN/PYRS	12/17/08	Added CY7C024A part Updated Ordering information table
*E	2896038	RAME	03/19/10	Removed inactive parts from ordering information table Updated package diagram
*F	3058184	ADMU	10/13/2010	Removed CY7C024-55AC from <a href="#">Ordering Information (4K x16 Dual-Port SRAM)</a> and CY7C025-25AC from <a href="#">Ordering Information (8K x 16 Dual-Port SRAM)</a> and added <a href="#">Ordering Code Definitions</a> .

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