ADG774* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

DOCUMENTATION

Application Notes

- AN-1024: How to Calculate the Settling Time and Sampling Rate of a Multiplexer

Data Sheet

- ADG774: CMOS 3 V/5 V, Wide Bandwidth Quad 2:1 Mux Data Sheet

REFERENCE MATERIALS

Product Selection Guide

- Switches and Multiplexers Product Selection Guide

Technical Articles

- CMOS Switches Offer High Performance in Low Power, Wideband Applications
- Data-acquisition system uses fault protection
- Enhanced Multiplexing for MEMS Optical Cross Connects
- Temperature monitor measures three thermal zones

DESIGN RESOURCES

- ADG774 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all ADG774 EngineerZone Discussions.

SAMPLE AND BUY

Visit the product page to see pricing options.

TECHNICAL SUPPORT

Submit a technical question or find your regional support number.

DOCUMENT FEEDBACK

Submit feedback for this data sheet.

ADG774–SPECIFICATIONS

SINGLE SUPPLY (V_{DD} = 5 V ± 10%, GND = 0 V. All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	B Version[1] +25°C	–40°C to +85°C	–40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			0 V to V_{DD}	V	
On Resistance (R_{ON})	2.2			Ω typ	V_D = 0 V to V_{DD}, I_S = –10 mA
		5	7	Ω max	
On Resistance Match between Channels (ΔR_{ON})	0.15			Ω typ	V_D = 0 V to V_{DD}, I_S = –10 mA
		0.5	0.5	Ω max	
On Resistance Flatness ($R_{FLAT(ON)}$)	0.5			Ω typ	V_D = 0 V to V_{DD}, I_S = –1 mA
		1	1	Ω max	
LEAKAGE CURRENTS					
Source OFF Leakage I_S (OFF)	±0.01			nA typ	V_D = 4.5 V, V_S = 1 V; V_D = 1 V, V_S = 4.5 V;
	±0.5	±1	±1.5	nA max	Test Circuit 2
Drain OFF Leakage I_D (OFF)	±0.01			nA typ	V_D = 4.5 V, V_S = 1 V; V_D = 1 V, V_S = 4.5 V;
	±0.5	±1	±1.5	nA max	Test Circuit 2
Channel ON Leakage I_D, I_S (ON)	±0.01			nA typ	V_D = V_S = 4.5 V; V_D = V_S = 1 V; Test Circuit 3
	±0.5	±1	±1.5	nA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.0	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current					
I_{INL} or I_{INH}	0.001			µA typ	V_{IN} = V_{INL} or V_{INH}
			±0.5	µA max	
DYNAMIC CHARACTERISTICS[2]					
t_{ON}		7		ns typ	R_L = 100 Ω, C_L = 35 pF,
		15	20	ns max	V_S = +3 V; Test Circuit 4
t_{OFF}		4		ns typ	R_L = 100 Ω, C_L = 35 pF,
		8	9	ns max	V_S = +3 V; Test Circuit 4
Break-Before-Make Time Delay, t_D		5		ns typ	R_L = 100 Ω, C_L = 35 pF,
		1		ns min	V_{S1} = V_{S2} = +5 V; Test Circuit 5
Off Isolation		–65		dB typ	R_L = 100 Ω, f = 10 MHz; Test Circuit 7
Channel-to-Channel Crosstalk		–75		dB typ	R_L = 100 Ω, f = 10 MHz; Test Circuit 8
Bandwidth –3 dB		240		MHz typ	R_L = 100 Ω; Test Circuit 6
Distortion		0.5		% typ	R_L = 100 Ω
Charge Injection		10		pC typ	C_L = 1 nF; Test Circuit 9
C_S (OFF)		10		pF typ	f = 1 kHz
C_D (OFF)		20		pF typ	f = 1 kHz
C_D, C_S (ON)		30		pF typ	f = 1 MHz
POWER REQUIREMENTS					V_{DD} = +5.5 V Digital Inputs = 0 V or V_{DD}
I_{DD}		1	1	µA max	
	0.001			µA typ	
I_{IN}		1	1	µA typ	V_{IN} = +5 V
I_O		100		mA max	V_S/V_D = 0 V

NOTES
[1]Temperature range: B Version, –40°C to +125°C.
[2]Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

SINGLE SUPPLY (V_{DD} = 3 V ± 10%, GND = 0 V. All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	B Version[1] +25°C	–40°C to +85°C	–40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			0 V to V_{DD}	V	
On Resistance (R_{ON})	4			Ω typ	V_D = 0 V to V_{DD}, I_S = –10 mA
		8	9	Ω max	
On Resistance Match between Channels (ΔR_{ON})	0.15			Ω typ	V_D = 0 V to V_{DD}, I_S = –10 mA
		0.5	0.5	Ω max	
On Resistance Flatness ($R_{FLAT(ON)}$)	2			Ω typ	V_D = 0 V to V_{DD}, I_S = –10 mA
		4	4	Ω max	
LEAKAGE CURRENTS					
Source OFF Leakage I_S (OFF)	±0.01			nA typ	V_D = 3 V, V_S = 1 V; V_D = 1 V, V_S = 3 V;
	±0.5	±1	±1.5	nA max	Test Circuit 2
Drain OFF Leakage I_D (OFF)	±0.01			nA typ	V_D = 3 V, V_S = 1 V; V_D = 1 V, V_S = 3 V;
	±0.5	±1	±1.5	nA max	Test Circuit 2
Channel ON Leakage I_D, I_S (ON)	±0.01			nA typ	V_D = V_S = 3 V; V_D = V_S = 1 V; Test Circuit 3
	±0.5	±1	±1.5	nA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.0	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current					
I_{INL} or I_{INH}	0.001			µA typ	V_{IN} = V_{INL} or V_{INH}
			±0.5	µA max	
DYNAMIC CHARACTERISTICS[2]					
t_{ON}		8		ns typ	R_L = 100 Ω, C_L = 35 pF,
		16	21	ns max	V_S = +1.5 V; Test Circuit 4
t_{OFF}		5		ns typ	R_L = 100 Ω, C_L = 35 pF,
		10	11	ns max	V_S = +1.5 V; Test Circuit 4
Break-Before-Make Time Delay, t_D		5		ns typ	R_L = 100 Ω, C_L = 35 pF,
		1		ns min	V_{S1} = V_{S2} = 3 V; Test Circuit 5
Off Isolation		–65		dB typ	R_L = 50 Ω, f = 10 MHz; Test Circuit 7
Channel-to-Channel Crosstalk		–75		dB typ	R_L = 50 Ω, f = 10 MHz; Test Circuit 8
Bandwidth –3 dB		240		MHz typ	R_L = 50 Ω; Test Circuit 6
Distortion		2		% typ	R_L = 50 Ω
Charge Injection		3		pC typ	C_L = 1 nF; Test Circuit 9
C_S (OFF)		10		pF typ	f = 1 kHz
C_D (OFF)		20		pF typ	f = 1 kHz
C_D, C_S (ON)		30		pF typ	f = 1 MHz
POWER REQUIREMENTS					V_{DD} = +3.3 V Digital Inputs = 0 V or V_{DD}
I_{DD}		1	1	µA max	
	0.001			µA typ	
I_{IN}		1	1	µA typ	V_{IN} = +3 V
I_O		100		mA max	V_S/V_D = 0 V

NOTES
[1]Temperature range: B Version, –40°C to +125°C.
[2]Guaranteed by design, not subject to production test.
Specifications subject to change without notice.

Table I. Truth Table

$\overline{EN}$	IN	D1	D2	D3	D4	Function
1	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z	DISABLE
0	0	S1A	S2A	S3A	S4A	IN = 0
0	1	S1B	S2B	S3B	S4B	IN = 1

ABSOLUTE MAXIMUM RATINGS[1]

(T_A = 25°C unless otherwise noted.)

V_{DD} to GND . . . . . –0.3 V to +6 V
Analog, Digital Inputs[2] . . . . . –0.3 V to V_{DD} + 0.3 V or 30 mA, Whichever Occurs First
Continuous Current, S or D . . . . . 100 mA
Peak Current, S or D . . . . . 300 mA
(Pulsed at 1 ms, 10% Duty Cycle max)
Operating Temperature Range
Industrial (B Version) . . . . . –40°C to +125°C
Storage Temperature Range . . . . . –65°C to +150°C
Junction Temperature . . . . . 150°C
SOIC Package, Power Dissipation . . . . . 600 mW
θ_{JA} Thermal Impedance . . . . . 100°C/W
QSOP Package, Power Dissipation . . . . . 566 mW
θ_{JA} Thermal Impedance . . . . . 149.97°C/W
Lead Temperature, Soldering (10 sec) . . . . . 300°C
I R Reflow, Peak Temperature (<20 sec) . . . . . 235°C
ESD . . . . . 2 kV

NOTES

[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one absolute maximum rating may be applied at any one time.

[2]Overvoltages at IN, S, or D will be clamped by internal diodes. Current should be limited to the maximum ratings given.

ORDERING GUIDE

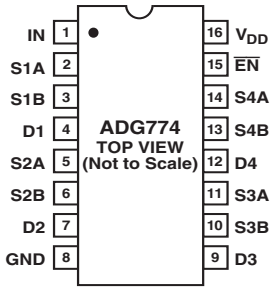
Model	Temperature Range	Package Descriptions	Package Options
ADG774BR	–40°C to +125°C	Standard Small Outline Package (SOIC)	R-16
ADG774BR-REEL	–40°C to +125°C	Standard Small Outline Package (SOIC)	R-16
ADG774BR-REEL7	–40°C to +125°C	Standard Small Outline Package (SOIC)	R-16
ADG774BRZ*	–40°C to +125°C	Standard Small Outline Package (SOIC)	R-16
ADG774BRZ-REEL*	–40°C to +125°C	Standard Small Outline Package (SOIC)	R-16
ADG774BRZ-REEL7*	–40°C to +125°C	Standard Small Outline Package (SOIC)	R-16
ADG774BRQ	–40°C to +125°C	Shrink Small Outline Package (QSOP)	RQ-16
ADG774BRQ-REEL	–40°C to +125°C	Shrink Small Outline Package (QSOP)	RQ-16
ADG774BRQ-REEL7	–40°C to +125°C	Shrink Small Outline Package (QSOP)	RQ-16
ADG774BRQZ*	–40°C to +125°C	Shrink Small Outline Package (QSOP)	RQ-16
ADG774BRQZ-REEL*	–40°C to +125°C	Shrink Small Outline Package (QSOP)	RQ-16
ADG774BRQZ-REEL7*	–40°C to +125°C	Shrink Small Outline Package (QSOP)	RQ-16

*Z = Pb-free part.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADG774 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

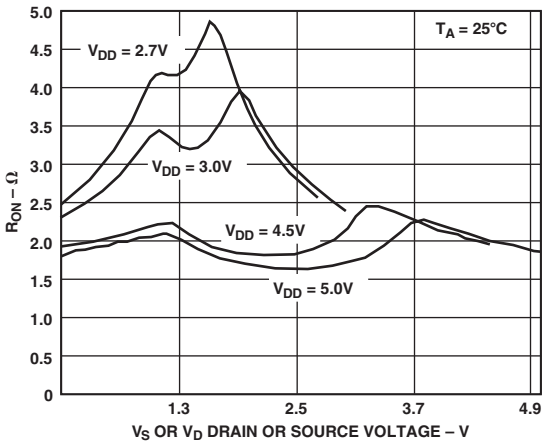
PIN CONFIGURATION (SOIC/QSOP)



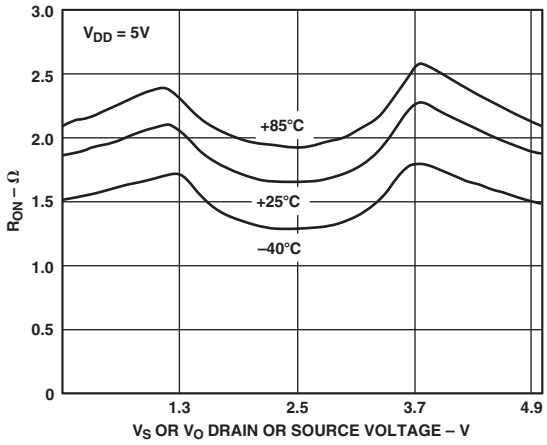
TERMINOLOGY

V_{DD}	Most Positive Power Supply Potential.
GND	Ground (0 V) Reference.
S	Source Terminal. May be an input or output.
D	Drain Terminal. May be an input or output.
IN	Logic Control Input.
$\overline{EN}$	Logic Control Input.
R_{ON}	Ohmic Resistance between D and S.
ΔR_{ON}	On Resistance Match between any Two Channels, i.e., R_{ON} max – R_{ON} min.
$R_{FLAT(ON)}$	Flatness is defined as the difference between the maximum and minimum value of on resistance as measured over the specified analog signal range.
I_S (OFF)	Source Leakage Current with the Switch OFF.
I_D (OFF)	Drain Leakage Current with the Switch OFF.
I_D, I_S (ON)	Channel Leakage Current with the Switch ON.
V_D (V_S)	Analog Voltage on Terminals D, S.
C_S (OFF)	OFF Switch Source Capacitance.
C_D (OFF)	OFF Switch Drain Capacitance.
C_D, C_S (ON)	ON Switch Capacitance.
t_{ON}	Delay between Applying the Digital Control Input and the Output Switching on. See Test Circuit 4.
t_{OFF}	Delay between Applying the Digital Control Input and the Output Switching Off.
t_D	OFF Time or ON Time Measured between the 90% Points of Both Switches, When Switching from One Address State to Another. See Test Circuit 5.
Crosstalk	A Measure of Unwanted Signal that is Coupled through from One Channel to Another as a Result of Parasitic Capacitance.
Off Isolation	A Measure of Unwanted Signal Coupling through an OFF Switch.
Bandwidth	Frequency Response of the Switch in the ON State Measured at 3 dB Down.
Distortion	$R_{FLAT(ON)}/R_L$

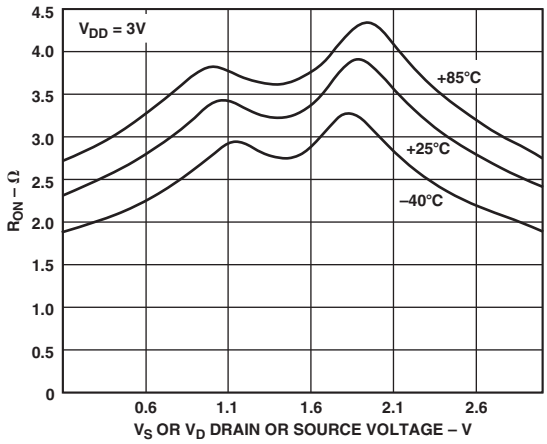
ADG774–Typical Performance Characteristics



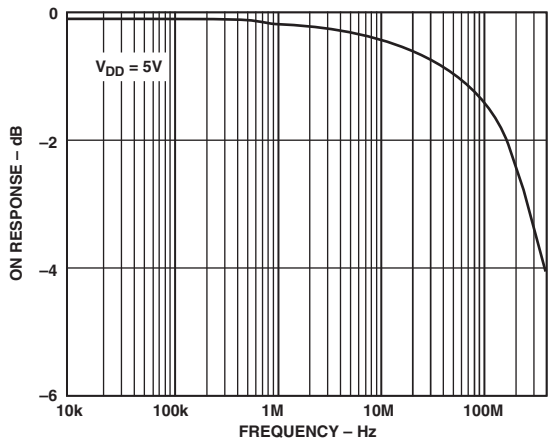
TPC 1. On Resistance as a Function of V_D (V_S) for Various Single Supplies



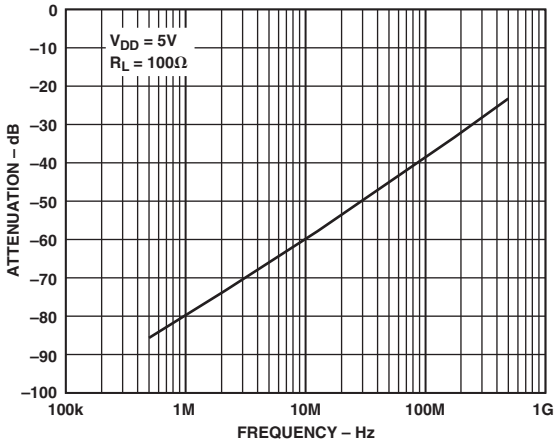
TPC 2. On Resistance as a Function of V_D (V_S) for Different Temperatures with 5 V Single Supplies



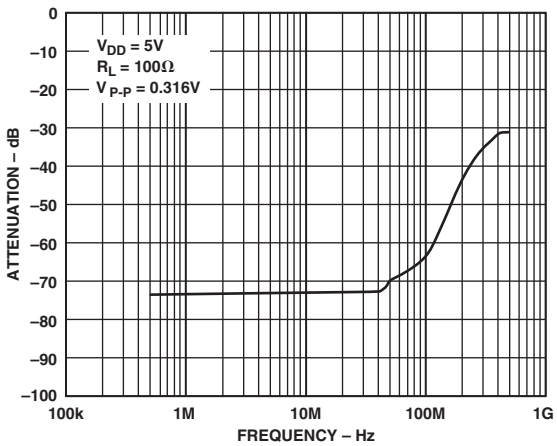
TPC 3. On Resistance as a Function of V_D (V_S) for Different Temperatures with 3 V Single Supplies



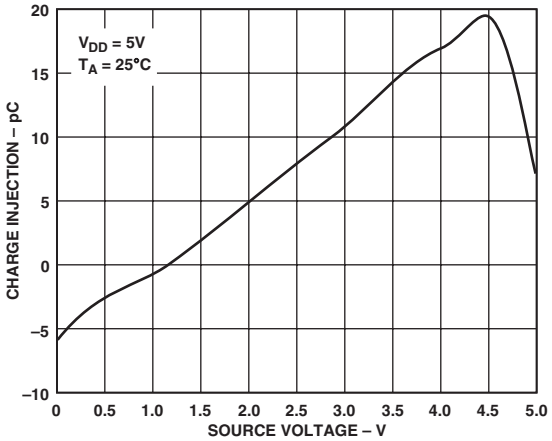
TPC 4. On Response vs. Frequency



TPC 5. Off Isolation vs. Frequency



TPC 6. Crosstalk vs. Frequency



TPC 7. Charge Injection vs. Source Voltage

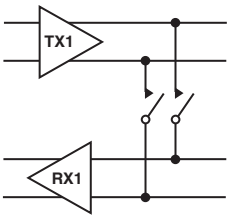


Figure 1. Loop Back

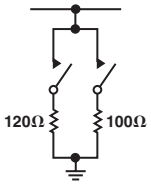


Figure 2. Line Termination

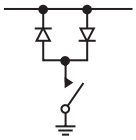
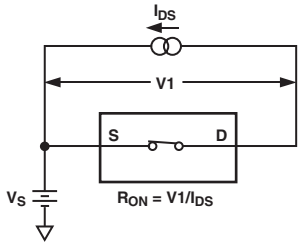
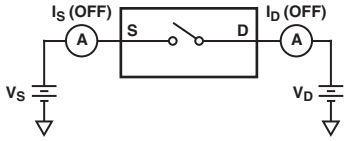


Figure 3. Line Clamp

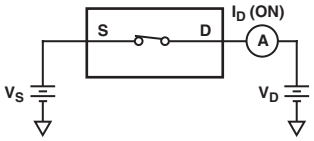
Test Circuits



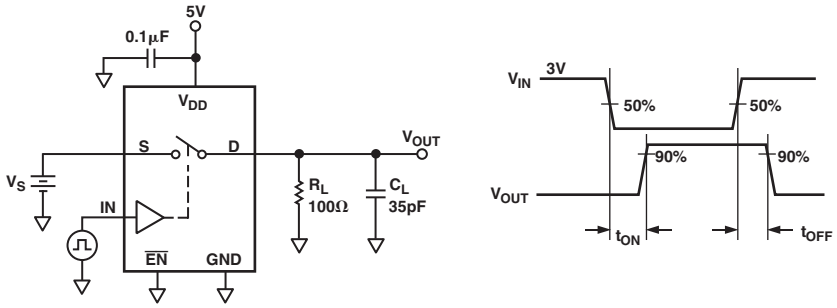
Test Circuit 1. On Resistance



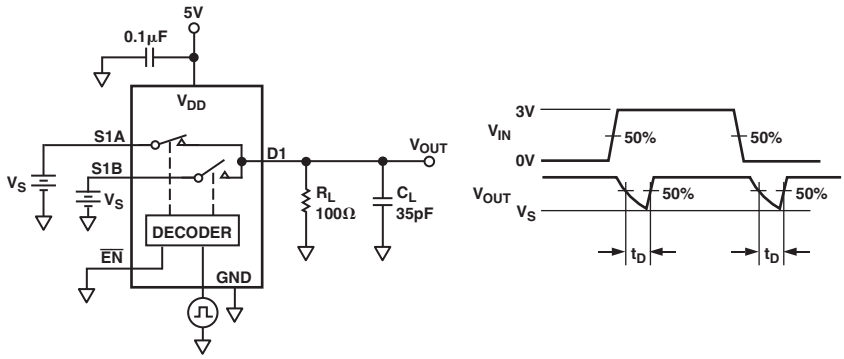
Test Circuit 2. Off Leakage



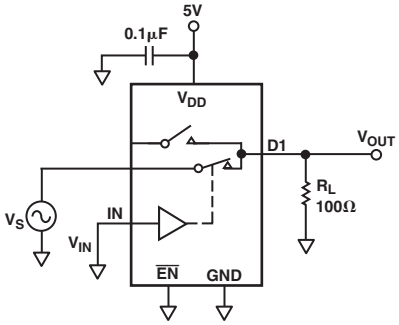
Test Circuit 3. On Leakage



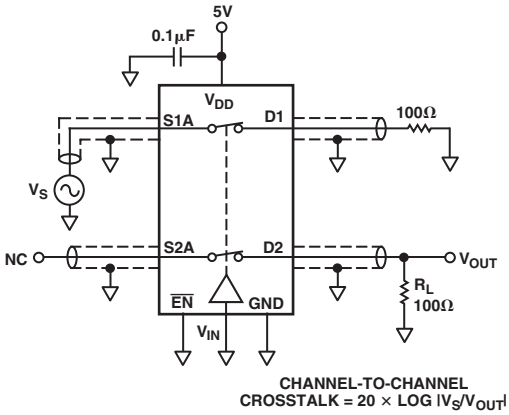
Test Circuit 4. Switching Times



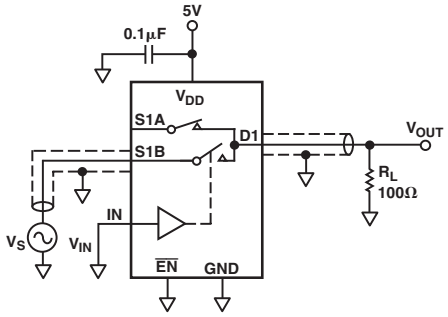
Test Circuit 5. Break-Before-Make Time Delay



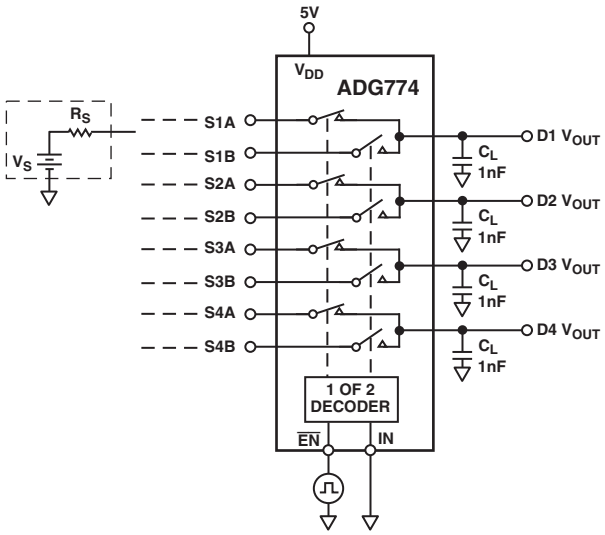
Test Circuit 6. Bandwidth

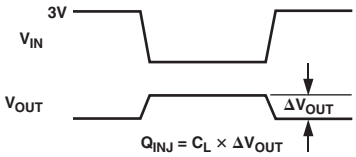


Test Circuit 7. Channel-to-Channel Crosstalk



Test Circuit 8. Off Isolation



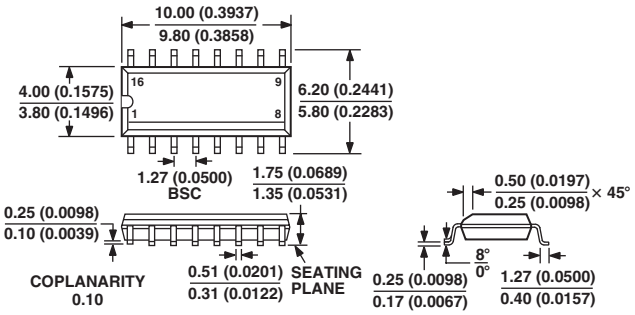


Test Circuit 9. Charge Injection

OUTLINE DIMENSIONS

16-Lead Standard Small Outline Package [SOIC]
Narrow Body
(R-16)

Dimensions shown in millimeters and (inches)

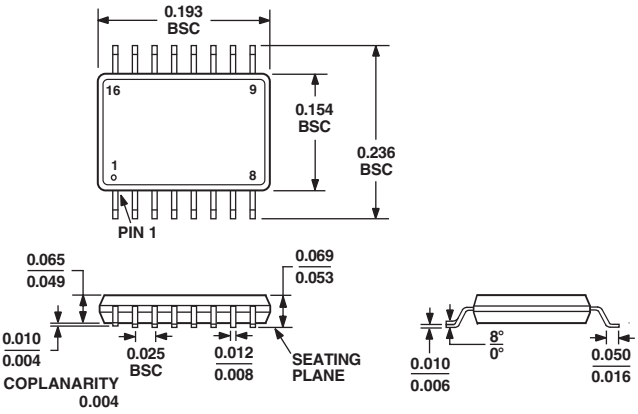


COMPLIANT TO JEDEC STANDARDS MS-012AC

CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

16-Lead Shrink Small Outline Package [QSOP]
(RQ-16)

Dimensions shown in inches



COMPLIANT TO JEDEC STANDARDS MO-137AB

Revision History

Location	Page
3/04—Data Sheet changed from REV. B to REV. C.	
Added APPLICATIONS	1
Changes to ORDERING GUIDE	4
10/03—Data Sheet changed from REV. A to REV. B.	
Updated formatting	Universal
Renumbered TPCs amd Figures	Universal
Changes to FEATURES	1
Changes to APPLICATIONS	1
Changes to PRODUCT HIGHLIGHTS	1
Changes to SPECIFICATIONS	2
Changes to ABSOLUTE MAXIMUM RATINGS	4
Updated ORDERING GUIDE	4
Delete Figure 2	7
Updated OUTLINE DIMENSIONS	10
4/03—Data Sheet changed from REV. 0 to REV. A.	
Renumbered TPCs and Figures	Universal
Updated OUTLINE DIMENSIONS	8