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SPECIFICATIONS

V_S = 0 V, 5 V @ T_A = 25°C, V_{CM} = 0 V, V_{OUT} = 0.2 V, unless otherwise noted.

Table 1.

		AD820A			AD820B			
Parameter	**Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
DC PERFORMANCE								
Initial Offset			0.1	0.8		0.1	0.4	mV
Maximum Offset over Temperature			0.5	1.2		0.5	0.9	mV
Offset Drift			2			2		µV/°C
Input Bias Current	V_{CM} = 0 V to 4 V		2	25		2	10	pA
At T_{MAX}			0.5	5		0.5	2.5	nA
Input Offset Current			2	20		2	10	pA
At T_{MAX}			0.5			0.5		nA
Open-Loop Gain	V_{OUT} = 0.2 V to 4 V							
	R_L = 100 kΩ	400	1000		500	1000		V/mV
T_{MIN} to T_{MAX}		400			400			V/mV
	R_L = 10 kΩ	80	150		80	150		V/mV
T_{MIN} to T_{MAX}		80			80			V/mV
	R_L = 1 kΩ	15	30		15	30		V/mV
T_{MIN} to T_{MAX}		10			10			V/mV
NOISE/HARMONIC PERFORMANCE								
Input Voltage Noise								
f = 0.1 Hz to 10 Hz			2			2		µV p-p
f = 10 Hz			25			25		nV/√Hz
f = 100 Hz			21			21		nV/√Hz
f = 1 kHz			16			16		nV/√Hz
f = 10 kHz			13			13		nV/√Hz
Input Current Noise								
f = 0.1 Hz to 10 Hz			18			18		fA p-p
f = 1 kHz			0.8			0.8		fA/√Hz
Harmonic Distortion	R_L = 10 kΩ to 2.5 V							
f = 10 kHz	V_{OUT} = 0.25 V to 4.75 V		−93			−93		dB
DYNAMIC PERFORMANCE								
Unity Gain Frequency			1.8			1.8		MHz
Full Power Response	V_{OUT} p-p = 4.5 V		210			210		kHz
Slew Rate			3			3		V/µs
Settling Time	V_{OUT} = 0.2 V to 4.5 V							
To 0.1%			1.4			1.4		µs
To 0.01%			1.8			1.8		µs
INPUT CHARACTERISTICS								
Common-Mode Voltage Range[1]								
T_{MIN} to T_{MAX}		−0.2		+4	−0.2		+4	V
CMRR	V_{CM} = 0 V to 2 V	66	80		72	80		dB
T_{MIN} to T_{MAX}		66			66			dB
Input Impedance								
Differential			10^{13}‖0.5			10^{13}‖0.5		Ω‖pF
Common Mode			10^{13}‖2.8			10^{13}‖2.8		Ω‖pF

Parameter	Conditions	AD820A Min	AD820A Typ	AD820A Max	AD820B Min	AD820B Typ	AD820B Max	Unit
OUTPUT CHARACTERISTICS								
Output Saturation Voltage[2]								
$V_{OL} - V_{EE}$	I_{SINK} = 20 µA		5	7		5	7	mV
T_{MIN} to T_{MAX}				10			10	mV
$V_{CC} - V_{OH}$	I_{SOURCE} = 20 µA		10	14		10	14	mV
T_{MIN} to T_{MAX}				20			20	mV
$V_{OL} - V_{EE}$	I_{SINK} = 2 mA		40	55		40	55	mV
T_{MIN} to T_{MAX}				80			80	mV
$V_{CC} - V_{OH}$	I_{SOURCE} = 2 mA		80	110		80	110	mV
T_{MIN} to T_{MAX}				160			160	mV
$V_{OL} - V_{EE}$	I_{SINK} = 15 mA		300	500		300	500	mV
T_{MIN} to T_{MAX}				1000			1000	mV
$V_{CC} - V_{OH}$	I_{SOURCE} = 15 mA		800	1500		800	1500	mV
T_{MIN} to T_{MAX}				1900			1900	mV
Operating Output Current		15			15			mA
T_{MIN} to T_{MAX}		12			12			mA
Short-Circuit Current			25			25		mA
Capacitive Load Drive			350			350		pF
POWER SUPPLY								
Quiescent Current	T_{MIN} to T_{MAX}		620	800		620	800	µA
Power Supply Rejection	V+ = 5 V to 15 V	70	80		66	80		dB
T_{MIN} to T_{MAX}		70			66			dB

[1] This is a functional specification. Amplifier bandwidth decreases when the input common-mode voltage is driven in the range ((V+) − 1 V) to V+. Common-mode error voltage is typically less than 5 mV with the common-mode voltage set at 1 V below the positive supply.
[2] $V_{OL} - V_{EE}$ is defined as the difference between the lowest possible output voltage (V_{OL}) and the negative voltage supply rail (V_{EE}). $V_{CC} - V_{OH}$ is defined as the difference between the highest possible output voltage (V_{OH}) and the positive supply voltage (V_{CC}).

V_S = ±5 V @ T_A = 25°C, V_{CM} = 0 V, V_{OUT} = 0 V, unless otherwise noted.

Table 2.

Parameter	Conditions	AD820A Min	AD820A Typ	AD820A Max	AD820B Min	AD820B Typ	AD820B Max	Unit
DC PERFORMANCE								
Initial Offset			0.1	0.8		0.3	0.4	mV
Maximum Offset over Temperature			0.5	1.5		0.5	1	mV
Offset Drift			2			2		μV/°C
Input Bias Current	V_{CM} = −5 V to +4 V		2	25		2	10	pA
At T_{MAX}			0.5	5		0.5	2.5	nA
Input Offset Current			2	20		2	10	pA
At T_{MAX}			0.5			0.5		nA
Open-Loop Gain	V_{OUT} = −4 V to +4 V							
	R_L = 100 kΩ	400	1000		400	1000		V/mV
T_{MIN} to T_{MAX}		400			400			V/mV
	R_L = 10 kΩ	80	150		80	150		V/mV
T_{MIN} to T_{MAX}		80			80			V/mV
	R_L = 1 kΩ	20	30		20	30		V/mV
T_{MIN} to T_{MAX}		10			10			V/mV
NOISE/HARMONIC PERFORMANCE								
Input Voltage Noise								
f = 0.1 Hz to 10 Hz			2			2		μV p-p
f = 10 Hz			25			25		nV/√Hz
f = 100 Hz			21			21		nV/√Hz
f = 1 kHz			16			16		nV/√Hz
f = 10 kHz			13			13		nV/√Hz
Input Current Noise								
f = 0.1 Hz to 10 Hz			18			18		fA p-p
f = 1 kHz			0.8			0.8		fA/√Hz
Harmonic Distortion	R_L = 10 kΩ							
f = 10 kHz	V_{OUT} = ±4.5 V		−93			−93		dB
DYNAMIC PERFORMANCE								
Unity Gain Frequency			1.9			1.8		MHz
Full Power Response	V_{OUT} p-p = 9 V		105			105		kHz
Slew Rate			3			3		V/μs
Settling Time	V_{OUT} = 0 V to ±4.5 V							
To 0.1%			1.4			1.4		μs
To 0.01%			1.8			1.8		μs
INPUT CHARACTERISTICS								
Common-Mode Voltage Range[1]								
T_{MIN} to T_{MAX}		−5.2		+4	−5.2		+4	V
CMRR	V_{CM} = −5 V to +2 V	66	80		72	80		dB
T_{MIN} to T_{MAX}		66			66			dB
Input Impedance								
Differential			10^{13}‖0.5			10^{13}‖0.5		Ω‖pF
Common Mode			10^{13}‖2.8			10^{13}‖2.8		Ω‖pF

Parameter	Conditions	AD820A Min	AD820A Typ	AD820A Max	AD820B Min	AD820B Typ	AD820B Max	Unit
OUTPUT CHARACTERISTICS								
Output Saturation Voltage[2]								
$V_{OL} - V_{EE}$	I_{SINK} = 20 µA		5	7		5	7	mV
T_{MIN} to T_{MAX}				10			10	mV
$V_{CC} - V_{OH}$	I_{SOURCE} = 20 µA		10	14		10	14	mV
T_{MIN} to T_{MAX}				20			20	mV
$V_{OL} - V_{EE}$	I_{SINK} = 2 mA		40	55		40	55	mV
T_{MIN} to T_{MAX}				80			80	mV
$V_{CC} - V_{OH}$	I_{SOURCE} = 2 mA		80	110		80	110	mV
T_{MIN} to T_{MAX}				160			160	mV
$V_{OL} - V_{EE}$	I_{SINK} = 15 mA		300	500		300	500	mV
T_{MIN} to T_{MAX}				1000			1000	mV
$V_{CC} - V_{OH}$	I_{SOURCE} = 15 mA		800	1500		800	1500	mV
T_{MIN} to T_{MAX}				1900			1900	mV
Operating Output Current		15			15			mA
T_{MIN} to T_{MAX}		12			12			mA
Short-Circuit Current			30			30		mA
Capacitive Load Drive			350			350		pF
POWER SUPPLY								
Quiescent Current	T_{MIN} to T_{MAX}		650	800		620	800	µA
Power Supply Rejection	V+ = 5 V to 15 V	70	80		70	80		dB
T_{MIN} to T_{MAX}		70			70			dB

[1] This is a functional specification. Amplifier bandwidth decreases when the input common-mode voltage is driven in the range ((V+) − 1 V) to V+. Common-mode error voltage is typically less than 5 mV with the common-mode voltage set at 1 V below the positive supply.
[2] $V_{OL} - V_{EE}$ is defined as the difference between the lowest possible output voltage (V_{OL}) and the negative voltage supply rail (V_{EE}). $V_{CC} - V_{OH}$ is defined as the difference between the highest possible output voltage (V_{OH}) and the positive supply voltage (V_{CC}).

V_S = ±15 V @ T_A = 25°C, V_{CM} = 0 V, V_{OUT} = 0 V, unless otherwise noted.

Table 3.

Parameter	Conditions	AD820A Min	AD820A Typ	AD820A Max	AD820B Min	AD820B Typ	AD820B Max	Unit
DC PERFORMANCE								
Initial Offset			0.4	2		0.3	1.0	mV
Maximum Offset over Temperature			0.5	3		0.5	2	mV
Offset Drift			2			2		µV/°C
Input Bias Current	V_{CM} = 0 V		2	25		2	10	pA
	V_{CM} = −10 V		40			40		pA
At T_{MAX}	V_{CM} = 0 V		0.5	5		0.5	2.5	nA
Input Offset Current			2	20		2	10	pA
At T_{MAX}			0.5			0.5		nA
Open-Loop Gain	V_{OUT} = −10 V to +10 V							
	R_L = 100 kΩ	500	2000		500	2000		V/mV
T_{MIN} to T_{MAX}		500			500			V/mV
	R_L = 10 kΩ	100	500		100	500		V/mV
T_{MIN} to T_{MAX}		100			100			V/mV
	R_L = 1 kΩ	30	45		30	45		V/mV
T_{MIN} to T_{MAX}		20			20			V/mV
NOISE/HARMONIC PERFORMANCE								
Input Voltage Noise								
f = 0.1 Hz to 10 Hz			2			2		µV p-p
f = 10 Hz			25			25		nV/√Hz
f = 100 Hz			21			21		nV/√Hz
f = 1 kHz			16			16		nV/√Hz
f = 10 kHz			13			13		nV/√Hz
Input Current Noise								
f = 0.1 Hz to 10 Hz			18			18		fA p-p
f = 1 kHz			0.8			0.8		fA/√Hz
Harmonic Distortion	R_L = 10 kΩ							
f = 10 kHz	V_{OUT} = ±10 V		−85			−85		dB
DYNAMIC PERFORMANCE								
Unity Gain Frequency			1.9			1.9		MHz
Full Power Response	V_{OUT} p-p = 20 V		45			45		kHz
Slew Rate			3			3		V/µs
Settling Time	V_{OUT} = 0 V to ±10 V							
To 0.1%			4.1			4.1		µs
To 0.01%			4.5			4.5		µs
INPUT CHARACTERISTICS								
Common-Mode Voltage Range[1]								
T_{MIN} to T_{MAX}		−15.2		+14	−15.2		+14	V
CMRR	V_{CM} = −15 V to +12 V	70	80		74	90		dB
T_{MIN} to T_{MAX}		70			74			dB
Input Impedance								
Differential			10^{13}‖0.5			10^{13}‖0.5		Ω‖pF
Common Mode			10^{13}‖2.8			10^{13}‖2.8		Ω‖pF

Parameter	Conditions	AD820A Min	AD820A Typ	AD820A Max	AD820B Min	AD820B Typ	AD820B Max	Unit
OUTPUT CHARACTERISTICS								
Output Saturation Voltage[2]								
$V_{OL} - V_{EE}$	I_{SINK} = 20 μA		5	7		5	7	mV
T_{MIN} to T_{MAX}				10			10	mV
$V_{CC} - V_{OH}$	I_{SOURCE} = 20 μA		10	14		10	14	mV
T_{MIN} to T_{MAX}				20			20	mV
$V_{OL} - V_{EE}$	I_{SINK} = 2 mA		40	55		40	55	mV
T_{MIN} to T_{MAX}				80			80	mV
$V_{CC} - V_{OH}$	I_{SOURCE} = 2 mA		80	110		80	110	mV
T_{MIN} to T_{MAX}				160			160	mV
$V_{OL} - V_{EE}$	I_{SINK} = 15 mA		300	500		300	500	mV
T_{MIN} to T_{MAX}				1000			1000	mV
$V_{CC} - V_{OH}$	I_{SOURCE} = 15 mA		800	1500		800	1500	mV
T_{MIN} to T_{MAX}				1900			1900	mV
Operating Output Current		20			20			mA
T_{MIN} to T_{MAX}		15			15			mA
Short-Circuit Current			45			45		mA
Capacitive Load Drive			350			350		pF
POWER SUPPLY								
Quiescent Current	T_{MIN} to T_{MAX}		700	900		700	900	μA
Power Supply Rejection	V+ = 5 V to 15 V	70	80		70	80		dB
T_{MIN} to T_{MAX}		70			70			dB

[1] This is a functional specification. Amplifier bandwidth decreases when the input common-mode voltage is driven in the range ((V+) − 1 V) to V+. Common-mode error voltage is typically less than 5 mV with the common-mode voltage set at 1 V below the positive supply.
[2] $V_{OL} - V_{EE}$ is defined as the difference between the lowest possible output voltage (V_{OL}) and the negative voltage supply rail (V_{EE}). $V_{CC} - V_{OH}$ is defined as the difference between the highest possible output voltage (V_{OH}) and the positive supply voltage (V_{CC}).

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
Supply Voltage	±18 V
Internal Power Dissipation	
8-Lead PDIP (N)	1.6 W
8-Lead SOIC_N (R)	1.0 W
8-Lead MSOP (RM)	0.8 W
Input Voltage[1]	((V+) + 0.2 V) to (V−) − 20 V
Output Short-Circuit Duration	Indefinite
Differential Input Voltage	±30 V
Storage Temperature Range	
8-Lead PDIP (N)	−65°C to +125°C
8-Lead SOIC_N (R)	−65°C to +150°C
8-Lead MSOP (RM)	−65°C to +150°C
Operating Temperature Range	
AD820A/AD820B	−40°C to +85°C
Lead Temperature(Soldering, 60 sec)	260°C

[1] See Input Characteristics section.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 5. Thermal Resistance

Package Type	θ_{JA}	Unit
8-Lead PDIP (N)	90	°C/W
8-Lead SOIC_N (R)	160	°C/W
8-Lead MSOP (RM)	190	°C/W

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

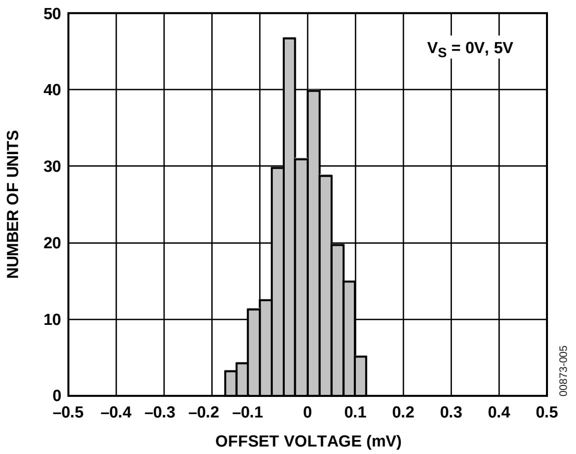


Figure 4. Typical Distribution of Offset Voltage (248 Units)

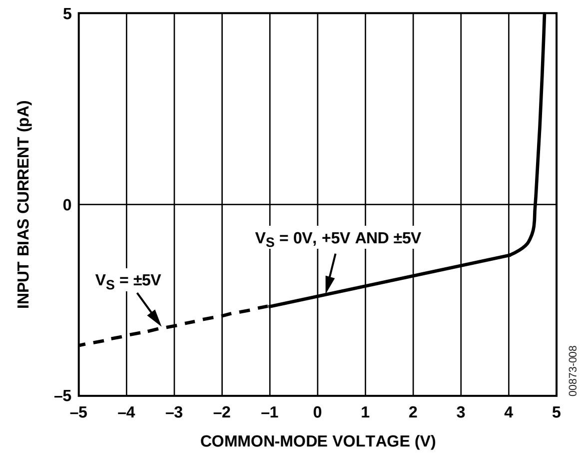


Figure 7. Input Bias Current vs. Common-Mode Voltage; V_S = +5 V, 0 V and V_S = ±5 V

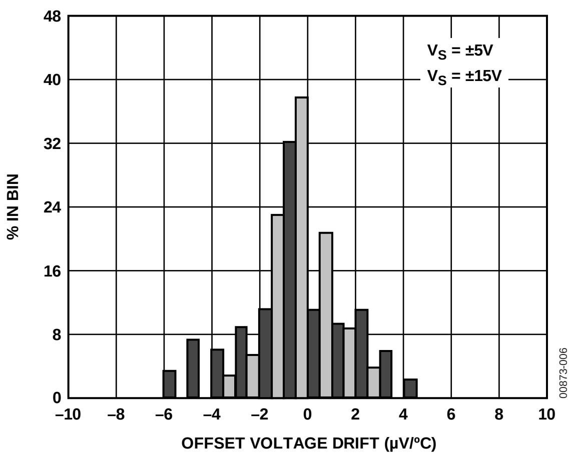


Figure 5. Typical Distribution of Offset Voltage Drift (120 Units)

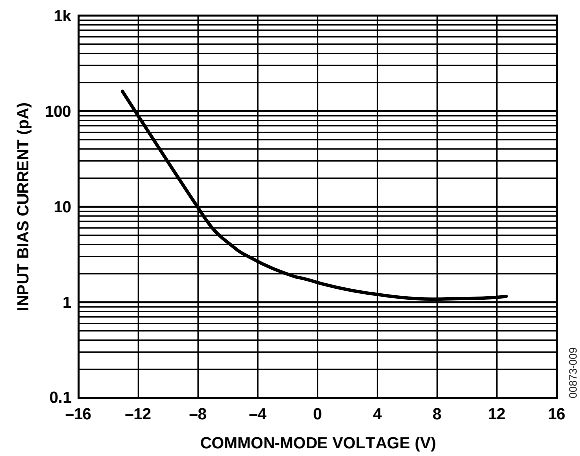


Figure 8. Input Bias Current vs. Common-Mode Voltage; V_S = ±15 V

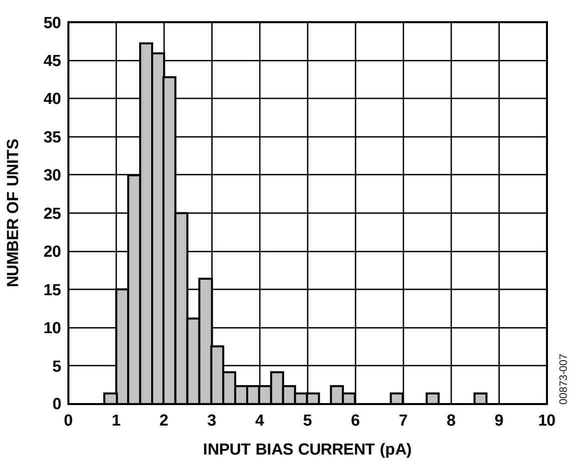


Figure 6. Typical Distribution of Input Bias Current (213 Units)

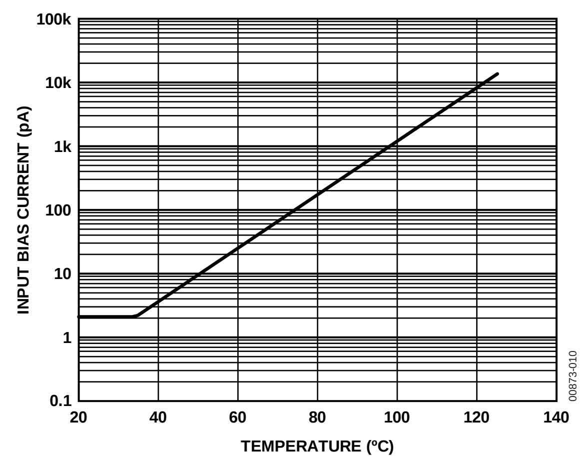


Figure 9. Input Bias Current vs. Temperature; V_S = 5 V, V_{CM} = 0 V

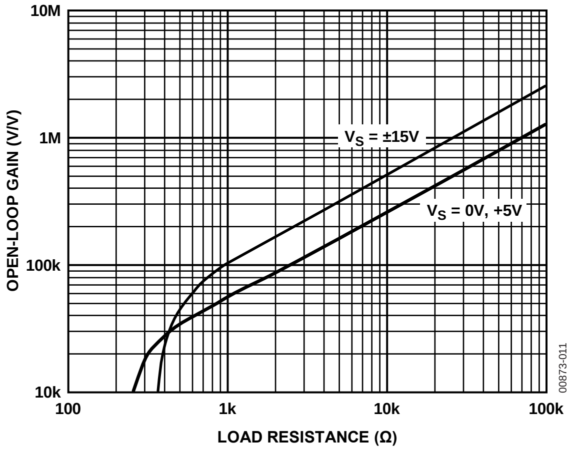


Figure 10. Open-Loop Gain vs. Load Resistance

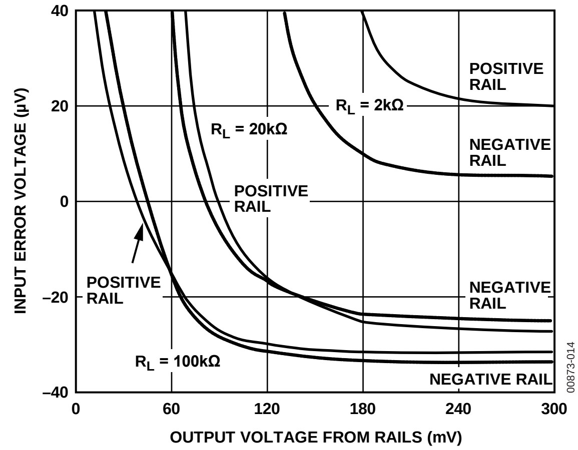


Figure 13. Input Error Voltage vs. Output Voltage Within 300 mV of Either Supply Rail for Various Resistive Loads; $V_S = \pm5$ V

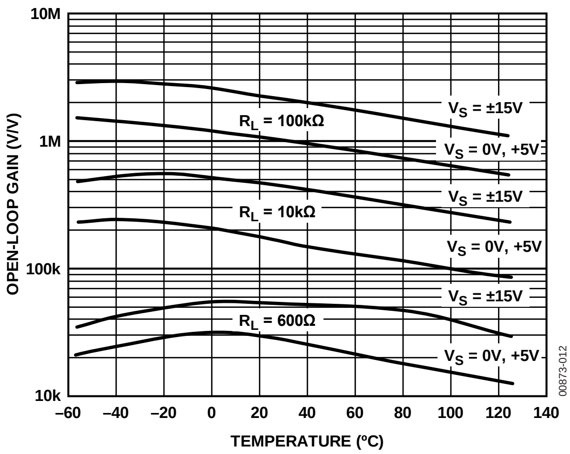


Figure 11. Open-Loop Gain vs. Temperature

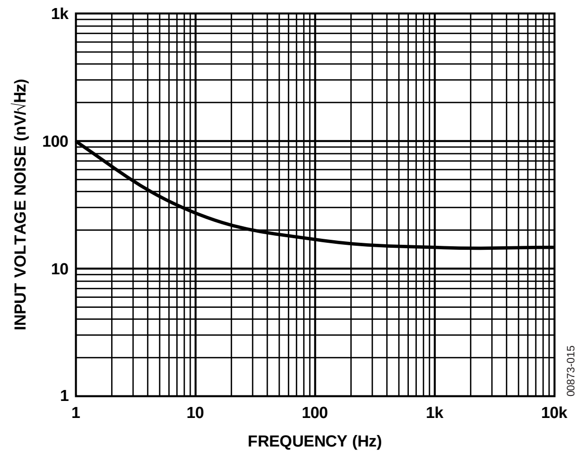


Figure 14. Input Voltage Noise vs. Frequency

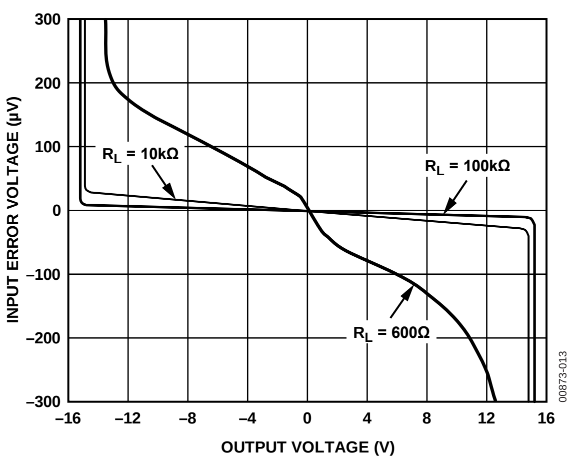


Figure 12. Input Error Voltage vs. Output Voltage for Resistive Loads

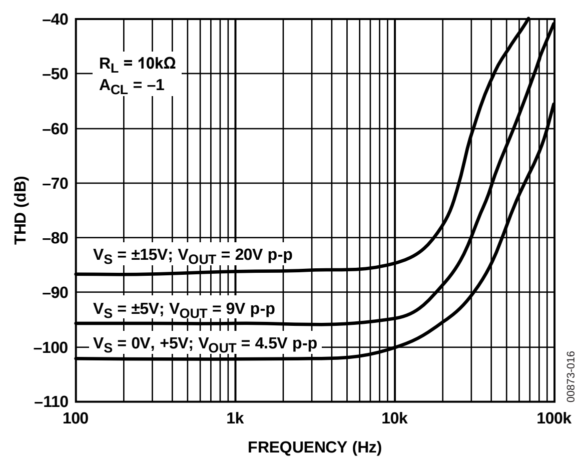


Figure 15. Total Harmonic Distortion vs. Frequency

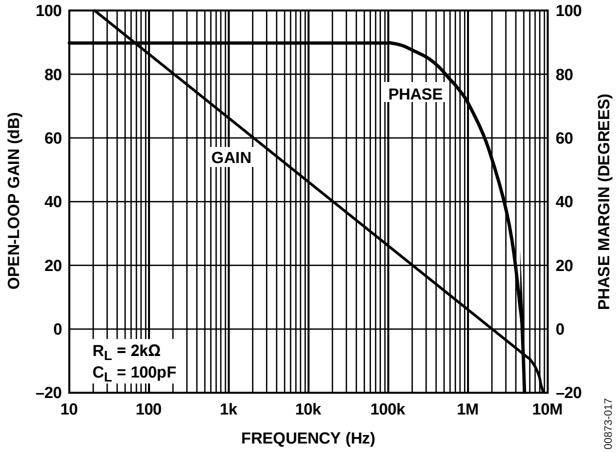


Figure 16. Open-Loop Gain and Phase Margin vs. Frequency

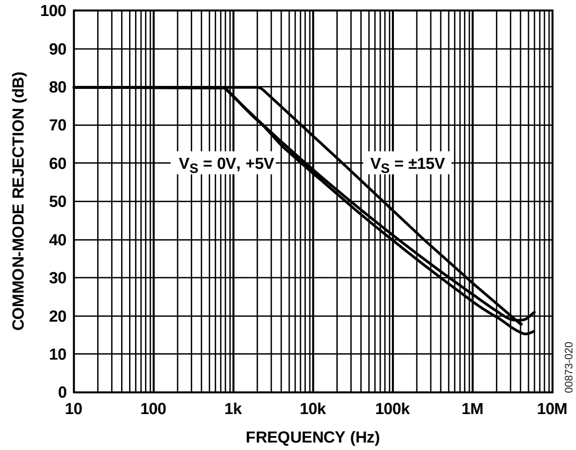


Figure 19. Common-Mode Rejection vs. Frequency

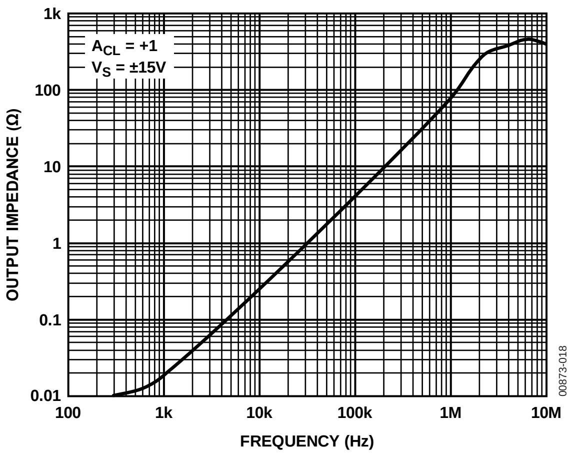


Figure 17. Output Impedance vs. Frequency

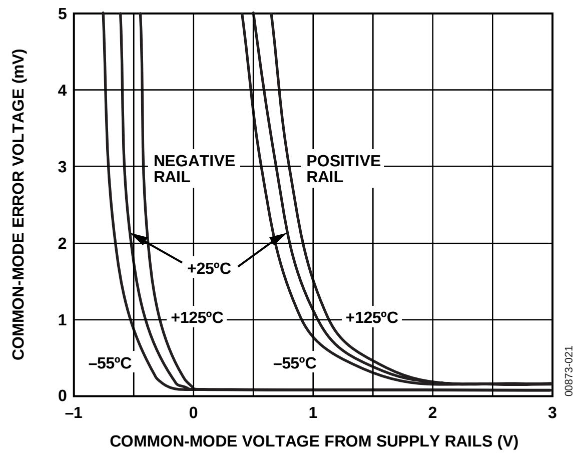


Figure 20. Absolute Common-Mode Error vs. Common-Mode Voltage from Supply Rails ($V_S – V_{CM}$)

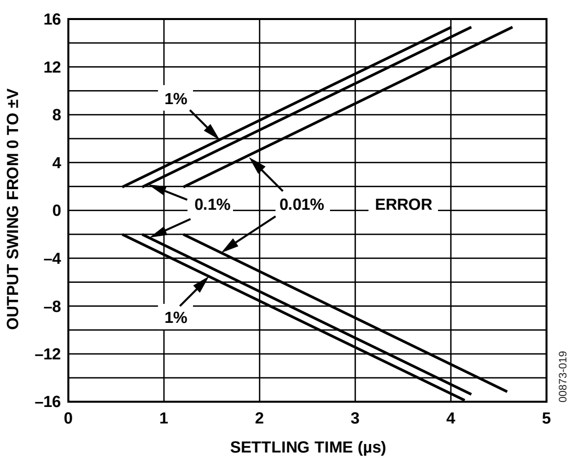


Figure 18. Output Swing and Error vs. Settling Time

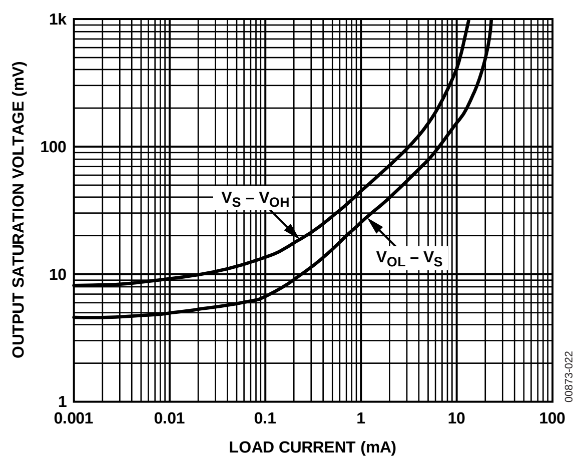


Figure 21. Output Saturation Voltage vs. Load Current

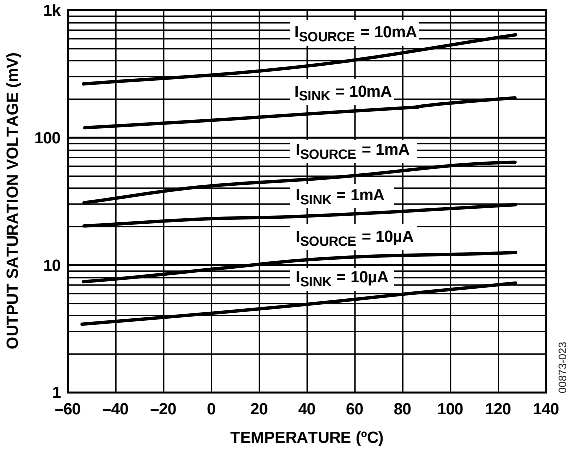


Figure 22. Output Saturation Voltage vs. Temperature

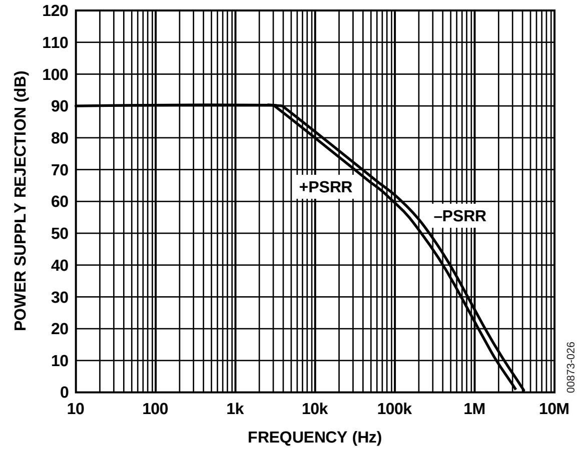


Figure 25. Power Supply Rejection vs. Frequency

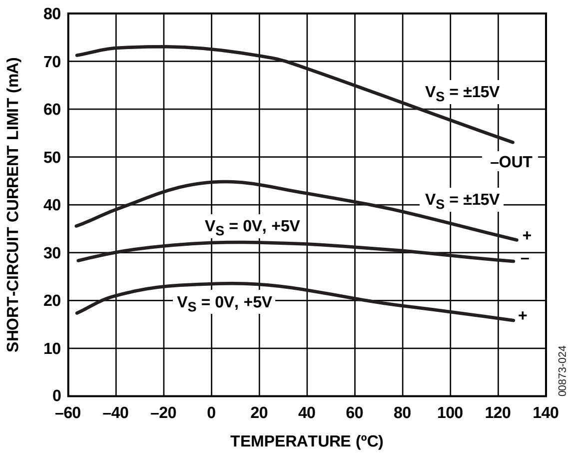


Figure 23. Short-Circuit Current Limit vs. Temperature

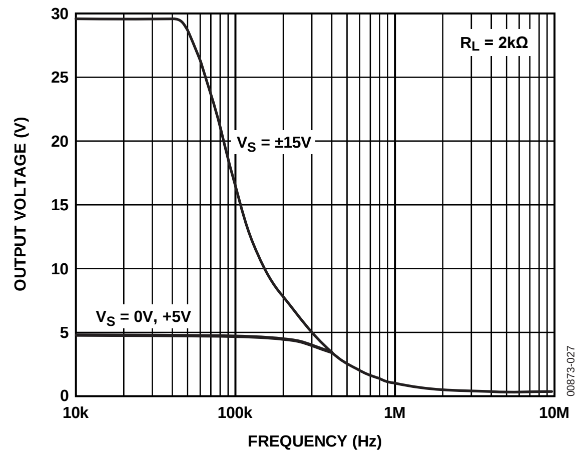


Figure 26. Large Signal Frequency Response

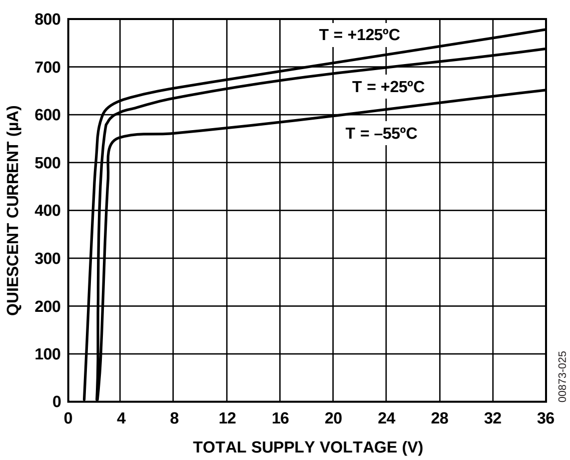


Figure 24. Quiescent Current vs. Supply Voltage over Different Temperatures

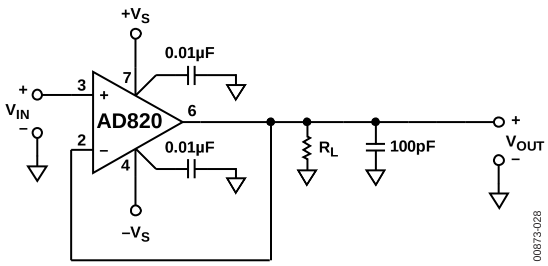


Figure 27. Unity-Gain Follower, Used for Figure 28 Through Figure 32

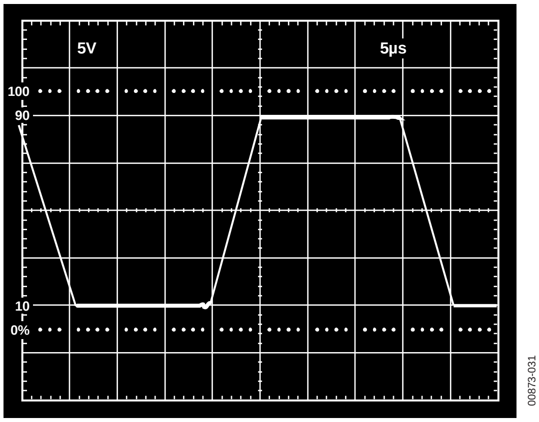


Figure 30. Large Signal Response Unity-Gain Follower; $V_S = \pm15$ V, $R_L = 10$ kΩ

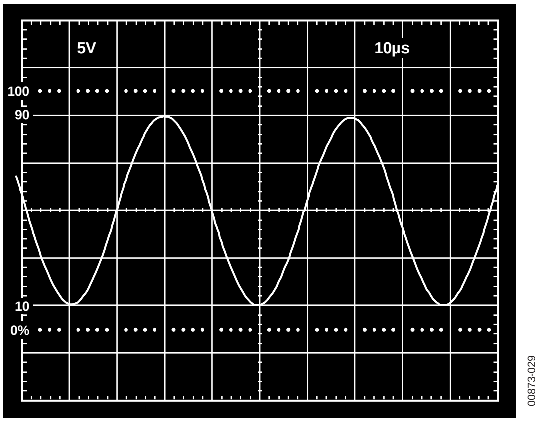


Figure 28. 20 V, 25 kHz Sine Input; Unity-Gain Follower; $R_L = 600$ Ω, $V_S = \pm15$ V

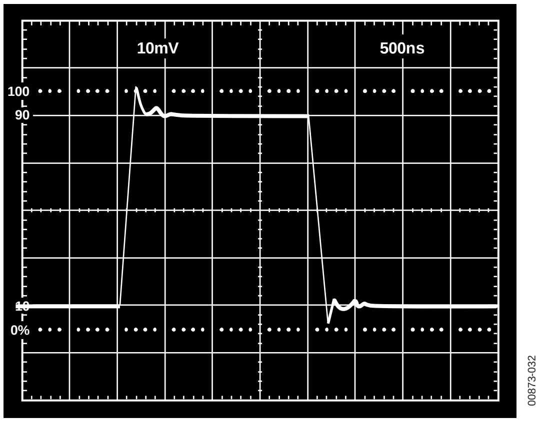


Figure 31. Small Signal Response Unity-Gain Follower; $V_S = \pm15$ V, $R_L = 10$ kΩ

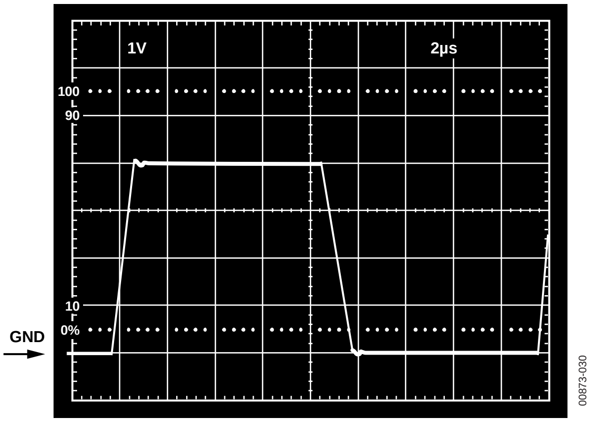


Figure 29. $V_S = 5$ V, 0 V; Unity-Gain Follower Response to 0 V to 4 V Step

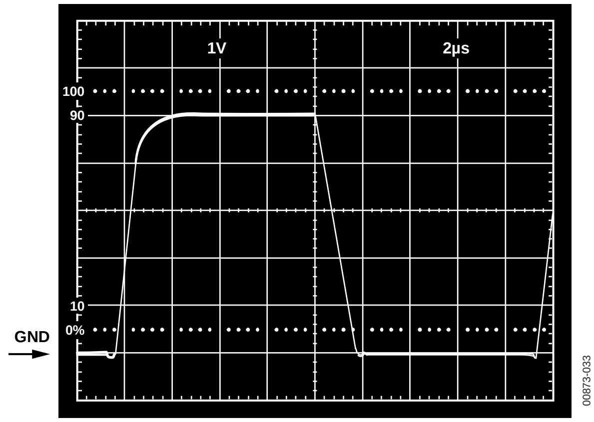


Figure 32. $V_S = 5$ V, 0 V; Unity-Gain Follower Response to 0 V to 5 V Step

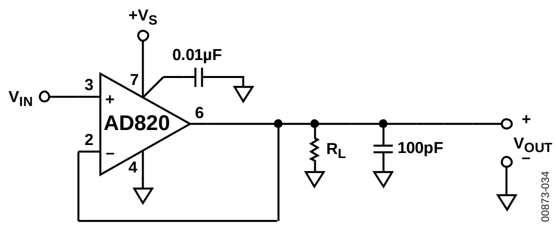


Figure 33. Unity-Gain Follower, Used for Figure 34

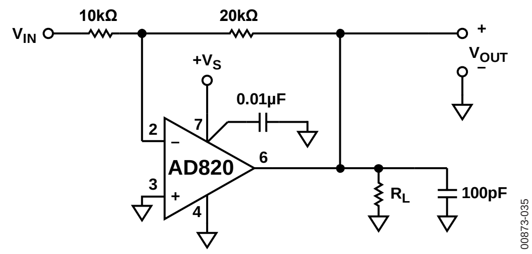


Figure 35. Gain-of-2 Inverter, Used for Figure 36 and Figure 37

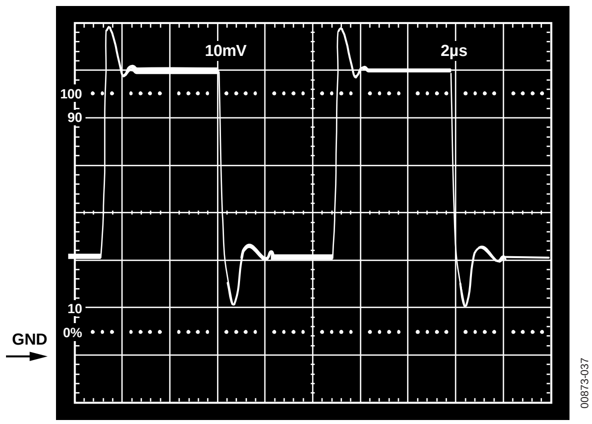


Figure 34. V_S = 5 V, 0 V; Unity-Gain Follower Response to 40 mV Step Centered 40 mV Above Ground

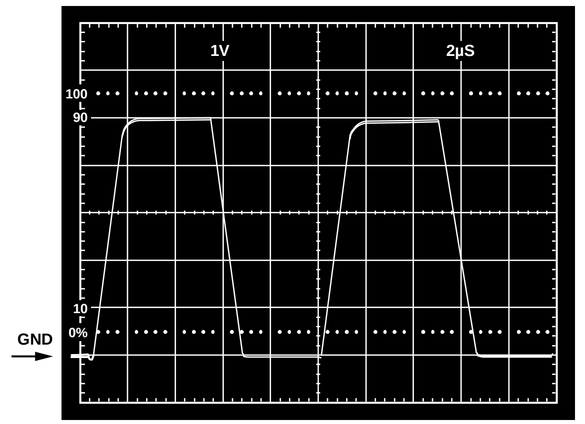


Figure 36. V_S = 5 V, 0 V; Gain-of-2 Inverter Response to 2.5 V Step, Centered −1.25 V Below Ground

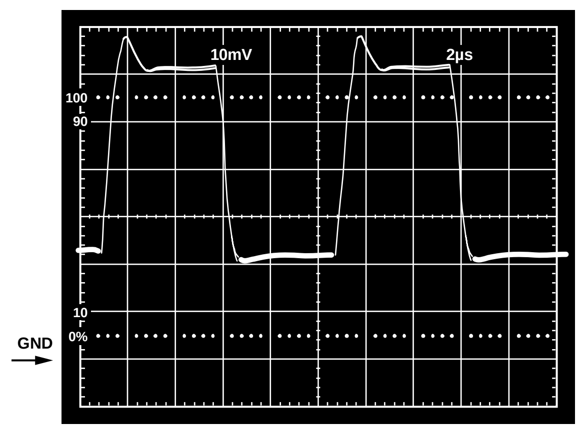


Figure 37. V_S = 5 V, 0 V; Gain-of-2 Inverter Response to 20 mV Step, Centered 20 mV Below Ground

APPLICATIONS INFORMATION

INPUT CHARACTERISTICS

In the AD820, N-channel JFETs are used to provide a low offset, low noise, high impedance input stage. Minimum input common-mode voltage extends from 0.2 V below $-V_S$ to 1 V less than $+V_S$. Driving the input voltage closer to the positive rail causes a loss of amplifier bandwidth (as can be seen by comparing the large signal responses shown in Figure 29 and Figure 32) and increased common-mode voltage error, as illustrated in Figure 20.

The AD820 does not exhibit phase reversal for input voltages up to and including $+V_S$. Figure 38a shows the response of an AD820 voltage follower to a 0 V to 5 V ($+V_S$) square wave input. The input and output are superimposed. The output polarity tracks the input polarity up to $+V_S$ with no phase reversal. The reduced bandwidth above a 4 V input causes the rounding of the output waveform. For input voltages greater than $+V_S$, a resistor in series with the AD820 positive input prevents phase reversal, at the expense of greater input voltage noise. This is illustrated in Figure 38b.

Because the input stage uses N-channel JFETs, input current during normal operation is negative; the current flows out from the input terminals. If the input voltage is driven more positive than $+V_S$ − 0.4 V, the input current reverses direction as internal device junctions become forward biased. This is illustrated in Figure 7.

A current-limiting resistor should be used in series with the input of the AD820 if there is a possibility of the input voltage exceeding the positive supply by more than 300 mV, or if an input voltage is applied to the AD820 when $\pm V_S = 0$ V. The amplifier can be damaged if left in that condition for more than 10 seconds. A 1 kΩ resistor allows the amplifier to withstand up to 10 V of continuous overvoltage, and increases the input voltage noise by a negligible amount.

Input voltages less than $-V_S$ are a completely different story. The amplifier can safely withstand input voltages 20 V below the negative supply voltage as long as the total voltage from the positive supply to the input terminal is less than 36 V. In addition, the input stage typically maintains picoamp level input currents across that input voltage range.

The AD820 is designed for 13 nV/√Hz wideband input voltage noise and maintains low noise performance to low frequencies (refer to Figure 14). This noise performance, along with the AD820 low input current and current noise, means that the AD820 contributes negligible noise for applications with source resistances greater than 10 kΩ and signal bandwidths greater than 1 kHz. This is illustrated in Figure 39.

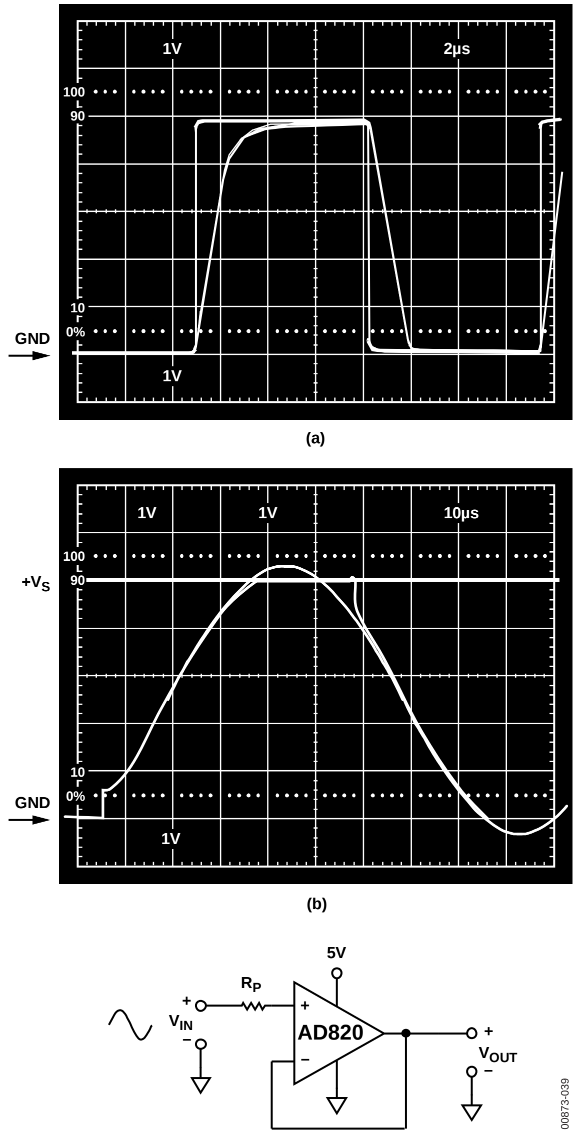


Figure 38. (a) Response with $R_P = 0\ \Omega$; V_{IN} from 0 V to $+V_S$ (b) $V_{IN} = 0$ V to $+V_S + 200$ mV, $V_{OUT} = 0$ V to $+V_S$, $R_P = 49.9$ kΩ

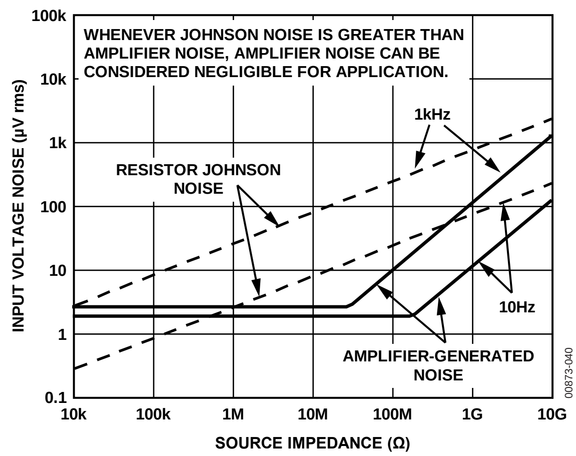


Figure 39. Total Noise vs. Source Impedance

OUTPUT CHARACTERISTICS

The AD820 unique bipolar rail-to-rail output stage swings within 5 mV of the negative supply and 10 mV of the positive supply with no external resistive load. The approximate output saturation resistance of the AD820 is 40 Ω sourcing and 20 Ω sinking. This can be used to estimate output saturation voltage when driving heavier current loads. For instance, when sourcing 5 mA, the saturation voltage to the positive supply rail is 200 mV; when sinking 5 mA, the saturation voltage to the negative rail is 100 mV.

The open-loop gain characteristic of the amplifier changes as a function of resistive load, as shown in Figure 10 through Figure 13. For load resistances over 20 kΩ, the AD820 input error voltage is virtually unchanged until the output voltage is driven to 180 mV of either supply.

If the AD820 output is driven hard against the output saturation voltage, it recovers within 2 μs of the input returning to the linear operating region of the amplifier.

Direct capacitive load interacts with the effective output impedance of the amplifier to form an additional pole in the amplifier feedback loop, which can cause excessive peaking on the pulse response or loss of stability. The worst case occurs when the amplifier is used as a unity-gain follower. Figure 40 shows AD820 pulse response as a unity-gain follower driving 350 pF. This amount of overshoot indicates approximately 20 degrees of phase margin—the system is stable, but is nearing the edge. Configurations with less loop gain, and as a result less loop bandwidth, are much less sensitive to capacitance load effects. Figure 41 is a plot of noise gain vs. the capacitive load that results in a 20 degree phase margin for the AD820. Noise gain is the inverse of the feedback attenuation factor provided by the feedback network in use.

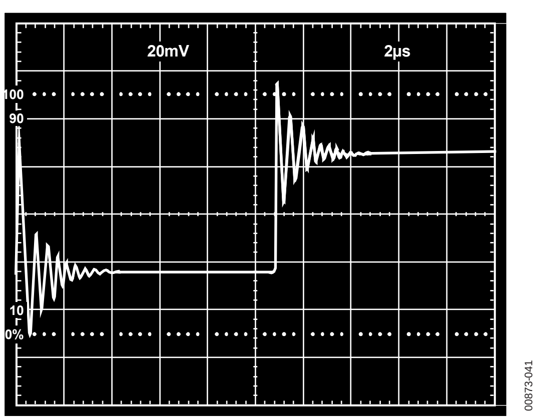


Figure 40. Small Signal Response of AD820 as Unity-Gain Follower Driving 350 pF Capacitive Load

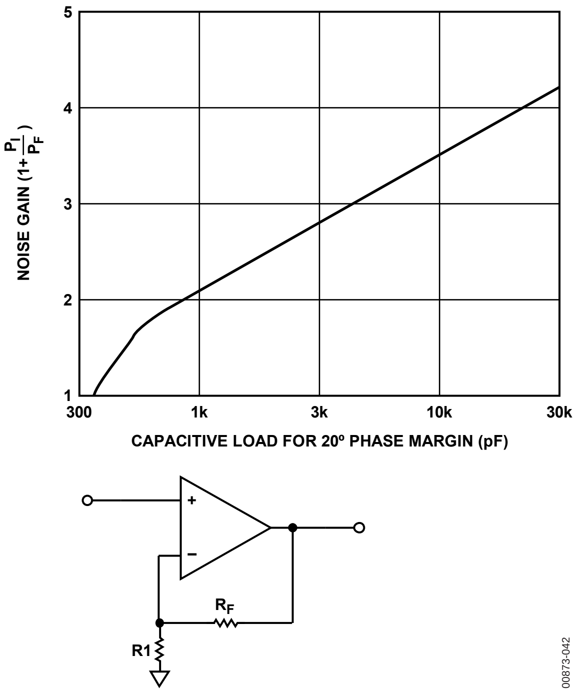


Figure 41. Noise Gain vs. Capacitive Load Tolerance

Figure 42 shows a possible configuration for extending capacitance load drive capability for a unity-gain follower. With these component values, the circuit drives 5000 pF with a 10% overshoot.

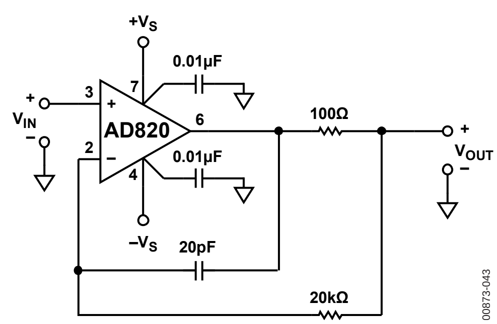


Figure 42. Extending Unity-Gain Follower Capacitive Load Capability Beyond 350 pF

SINGLE-SUPPLY HALF-WAVE AND FULL-WAVE RECTIFIERS

An AD820 configured as a unity-gain follower and operated with a single supply can be used as a simple half-wave rectifier. The AD820 inputs maintain picoamp level input currents even when driven well below the negative supply. The rectifier puts that behavior to good use, maintaining an input impedance of over 10^{11} Ω for input voltages from 1 V from the positive supply to 20 V below the negative supply.

The full- and half-wave rectifier shown in Figure 43 operates as follows: when V_{IN} is above ground, R1 is bootstrapped through the unity-gain follower, A1, and the loop of Amplifier A2. This forces the inputs of A2 to be equal; thus, no current flows through R1 or R2, and the circuit output tracks the input. When V_{IN} is below ground, the output of A1 is forced to ground. The noninverting input of Amplifier A2 sees the ground level output of A1; therefore, A2 operates as a unity-gain inverter. The output at Node C is then a full-wave rectified version of the input. Node B is a buffered half-wave rectified version of the input. Input voltages up to ±18 V can be rectified, depending on the voltage supply used.

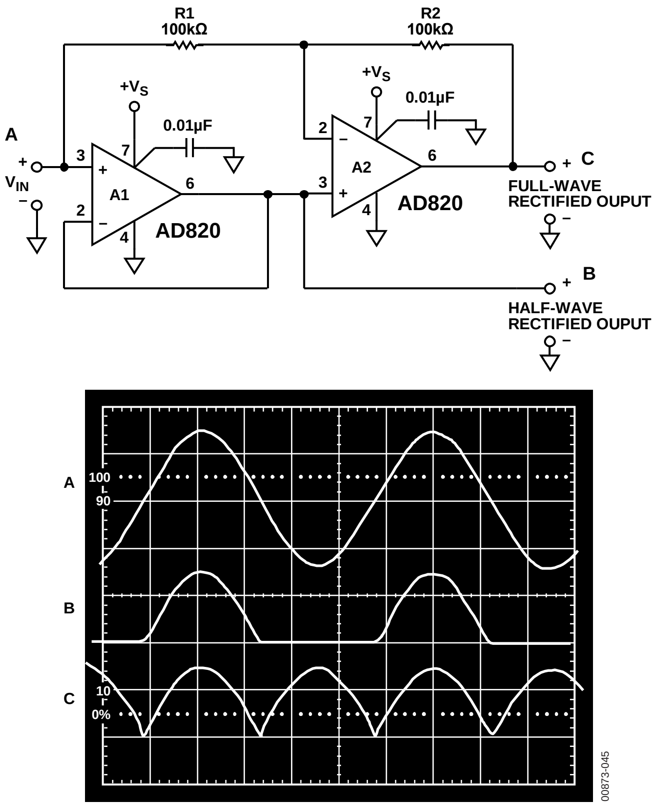


Figure 43. Single-Supply Half- and Full-Wave Rectifier

4.5 V LOW DROPOUT, LOW POWER REFERENCE

The rail-to-rail performance of the AD820 can be used to provide low dropout performance for low power reference circuits powered with a single low voltage supply. Figure 44 shows a 4.5 V reference using the AD820 and the AD680, a low power 2.5 V band gap reference. R2 and R3 set up the required gain of 1.8 to develop the 4.5 V output. R1 and C2 form a low-pass RC filter to reduce the noise contribution of the AD680.

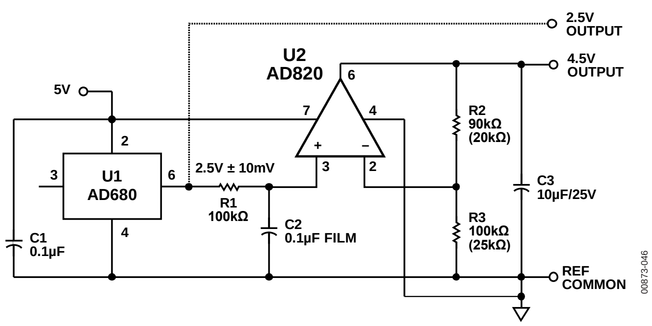


Figure 44. Single Supply 4.5 V Low Dropout Reference

With a 1 mA load, this reference maintains the 4.5 V output with a supply voltage down to 4.7 V. The amplitude of the recovery transient for a 1 mA to 10 mA step change in load current is under 20 mV, and settles out in a few microseconds. Output voltage noise is less than 10 µV rms in a 25 kHz noise bandwidth.

LOW POWER, 3-POLE, SALLEN KEY LOW-PASS FILTER

The high input impedance of the AD820 makes it a good selection for active filters. High value resistors can be used to construct low frequency filters with capacitors much less than 1 µF. The AD820 picoamp level input currents contribute minimal dc errors.

Figure 45 shows an example of a 10 Hz three-pole Sallen Key filter. The high value used for R1 minimizes interaction with signal source resistance. Pole placement in this version of the filter minimizes the Q associated with the two-pole section of the filter. This eliminates any peaking of the noise contribution of Resistor R1, Resistor R2, and Resistor R3, thus minimizing the inherent output voltage noise of the filter.

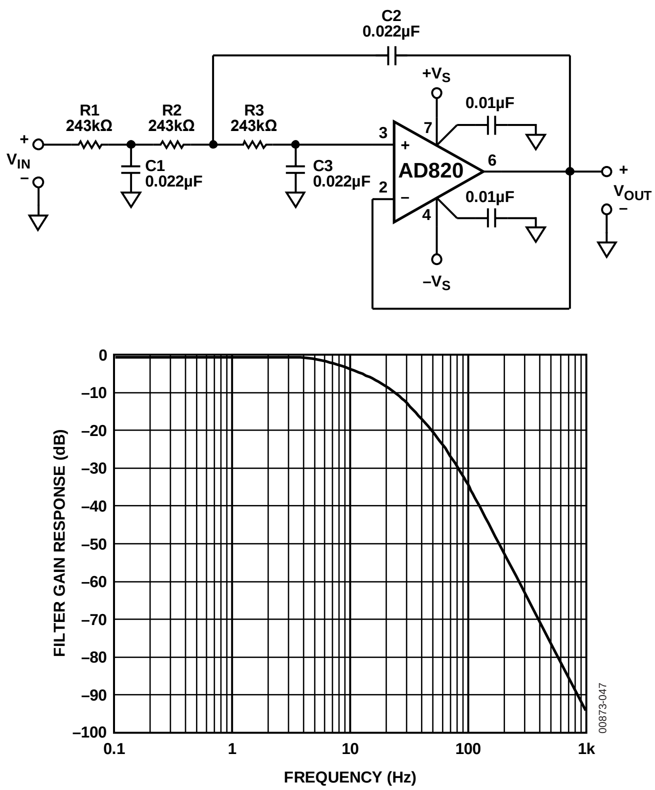


Figure 45. 10 Hz Sallen Key Low-Pass Filter

OFFSET VOLTAGE ADJUSTMENT

The offset voltage of the AD820 is low, so external offset voltage nulling is not usually required. Figure 46 shows the recommended technique for the AD820 packaged in plastic DIP. Adjusting offset voltage in this manner changes the offset voltage temperature drift by 4 μV/°C for every millivolt of induced offset. The null pins are not functional for the AD820 in the 8-lead SOIC and MSOP packages.

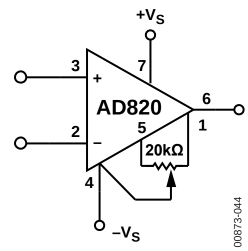
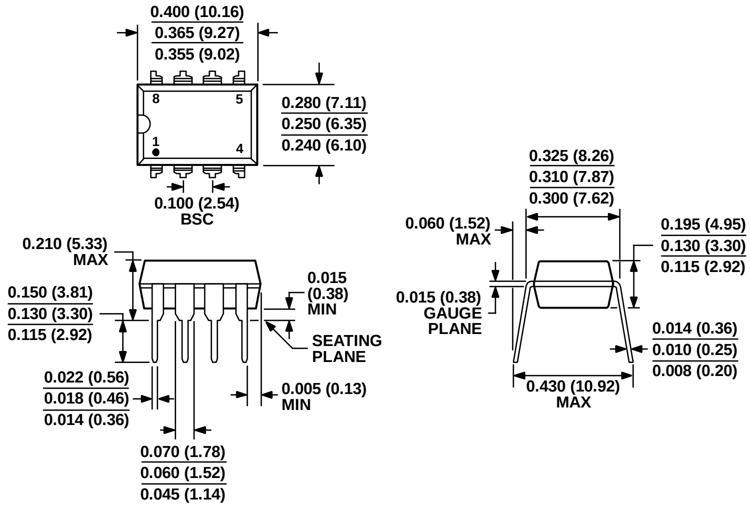


Figure 46. Offset Null

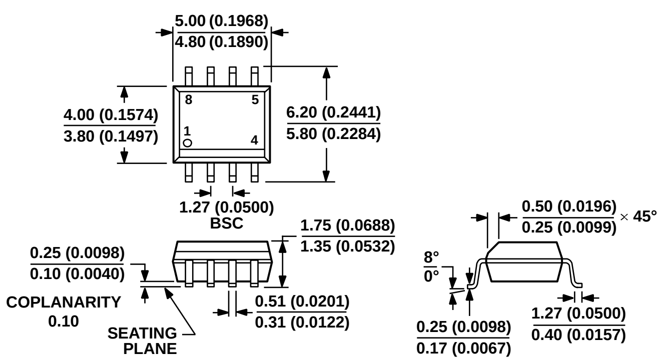
OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-001
CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.
CORNER LEADS MAY BE CONFIGURED AS WHOLE OR HALF LEADS.

070606-A

Figure 47. 8-Lead Plastic Dual In-Line Package [PDIP]
Narrow Body
(N-8)
Dimensions shown in inches and (millimeters)



COMPLIANT TO JEDEC STANDARDS MS-012-AA
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

012407-A

Figure 48. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-8)
Dimensions shown in millimeters and (inches)

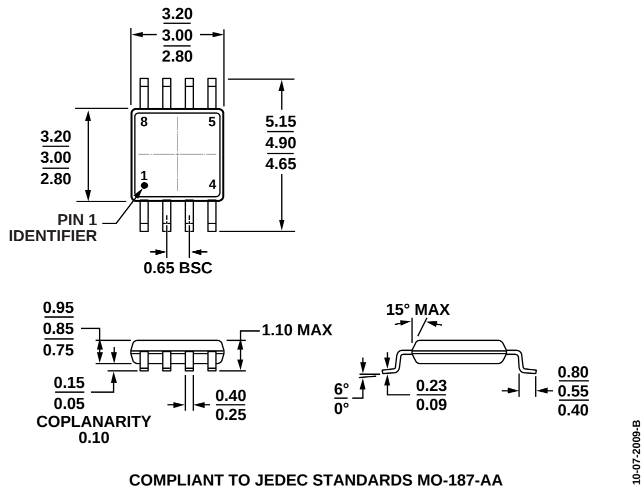


Figure 49. 8-Lead Mini Small Outline Package [MSOP]
(RM-8)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Branding
AD820AN	−40°C to +85°C	8-Lead PDIP	N-8	
AD820ANZ	−40°C to +85°C	8-Lead PDIP	N-8	
AD820AR	−40°C to +85°C	8-Lead SOIC_N	R-8	
AD820AR-REEL	−40°C to +85°C	8-Lead SOIC_N	R-8	
AD820AR-REEL7	−40°C to +85°C	8-Lead SOIC_N	R-8	
AD820ARZ	−40°C to +85°C	8-Lead SOIC_N	R-8	
AD820ARZ-REEL	−40°C to +85°C	8-Lead SOIC_N	R-8	
AD820ARZ-REEL7	−40°C to +85°C	8-Lead SOIC_N	R-8	
AD820ARMZ	−40°C to +85°C	8-Lead MSOP	RM-8	A2L
AD820ARMZ-RL	−40°C to +85°C	8-Lead MSOP	RM-8	A2L
AD820ARMZ-R7	−40°C to +85°C	8-Lead MSOP	RM-8	A2L
AD820BR	−40°C to +85°C	8-Lead SOIC_N	R-8	
AD820BR-REEL	−40°C to +85°C	8-Lead SOIC_N	R-8	
AD820BRZ	−40°C to +85°C	8-Lead SOIC_N	R-8	
AD820BRZ-REEL	−40°C to +85°C	8-Lead SOIC_N	R-8	
AD820BRZ-REEL7	−40°C to +85°C	8-Lead SOIC_N	R-8	

[1] Z = RoHS Compliant Part.

NOTES

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