MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Peak Power Dissipation (Note 1) @ T_L = 25°C, Pulse Width = 1 ms	P_{PK}	1500	W
DC Power Dissipation @ T_L = 75°C Measured Zero Lead Length (Note 2) Derate Above 75°C Thermal Resistance from Junction−to−Lead	P_D $R_{\theta JL}$	4.0 54.6 18.3	W mW/°C °C/W
DC Power Dissipation (Note 3) @ T_A = 25°C Derate Above 25°C Thermal Resistance from Junction−to−Ambient	P_D $R_{\theta JA}$	0.75 6.1 165	W mW/°C °C/W
Forward Surge Current (Note 4) @ T_A = 25°C	I_{FSM}	200	A
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to +150	°C

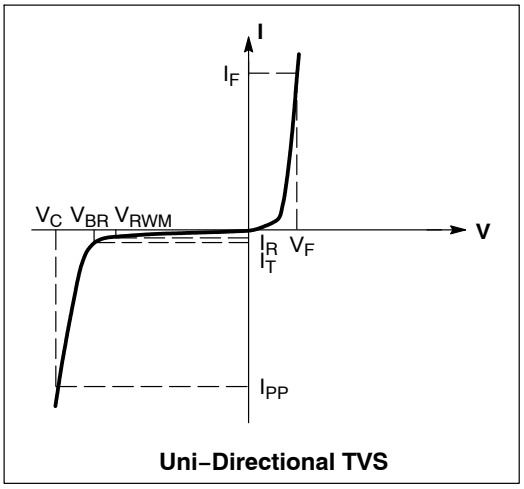
Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. 10 x 1000 μs, non−repetitive.
2. 1 in square copper pad, FR−4 board.
3. FR−4 board, using ON Semiconductor minimum recommended footprint, as shown in 403 case outline dimensions spec.
4. 1/2 sine wave (or equivalent square wave), PW = 8.3 ms, duty cycle = 4 pulses per minute maximum.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted, V_F = 3.5 V Max @ I_F = 100 A) (Note 5)

Symbol	Parameter
I_{PP}	Maximum Reverse Peak Pulse Current
V_C	Clamping Voltage @ I_{PP}
V_{RWM}	Working Peak Reverse Voltage
I_R	Maximum Reverse Leakage Current @ V_{RWM}
V_{BR}	Breakdown Voltage @ I_T
I_T	Test Current
I_F	Forward Current
V_F	Forward Voltage @ I_F

5. 1/2 sine wave or equivalent, PW = 8.3 ms non−repetitive duty cycle



Uni−Directional TVS

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Device*	Device Marking	V_{RWM} (Note 6)	I_R @ V_{RWM}	Breakdown Voltage				V_C @ I_{PP} (Note 8)	
				V_{BR} V (Note 7)			@ I_T	V_C	I_{PP}
		V	μA	Min	Nom	Max	mA	V	A
1SMC5.0AT3G	GDE	5.0	1000	6.4	6.7	7.0	10	9.2	163
1SMC6.0AT3G	GDG	6.0	1000	6.67	7.02	7.37	10	10.3	145.6
1SMC6.5AT3G	GDK	6.5	500	7.22	7.6	7.98	10	11.2	133.9
1SMC7.5AT3G	GDP	7.5	100	8.33	8.77	9.21	1	12.9	116.3
1SMC8.0AT3G	GDR	8.0	50	8.89	9.36	9.83	1	13.6	110.3
1SMC9.0AT3G	GDV	9.0	10	10	10.55	11.1	1	15.4	97.4
1SMC10AT3G	GDX	10	5	11.1	11.7	12.3	1	17	88.2
1SMC12AT3G	GEE	12	5	13.3	14	14.7	1	19.9	75.3
1SMC13AT3G	GEG	13	5	14.4	15.15	15.9	1	21.5	69.7
1SMC14AT3G	GEK	14	5	15.6	16.4	17.2	1	23.2	64.7
1SMC15AT3G	GEM	15	5	16.7	17.6	18.5	1	24.4	61.5
1SMC16AT3G	GEP	16	5	17.8	18.75	19.7	1	26	57.7
1SMC17AT3G	GER	17	5	18.9	19.9	20.9	1	27.6	53.3
1SMC18AT3G	GET	18	5	20	21.05	22.1	1	29.2	51.4
1SMC20AT3G	GEV	20	5	22.2	23.35	24.5	1	32.4	46.3
1SMC22AT3G	GEX	22	5	24.4	25.65	26.9	1	35.5	42.2
1SMC24AT3G	GEZ	24	5	26.7	28.1	29.5	1	38.9	38.6
1SMC26AT3G	GFE	26	5	28.9	30.4	31.9	1	42.1	35.6
1SMC28AT3G	GFG	28	5	31.1	32.75	34.4	1	45.4	33
1SMC30AT3G	GFK	30	5	33.3	35.05	36.8	1	48.4	31
1SMC33AT3G	GFM	33	5	36.7	38.65	40.6	1	53.3	28.1
1SMC36AT3G	GFP	36	5	40	42.1	44.2	1	58.1	25.8
1SMC40AT3G	GFR	40	5	44.4	46.75	49.1	1	64.5	32.2
1SMC43AT3G	GFT	43	5	47.8	50.3	52.8	1	69.4	21.6
1SMC48AT3G	GFX	48	5	53.3	56.1	58.9	1	77.4	19.4
1SMC51AT3G	GFZ	51	5	56.7	59.7	62.7	1	82.4	18.2
1SMC54AT3G	GGE	54	5	60	63.15	66.3	1	87.1	17.2
1SMC58AT3G	GGG	58	5	64.4	67.8	71.2	1	93.6	16
1SMC60AT3G	GGK	60	5	66.7	70.2	73.7	1	96.8	15.5
1SMC64AT3G	GGM	64	5	71.1	74.85	78.6	1	103	14.6
1SMC70AT3G	GGP	70	5	77.8	81.9	86	1	113	13.3
1SMC75AT3G	GGR	75	5	83.3	87.7	92.1	1	121	12.4
1SMC78AT3G	GGT	78	5	86.7	91.25	95.8	1	126	11.4

6. A transient suppressor is normally selected according to the maximum working peak reverse voltage (V_{RWM}), which should be equal to or greater than the DC or continuous peak operating voltage level.
7. V_{BR} measured at pulse test current I_T at an ambient temperature of 25°C.
8. Surge current waveform per Figure 2 and derate per Figure 3 of the General Data − 1500 Watt at the beginning of this group.

*Include SZ-prefix devices where applicable.

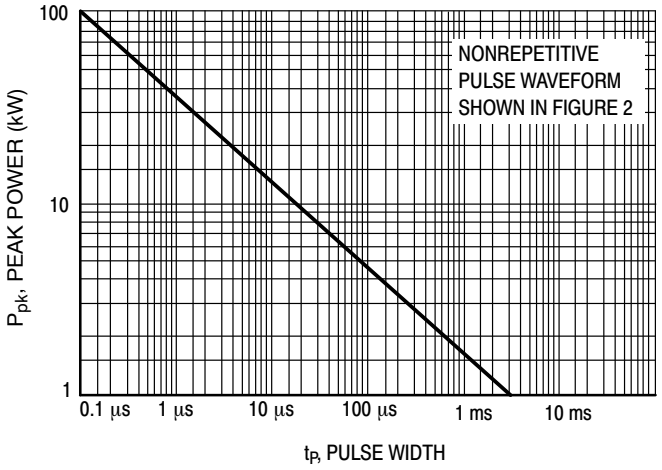


Figure 1. Pulse Rating Curve

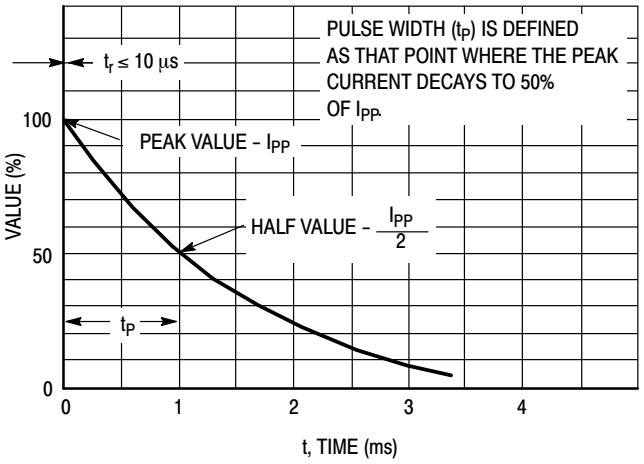


Figure 2. Pulse Waveform

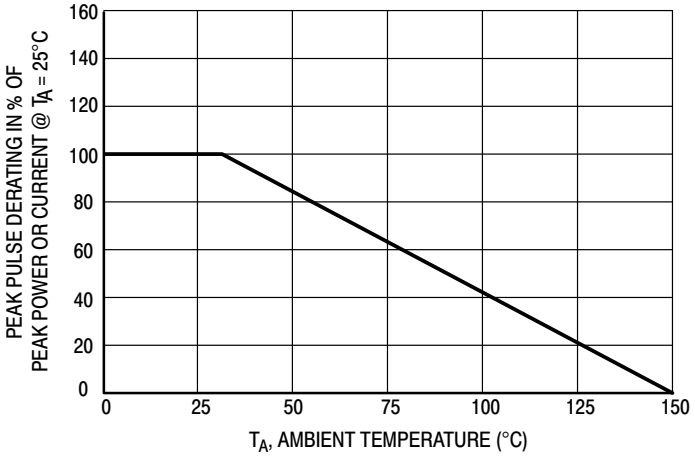


Figure 3. Pulse Derating Curve

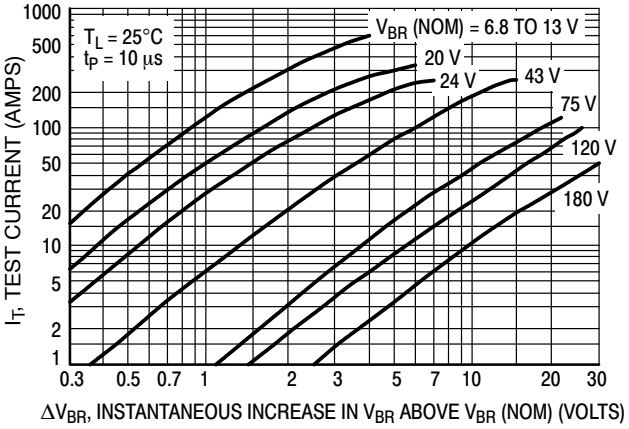


Figure 4. Dynamic Impedance

UL RECOGNITION

The entire series has *Underwriters Laboratory Recognition* for the classification of protectors (QVGQ2) under the UL standard for safety 497B and File #E210057. Many competitors only have one or two devices recognized or have recognition in a non-protective category. Some competitors have no recognition at all. With the UL497B recognition, our parts successfully passed several tests including Strike Voltage Breakdown test, Endurance Conditioning, Temperature test, Dielectric Voltage-Withstand test, Discharge test and several more.

Whereas, some competitors have only passed a flammability test for the package material, we have been recognized for much more to be included in their Protector category.

APPLICATION NOTES

Response Time

In most applications, the transient suppressor device is placed in parallel with the equipment or component to be protected. In this situation, there is a time delay associated with the capacitance of the device and an overshoot condition associated with the inductance of the device and the inductance of the connection method. The capacitive effect is of minor importance in the parallel protection scheme because it only produces a time delay in the transition from the operating voltage to the clamp voltage as shown in Figure 5.

The inductive effects in the device are due to actual turn-on time (time required for the device to go from zero current to full current) and lead inductance. This inductive effect produces an overshoot in the voltage across the equipment or component being protected as shown in Figure 6. Minimizing this overshoot is very important in the application, since the main purpose for adding a transient suppressor is to clamp voltage spikes. The SMC series have a very good response time, typically < 1 ns and negligible inductance. However, external inductive effects could produce unacceptable overshoot. Proper circuit layout, minimum lead lengths and placing the suppressor device as close as possible to the equipment or components to be protected will minimize this overshoot.

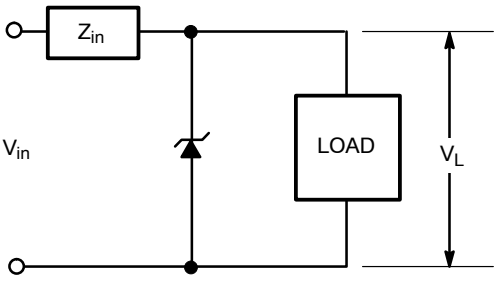
Some input impedance represented by Z_{in} is essential to prevent overstress of the protection device. This impedance should be as high as possible, without restricting the circuit operation.

Duty Cycle Derating

The data of Figure 1 applies for non-repetitive conditions and at a lead temperature of 25°C. If the duty cycle increases, the peak power must be reduced as indicated by the curves of Figure 7. Average power must be derated as the lead or ambient temperature rises above 25°C. The average power derating curve normally given on data sheets may be normalized and used for this purpose.

At first glance the derating curves of Figure 7 appear to be in error as the 10 ms pulse has a higher derating factor than the 10 μs pulse. However, when the derating factor for a given pulse of Figure 7 is multiplied by the peak power value of Figure 1 for the same pulse, the results follow the expected trend.

TYPICAL PROTECTION CIRCUIT



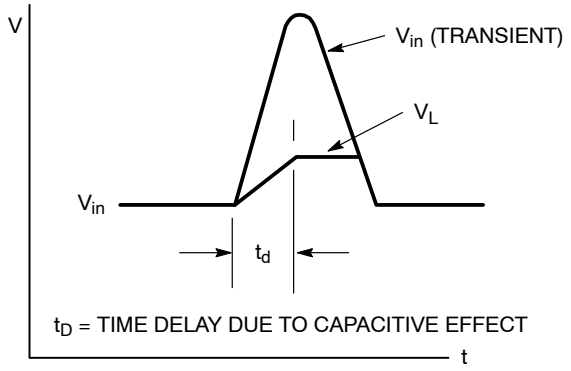


Figure 5.

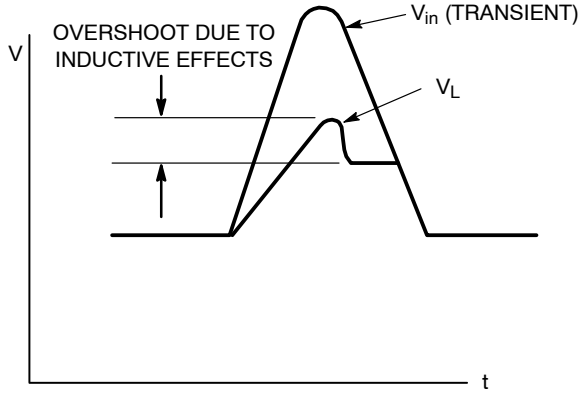


Figure 6.

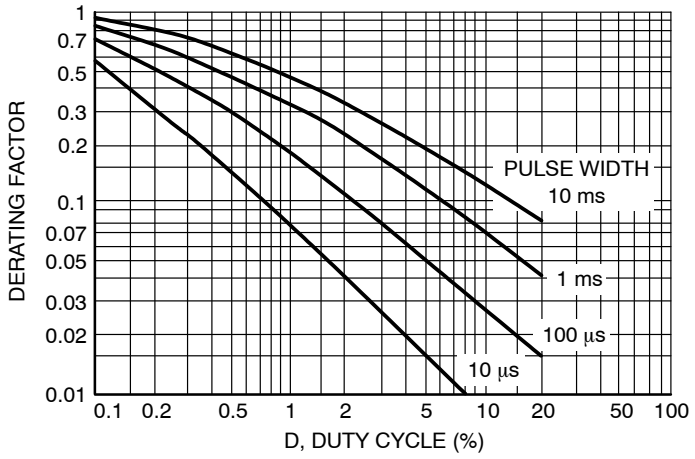
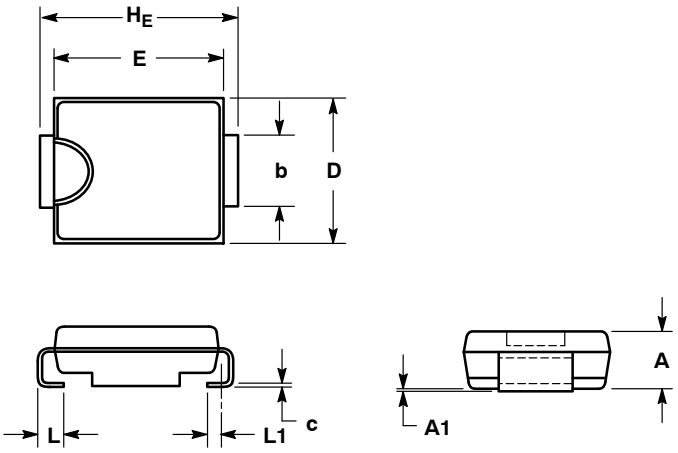


Figure 7. Typical Derating Factor for Duty Cycle

PACKAGE DIMENSIONS

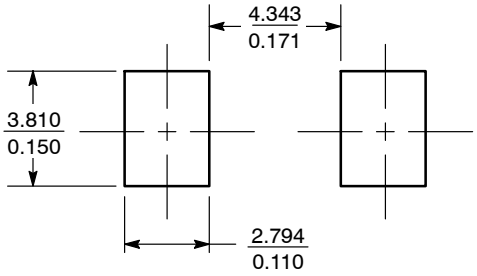
SMC
CASE 403−03
ISSUE E



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. D DIMENSION SHALL BE MEASURED WITHIN DIMENSION P.
4. 403−01 THRU −02 OBSOLETE, NEW STANDARD 403−03.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	1.90	2.13	2.41	0.075	0.084	0.095
A1	0.05	0.10	0.15	0.002	0.004	0.006
b	2.92	3.00	3.07	0.115	0.118	0.121
c	0.15	0.23	0.30	0.006	0.009	0.012
D	5.59	5.84	6.10	0.220	0.230	0.240
E	6.60	6.86	7.11	0.260	0.270	0.280
H_E	7.75	7.94	8.13	0.305	0.313	0.320
L	0.76	1.02	1.27	0.030	0.040	0.050
L1	0.51 REF			0.020 REF		

SOLDERING FOOTPRINT*



SCALE 4:1 $\left(\frac{\text{mm}}{\text{inches}}\right)$

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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