Absolute Maximum Ratings

Stresses beyond the limits listed below may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

PV_{IN}, V_{IN}....................-0.3V to 25V

V_{CC}....................-0.3V to 6.0V

BST....................-0.3V to 36V[1]

BST-SW....................-0.3V to 6V

SW, ILIM....................-1V to 30V[1, 2]

ALL other pins....................-0.3V to VCC+0.3V

Storage temperature....................-65°C to +150°C

Junction temperature....................150°C

Power dissipation....................Internally Limited

Lead temperature (soldering, 10 sec)....................260°C MSL3

ESD Rating (HBM - Human Body Model)....................2kV

ESD Rating (CDM - Charged Device Model)....................750V

Operating Conditions

PV_{IN}....................3V to 22V

V_{IN}....................4.5V to 22V

V_{CC}....................4.5V to 5.5V

SW, ILIM....................-1V to 22V[1]

PGOOD, V_{CC}, T_{ON}, SS, EN, FB....................-0.3V to 5.5V

Switching frequency....................400kHz to 800kHz[3]

Junction temperature range.................... -40°C to +125°C

JEDEC51 package thermal resistance, θ_{JA}.................... 18.1°C/W

Package power dissipation at 25°C....................5.5W

Note 1: No external voltage applied.

Note 2: The SW pin's minimum DC range is -1V, transient is -5V for less than 50ns, -7V for less than 20ns, and -9V for less than 10ns.

Note 3: Upper limit is a guideline based upon thermal performance.

Electrical Characteristics

Unless otherwise noted: T_J = 25°C, V_{IN} = 12V, BST = V_{CC}, SW = AGND = PGND = 0V, C_{VCC} = 4.7µF. Limits applying over the full operating temperature range are denoted by a "•"

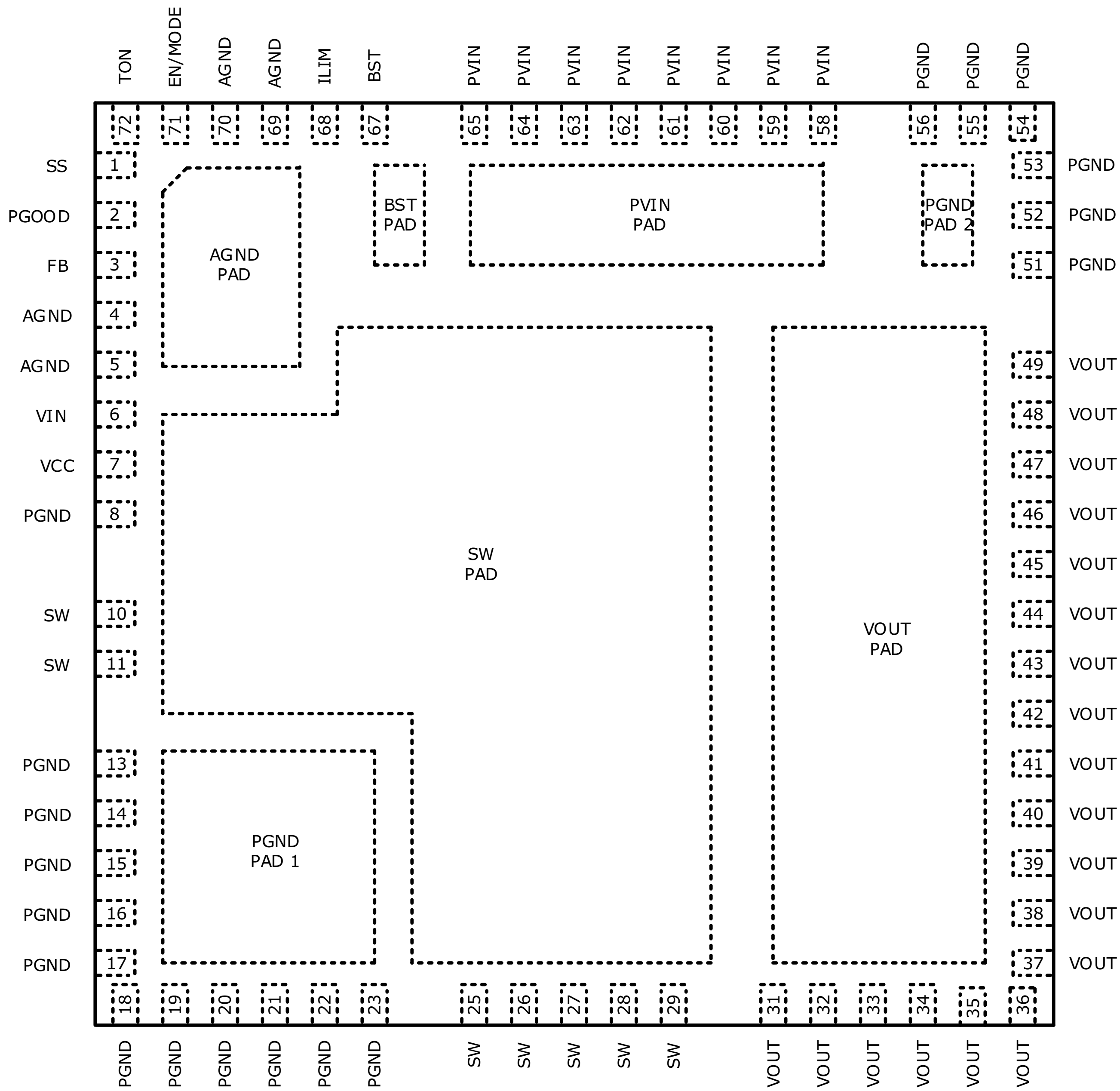
Symbol	Parameter	Conditions		Min	Typ	Max	Units
Power Supply Characteristics							
V_{IN}	Input voltage range	VCC regulating or in dropout	•	4.5		22	V
		VCC tied to VIN	•	4.5		5.5	
I_{VIN}	VIN input supply current	Not switching, V_{IN} = 12V, V_{FB} = 0.7V	•		0.7	2	mA
I_{VCC}	VCC quiescent current	Not switching, V_{CC} = V_{IN} = 5V, V_{FB} = 0.7V	•		0.7	2	mA
I_{VIN}	VIN input supply current	f = 500kHz, R_{ON} = 61.9kΩ, VFB = 0.58V			11		mA
I_{OFF}	Shutdown current	Enable = 0V, V_{IN} = 12V			1		µA
Enable and Under-Voltage Lock-Out UVLO							
V_{IH_EN}	EN pin rising threshold		•	1.8	1.9	2.0	V
V_{EN_HYS}	EN pin hysteresis				50		mV
V_{IH_EN}	EN pin rising threshold for DCM / CCM operation		•	2.8	3.0	3.1	V
V_{EN_HYS}	EN pin hysteresis				100		mV

Symbol	Parameter	Conditions		Min	Typ	Max	Units
	VCC UVLO start threshold, rising edge		•	4.00	4.25	4.40	V
	VCC UVLO hysteresis		•	150	200		mV
Reference Voltage							
V_{REF}	Reference voltage	V_{IN} = 5V to 22V, VCC regulating		0.597	0.600	0.603	V
		V_{IN} = 4.5V to 5.5V, VCC tied to VIN		0.596	0.600	0.604	V
		V_{IN} = 5V to 22V, VCC regulating V_{IN} = 4.5V to 5.5V, VCC tied to VIN	•	0.594	0.600	0.606	V
	DC line regulation	CCM, closed loop, V_{IN}=4.5V-22V, applies to any C_{OUT}			±0.10		%
	DC load regulation	CCM, closed loop, I_{OUT} = 0A - 15A, applies to any C_{OUT}			±0.35		%
Programmable Constant On-Time							
$T_{ON(MIN)}$	Minimum programmable on-time	R_{ON} = 6.98kΩ, V_{IN} = 22V			120		ns
T_{ON2}	On-time 2	R_{ON} = 6.98kΩ, V_{IN} = 12V	•	148	184	220	ns
	f corresponding to on-time 2	V_{OUT} = 1.0V		468	560	695	kHz
T_{ON3}	On-time 3	R_{ON} = 16.2kΩ, V_{IN} = 12V	•	319	390	461	ns
	Minimum off-time		•		250	350	ns
Diode Emulation Mode							
	Zero crossing threshold	DC value measured during test			-2		mV
Soft-start							
	SS charge current		•	-14	-10	-6	µA
	SS discharge current	Fault present	•	1			mA
VCC Linear Regulator							
	VCC output voltage	V_{IN} = 6V to 22V, I_{LOAD} = 0 to 30mA	•	4.8	5.0	5.2	V
		V_{IN} = 4.5V, R_{ON} = 16.2kΩ, f = 670kHz	•	4.3	4.37		V
Power Good Output							
	Power Good threshold			-10	-7.5	-5	%
	Power Good hysteresis				2	4	%
	Power Good sink current			1			mA
Protection: OCP, OTP, Short-Circuit							
	Hiccup timeout				110		ms
	ILIM pin source current			45	50	55	µA
	ILIM current temperature coefficient				0.4		%/°C
	OCP comparator offset		•	-8	0	+8	mV

Symbol	Parameter	Conditions		Min	Typ	Max	Units
	Current limit blanking	GL rising > 1V			100		ns
	Thermal shutdown threshold[1]	Rising temperature			150		°C
	Thermal hysteresis[1]				15		°C
	VSCTH feedback pin short-circuit threshold	Percent of V_{REF}, short circuit is active after PGOOD is asserted	•	50	60	70	%
Output Power Stage							
R_{DSON}	High-side MOSFET R_{DSON}	I_{DS} = 2A, V_{GS} = 4.5V			8.2	10	mΩ
	Low-side MOSFET R_{DSON}				7.8	10	mΩ
I_{OUT}	Maximum output current		•	10			A
L	Output inductance			0.64	0.80	0.96	uH
C_{IN}	Input capacitance				1		uF
C_{OUT}	Output capacitance				2.2		uF
C_{BST}	Bootstrap capacitance				0.1		uF

Note 1: Guaranteed by design

Pin Configuration, Top View

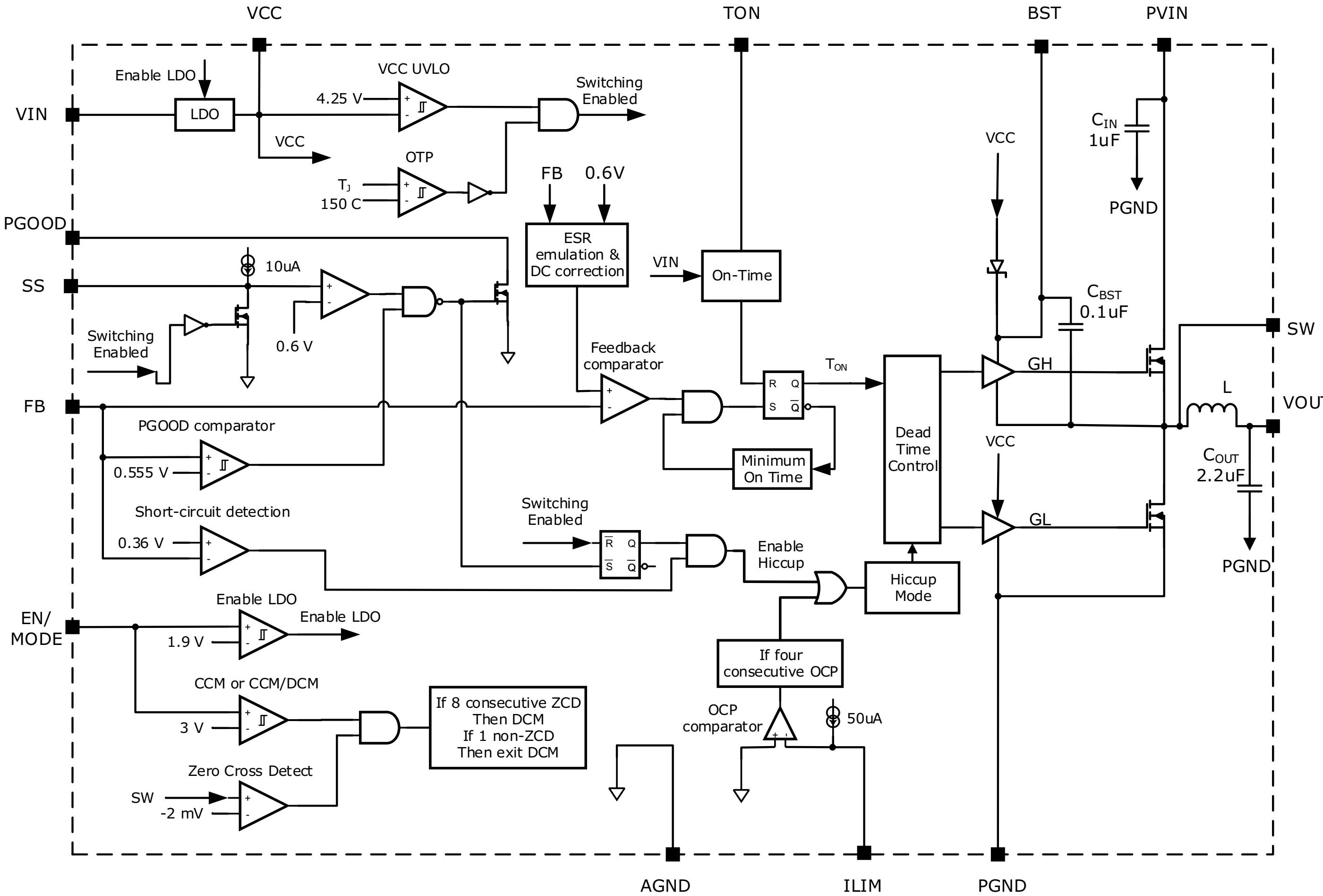


Pin Assignments

Pin No.	Pin Name	Type	Description
1	SS	A	Soft-start pin. Connect an external capacitor between SS and AGND to program the soft-start rate based on the 10μA internal source current.
2	PGOOD	OD, O	Power-good output. This open-drain output is pulled low when V_{OUT} is outside the regulation.
3	FB	A	Feedback input to feedback comparator. Connect with a set of resistors to VOUT and AGND in order to program VOUT.
4, 5, 69, 70, AGND Pad	AGND	A	Analog ground. Control circuitry of the IC is referenced to this pin.
6	VIN	PWR	IC supply input. Provides power to internal LDO.
7	VCC	PWR	The output of LDO. Bypass with a 4.7μF capacitor to AGND. For operation from a $5V_{IN}$ rail, VCC should be tied to VIN.
8	PGND	PWR	Controller low-side driver ground. Connect with a short trace to the closest PGND pins or PGND pad.
13-23, 51-56, PGND pads	PGND	PWR	Ground of the power stage. Should be connected to the system's power ground plane.
10-11, 25-29, SW Pad	SW	PWR	Switching node. It is internally connected. Use thermal vias and / or sufficient PCB land area in order to heatsink the low-side FET and the inductor. Note: If the spike voltage approaches the limit in Absolute Maximum Ratings, then use an optional snubber as shown in the Application Circuit (page 15).
31-49, VOUT Pad	VOUT	PWR	Output of the power stage. Place the output filter capacitors as close as possible to these pins.
58-65, PVIN Pad	PVIN	PWR	Power stage input voltage. Place the input filter capacitors as close as possible to these pins.
67, BST Pad	BST	A	Controller high-side driver supply pin. It is internally connected to SW via a 0.1μF bootstrap capacitor. Leave these pins floating.
68	ILIM	A	Over-current protection programming. Connect with a short trace to the SW pins.
71	EN/MODE	I	Precision enable pin. Pulling this pin above 1.9V will turn the IC on and it will operate in Forced CCM. If the voltage is raised above 3.0V, then the IC will operate in DCM or CCM depending on load.
72	TON	A	Constant on-time programming pin. Connect with a resistor to AGND.
9, 12, 24, 30, 50, 57, 66			Omitted pins.

Type: A = Analog, I = Input, O = Output, I/O = Input/Output, PWR = Power, OD = Open-Drain

Functional Block Diagram



Typical Performance Characteristics

Unless otherwise noted: V_{IN} = 12V, V_{OUT} = 1.2V, I_{OUT} = 10A, f = 500kHz, T_A = 25°C. The schematic is from the application information section.

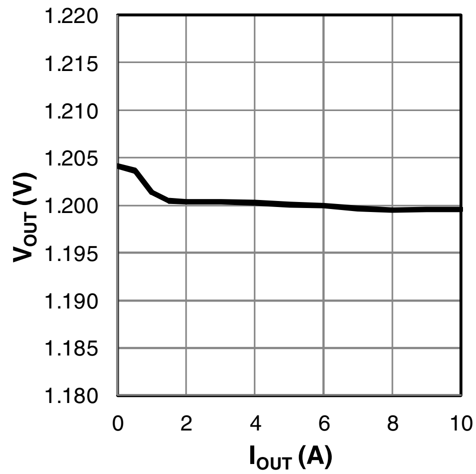


Figure 1: Load Regulation

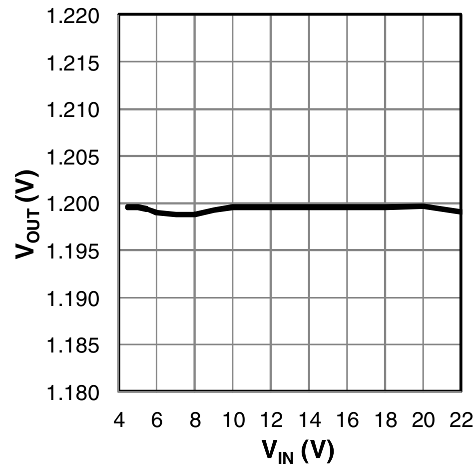


Figure 2: Line regulation

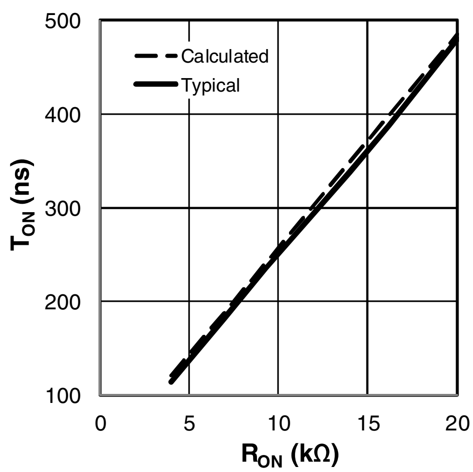


Figure 3: T_{ON} versus R_{ON}

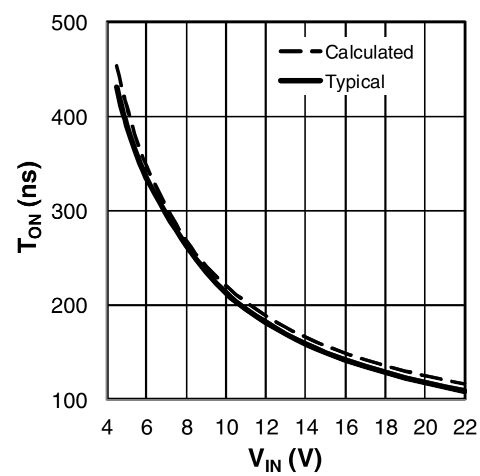


Figure 4: T_{ON} versus V_{IN}, R_{ON}=6.98k

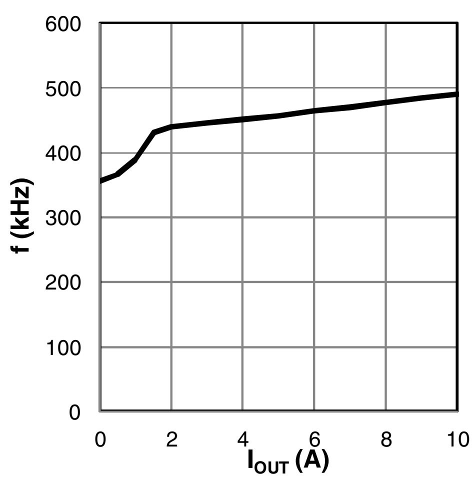


Figure 5: frequency versus I_{OUT}

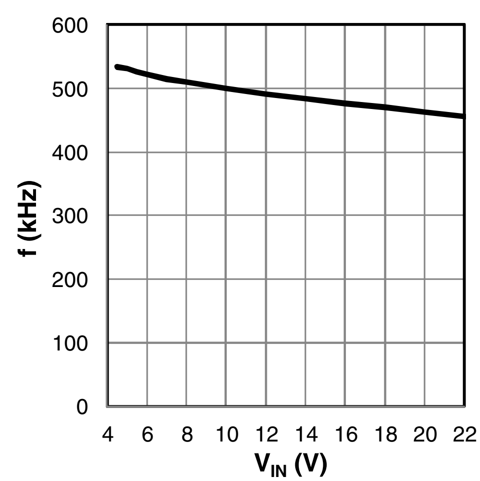


Figure 6: frequency versus V_{IN}

Typical Performance Characteristics

Unless otherwise noted: V_{IN} = 12V, V_{OUT} = 1.2V, I_{OUT} = 10A, f = 500kHz, T_A = 25°C. The schematic is from the application information section.

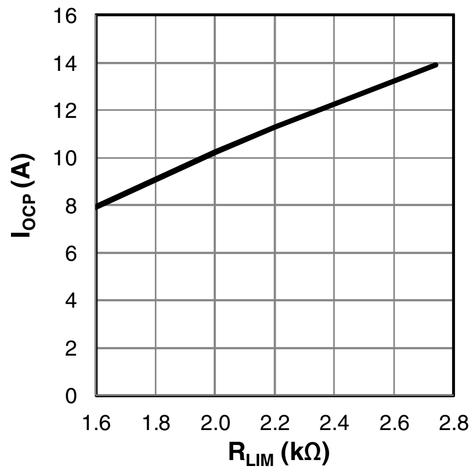


Figure 7: I_{OCP} versus R_{LIM}

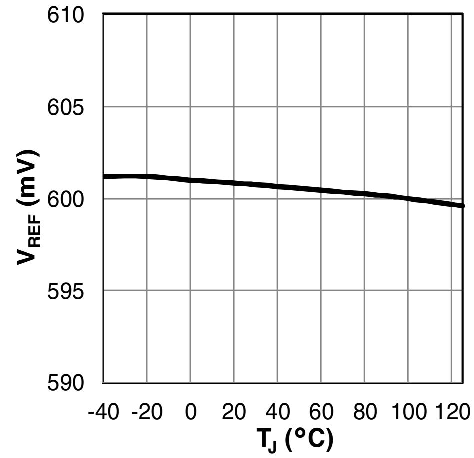


Figure 8: V_{REF} versus temperature

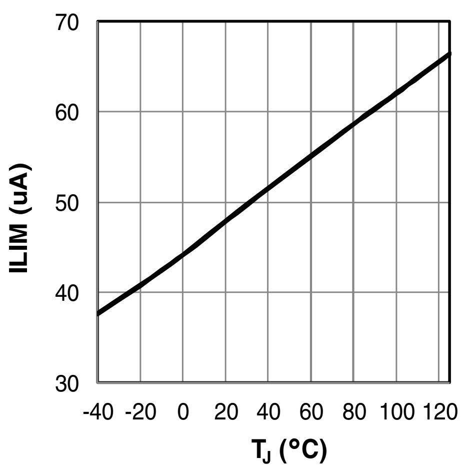


Figure 9: I_{LIM} versus temperature

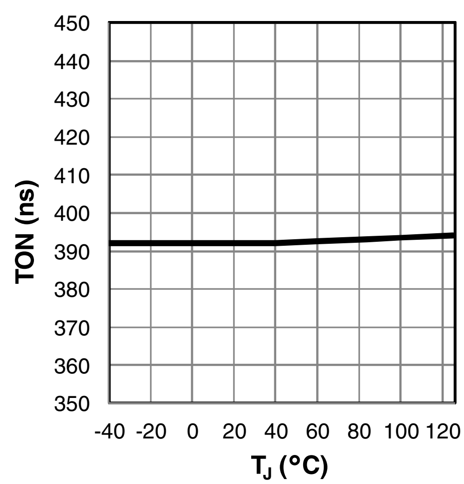


Figure 10: T_{ON} versus temperature, R_{ON}=16.2kΩ

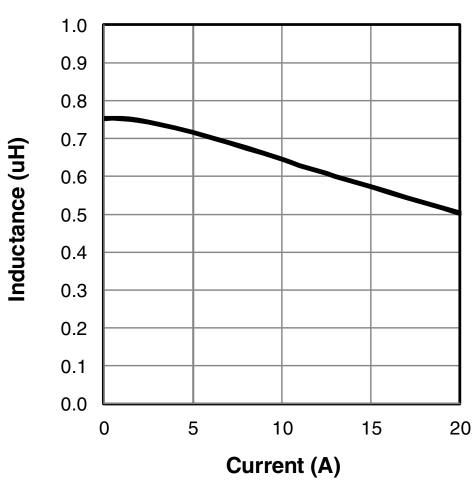


Figure 11: Inductance versus Current

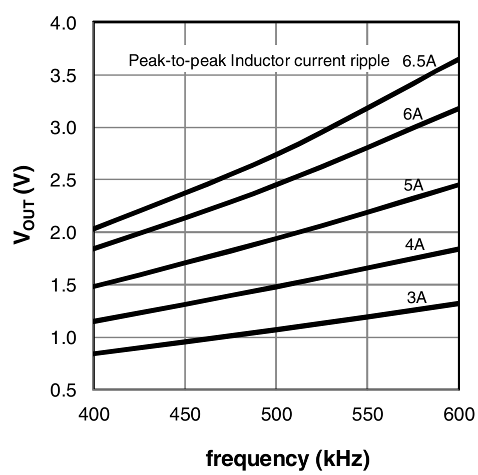


Figure 12: V_{OUT} versus f, V_{IN}=12V

Typical Performance Characteristics

Unless otherwise noted: V_{IN} = 12V, V_{OUT} = 1.2V, I_{OUT} = 10A, f = 500kHz, T_A = 25°C. The schematic is from the application information section.

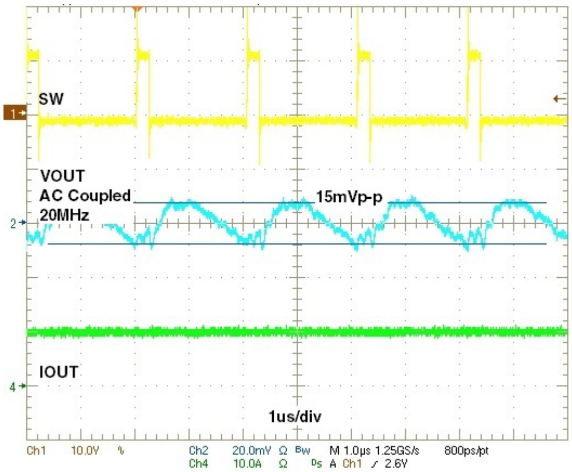


Figure 13: Steady state, CCM, I_{OUT}=10A

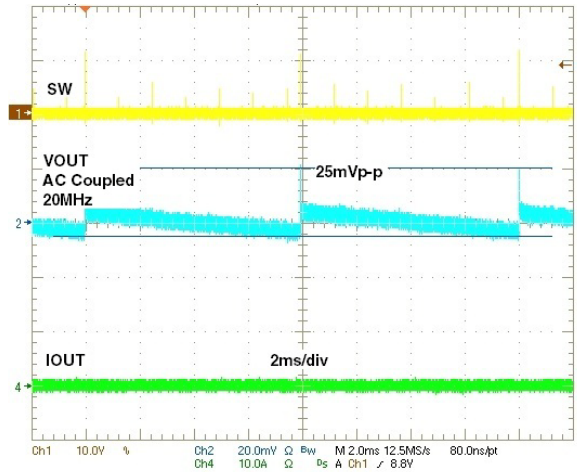


Figure 14: Steady state, DCM, I_{OUT}=0A

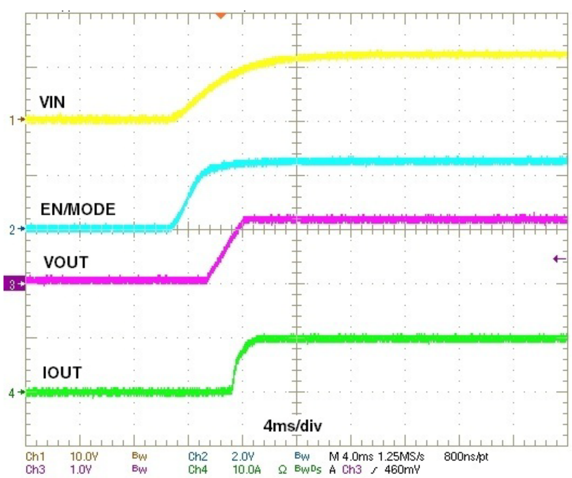


Figure 15: Power up, Forced CCM

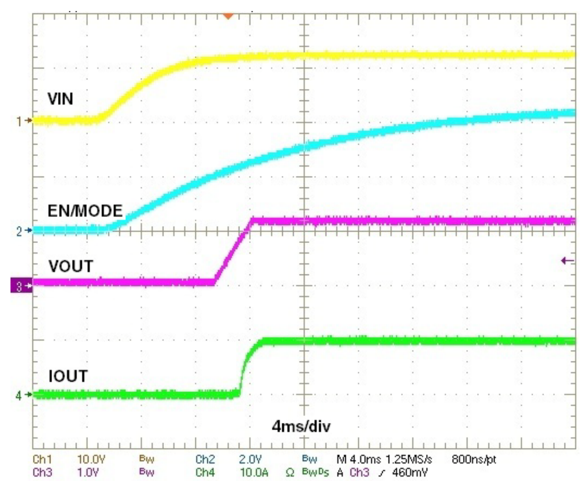


Figure 16: Power up, DCM/CCM

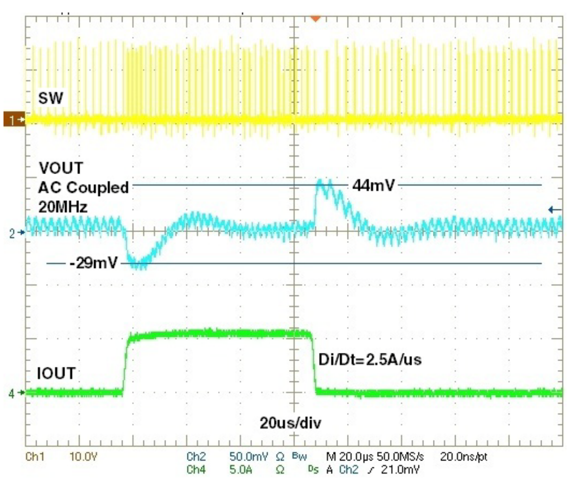


Figure 17: Load step, Forced CCM, 0A-5A-0A

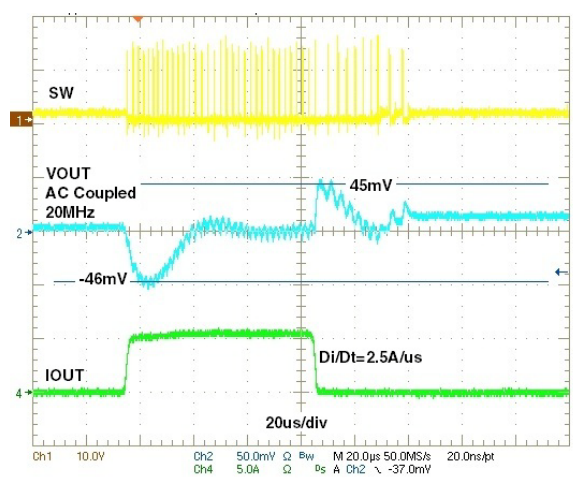


Figure 18: Load step, DCM/CCM, 0A-5A-0A

Efficiency and Package Thermal Derating

Unless otherwise noted: $T_{AMBIENT}$ = 25°C, no air flow, f = 500kHz, the schematic is from the application information section.

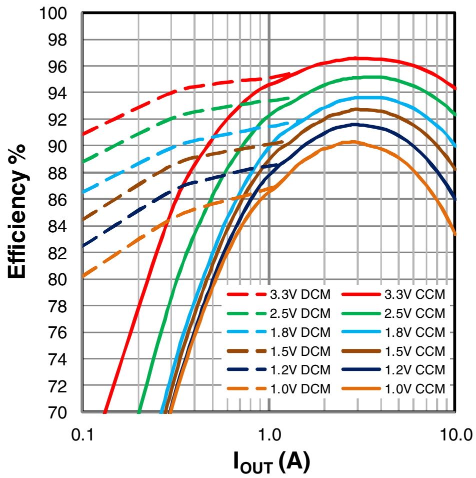


Figure 19: Efficiency, V_{IN}=5V

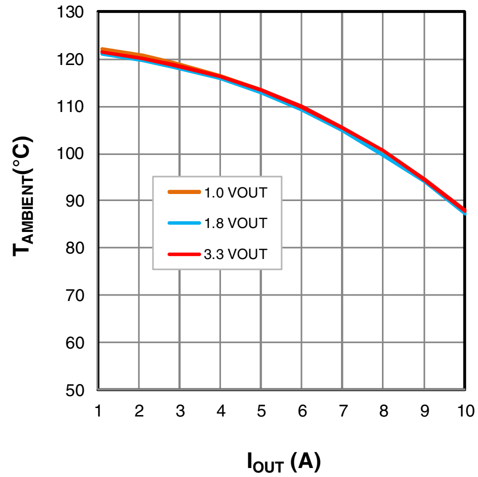


Figure 20: Maximum $T_{AMBIENT}$ vs I_{OUT}, V_{IN}=5V

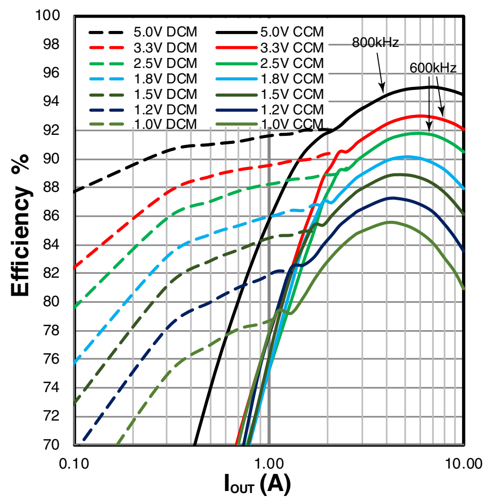


Figure 21: Efficiency, V_{IN}=12V

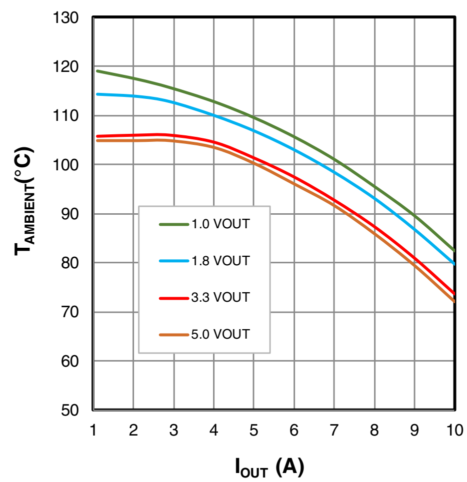


Figure 22: Maximum $T_{AMBIENT}$ vs I_{OUT}, V_{IN}=12V

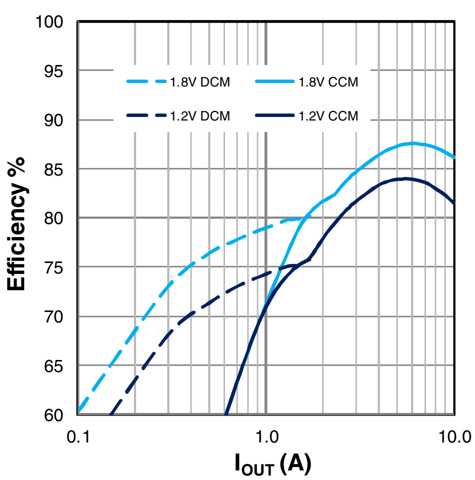


Figure 23: Efficiency, V_{IN}=19.6V

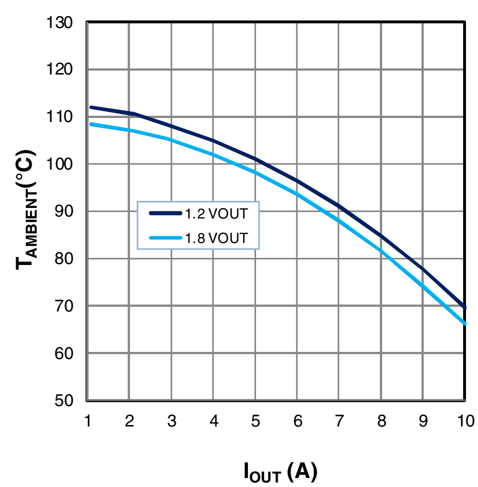


Figure 24: Maximum $T_{AMBIENT}$ vs I_{OUT}, V_{IN}=19.6V

Functional Description

XR79110 is a synchronous step-down, proprietary emulated current-mode Constant On-Time (COT) Module. The on-time, which is programmed via R_{ON}, is inversely proportional to V_{IN} and maintains a nearly constant frequency. The emulated current-mode control is stable with ceramic output capacitors.

Each switching cycle begins with the GH signal turning on the high-side (switching) FET for a preprogrammed time. At the end of the on-time, the high-side FET is turned off and the low-side (synchronous) FET is turned on for a preset minimum time (250ns nominal). This parameter is termed Minimum Off-Time. After the Minimum Off-Time, the voltage at the feedback pin FB is compared to an internal voltage ramp at the feedback comparator. When V_{FB} drops below the ramp voltage, the high-side FET is turned on and the cycle repeats. This voltage ramp constitutes an emulated current ramp and makes possible the use of ceramic capacitors, in addition to other capacitor types, for output filtering.

Enable / Mode Input (EN/MODE)

The EN/MODE pin accepts a tri-level signal that is used to control turn on and turn off. It also selects between two modes of operation: 'Forced CCM' and 'DCM / CCM'. If EN/MODE is pulled below 1.8V, the module shuts down. A voltage between 2.0V and 2.8V selects the Forced CCM mode, which will run the module in continuous conduction at all times. A voltage higher than 3.1V selects the DCM / CCM mode, which will run the module in discontinuous conduction at light loads.

Selecting the Forced CCM Mode

In order to set the module to operate in Forced CCM, a voltage between 2.0V and 2.8V must be applied to EN/MODE. This can be achieved with an external control signal that meets the above voltage requirement. Where an external control is not available, the EN/MODE can be derived from V_{IN}. If V_{IN} is well regulated, use a resistor divider and set the voltage to 2.5V. If V_{IN} varies over a wide range, the circuit shown in Figure 25 can be used to generate the required voltage. Note that at V_{IN} of 5V and 22V, the nominal Zener voltage is 3.8V and 4.7V, respectively. Therefore for V_{IN} in the range of 5V to 22V, the circuit shown in Figure 25 will generate the V_{EN} required for Forced CCM.

Selecting the DCM / CCM Mode

In order to set the module operation to DCM / CCM, a voltage between 3.1V and 5.5V must be applied to the EN/MODE pin. If an external control signal is available, it can be directly connected to EN/MODE. In applications where an external control is not available, the EN/MODE input can be derived from V_{IN}. If V_{IN} is well regulated, use a resistor divider and set the voltage to 4V. If V_{IN} varies over a wide range, the circuit shown in Figure 26 can be used to generate the required voltage.

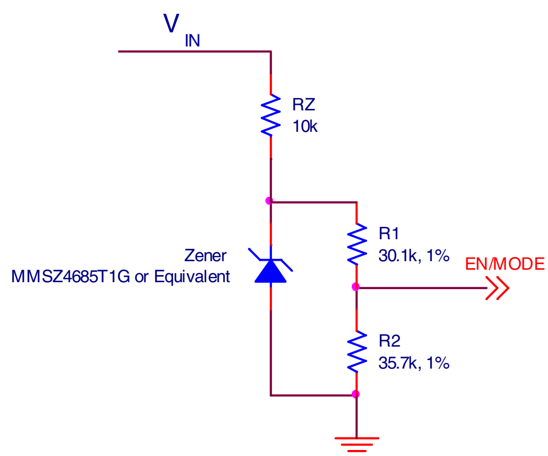


Figure 25: Selecting Forced CCM by deriving EN/MODE from V_{IN}

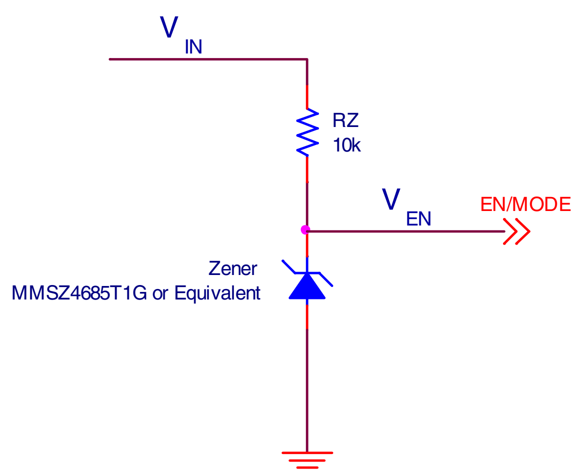


Figure 26: Selecting DCM/CCM by deriving EN/MODE from V_{IN}

Programming the On-Time

The On-time T_{ON} is programmed via resistor R_{ON} according to following equation:

$$R_{ON} = \frac{V_{IN} \times [T_{ON} - (25 \times 10^{-9})]}{2.7 \times 10^{-10}}$$

where T_{ON} is calculated from:

$$T_{ON} = \frac{V_{OUT}}{V_{IN} \times f \times Eff}$$

Where:

f is the desired switching frequency at nominal I_{OUT}

Eff is the module efficiency corresponding to nominal I_{OUT} shown in Figures 19, 21, 23

Substituting for T_{ON} in the first equation we get:

$$R_{ON} = \frac{\left(\frac{V_{OUT}}{f \times Eff}\right) - [(25 \times 10^{-9}) \times V_{IN}]}{2.7 \times 10^{-10}}$$

Over-Current Protection (OCP)

If load current exceeds the programmed over-current, I_{OCP}, for four consecutive switching cycles, then Module enters hiccup mode of operation. In hiccup, the MOSFET gates are turned off for 110ms (hiccup timeout). Following the hiccup timeout, a soft-start is attempted. If OCP persists, hiccup timeout will repeat. The Module will remain in hiccup mode until load current is reduced below the programmed I_{OCP} . In order to program the over-current protection, use the following equation:

$$RLIM = \frac{(I_{OCP} \times RDS) + 8mV}{ILIM}$$

Where:

RLIM is resistor value for programming I_{OCP}

I_{OCP} is the over-current threshold to be programmed

RDS is the MOSFET rated on resistance (10mΩ)

8mV is the OCP comparator maximum offset

ILIM is the internal current that generates the necessary OCP comparator threshold (use 45µA).

Note that ILIM has a positive temperature coefficient of 0.4%/°C (Figure 9). This is meant to roughly match and compensate for the positive temperature coefficient of the synchronous FET. A graph of typical I_{OCP} versus RLIM is shown in Figure 7.

Short-Circuit Protection (SCP)

If the output voltage drops below 60% of its programmed value, the module will enter Hiccup Mode. Hiccup will persist until the short-circuit is removed. The SCP circuit becomes active after PGOOD asserts high.

Over-Temperature (OTP)

OTP triggers at a nominal die temperature of 150°C. The gates of the switching FET and synchronous FET are turned off. When die temperature cools down to 135°C, soft-start is initiated and operation resumes.

Programming the Output Voltage

Use an external voltage divider as shown in the Application Circuit to program the output voltage V_{OUT}.

$$R1 = R2 \times \left(\frac{V_{OUT}}{0.6} - 1\right)$$

where R2 has a nominal value of 2kΩ.

Programming the Soft-Start

Place a capacitor CSS between the SS and AGND pins to program the soft-start. In order to program a soft-start time of TSS, calculate the required capacitance CSS from the following equation:

$$CSS = TSS \times \left(\frac{10\mu A}{0.6V}\right)$$

Feed-Forward Capacitor (C_{FF})

A feed-forward capacitor (C_{FF}) may be necessary, depending on the Equivalent Series Resistance (ESR) of C_{OUT}. If only ceramic output capacitors are used for C_{OUT}, then a C_{FF} is necessary. Calculate C_{FF} from:

$$C_{FF} = \frac{1}{2 \times \pi \times 80kHz \times R1}$$

Where:

R1 is the resistor that C_{FF} is placed in parallel with

80kHz is the location of the Zero formed by R1 and C_{FF}

Note that the minimum required C_{OUT} is 90μF when using ceramic capacitors.

When using capacitors with higher ESR, such as the PANASONIC TPE series, a C_{FF} is not required provided following conditions are met:

1. The frequency of output filter LC double-pole f_{LC} should be less than 15kHz.

2. The frequency of ESR Zero $f_{Zero,ESR}$ should be at least three times larger than f_{LC}.

As an example, the application circuit has f_{LC} = 8.3kHz and $f_{Zero,ESR}$ = 48kHz.

Maximum Allowable Voltage Ripple at FB pin

Note that the steady-state voltage ripple at feedback pin FB ($V_{FB,RIPPLE}$) must not exceed 50mV in order for the module to function correctly. If $V_{FB,RIPPLE}$ is larger than 50mV, then C_{OUT} should be increased as necessary in order to keep the $V_{FB,RIPPLE}$ below 50mV.

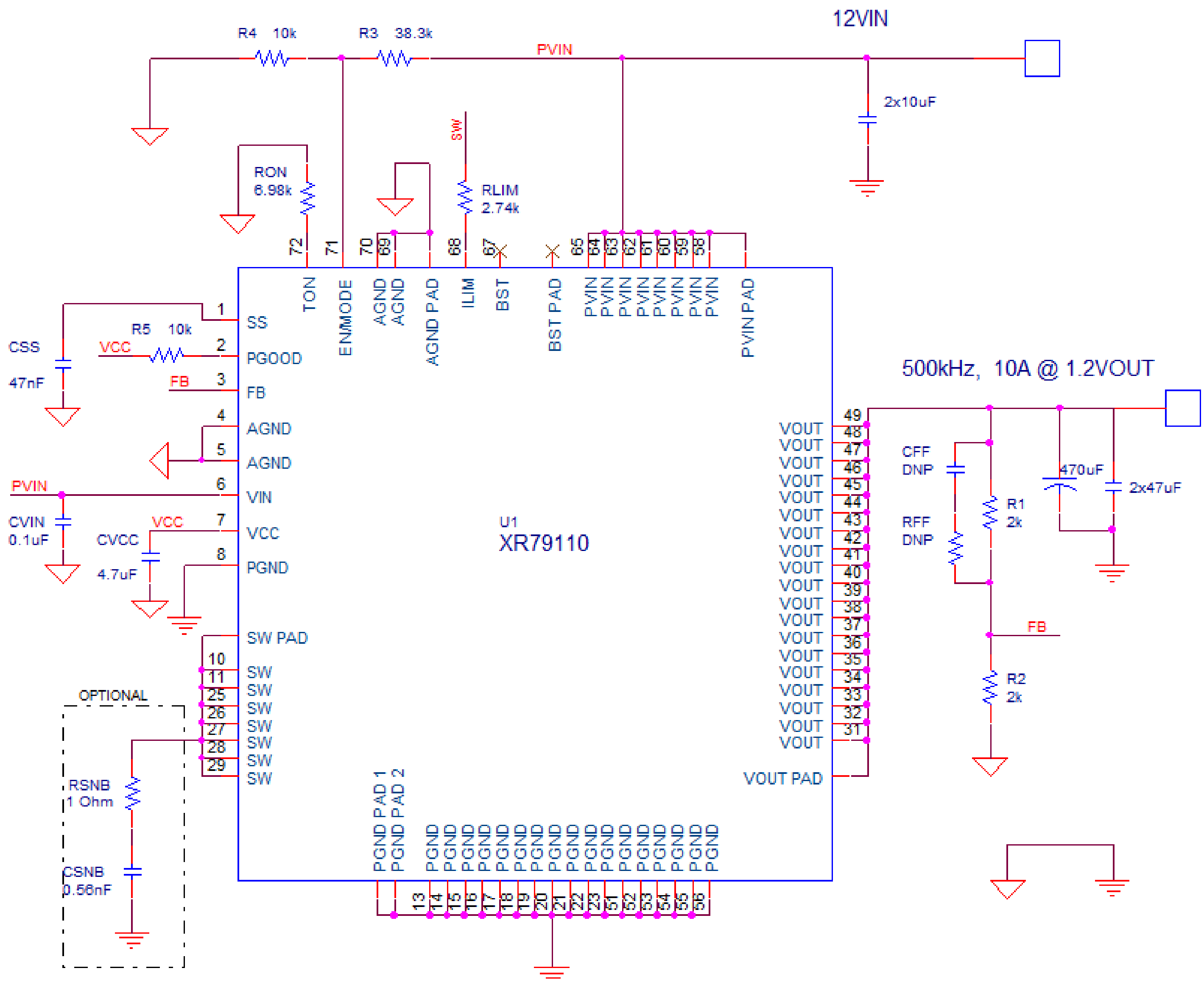
Feed-Forward Resistor (R_{FF})

Poor PCB layout can cause FET switching noise at the output that may couple to the FB pin via C_{FF}. Excessive noise at FB will cause poor load regulation. To solve this problem place a resistor R_{FF} in series with C_{FF}. An R_{FF} value of up to 2% of R1 is acceptable.

V_{OUT} versus Frequency Curves

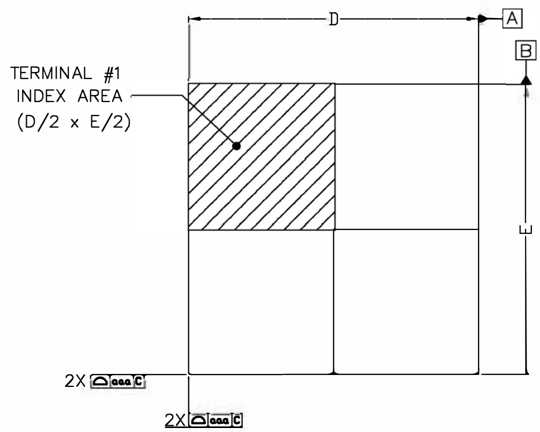
V_{OUT} versus switching frequency (f) curves corresponding to peak-to-peak inductor current ripple (ΔIL) are plotted in Figure 12. For a particular V_{IN}, V_{OUT} and f the magnitude of ΔIL can be determined from Figure 12. As an example, for V_{IN} = 12V, V_{OUT} = 1.5V and f = 400kHz, the ΔIL is 5A. Alternately for a given V_{IN}, V_{OUT} and ΔIL, the required switching frequency can be ascertained. For example, for V_{IN} = 12V, V_{OUT} = 1.5V and ΔIL = 4A, the required f is 500kHz.

Application Circuit

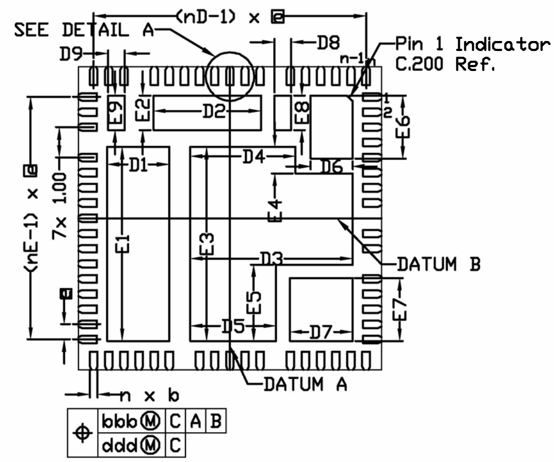


Note 1: Snubber circuit to be used when large transients on SW node.

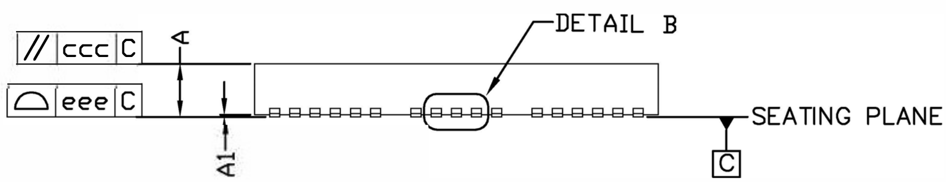
Mechanical Dimensions



TOP VIEW



BOTTOM VIEW

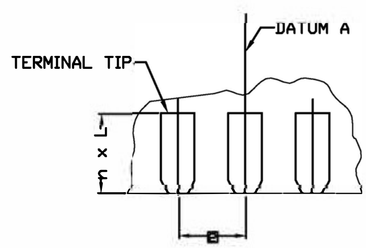


SIDE VIEW

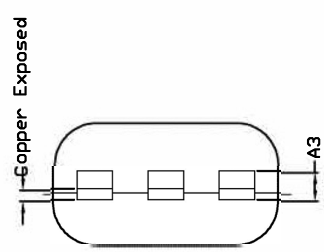
PACKAGE	65L 10x10 GQFNI-SIP		
REF.	MIN.	NOM.	MAX.
A	3.85	3.95	4.05
b	0.20	0.25	0.30
L	0.50	0.60	0.70
D	10.00 BSC		
D1	1.94	2.04	2.14
D2	3.45	3.55	3.65
D3	5.26	5.36	5.46
D4	3.38	3.48	3.58
D5	2.735	2.835	2.935
D6	1.28	1.38	1.48
D7	1.975	2.075	2.175
D8	0.45	0.55	0.65
D9	0.45	0.55	0.65
E	10.00 BSC		
E1	6.30	6.40	6.50
E2	1.05	1.15	1.25
E3	6.30	6.40	6.50
E4	0.78	0.88	0.98
E5	2.425	2.525	2.625
E6	1.98	2.08	2.18
E7	1.975	2.075	2.175
E8	1.05	1.15	1.25
E9	1.05	1.15	1.25
e	0.50 BSC		
n	65		
nD	17		
nE	16		

SYMBOL	COMMON DIMENSIONS			NOTE
	MIN.	NOM.	MAX.	
A1	0.010	-	0.070	
A3	0.152 REF.			
TOLERANCES OF FORM AND POSITION				
aaa	0.10			
bbb	0.10			
ccc	0.10			
ddd	0.05			
eee	0.08			

TERMINAL DETAILS



DETAIL A



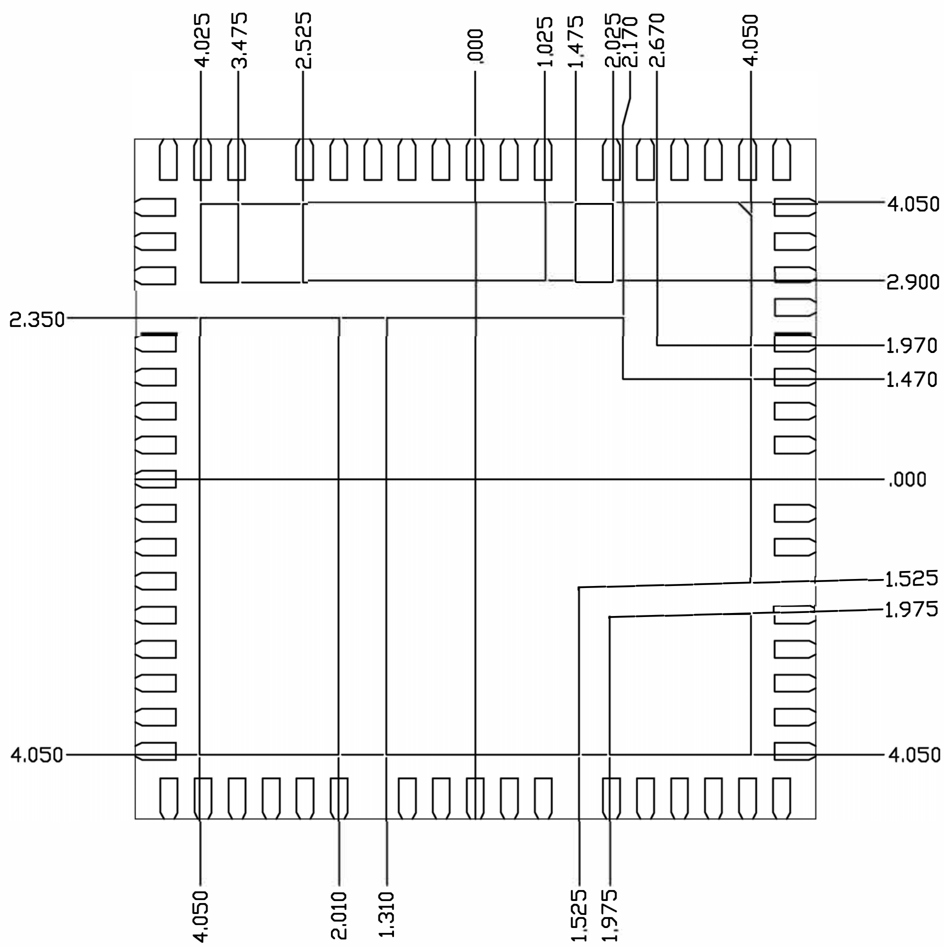
DETAIL B

NOTE : ALL DIMENSIONS ARE IN MILLIMETERS, ANGLES ARE IN DEGREES.

Drawing No.: POD-00000147

Revision: B

Terminal and Pad Edge Details



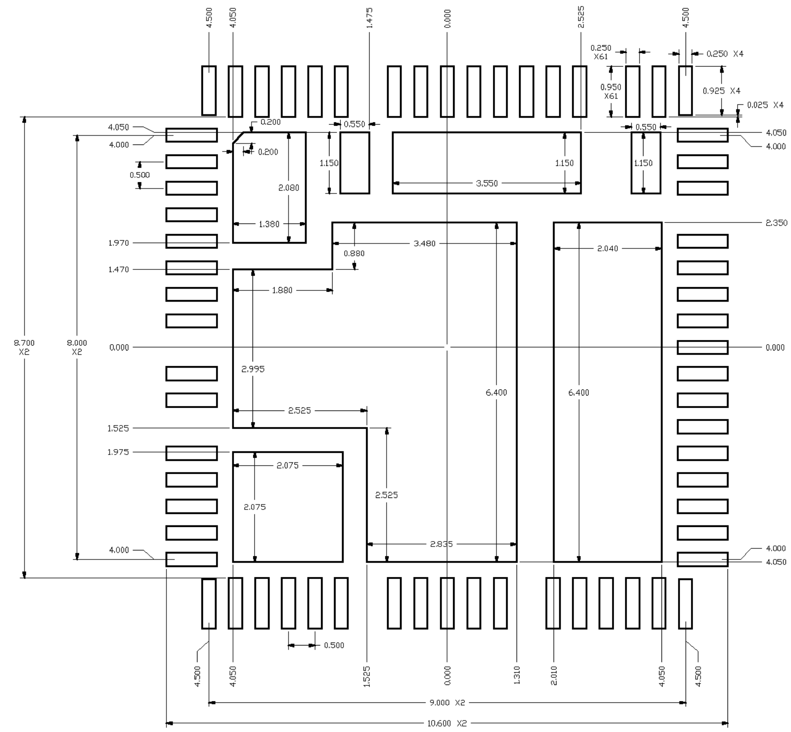
TERMINAL AND PAD EDGE DETAILS

NOTE : ALL DIMENSIONS ARE IN MILLIMETERS, ANGLES ARE IN DEGREES.

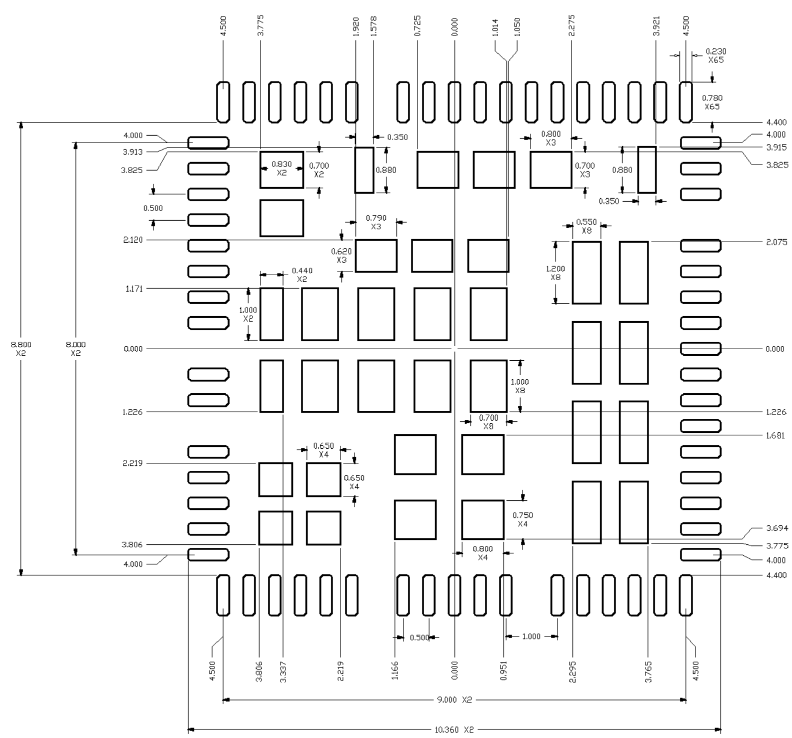
Drawing No.: POD-00000147

Revision: B

Recommended Land Pattern and Stencil



Typical Recommended Land Pattern



Typical Recommended Stencil

Ordering Information[1]

Part Number	Operating Temperature Range	Package	Packaging Method	Lead-Free
XR79110EL-F	-40°C ≤ T_J ≤ +125°C	10x10mm GQFN	Tray	Yes[2]
XR79110EVB	XR79110 Evaluation Board			

NOTE:

1. Refer to www.maxlinear.com/XR79110 for most up-to-date Ordering Information.
2. Visit www.maxlinear.com for additional information on Environmental Rating

Revision History

Revision	Date	Description
1A	December 2014	ECN 1451-08
1B	January 2015	Corrected schematic on page 1, ECN 1504-05
1C	June 2015	Added CFF/RFF to Application Circuit, updated figure 12, added writeup “maximum allowable ripple at FB pin” and “VOUT versus frequency curves”
2A	January 2016	Changed minimum VIN to 4.5V, Added CDM rating, changed VCC(MIN)=4.3V at VIN=4.5V, added VCC UVLO Hysteresis min=150mV across temperature, changed POD
2B	May 2017	Added more transient information to Note 2 under Absolute Maximum Ratings. Updated package drawing and ordering information format.
2C	January 2018	Updated to MaxLinear logo. Updated format and Ordering Information. Added $5V_{OUT}$ to Figures 21 and 22. Clarified operating temperature range in Ordering Information. Changed switching frequency upper limit to 800kHz.
2D	April 2019	Changed absolute max and pin description for SW pin. Updated Application Circuit, Mechanical Dimensions and Recommended Land Pattern and Stencil drawings.
2E	November 2019	Correct block diagram by changing the input gate that connects to the Hiccup Mode block from an AND gate to an OR gate.
3A	December 2019	Update POD’s Mechanical Dimensions and Recommended Land Pattern and Stencil. Update Pin Configuration, Pin Functions and Typical Application Circuit. Correct ESD rating for CDM model.

Corporate Headquarters:
5966 La Place Court
Suite 100
Carlsbad, CA 92008
Tel.:+1 (760) 692-0711
Fax: +1 (760) 444-8598
www.maxlinear.com