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Contents

1.0	Pin Assignments and Signal Descriptions	7
2.0	Functional Description.....	9
2.1	Introduction	9
2.2	Controller Compatibility Modes	9
2.3	Transmit Function	10
2.4	Jabber Control Function	10
2.5	SQE Function	11
2.6	Receive Function	12
2.7	Polarity Reverse Function.....	12
2.8	Collision Detection Function	13
2.9	Loopback Functions.....	14
2.9.1	Internal Loopback	14
2.9.2	External Loopback/Full Duplex	14
2.10	Link Integrity Test Function.....	14
3.0	Application Information	16
3.1	Introduction	16
3.1.1	Termination Circuitry.....	16
3.1.2	Twisted-Pair Interface	16
3.1.3	RBIAS Pin	16
3.1.4	Crystal Information.....	16
3.1.5	Magnetic Information	17
3.2	Typical 10BASE-T Application.....	17
3.3	Dual Network Support - 10BASE-T and Token Ring	18
3.4	Simple 10BASE-T Connection.....	20
4.0	Test Specifications	21
4.1	Timing Diagrams for Mode 1 (MD1 = Low, MD0 = Low)	24
4.2	Timing Diagrams for Mode 2 (MD1 = Low, MD0 = High).....	27
4.3	Timing Diagrams for Mode 3 (MD1 = High, MD0 = Low).....	29
4.4	Timing Diagrams for Mode 4 (MD1 = High, MD0 = High).....	31
5.0	Mechanical Specifications.....	33

Figures

1	LXT905 Transceiver Block Diagram	6
2	LXT905 Pin Assignments	7
3	LXT905 Transceiver TPO Output Waveform.....	9
4	Jabber Control Function	11
5	SQE Function	12
6	Collision Detection Function	13
7	Link Integrity Test Function	15
8	Intel* Controller Application (Mode 2).....	18
9	LXT905 Transceiver/380C26 Interface for Dual 10BASE-T and Token Ring Support .. (Mode 4).....	19
10	LXT905 Transceiver/MC68EN360 Interface for Full Duplex 10BASE-T (Mode 1)	20
11	Mode 1 RCLK/Start-of-Frame Timing	24

12	Mode 1 RCLK/End-of-Frame Timing	25
13	Mode 1 Transmit Timing	25
14	Mode 1 COL Output Timing	26
15	Mode 2 RCLK/Start-of-Frame	27
16	Mode 2 RCLK/End-of-Frame Timing	27
17	Mode 2 Transmit Timing	28
18	Mode 2 COL Output Timing	28
19	Mode 3 RCLK/Start-of-Frame Timing	29
20	Mode 3 RCLK/End-of-Frame Timing	29
21	Mode 3 Transmit Timing	30
22	Mode 3 COL Output Timing	30
23	Mode 4 RCLK/Start-of-Frame Timing	31
24	Mode 4 RCLK/End-of-Frame Timing	31
25	Mode 4 Transmit Timing	32
26	Mode 4 COL Output Timing	32
27	LXT905PC Package Specifications	33
28	LXT905LC Package Specifications	34

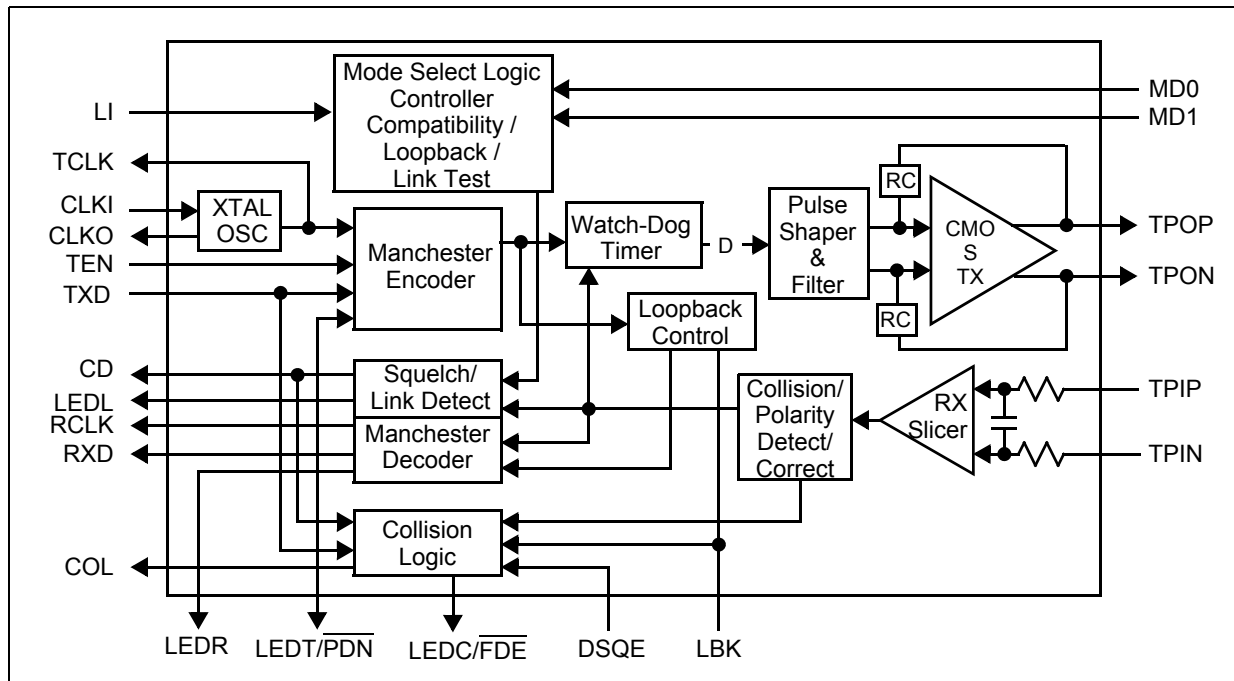
Tables

1	LXT905 Transceiver Signal Descriptions	7
2	Controller Compatibility Mode Options	10
3	Loopback Modes	14
4	Suitable Crystals	16
5	Absolute Maximum Values	21
6	Recommended Operating Conditions	21
7	I/O Electrical Characteristics	21
8	TP Electrical Characteristics	22
9	Switching Characteristics	22
10	RCLK/Start-of-Frame Timing	22
11	RCLK/End-of-Frame Timing	23
12	Transmit Timing	23
13	Miscellaneous Timing	23

Revision History

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Removed ordering and marking information. This information is now available from www.cortina-systems.com .
Revision 5.0 Revision Date: 27 July 2007
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Revision 001 Revision Date: October 2000
<ul style="list-style-type: none">Change resistor values for Figures 7, 8, and 9.

Figure 1 LXT905 Transceiver Block Diagram



1.0 Pin Assignments and Signal Descriptions

Figure 2 LXT905 Pin Assignments

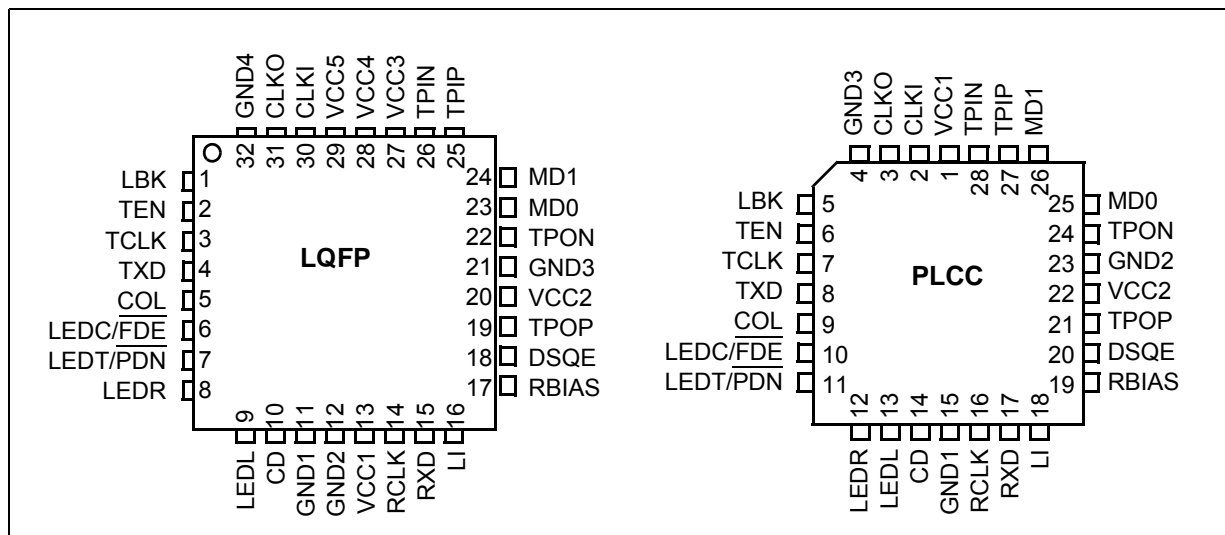


Table 1 LXT905 Transceiver Signal Descriptions (Sheet 1 of 2)

LQFP Pin #	PLCC Pin #	Symbol	I/O	Description
13	1	VCC1	—	Power Inputs 1 thru 5. Power supply inputs of 3.3 V or 5 V.
20	22	VCC2	—	
27	—	VCC3	—	
28	—	VCC4	—	
29	—	VCC5	—	
30	2	CLKI	I	Crystal Oscillator. Connect a 20 MHz crystal across these pins, or apply a 20 MHz clock at CLKI, with CLKO left open.
31	3	CLKO	O	
11	15	GND1	—	Ground.
12	23	GND2	—	
21	4	GND3	—	
32	—	GND4	—	
1	5	LBK	I	Loopback. When High, forces internal loopback. Disables collision and the transmission of both data and link pulses. Pulled Low internally. ¹
2	6	TEN	I	Transmit Enable. Enables data transmission and starts the Watch-Dog Timer (WDT). Synchronous to TCLK. Pulled Low internally. ¹
3	7	TCLK	O	Transmit Clock. A 10 MHz clock output. Connect this clock signal directly to the transmit clock input of the controller.
4	8	TXD	I	Transmit Data. Input signal containing NRZ data to transmit on the network. Connect TXD directly to the transmit data output of the controller. Pulled Low internally. ¹
5	9	COL	O	Collision Signal. Output that drives the collision detect input of the controller.

1. Externally pull-up or pull-down each pin separately using a 10 k Ω , 1% termination resistor, or tie directly to Vcc or ground.
2. Do not allow this pin to float. If unused, tie High.

Table 1 LXT905 Transceiver Signal Descriptions (Sheet 2 of 2)

LQFP Pin #	PLCC Pin #	Symbol	I/O	Description
6	10	LEDC/ FDE	O I	LED Collision or Full Duplex Enable. LEDC is an open drain driver for the collision indicator, and pulls Low during collision. Extends LED "on" (which is Low output) time by approximately 100 ms. FDE enables full duplex mode (external loopback) if tied Low externally. Pulled High internally ¹ .
7	11	LEDT/ PDN	O I	LED Transmit or Power Down. LEDT is an open drain driver for the transmit indicator. Extends LED "on" (which is Low output) time by approximately 100 ms. Pulls output Low during transmit ² . If externally tied Low, the LXT905 goes to power down state (PDN). In power-down mode, LEDT trislates all logic inputs and outputs.
8	12	LEDR	O	LED Receive. Open drain driver for the receive indicator LED. Extends LED "on" (which is Low output) time by approximately 100 ms. Pulls output Low during receive. Pulled High internally ¹ .
9	13	LEDL	O	LED Link. Open drain driver for link integrity indicator. Pulls output Low during link test pass. Pulled High internally ¹ .
10	14	CD	O	Carrier Detect. An output for notifying the controller that activity exists on the network.
14	16	RCLK	O	Receive Clock. A recovered 10 MHz clock that is synchronous to the received data and connects to the controller receive clock input.
15	17	RXD	O	Receive Data. Output signal connected directly to the receive data input of the controller.
16	18	LI	I	Link Enable. Controls link integrity test <ul style="list-style-type: none"> • Enabled when LI is High • Disabled when LI is Low
17	19	RBIAS	I	Bias Circuitry. A 7.5 kW 1% resistor to ground at this pin controls operating circuit bias.
18	20	DSQE	I	SQE Disable. <ul style="list-style-type: none"> • When DSQE is High, the SQE function is disabled. • When DSQE is Low, the SQE function is enabled. Disable SQE for normal operation in Hub/Switch/Repeater applications. Pulled Low internally ¹ .
19 22	21 24	TPOP TPON	O O	Twisted-Pair Outputs. Differential outputs to the twisted-pair cable. The outputs are pre-equalized.
23 24	25 26	MDO MDI	I I	Mode Select 0 and 1. Mode select pins determine controller compatibility mode in accordance with Table 2. Pulled Low internally ¹ .
25 26	27 28	TPIP TPIN	I I	Twisted-Pair Inputs. A differential input pair from the twisted-pair cable. Receive filter is integrated on-chip. Does not require external filters.
<p>1. Externally pull-up or pull-down each pin separately using a 10 k Ω, 1% termination resistor, or tie directly to Vcc or ground. 2. Do not allow this pin to float. If unused, tie High.</p>				

2.0 Functional Description

2.1 Introduction

The LXT905 Transceiver performs the physical layer signaling (PLS) and Media Attachment Unit (MAU) functions, as defined in the IEEE 802.3 specification. It functions as an integrated PLS/MAU for use with 10BASE-T twisted-pair networks.

The LXT905 Transceiver interfaces a back-end controller to a twisted-pair (TP) cable. The controller interface includes a transmit and receive clock and NRZ data channels, and mode control logic and signaling. The twisted-pair interface comprises the following two circuits:

- Twisted-Pair Input (TPI)
- Twisted-Pair Output (TPO)

In addition to the two basic interfaces, the LXT905 Transceiver contains an internal crystal oscillator and four LED drivers for visual status reporting.

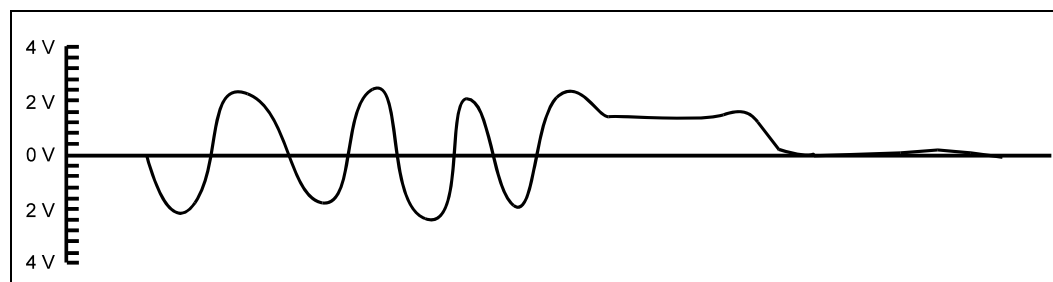
The back-end controller side of the interface defines functions.

- The LXT905 Transceiver transmit function refers to data transmitted by the back-end to the twisted-pair network.
- The LXT905 Transceiver receive function refers to data received by the back-end of the twisted-pair network.

The LXT905 Transceiver performs all required functions defined in the *IEEE 802.3 10BASE-T MAU* specification as follows:

- Collision detection
- Link integrity testing
- Signal quality error messaging
- Jabber control
- Loopback

Figure 3 LXT905 Transceiver TPO Output Waveform



2.2 Controller Compatibility Modes

The LXT905 Transceiver is compatible with most industry standard controllers, including devices from Advanced Micro Devices* (AMD), Fujitsu*, National Semiconductor*, Seeq*, Motorola* and Texas Instruments*. Four different control signal timing and polarity

schemes (Modes 1 through 4) provide this compatibility. The MD0 and MD1 mode select pins determine controller compatibility modes (see [Table 2](#)). Refer to [Section 4.0, Test Specifications](#), on page 21 for timing diagrams and parameters.

2.3 Transmit Function

The LXT905 Transceiver receives NRZ data from the controller at the TXD input, as shown in [Figure 1, LXT905 Transceiver Block Diagram](#), on page 6, and passes it through a Manchester encoder. The LXT905 Transceiver then transfers encoded data to the twisted-pair network (TPO circuit). The advanced integrated pulse shaping and filtering network produces the output signal on TPON and TPOP, shown in [Figure 3, LXT905 Transceiver TPO Output Waveform](#), on page 9. The TPO output is pre-distorted and pre-filtered to meet the 10BASE-T jitter template. An internal, continuous resistor-capacitor filter removes any high-frequency clocking noise from the pulse shaping circuitry. Integrated filters simplify the design work required for FCC compliant EMI performance. During idle periods, the LXT905 Transceiver transmits link integrity test pulses on the TPO circuit (if LI is enabled and LBK is disabled).

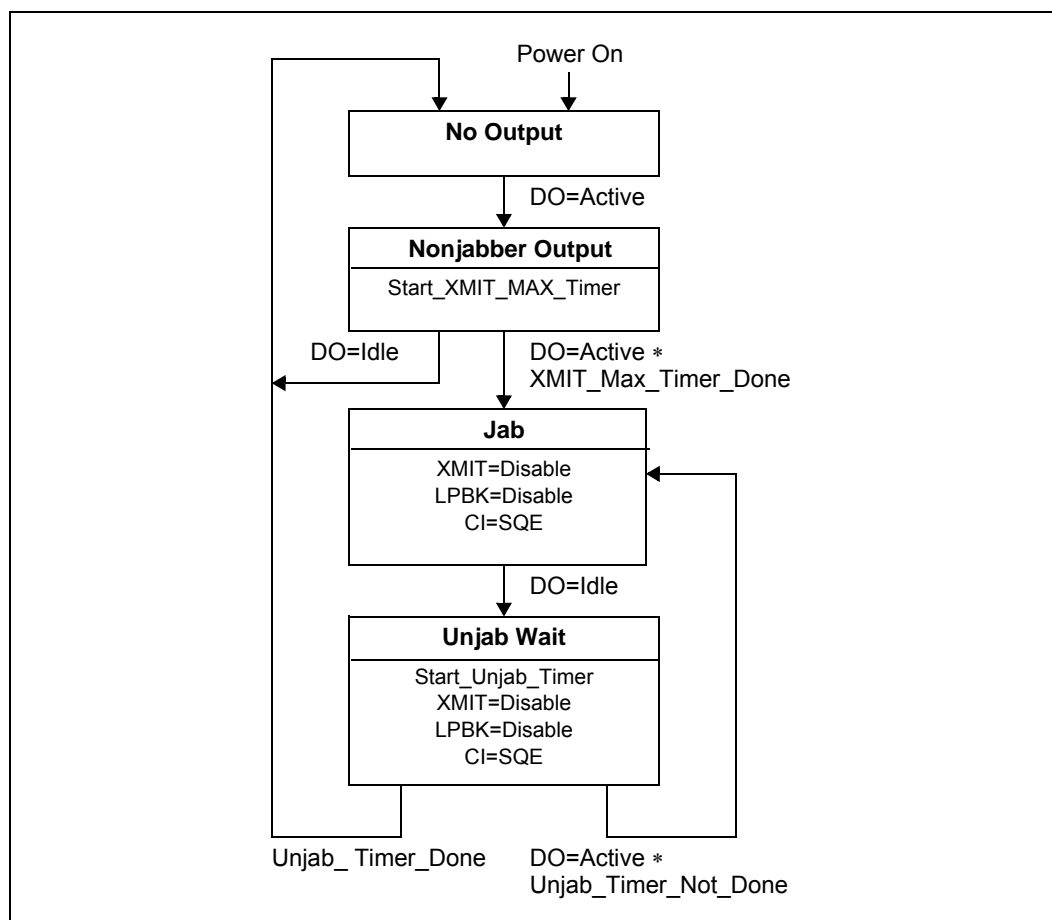
Table 2 Controller Compatibility Mode Options

Controller Mode	MD1	MD0
Mode 1 - For Motorola* MC68EN360 or compatible controllers (AMD* AM7990)	Low	Low
Mode 2 - For Intel* 82596 or compatible controllers	Low	High
Mode 3 - For Fujitsu* MB86950, MB86960 or compatible controllers (Seeq* 8005) ¹	High	Low
Mode 4 - For TI* TMS380C26 or compatible controllers	High	High
1. Seeq* controllers require inverters on CLKI, LBK, RCLK and COL.		

2.4 Jabber Control Function

[Figure 4](#) is a state diagram of the LXT905 Transceiver jabber control function. The LXT905 Transceiver on-chip Watch-Dog Timer (WDT) prevents the DTE from locking into a continuous transmit mode. When a transmission exceeds the time limit, the WDT disables the transmit and loopback functions and activates the COL pin. Once the LXT905 Transceiver is in the jabber state, the TXD circuit must remain idle for a period of 0.25 to 0.75 seconds before it exits the jabber state.

Figure 4 Jabber Control Function

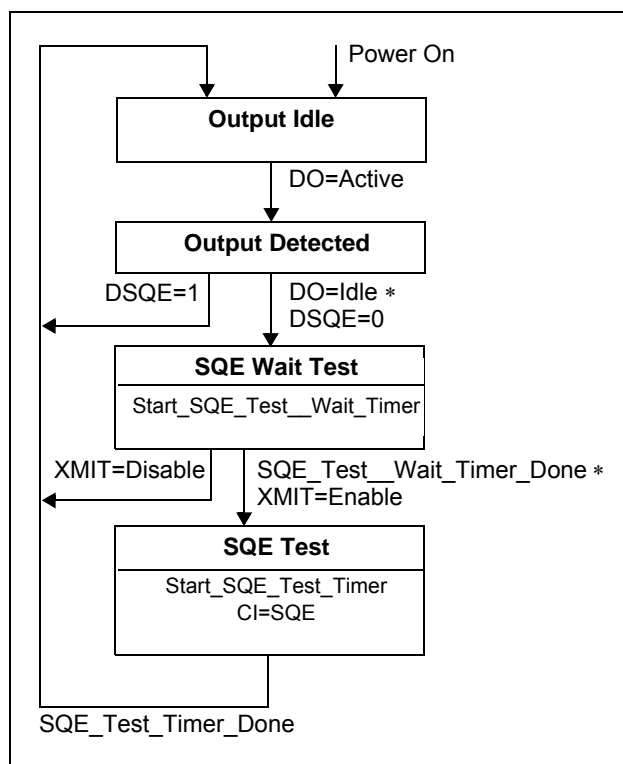


2.5 SQE Function

The LXT905 Transceiver supports the Signal Quality Error (SQE) function (see [Figure 5](#)). After every successful transmission on the 10BASE-T network, the LXT905 Transceiver transmits the SQE signal for 10 bit times (BT) \pm 5BT on the COL pin of the device.

- To disable the SQE function for repeater/switch applications, set DSQE High.
- To enable the SQE function, set DSQE Low.

Figure 5 SQE Function



2.6 Receive Function

The LXT905 Transceiver receive function acquires timing and data from the twisted-pair network (TPI circuit). The LXT905 Transceiver passes valid received signals through the on-chip filters and Manchester decoder, then outputs them as decoded NRZ data on the RXD pin, and as receive timing on the RCLK pin.

An internal RC filter and an intelligent squelch function discriminate noise from link test pulses and valid data streams. The receive function activates only when receiving valid data streams above the squelch level with proper timing.

If the differential signal at the TPI circuit inputs falls below 85 percent of the threshold level (unsquelched) for 8 bit times (typical), the LXT905 Transceiver receive function enters the idle state. The LXT905 Transceiver automatically corrects reversed polarity on the TPI circuit.

2.7 Polarity Reverse Function

The LXT905 Transceiver polarity reverse function uses both link pulses and end-of-frame data to determine the polarity of the received signal.

- If you disable Link Integrity testing, polarity detection is based only on received data. A reversed polarity condition exits if the LXT905 Transceiver detects eight consecutive opposite receive link pulses, without receiving a link pulse of the expected polarity.

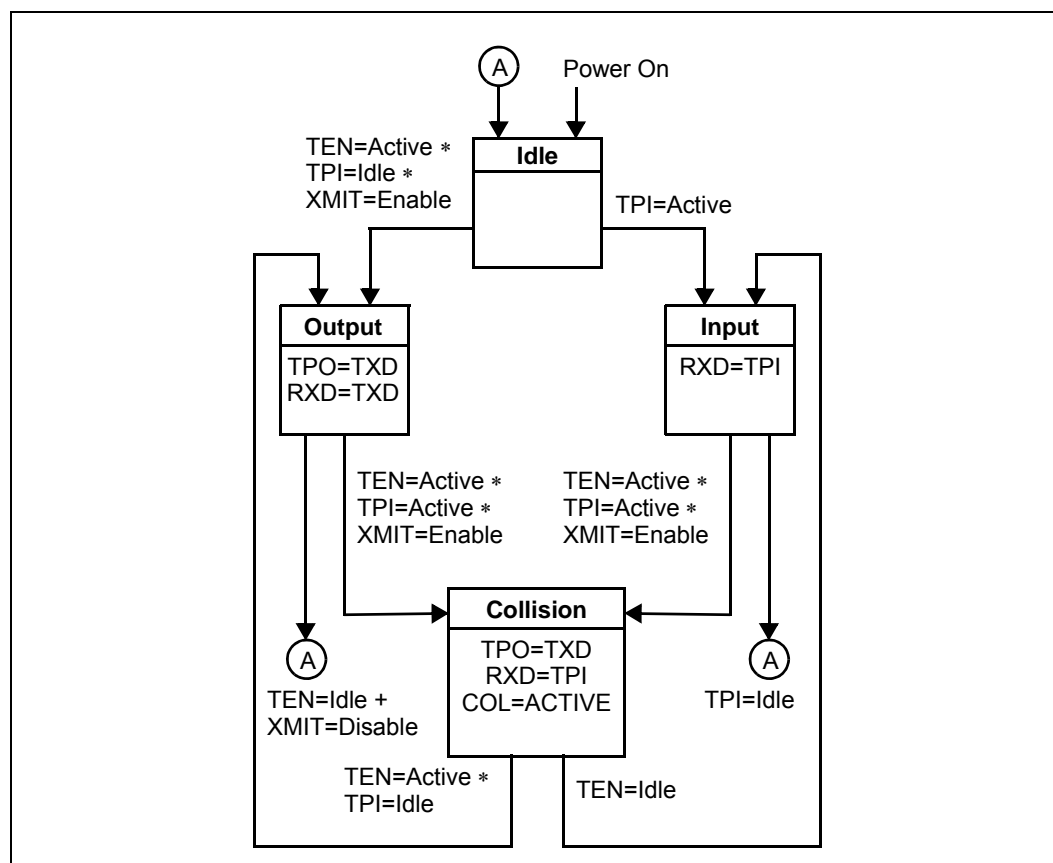
- Reversed polarity also occurs if the LXT905 Transceiver receives four consecutive frames with a reversed start-of-idle.
- Whenever the LXT905 Transceiver receives a correct polarity frame or a correct link pulse, it resets these two counters to zero.
- If the LXT905 Transceiver enters the link fail state, and does not receive any valid data or link pulses within 96 to 128 ms, it resets the polarity to the default non-flipped condition.

Polarity correction is always enabled.

2.8 Collision Detection Function

A collision is the simultaneous presence of valid signals on both the TPI circuit and the TPO circuit. The LXT905 Transceiver reports collisions to the back-end via the COL pin. If the TPI circuit becomes active while there is activity on the TPO circuit, the TPI data passes to the back-end over the RXD circuit, disabling normal loopback. Figure 6 is a state diagram of the LXT905 Transceiver collision detection function.

Figure 6 Collision Detection Function



2.9 Loopback Functions

2.9.1 Internal Loopback

The LXT905 Transceiver provides a standard loopback mode, as specified in the IEEE specification for the twisted-pair port. It also provides a forced internal loopback mode. Loopback mode operates in conjunction with the transmit function. The LXT905 Transceiver internally loops back data that the MAC transmits, from the TXD pin, through the Manchester encoder/decoder, to the RXD pin, and returning to the MAC.

A data collision disables standard loopback mode, clearing the RXD circuit for the TPI data. Link fail, jabber, and full-duplex states also disable standard loopback. Loopback is always enabled during forced internal loopback mode.

2.9.2 External Loopback/Full Duplex

The LXT905 Transceiver also provides an external loopback test mode for system-level testing. When both LEDC/FDE and LBK are Low, the LXT905 Transceiver enables external loopback and full-duplex mode, and disables internal loopback circuits, SQE, and collision detection. Refer to [Table 3](#) for a summary of loopback and duplex modes.

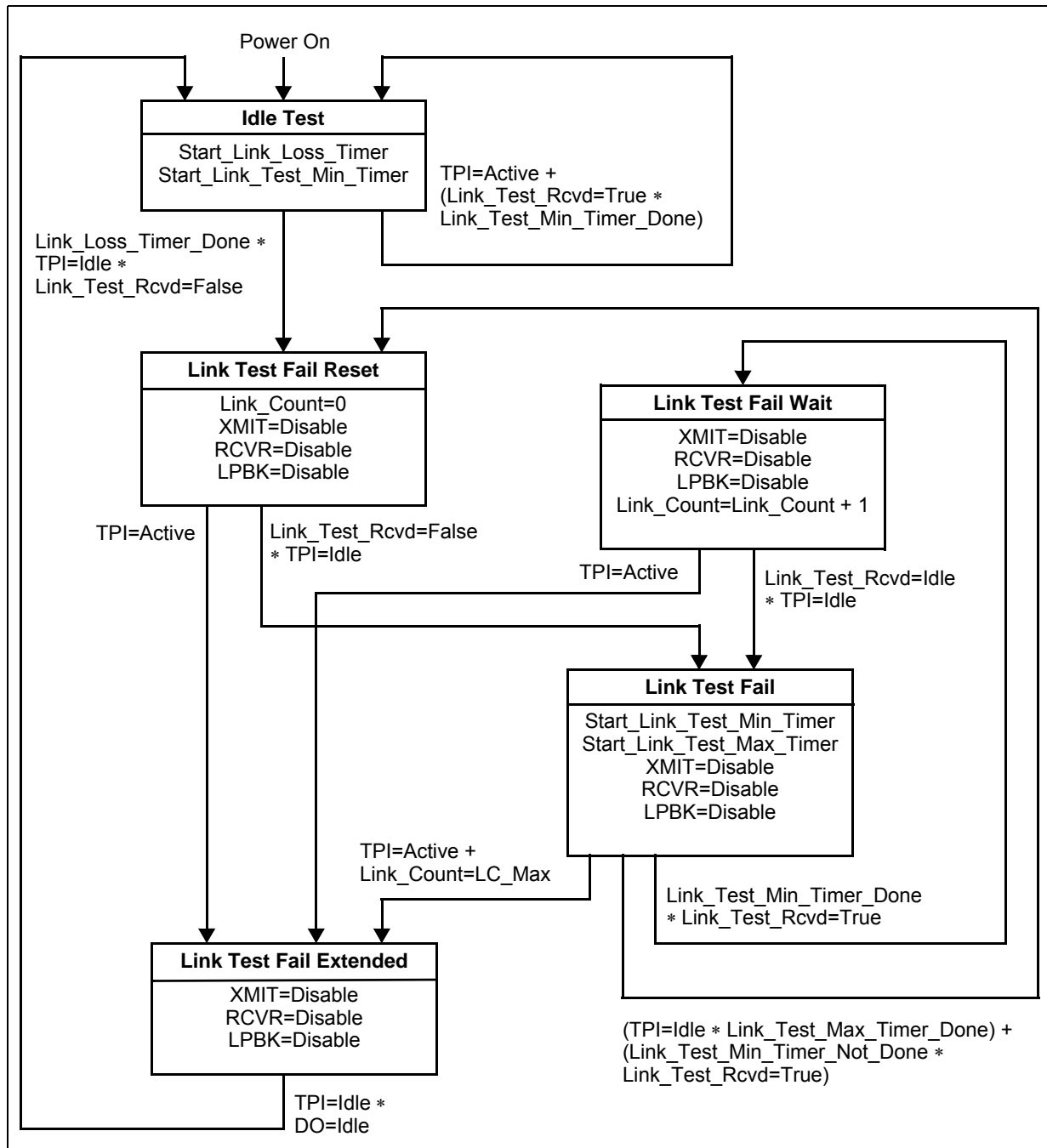
Table 3 Loopback Modes

Pin Settings		Mode Description
LBK	LEDC/ FDE	
Low	Low	Disable internal loopback. Enable external loopback test mode and full-duplex mode.
Low	High	Standard loopback mode (default). Internally loops back data that the MAC transmitted, and returns the data to the MAC, except during collision. A data collision disables standard loopback, clearing RXD for data on the twisted-pair port.
High	Low	Not Used.
High	High	Forced internal loopback. Loops-back transmit data on the receive data bus, and ignores the twisted-pair port.

2.10 Link Integrity Test Function

[Figure 7](#) is a state diagram of the LXT905 Transceiver link integrity test function. The link integrity test determines the status of the receive side twisted-pair cable. Link integrity testing is enabled when LI is tied High. When enabled, the receiver recognizes link integrity pulses that transmit in the absence of receive traffic. If the LXT905 Transceiver does not detect any serial data stream or link integrity pulses within 50~150 ms, the chip enters a link fail state and disables the transmit and normal loopback functions. The LXT905 Transceiver ignores any link integrity pulse with interval less than 2~7 ms. The LXT905 remains in the link fail state until it detects either a serial data packet, or two or more link integrity pulses.

Figure 7 Link Integrity Test Function



3.0 Application Information

3.1 Introduction

Figure 8, *Intel® Controller Application (Mode 2)*, on page 18 through Figure 10, *LXT905 Transceiver/MC68EN360 Interface for Full Duplex 10BASE-T (Mode 1)*, on page 20 show typical LXT905 Transceiver applications. These diagrams group similar pins; they do not portray the actual chip pinout. The controller interface pins [Transmit Data (TXD), Transmit Clock (TCLK) Transmit Enable (TEN), Receive Data (RXD), Receive Clock (RCLK), Collision Signal (COL), and Carrier Detect (CD)] are at the upper left of the diagram.

Power and ground pins are at the bottom of each diagram. Vcc1 and Vcc2 use a single power supply, with decoupling capacitors installed between the power and ground buses. Either a 5 V or 3.3 V supply can power Vcc.

3.1.1 Termination Circuitry

The LXT905 Transceiver pulls several I/O pins up or down internally, to keep the signals from floating. It is recommended to hard-wire these pins either High or Low. Externally pull-up pins (LEDT/PDN, LEDC/FDE, LEDR, LEDL) and pull-down pins (LBK, TEN, TXD, DSQE, MDO, MDI) separately, using a 10 k Ω 1% resistor, or tie them directly to Vcc or ground.

3.1.2 Twisted-Pair Interface

The Twisted-Pair interface (TPOP/N and TPIP/N) is at the upper right of the diagram. The I/O pairs have impedance-matching resistors for 100 Ω UTP, but do not require any external filters.

3.1.3 RBIAS Pin

The RBIAS pin sets the levels for the LXT905 Transceiver output drivers. The LXT905 Transceiver requires a 7.5 k Ω 1% resistor directly connected between the RBIAS pin and ground. Locate this resistor as close to the device as possible. Keep the traces as short as possible, isolated from all other high-speed signals.

3.1.4 Crystal Information

Table 4 lists some suitable crystals based on limited evaluation. Test and validate all crystals before committing to a specific component.

Table 4 Suitable Crystals

Manufacturer	Part Number
MTRON*	MP-1
	MP-2

3.1.5 Magnetic Information

The LXT905 Transceiver requires a 1:1 turns ratio for the receive transformer, and a 1:2 turns ratio for the transmit transformer. The Magnetic Manufacturers for Networking Product Applications Application Note (document number 248991) lists transformers suitable for the applications described in this datasheet.

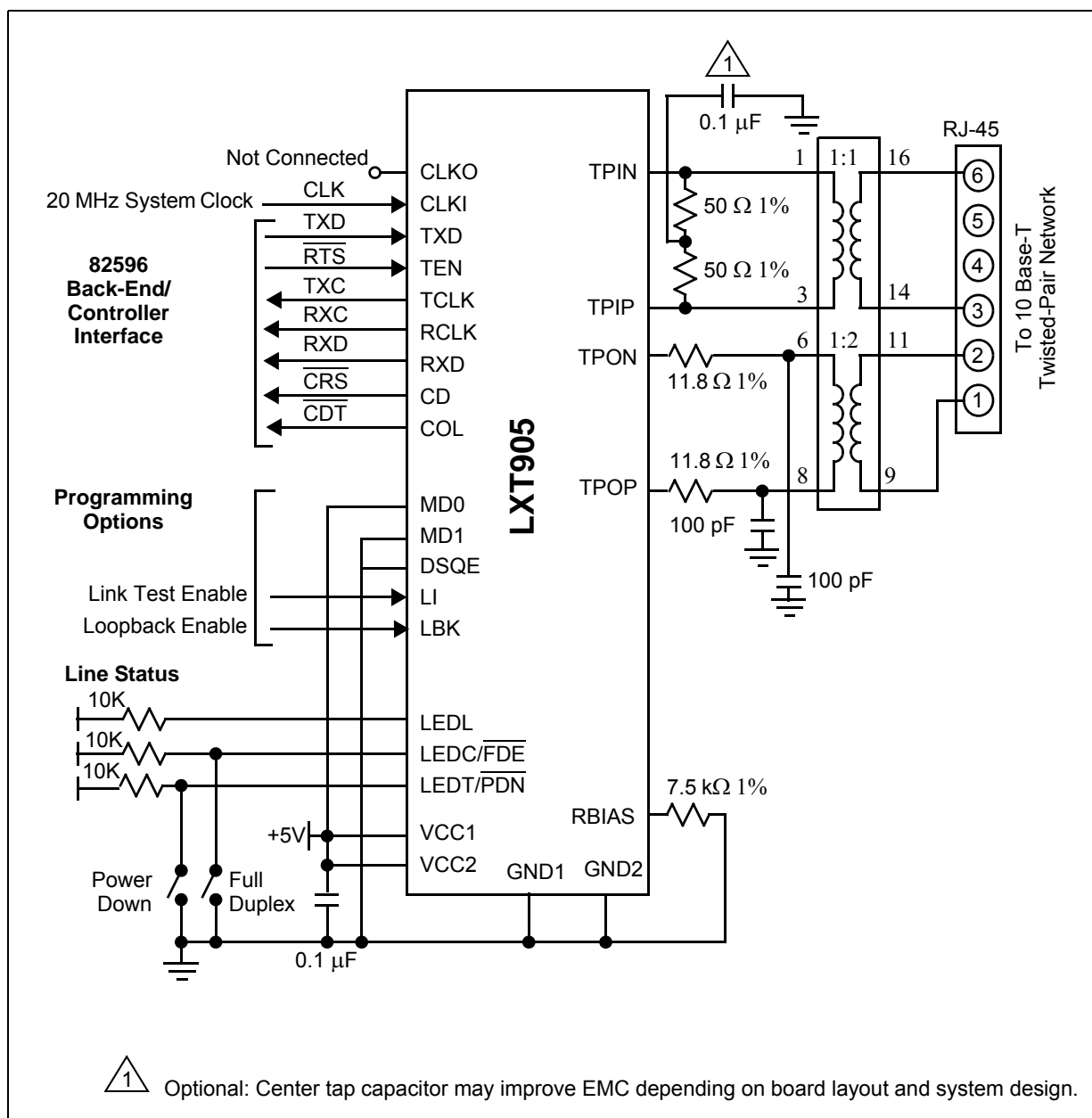
Note: Test and validate all magnetics before committing to a specific component.

3.2 Typical 10BASE-T Application

Figure 8 is a typical LXT905 Transceiver application. The DTE connects to a 10BASE-T network through the twisted-pair RJ-45 connector. With MD0 tied high and MD1 grounded, this example sets the LXT905 Transceiver logic and framing to Mode 2 (compatible with Intel® 82596 controllers). Connect 20 MHz system clock input at CLKI (leave CLKO open). The LI pin externally controls the link test function

Note: Refer to the Cortina Systems® MAC Interface Design Guide for Intel® Controllers Application Note (document number 249007) when designing with Intel® controllers.

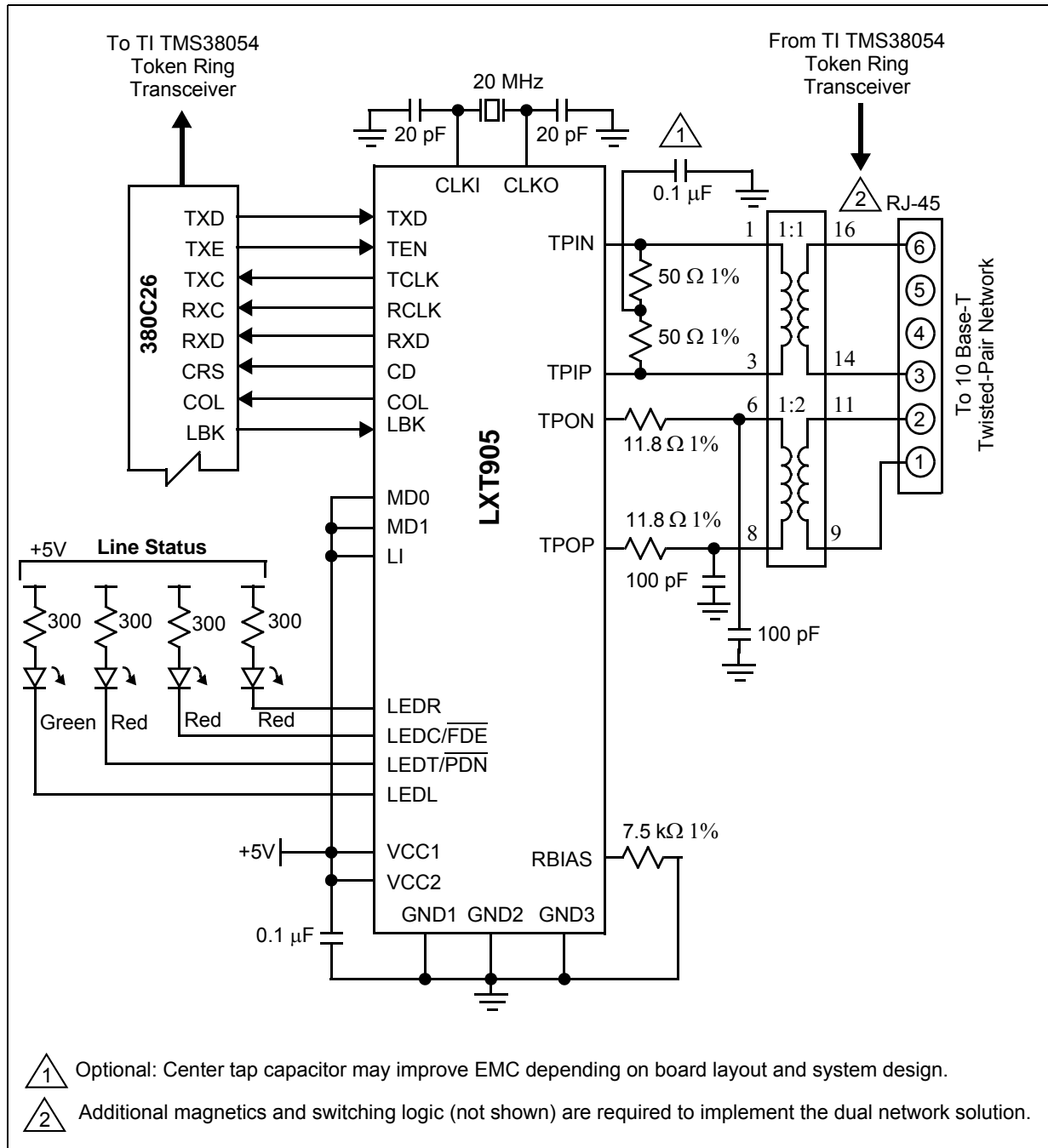
Figure 8 Intel® Controller Application (Mode 2)



3.3 Dual Network Support - 10BASE-T and Token Ring

Figure 9 shows the LXT905 Transceiver with a Texas Instruments* 380C26 CommProcessor. The 380C26 is compatible with Mode 4 (MD0 and MD1 both high). When you use the LXT905 Transceiver with the 380C26, you can tie both the LXT905 Transceiver and a TMS38054* Token Ring transceiver to a single RJ-45, allowing dual network support from a single connector.

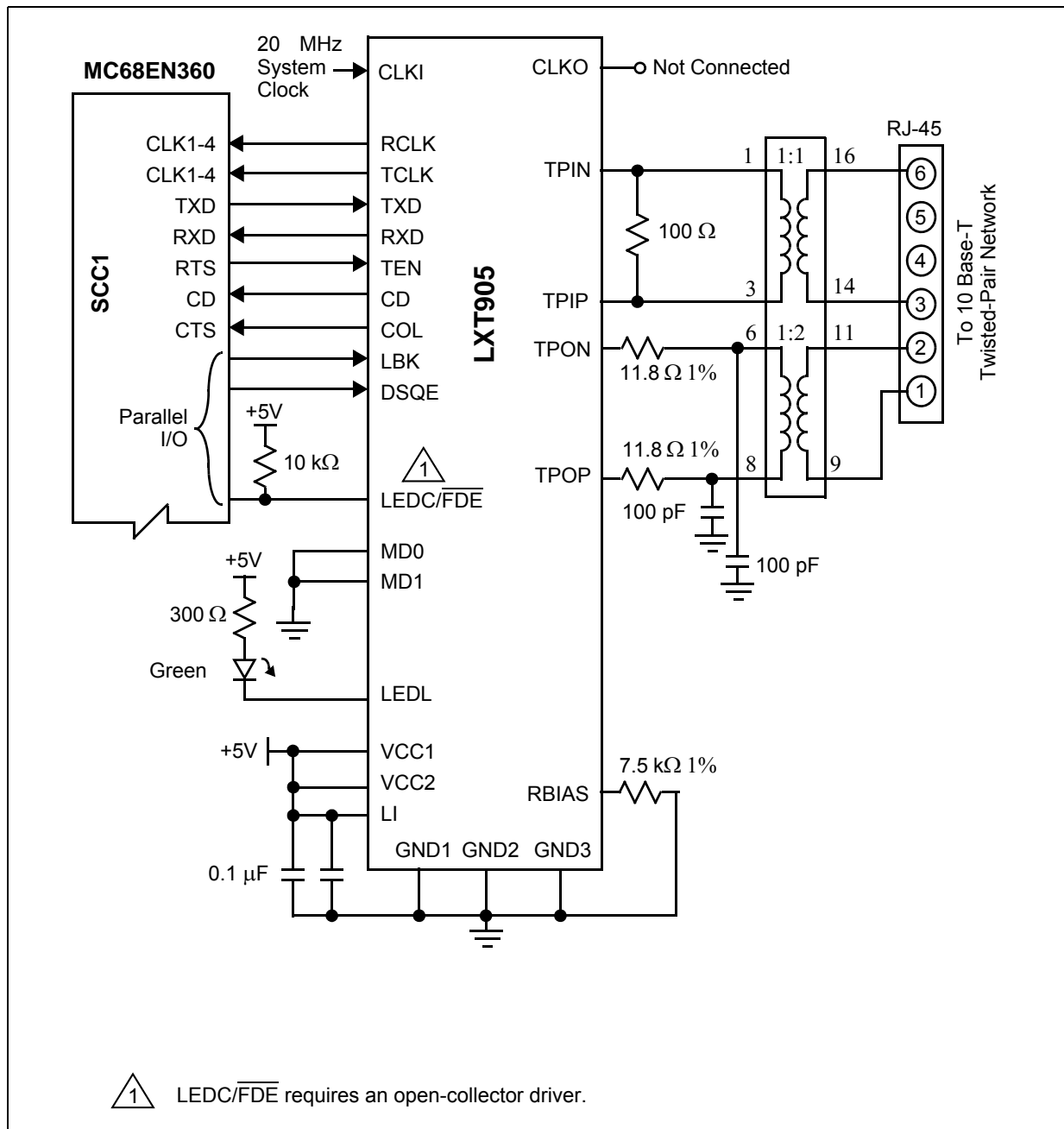
Figure 9 LXT905 Transceiver/380C26 Interface for Dual 10BASE-T and Token Ring Support (Mode 4)



3.4 Simple 10BASE-T Connection

Figure 10 shows a simple 10BASE-T application, using an LXT905 Transceiver and a Motorola® MC68EN360. The MC68EN360 is compatible with Mode 1 (MD0 and MD1 both Low).

Figure 10 LXT905 Transceiver/MC68EN360 Interface for Full Duplex 10BASE-T (Mode 1)



4.0 Test Specifications

Note: The minimum and maximum values in Table 5 through Table 13 and Figure 11 through Figure 26 represent the performance specifications of the LXT905 Transceiver. These specifications are guaranteed by test, except where noted by design. Minimum and maximum values in Table 7 through Table 13 apply over the recommended operating conditions specified in Table 6.

Table 5 Absolute Maximum Values

Parameter	Symbol	Min	Max	Units
Supply voltage	V _{CC}	-0.3	+6	V
Storage temperature	T _{ST}	-65	+150	°C

Caution: Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 6 Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Recommended supply voltage ¹	V _{CC}	3.135	5.0	5.25	V
Recommended operating temperature (Commercial)	T _{OP}	0	–	+70	°C
Recommended operating temperature (Extended)	T _{OP}	-40	–	+85	°C

1. Voltage is with respect to ground, unless specified otherwise.

Table 7 I/O Electrical Characteristics (Sheet 1 of 2)

Parameter		Sym	Min	Typ ¹	Max	Units	Test Conditions
Input low voltage ²		V _{IL}	–	–	0.8	V	–
Input high voltage ²		V _{IH}	2.0	–	–	V	–
Output low voltage		V _{OL}	–	–	0.4	V	I _{OL} = 1.6 mA
		V _{OL}	–	–	10	%V _{CC}	I _{OL} < 10 µA
Output low voltage (Open drain LED driver)		V _{OLL}	–	–	0.7	%V _{CC}	I _{OLL} = 10 mA
Output high voltage		V _{OH}	2.4	–	–	V	I _{OH} = 40 µA
		V _{OH}	90	–	–	%V _{CC}	I _{OH} < 10 µA
Output rise time	CMOS	–	–	3	15	ns	C _{LOAD} = 20 pF
TCLK & RCLK	TTL	–	–	2	15	ns	–
Output fall time	CMOS	–	–	3	15	ns	C _{LOAD} = 20 pF
TCLK & RCLK	TTL	–	–	2	15	ns	–
CLKI rise time (externally driven)		–	–	–	10	ns	–
1. Typical values are at 25 °C, are for design aid only, are not guaranteed, and are not subject to production testing. 2. Limited functional tests are performed at these input levels. The majority of functional tests are performed at levels of 0 V and 3 V. This applies to all inputs except TPIP and TPIN.							

Table 7 I/O Electrical Characteristics (Sheet 2 of 2)

Parameter		Sym	Min	Typ ¹	Max	Units	Test Conditions
CLKI duty cycle (externally driven)		–	–	50/50	40/60	%	–
Supply current	Normal Mode	I _{CC}	–	40	80	mA	Idle Mode
		I _{CC}	–	70	100	mA	Transmitting on TP
	Power Down Mode	I _{CC}	–	0.01	1	μA	–

1. Typical values are at 25 °C, are for design aid only, are not guaranteed, and are not subject to production testing.
2. Limited functional tests are performed at these input levels. The majority of functional tests are performed at levels of 0 V and 3 V. This applies to all inputs except TPIP and TPIN.

Table 8 TP Electrical Characteristics

Parameter	Symbol	Min	Typ ¹	Max	Units	Test Conditions
Transmit output impedance	Z _{OUT}	–	5	–	Ω	–
Transmit timing jitter addition ²	–	–	±6.4	±10	ns	0 line length for internal MAU
Transmit timing jitter added by the MAU and PLS sections ^{2,3}	–	–	±3.5	±5.5	ns	After line model specified by <i>IEEE 802.3 for 10BASE-T internal MAU</i>
Receive input impedance	Z _{IN}	–	24	–	kΩ	Between TPIP/TPIN
Differential squelch threshold	V _{DS}	300	420	585	mV	5 MHz square wave input

1. Typical values are at 25 °C, are for design aid only, are not guaranteed, and are not subject to production testing.
2. Parameter is guaranteed by design; not subject to production testing.
3. *IEEE 802.3* specifies maximum jitter additions at 0.5 ns from the encoder, and 3.5 ns from the MAU.

Table 9 Switching Characteristics

Parameter		Symbol	Minimum	Typical ¹	Maximum	Units
Jabber Timing	Maximum transmit time	–	20	–	150	ms
	Unjab time	–	250	–	750	ms
Link Integrity Timing	Time link loss receive	–	50	–	150	ms
	Link min receive	–	2	–	7	ms
	Link max receive	–	50	–	150	ms
	Link transmit period	–	8	10	24	ms

1. Typical values are at 25 °C, are for design aid only, are not guaranteed, and are not subject to production testing.

Table 10 RCLK/Start-of-Frame Timing (Sheet 1 of 2)

Parameter		Symbol	Min	Typ ¹	Max	Units
Decoder acquisition time		t _{DATA}	–	1300	1500	ns
CD turn-on delay		t _{CD}	–	400	550	ns
Receive data setup from RCLK	Mode 1	t _{RDS}	60	70	–	ns
	Modes 2, 3, and 4	t _{RDS}	30	45	–	ns

1. Typical values are at 25° C, are for design aid only, are not guaranteed, and are not subject to production testing.

Table 10 RCLK/Start-of-Frame Timing (Sheet 2 of 2)

Parameter	Symbol	Min	Typ ¹	Max	Units
Receive data hold from RCLK	Mode 1	tRDH	10	20	ns
	Modes 2, 3, and 4	tRDH	30	45	ns
RCLK shut off delay from CD assert (Mode 3)	tsws	–	±100	–	ns

1. Typical values are at 25° C, are for design aid only, are not guaranteed, and are not subject to production testing.

Table 11 RCLK/End-of-Frame Timing

Parameter	Type	Sym	Mode 1	Mode 2	Mode 3	Mode 4	Units
RCLK after CD off	Min	tRC	5	1	–	5	BT
Rcv data through-put delay	Max	tRD	400	375	375	375	ns
CD turn-off delay ²	Max	tCDOFF	500	475	475	475	ns
Receive block out after TEN off ³	Typical ¹	tIFG	5	50	–	–	BT
RCLK switching delay after CD off	Typical ¹	tswe	–	–	120 (±80)	–	ns

1. Typical figures are at 25 °C, are for design aid only, are not guaranteed, and are not subject to production testing.
2. CD Turnoff delay, measured from middle of last bit: timing specification. The value of the last bit does not affect this value.
3. Disables blocking of Carrier Detect during full duplex operation.

Table 12 Transmit Timing

Parameter	Symbol	Minimum	Typical ¹	Maximum	Units
TEN setup from TCLK	tEHCH	22	–	–	ns
TXD setup from TCLK	tDSCH	22	–	–	ns
TEN hold after TCLK	tCHEL	5	–	–	ns
TXD hold after TCLK	tCHDU	5	–	–	ns
Transmit start-up delay	tSTUD	–	350	450	ns
Transmit through-put delay	tTPD	–	338	350	ns

1. Typical values are at 25° C, are for design aid only, are not guaranteed, and are not subject to production testing.

Table 13 Miscellaneous Timing

Parameter	Symbol	Minimum	Typical ¹	Maximum	Units
COL (SQE) Delay after TEN off ²	tsQED	0.65	–	1.6	µs
COL (SQE) Pulse Duration ²	tsQEP	500	–	1500	ns
Power Down recovery time	tPDR	–	25	–	ms

1. Typical values are at 25° C, are for design aid only, are not guaranteed, and are not subject to production testing.
2. When SQE is enabled (DSQE is Low).

4.1 Timing Diagrams for Mode 1 (MD1 = Low, MD0 = Low)

Timing diagrams for Mode 1 include Figure 11 through Figure 14.

Figure 11 Mode 1 RCLK/Start-of-Frame Timing

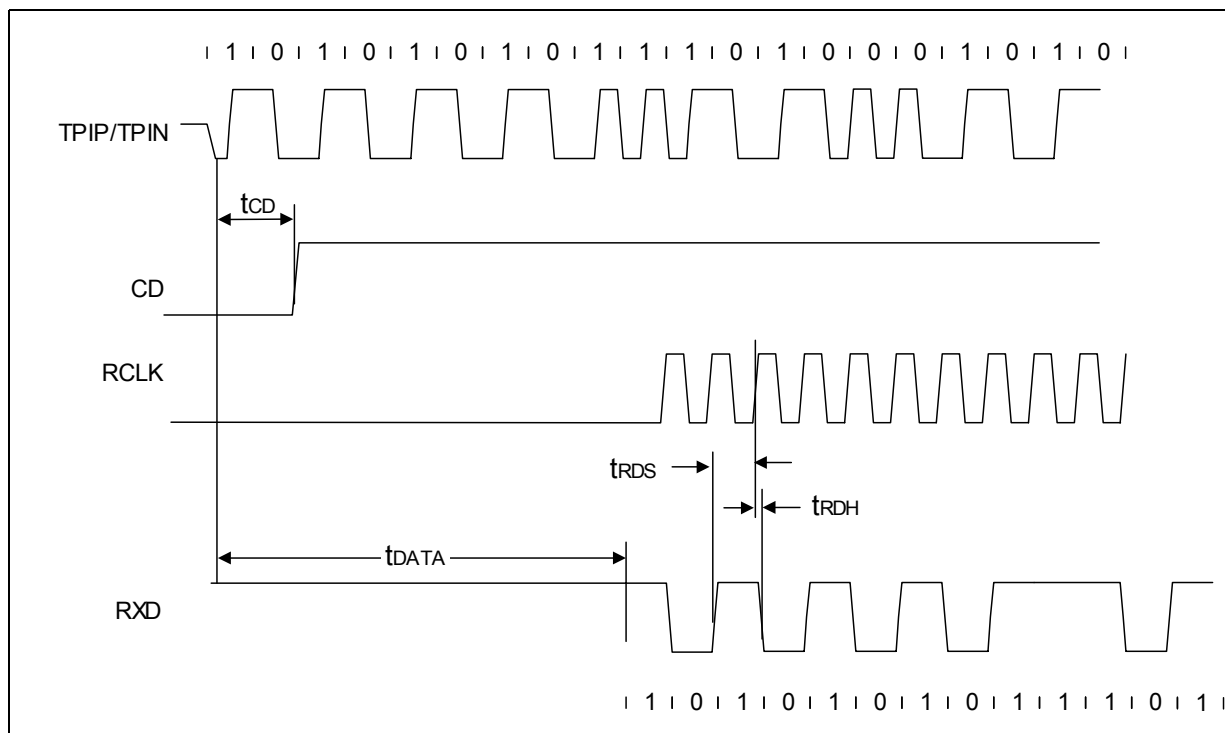


Figure 12 Mode 1 RCLK/End-of-Frame Timing

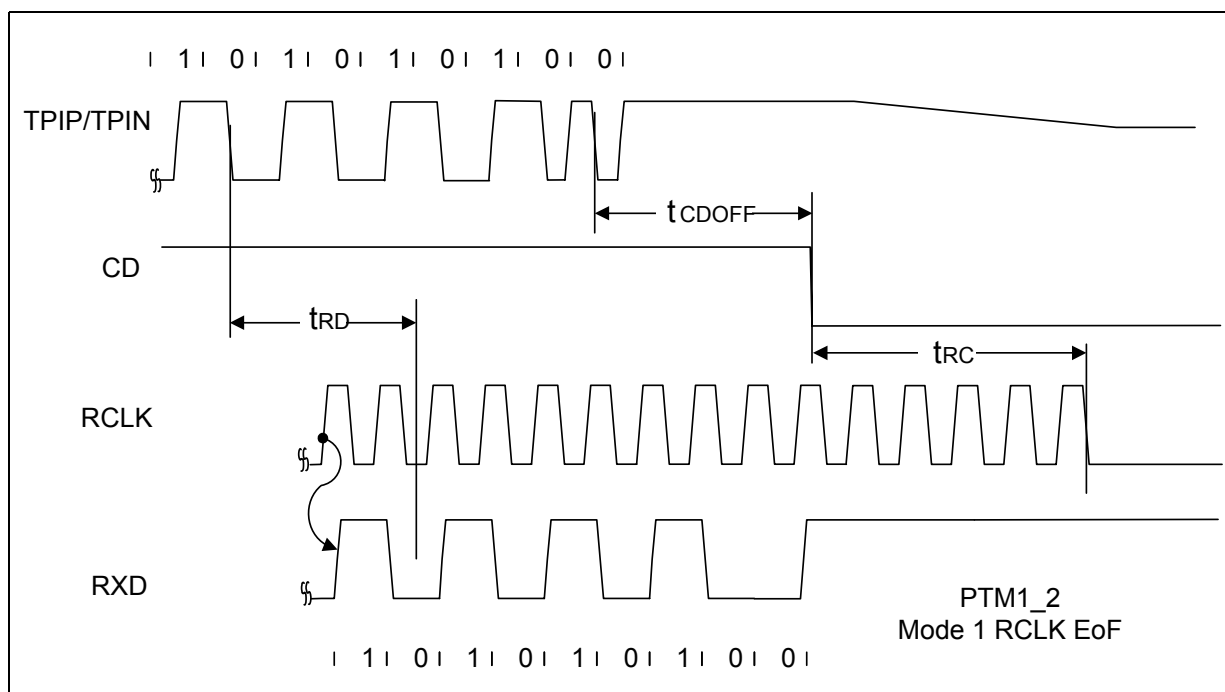


Figure 13 Mode 1 Transmit Timing

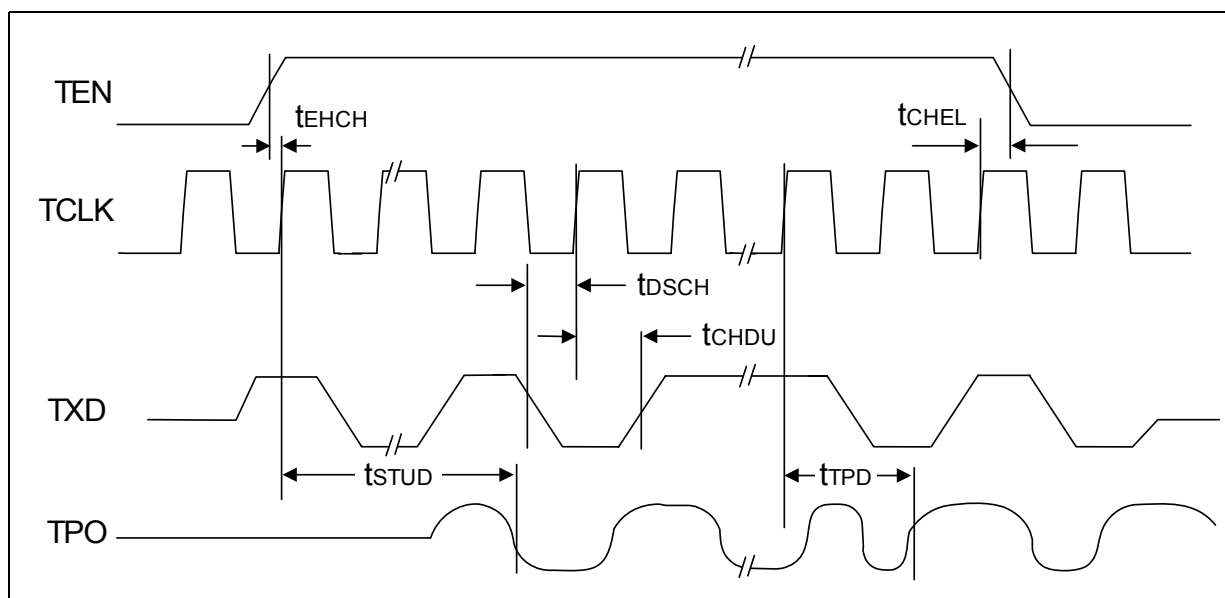
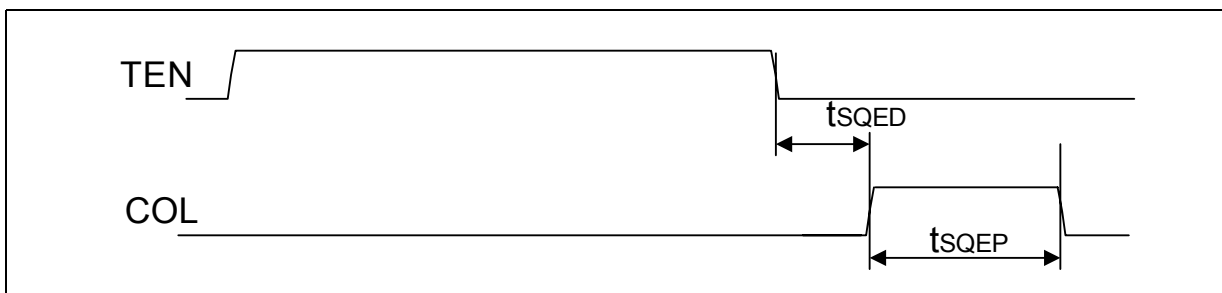


Figure 14 Mode 1 COL Output Timing



4.2 Timing Diagrams for Mode 2 (MD1 = Low, MD0 = High)

Timing diagrams for Mode 2 include Figure 15 through Figure 18.

Figure 15 Mode 2 RCLK/Start-of-Frame

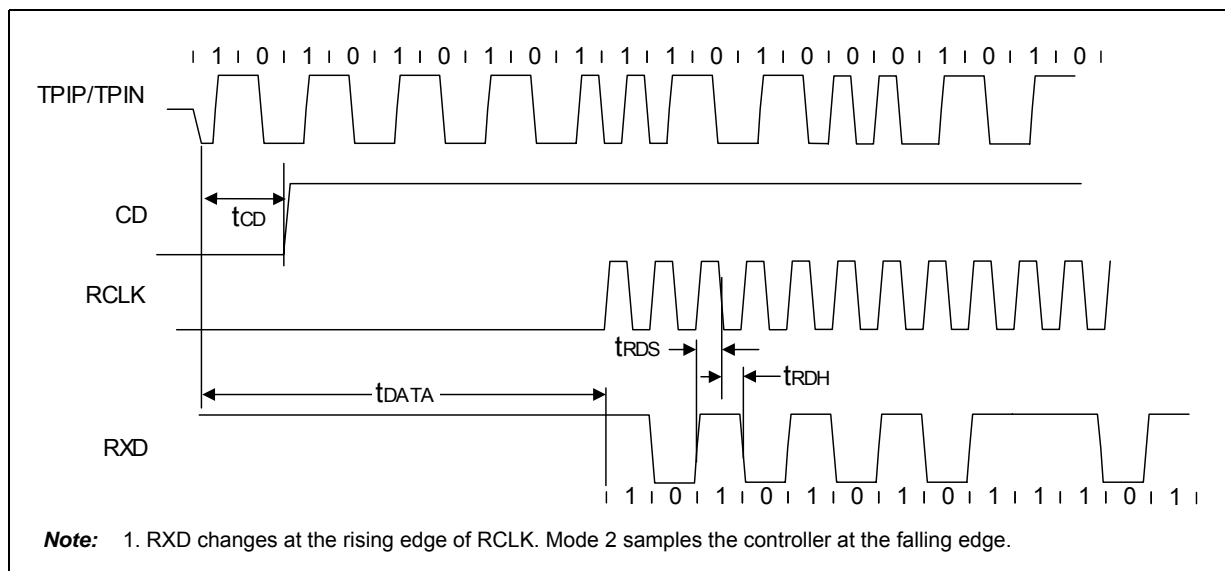


Figure 16 Mode 2 RCLK/End-of-Frame Timing

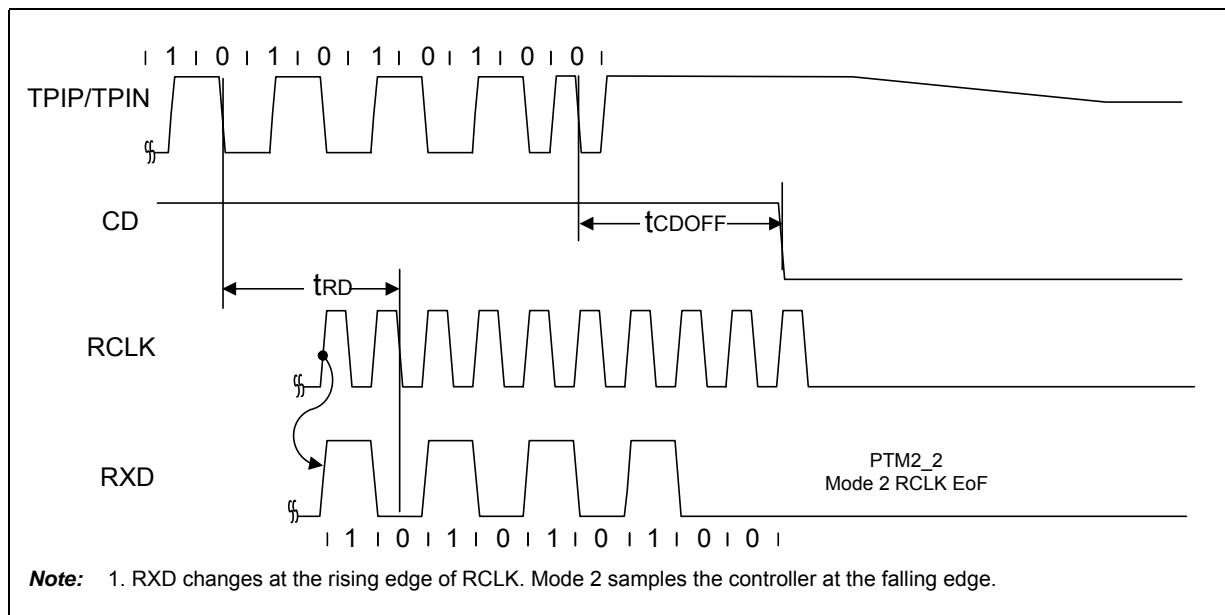


Figure 17 Mode 2 Transmit Timing

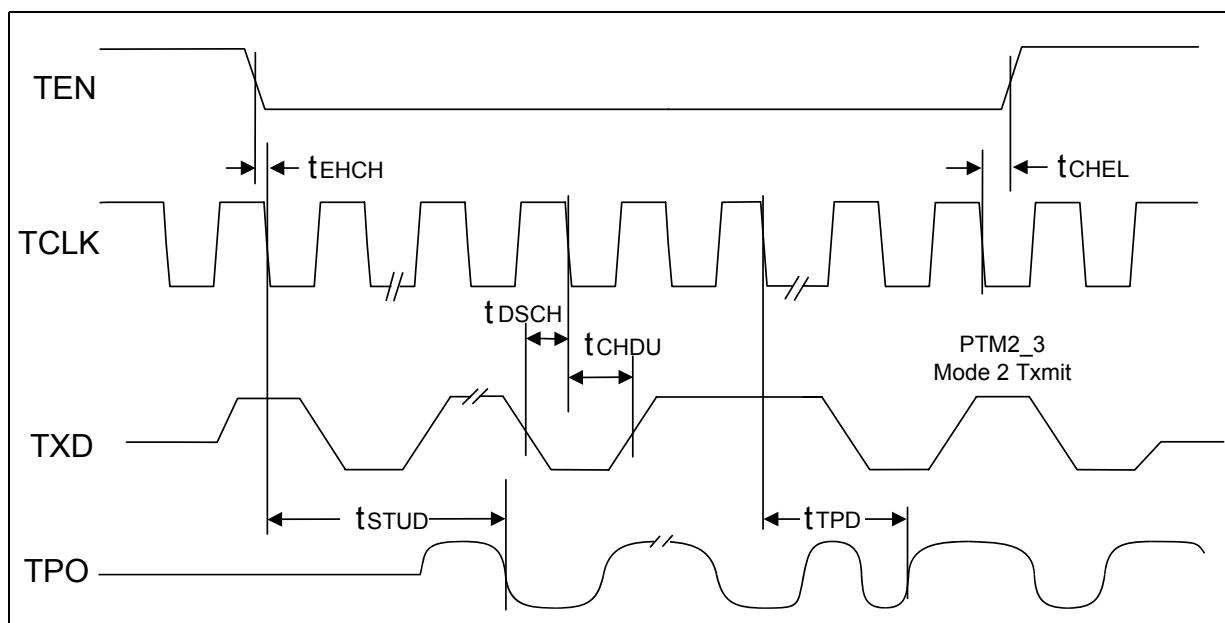
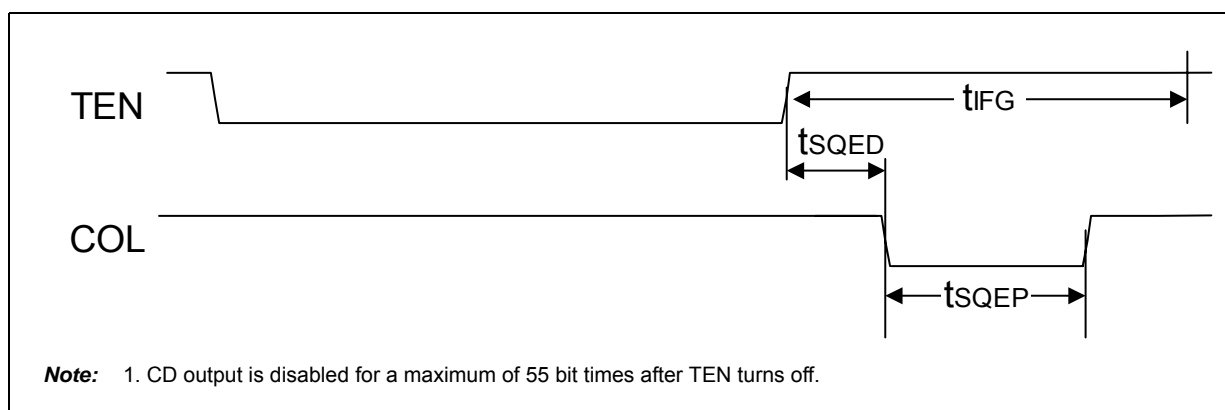


Figure 18 Mode 2 COL Output Timing



4.3 Timing Diagrams for Mode 3 (MD1 = High, MD0 = Low)

Timing diagrams for Mode 3 include Figure 19 through Figure 22.

Figure 19 Mode 3 RCLK/Start-of-Frame Timing

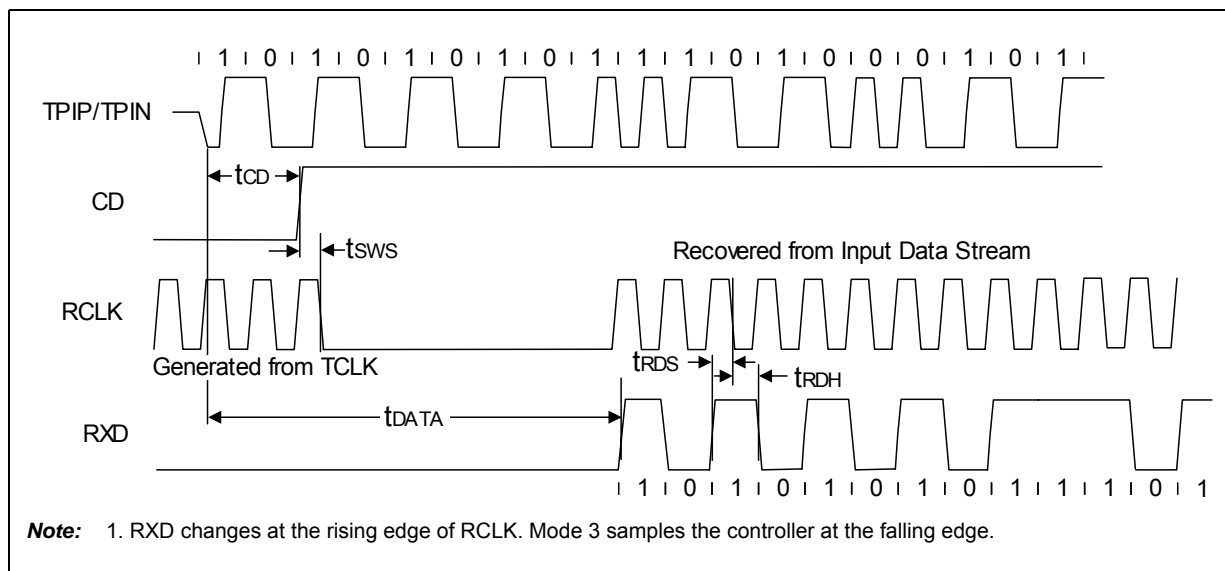


Figure 20 Mode 3 RCLK/End-of-Frame Timing

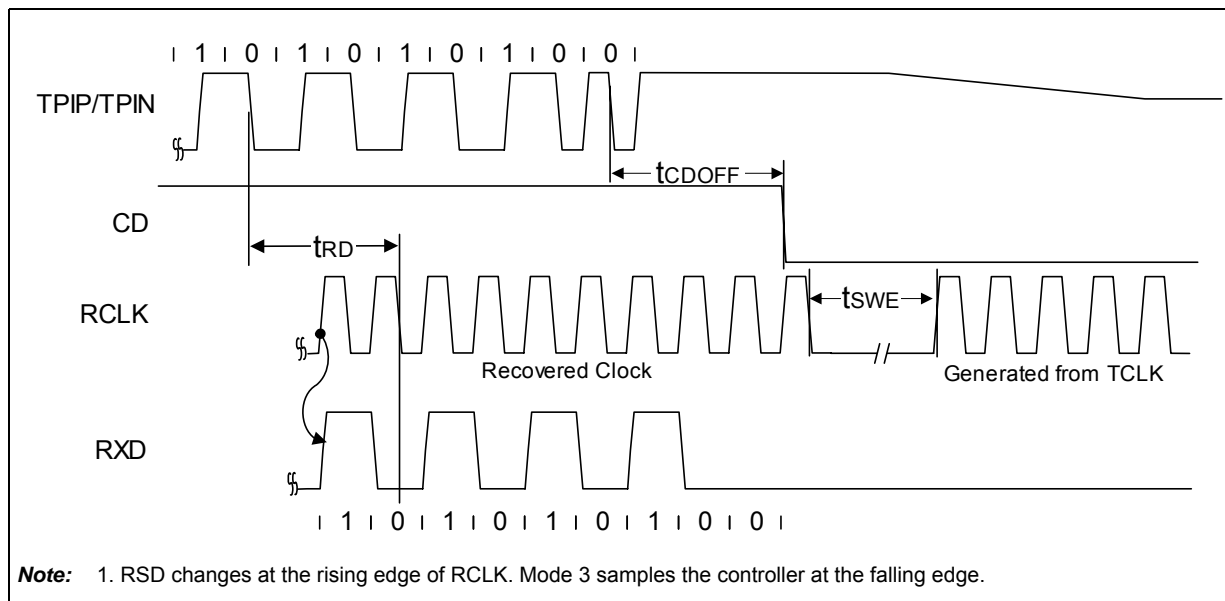


Figure 21 Mode 3 Transmit Timing

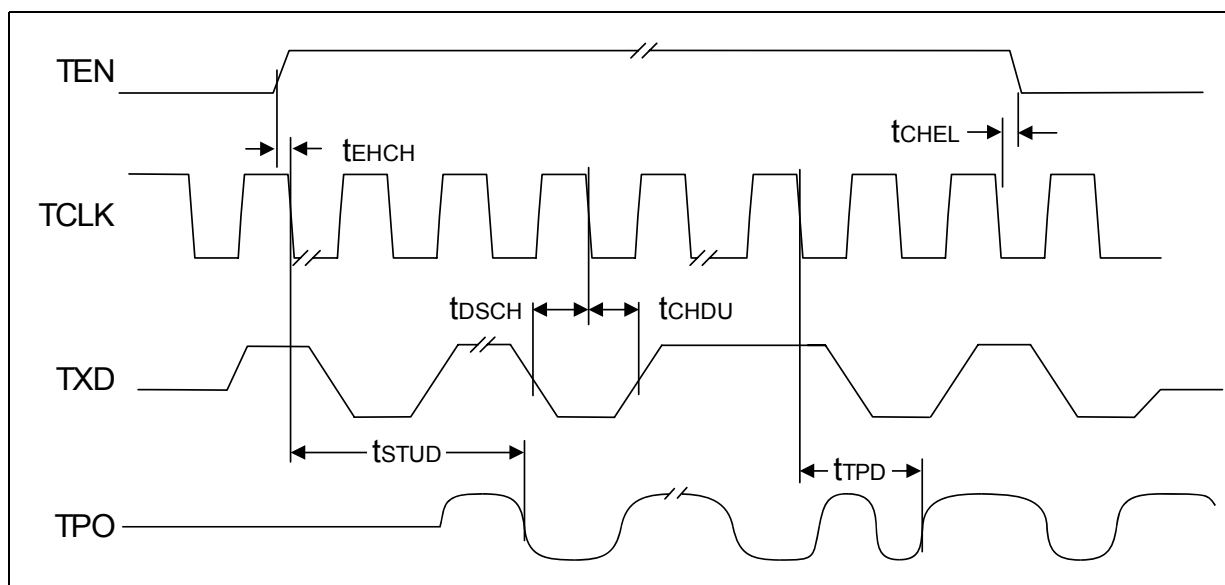
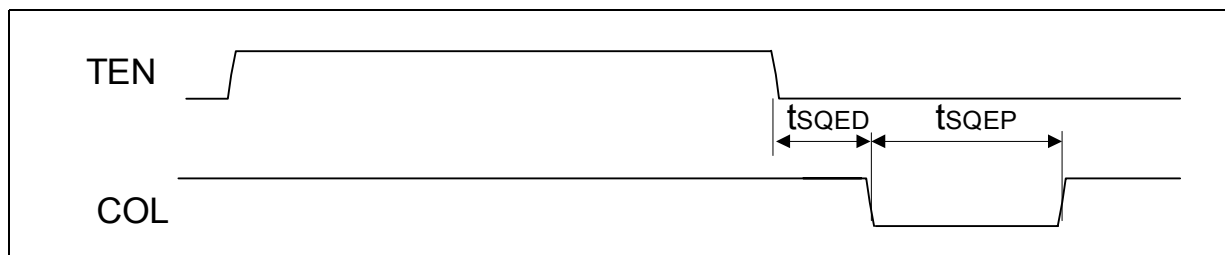


Figure 22 Mode 3 COL Output Timing



4.4 Timing Diagrams for Mode 4 (MD1 = High, MD0 = High)

Timing diagrams for Mode 4 include Figure 23 through Figure 26.

Figure 23 Mode 4 RCLK/Start-of-Frame Timing

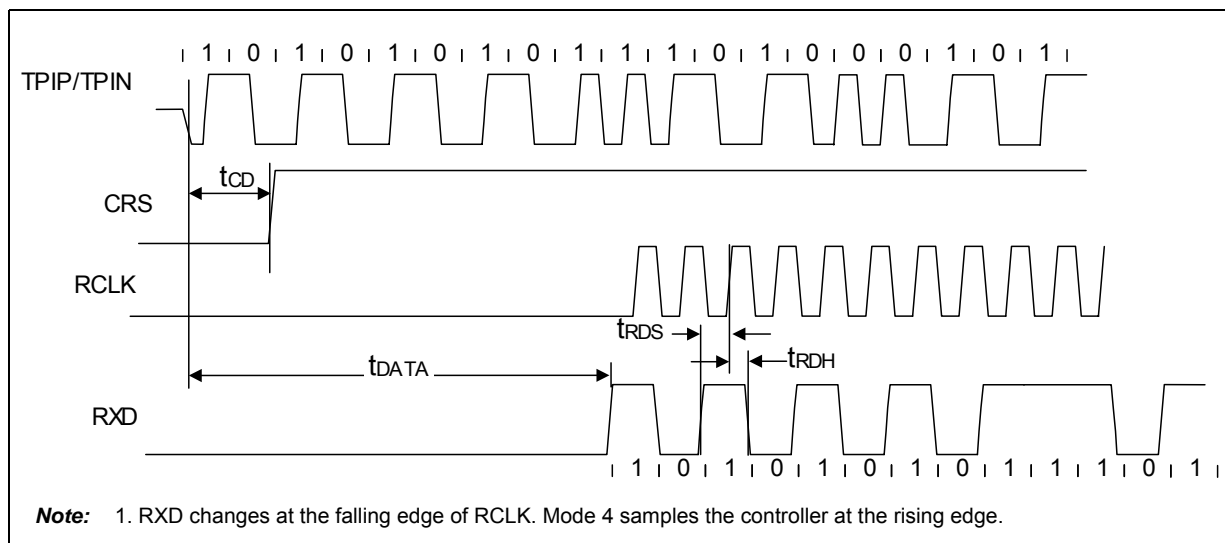


Figure 24 Mode 4 RCLK/End-of-Frame Timing

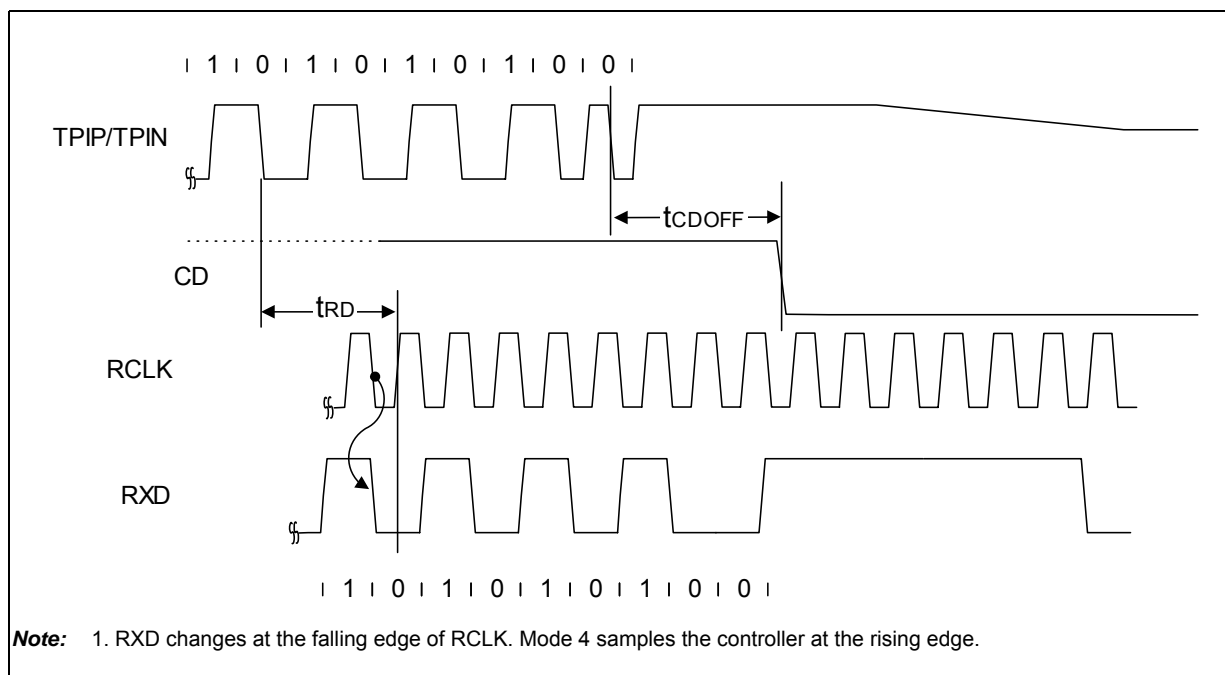


Figure 25 Mode 4 Transmit Timing

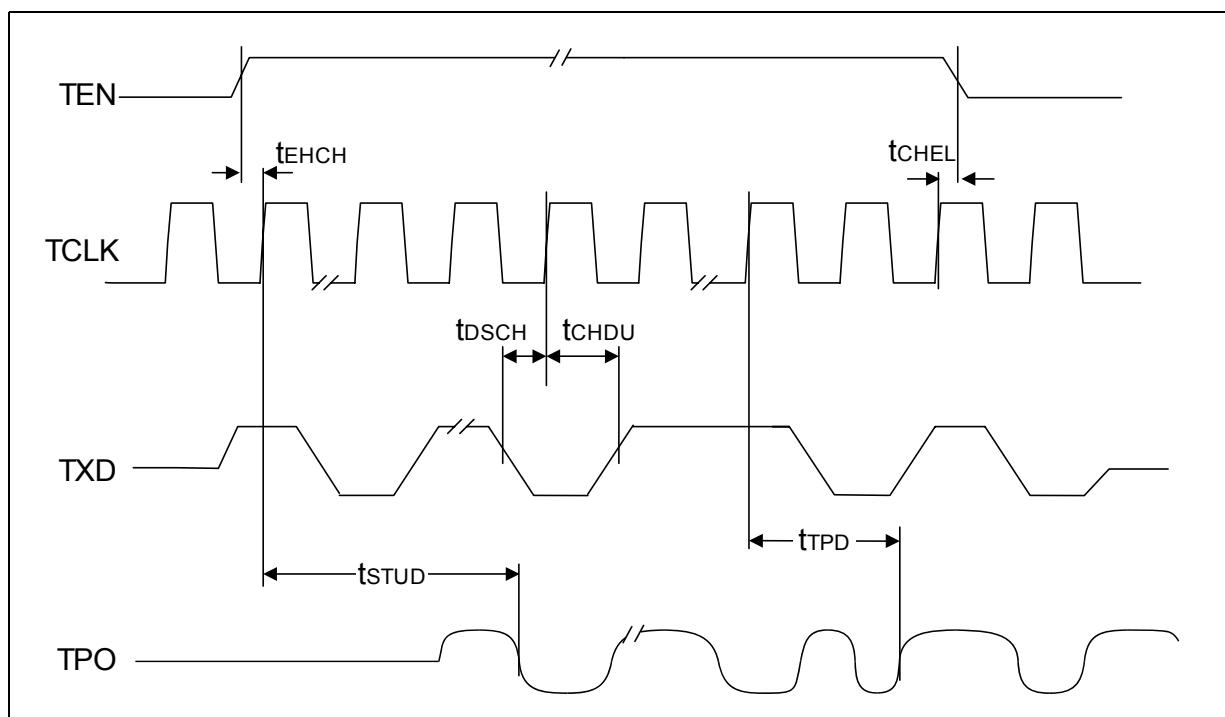
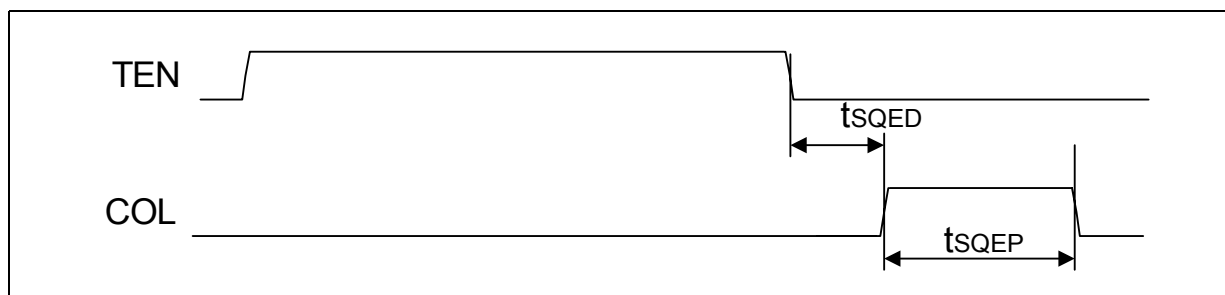


Figure 26 Mode 4 COL Output Timing

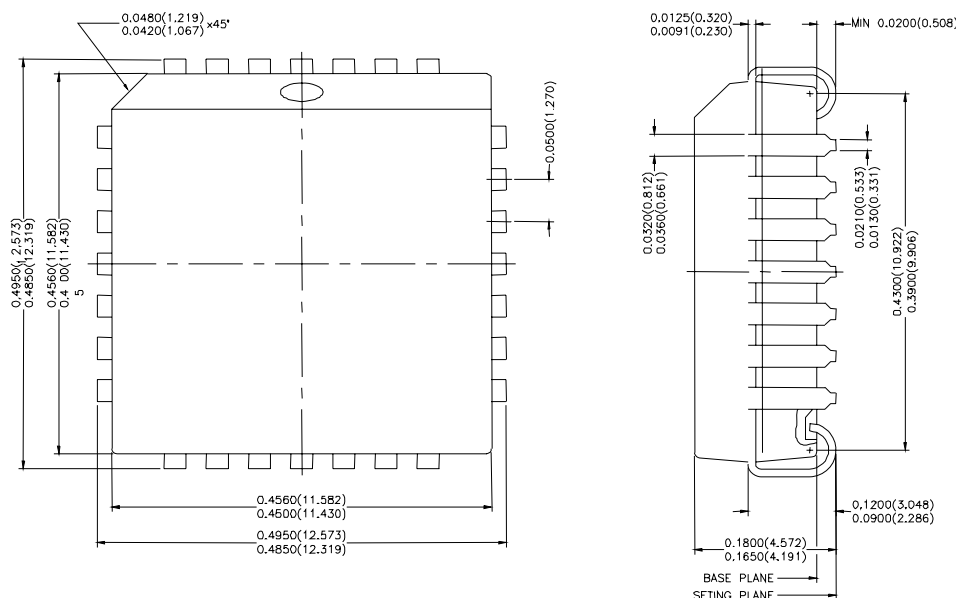


5.0 Mechanical Specifications

Figure 27 LXT905PC Package Specifications

28-Pin PLCC

- Part Number LXT905PC (Commercial Temperature Range)
- Part Number LXT905PE (Extended Temperature Range)



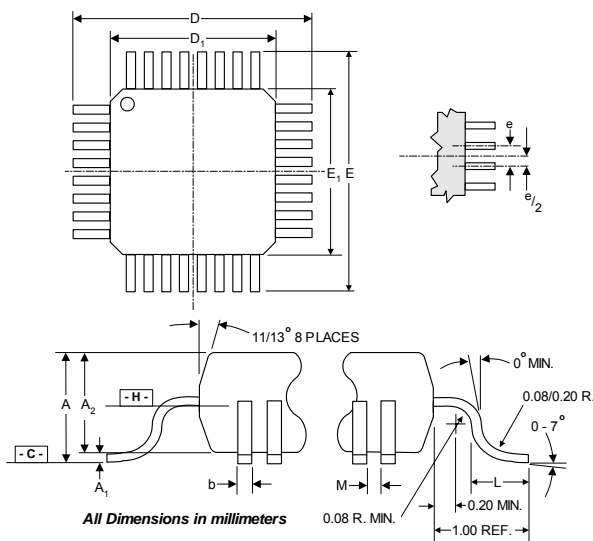
Plastic Leaded Chip Carrier

Dim	Inches		Millimeters	
	Min	Max	Min	Max
A	0.165	0.180	4.191	4.572
A ₁	0.090	0.120	2.286	3.048
A ₂	0.062	0.083	1.575	2.108
B	0.050	—	1.270	—
C	0.026	0.032	0.660	0.813
D	0.485	0.495	12.319	12.573
D ₁	0.450	0.456	11.430	11.582
F	0.013	0.021	0.330	0.533

Figure 28 LXT905LC Package Specifications

32-Pin LQFP

- Part Number LXT905LC (Commercial Temperature Range)
- Part Number LXT905LE (Extended Temperature Range)



All Dimensions in millimeters

Quad Flat Package

Dim.	All Dimensions in millimeters			
	Min.	Typ.	Max.	Notes
A	---	---	1.60	
A ₁	0.05	0.10	0.15	
A ₂	1.35	1.40	1.4	
D	9.00 BSC.			5
D ₁	7.00 BSC.			6, 7, 8
E	9.00 BSC			5
E ₁	7.00 BSC			6, 7, 8
L	0.45	0.60	0.75	
M	0.15	---	---	
b	0.30	0.37	0.45	9
e	0.80 BSC.			

Notes:

1. All dimensions are in millimeters.
2. This package conforms to JEDEC publication 95 registration MO-136, variation BC.
3. Datum plane -H- located at mold parting line and is coincident with leads where leads exit plastic body at bottom of parting line.
4. Measured at seating plane -C-.
5. Measured at datum plane -H-.
6. Dimensions D₁ and E₁ do not include mold protrusion. Allowable mold protrusion is 0.254 mm.
7. Package top dimensions are smaller than bottom dimensions. Top of package will not overhang bottom of package.
8. Dimension b does not include dambar protrusion. Allowable dambar protrusion is no more than 0.08 mm.

Contact Information

Cortina Systems, Inc.
840 W. California Ave
Sunnyvale, CA 94086

408-481-2300

sales@cortina-systems.com

apps@cortina-systems.com

www.cortina-systems.com

For additional product and ordering information:

www.cortina-systems.com

To provide comments on this document:

documentation@cortina-systems.com