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1 Block diagram and pin configuration

Figure 1. Block diagram

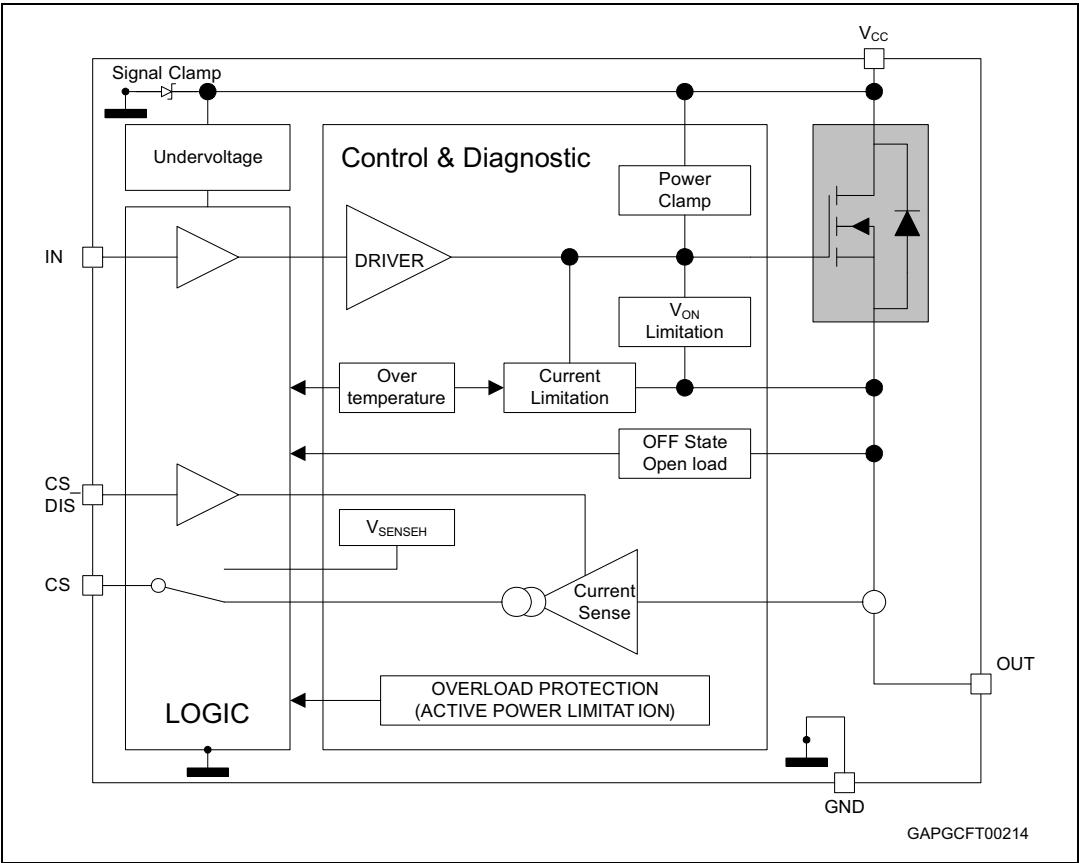


Table 1. Pin function

Name	Function
V _{CC}	Battery connection.
OUT	Power output.
GND	Ground connection. Must be reverse battery protected by an external diode/resistor network.
IN	Voltage-controlled input pin with hysteresis, CMOS compatible. Controls output switch state.
CS	Analog current sense pin, delivers a current proportional to the load current.
CS_DIS	Active high CMOS compatible pin, to disable the current sense pin.

Figure 2. Configuration diagram (top view)

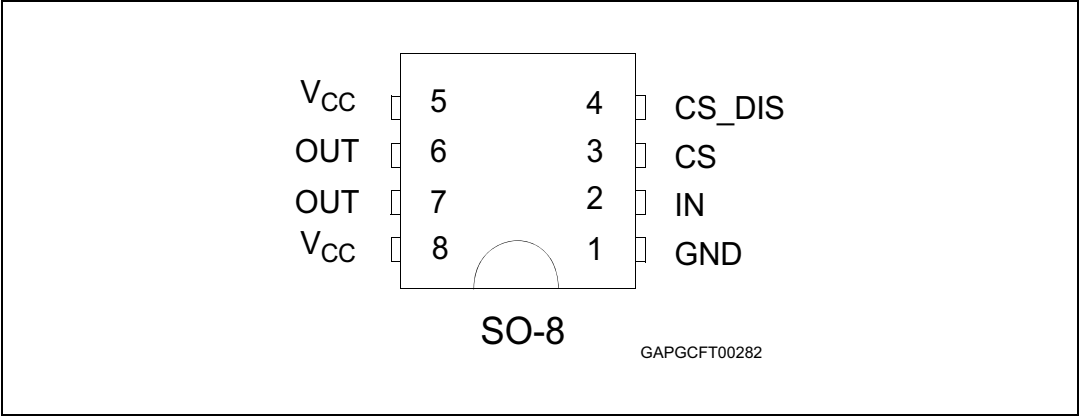
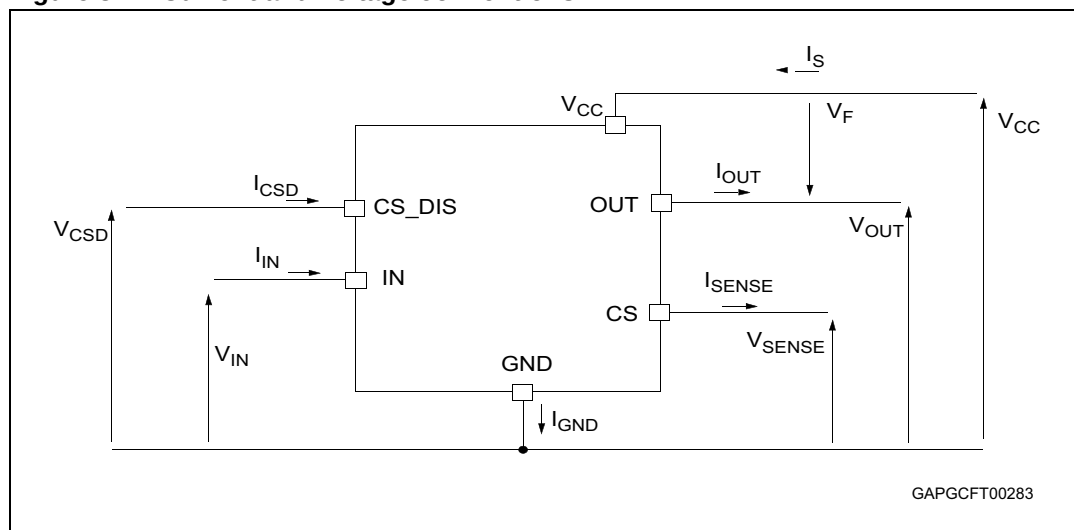


Table 2. Suggested connections for unused and not connected pins

Connection / pin	Current sense	N.C.	Output	Input	CS_DIS
Floating	Not allowed	X	X	X	X
To ground	Through 1 kΩ resistor	X	Not allowed	Through 10 kΩ resistor	Through 10 kΩ resistor

2 Electrical specifications

Figure 3. Current and voltage conventions⁽¹⁾



1. $V_F = V_{OUT} - V_{CC}$ during reverse battery condition.

2.1 Absolute maximum ratings

Stressing the device above the ratings listed in the “absolute maximum ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to the conditions in the “absolute maximum ratings” table for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE program and other relevant quality documents.

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	DC supply voltage	41	V
$-V_{CC}$	Reverse DC supply voltage	0.3	V
$-I_{GND}$	DC reverse ground pin current	200	mA
I_{OUT}	DC output current	Internally limited	A
$-I_{OUT}$	Reverse DC output current	6	A
I_{IN}	DC input current	-1 to 10	mA
I_{CSD}	DC current sense disable input current	-1 to 10	mA
$-I_{CSENSE}$	DC reverse CS pin current	200	mA
V_{CSENSE}	Current sense maximum voltage	$V_{CC} - 41$ $+V_{CC}$	V V

Table 3. Absolute maximum ratings (continued)

Symbol	Parameter	Value	Unit
E_{MAX}	Maximum switching energy (single pulse) ($L = 8\text{ mH}$; $R_L = 0\ \Omega$; $V_{bat} = 13.5\text{ V}$; $T_{jstart} = 150\text{ }^{\circ}\text{C}$; $I_{OUT} = I_{limL}(Typ.)$)	36	mJ
V_{ESD}	Electrostatic discharge (human body model: $R = 1.5\text{ K}\Omega$; $C = 100\text{ pF}$)		
	– IN	4000	V
	– CS	2000	V
	– CS_DIS	4000	V
	– OUT	5000	V
	– V_{CC}	5000	V
V_{ESD}	Charge device model (CDM-AEC-Q100-011)	750	V
T_j	Junction operating temperature	-40 to 150	$^{\circ}\text{C}$
T_{stg}	Storage temperature	-55 to 150	$^{\circ}\text{C}$

2.2 Thermal data

Table 4. Thermal data

Symbol	Parameter	Max value	Unit
$R_{thj-pins}$	Thermal resistance junction-pins	30	$^{\circ}\text{C/W}$
$R_{thj-amb}$	Thermal resistance junction-ambient	See Figure 36	$^{\circ}\text{C/W}$

2.3 Electrical characteristics

Values specified in this section are for $8\text{ V} < V_{CC} < 28\text{ V}$; $-40\text{ °C} < T_j < 150\text{ °C}$, unless otherwise stated.

Table 5. Power section

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{CC}	Operating supply voltage		4.5	13	28	V
V_{USD}	Undervoltage shut-down			3.5	4.5	V
$V_{USDhyst}$	Undervoltage shut-down hysteresis			0.5		V
R_{ON}	ON-state resistance	$I_{OUT} = 1\text{ A}$, $T_j = 25\text{ °C}$			160	mΩ
		$I_{OUT} = 1\text{ A}$, $T_j = 150\text{ °C}$			320	
		$I_{OUT} = 1\text{ A}$, $V_{CC} = 5\text{ V}$, $T_j = 25\text{ °C}$			210	
V_{clamp}	Voltage clamp	$I_S = 20\text{ mA}$	41	46	52	V
I_S	Supply current	OFF-state: $V_{CC} = 13\text{ V}$, $V_{IN} = V_{OUT} = 0\text{ V}$, $T_j = 25\text{ °C}$		2 ⁽¹⁾	5 ⁽¹⁾	μA
		ON-state: $V_{IN} = 5\text{ V}$, $V_{CC} = 13\text{ V}$, $I_{OUT} = 0\text{ A}$		1.9	3.5	mA
$I_{L(off1)}$	OFF-state output current	$V_{IN} = V_{OUT} = 0\text{ V}$, $V_{CC} = 13\text{ V}$, $T_j = 25\text{ °C}$	0	0.01	3	μA
		$V_{IN} = V_{OUT} = 0\text{ V}$, $V_{CC} = 13\text{ V}$, $T_j = 125\text{ °C}$	0		5	
V_F	Output - V_{CC} diode voltage	$-I_{OUT} = 1\text{ A}$, $T_j = 150\text{ °C}$			0.7	V

1. PowerMOS leakage included.

Table 6. Switching ($V_{CC} = 13\text{ V}$; $T_j = 25\text{ °C}$)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$R_L = 13\text{ Ω}$ (see Figure 6)	—	10	—	μs
$t_{d(off)}$	Turn-off delay time	$R_L = 13\text{ Ω}$ (see Figure 6)	—	10	—	μs
$dV_{OUT}/dt_{(on)}$	Turn-on voltage slope	$R_L = 13\text{ Ω}$	—	See Figure 26	—	V/μs
$dV_{OUT}/dt_{(off)}$	Turn-off voltage slope	$R_L = 13\text{ Ω}$	—	See Figure 28	—	V/μs
W_{ON}	Switching energy losses during t_{won}	$R_L = 13\text{ Ω}$ (see Figure 6)	—	0.05	—	mJ
W_{OFF}	Switching energy losses during t_{woff}	$R_L = 13\text{ Ω}$ (see Figure 6)	—	0.03	—	mJ

Table 7. Logic inputs

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IL}	Low-level input voltage				0.9	V
I_{IL}	Low-level input current	$V_{IN} = 0.9\text{ V}$	1			μA
V_{IH}	High-level input voltage		2.1			V
I_{IH}	High-level input current	$V_{IN} = 2.1\text{ V}$			10	μA
$V_{I(hyst)}$	Hysteresis input voltage		0.25			V
V_{ICL}	Input voltage clamp	$I_{IN} = 1\text{ mA}$	5.5		7	V
		$I_{IN} = -1\text{ mA}$		-0.7		
V_{CSDL}	Low-level CS_DIS voltage				0.9	V
I_{CSDL}	Low-level CS_DIS current	$V_{CSD} = 0.9\text{ V}$	1			μA
V_{CSDH}	High-level CS_DIS voltage		2.1			V
I_{CSDH}	High-level CS_DIS current	$V_{CSD} = 2.1\text{ V}$			10	μA
$V_{CSD(hyst)}$	Hysteresis CS_DIS voltage		0.25			V
V_{CSCL}	CS_DIS voltage clamp	$I_{CSD} = 1\text{ mA}$	5.5		7	V
		$I_{CSD} = -1\text{ mA}$		-0.7		

Table 8. Protection and diagnostics⁽¹⁾

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{limH}	DC short-circuit current	$V_{CC} = 13\text{ V}$	7	10	14	A
		$5\text{ V} < V_{CC} < 28\text{ V}$			14	A
I_{limL}	Short-circuit current during thermal cycling	$V_{CC} = 13\text{ V}$ $T_R < T_J < T_{TSD}$		2.5		A
T_{TSD}	Shutdown temperature		150	175	200	$^{\circ}\text{C}$
T_R	Reset temperature		$T_{RS} + 1$	$T_{RS} + 5$		$^{\circ}\text{C}$
T_{RS}	Thermal reset of STATUS		135			$^{\circ}\text{C}$
T_{HYST}	Thermal hysteresis ($T_{TSD} - T_R$)			7		$^{\circ}\text{C}$
V_{DEMAG}	Turn-off output voltage clamp	$I_{OUT} = 1\text{ A}$, $V_{IN} = 0$, $L = 20\text{ mH}$	$V_{CC} - 41$	$V_{CC} - 46$	$V_{CC} - 52$	V
V_{ON}	Output voltage drop limitation	$I_{OUT} = 0.03\text{ A}$ (see Figure 8) $T_J = -40\text{ }^{\circ}\text{C}$ to $+150\text{ }^{\circ}\text{C}$		25		mV

1. To ensure long term reliability under heavy overload or short circuit conditions, protection and related diagnostic signals must be used together with a proper software strategy. If the device is subjected to abnormal conditions, this software must limit the duration and number of activation cycles.

Table 9. Current sense (8 V < V_{CC} < 18 V)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
K ₀	I _{OUT} /I _{SENSE}	I _{OUT} = 0.025 A, V _{SENSE} = 0.5 V T _j = -40 °C to 150 °C	265	490	715	
K ₁	I _{OUT} /I _{SENSE}	I _{OUT} = 0.35 A, V _{SENSE} = 0.5 V T _j = -40 °C to 150 °C T _j = 25 °C to 150 °C	355 385	465 465	575 545	
dK ₁ /K ₁ ⁽¹⁾	Current sense ratio drift	I _{OUT} = 0.35 A, V _{SENSE} = 0.5 V T _j = -40 °C to 150 °C	-11		+11	%
K ₂	I _{OUT} /I _{SENSE}	I _{OUT} = 0.5 A, V _{SENSE} = 4 V T _j = -40 °C to 150 °C T _j = 25 °C to 150 °C	380 400	455 455	530 510	
dK ₂ /K ₂ ⁽¹⁾	Current sense ratio drift	I _{OUT} = 0.5 A; T _j = -40 °C to 150 °C	-8		+8	%
K ₃	I _{OUT} /I _{SENSE}	I _{OUT} = 1.5 A, V _{SENSE} = 4 V T _j = -40 °C to 150 °C T _j = 25 °C to 150 °C	420 420	455 455	490 480	
dK ₃ /K ₃ ⁽¹⁾	Current sense ratio drift	I _{OUT} = 1.5 A; T _j = -40 °C to 150 °C	-4		+4	%
I _{SENSE0}	Analog sense leakage current	I _{OUT} = 0 A, V _{SENSE} = 0 V, V _{CSD} = 5 V, V _{IN} = 0 V, T _j = -40 °C to 150 °C	0		1	μA
		I _{OUT} = 0 A, V _{SENSE} = 0 V, V _{CSD} = 0 V, V _{IN} = 5 V, T _j = -40 °C to 150 °C	0		2	
		I _{OUT} = 1 A, V _{SENSE} = 0 V, V _{CSD} = 5 V, V _{IN} = 5 V, T _j = -40 °C to 150 °C	0		1	
V _{SENSE}	Max analog sense output voltage	R _{SENSE} = 10 KΩ I _{OUT} = 1 A;	5			V
V _{SENSEH} ⁽²⁾	Analog sense output voltage in fault condition	V _{CC} = 13 V, R _{SENSE} = 3.9 KΩ		8		V
I _{SENSEH} ⁽²⁾	Analog sense output current in fault condition	V _{CC} = 13 V, V _{SENSE} = 5 V		9		mA
t _{DSENSE1H}	Delay response time from falling edge of CS_DIS pin	V _{SENSE} < 4 V, 0.025 A < I _{OUT} < 1.5 A I _{SENSE} = 90% of I _{SENSE max} (see Figure 4)		40	100	μs
t _{DSENSE1L}	Delay response time from rising edge of CS_DIS pin	V _{SENSE} < 4 V, 0.025 A < I _{OUT} < 1.5 A I _{SENSE} = 10% of I _{SENSE max} (see Figure 4)		5	20	μs

Table 9. Current sense (8 V < V_{CC} < 18 V) (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t _{DSENSE2H}	Delay response time from rising edge of IN pin	V _{SENSE} < 4 V, 0.025 A < I _{OUT} < 1.5 A I _{SENSE} =90% of I _{SENSE max} (see Figure 4)		30	160	μs
Δt _{DSENSE2H}	Delay response time between rising edge of output current and rising edge of current sense	V _{SENSE} < 4 V, I _{SENSE} = 90% of I _{SENSEMAX} , I _{OUT} = 90% of I _{OUTMAX} I _{OUTMAX} =1.5A (see Figure 7)			110	μs
t _{DSENSE2L}	Delay response time from falling edge of IN pin	V _{SENSE} < 4 V, 0.025 A < I _{OUT} < 1.5 A I _{SENSE} =10% of I _{SENSE max} (see Figure 4)		80	250	μs

1. Parameter guaranteed by design; it is not tested.
2. Fault condition includes: power limitation, overtemperature and open load OFF-state detection.

Table 10. Openload detection (8 V < V_{CC} < 18 V)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{OL}	OFF-state open-load voltage detection threshold	V _{IN} = 0 V, 8 V < V _{CC} < 18 V	2		4	V
I _{OL}	ON-state open-load current detection threshold	V _{IN} = 5V, 8 V < V _{CC} < 18 V I _{SENSE} = 5 μA	0.5		5	mA
t _{DSTKON}	Output short-circuit to V _{CC} detection delay at turn-off	See Figure 5	180		1200	μs
I _{L(off2)r}	OFF-state output current at V _{OUT} = 4 V	V _{IN} = 0 V, V _{SENSE} = 0 V V _{OUT} rising from 0 V to 4 V	-120		0	μA
I _{L(off2)f}	OFF-state output current at V _{OUT} = 2 V	V _{IN} = 0 V, V _{SENSE} = V _{SENSEH} V _{OUT} falling from V _{CC} to 2 V	-50		90	
td_vol	Delay response from output rising edge to V _{SENSE} rising edge in open-load	V _{OUT} = 4 V, V _{IN} = 0 V V _{SENSE} = 90% of V _{SENSEH}			20	μs

Figure 4. Current sense delay characteristics

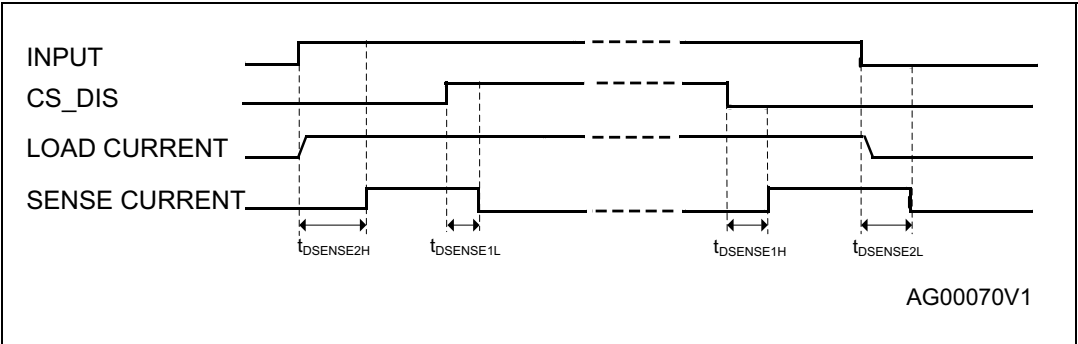


Figure 5. OFF-state open-load delay timing

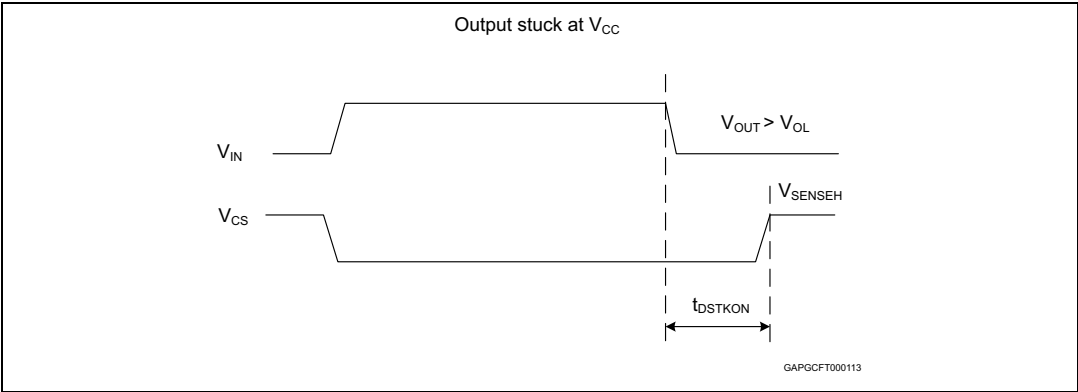


Figure 6. Switching characteristics

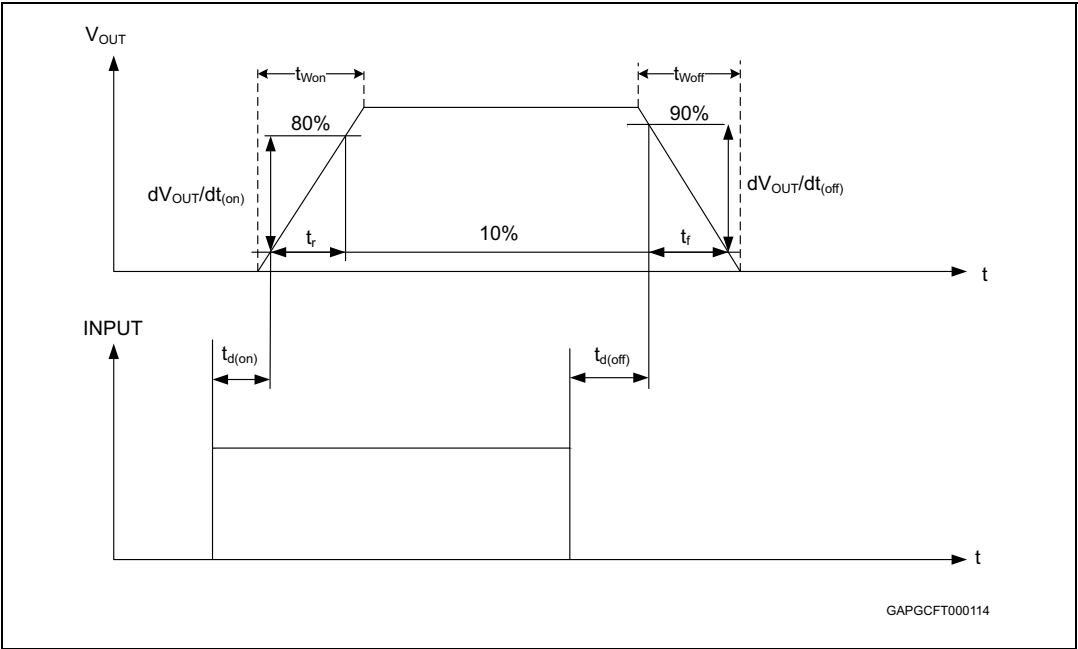


Figure 7. Delay response time between rising edge of ouput current and rising edge of current sense (CS enabled)

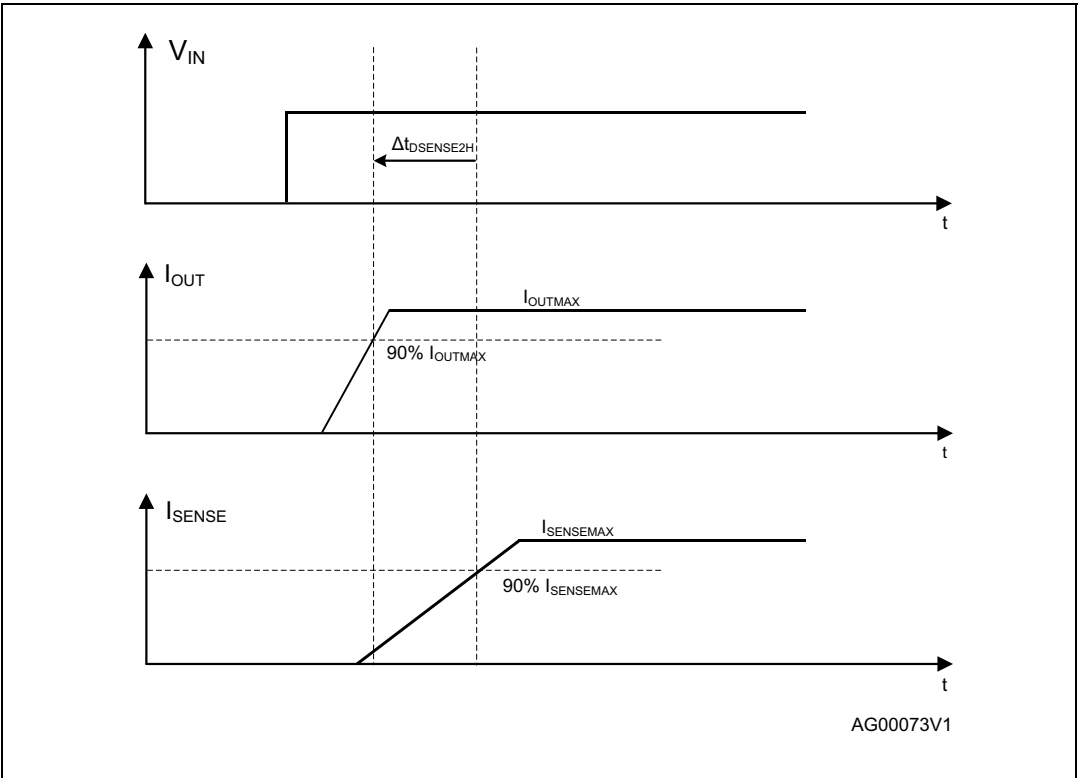


Figure 8. Output voltage drop limitation

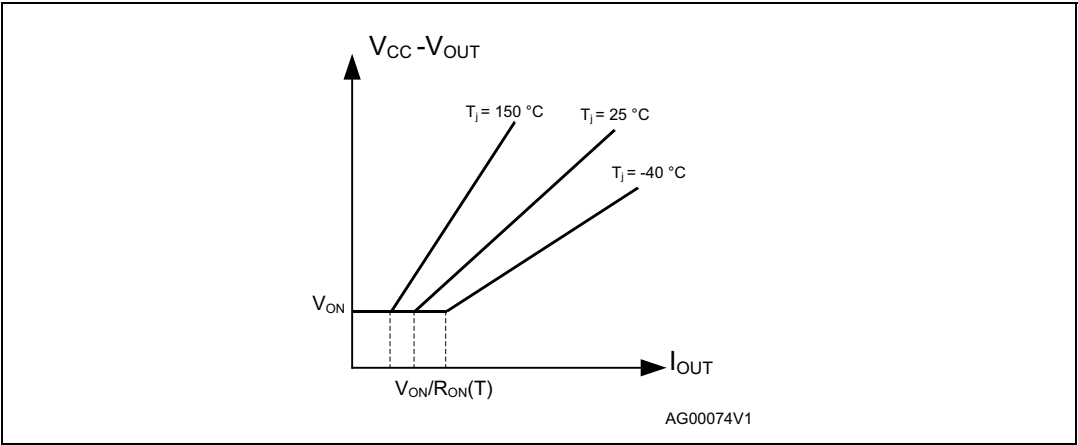
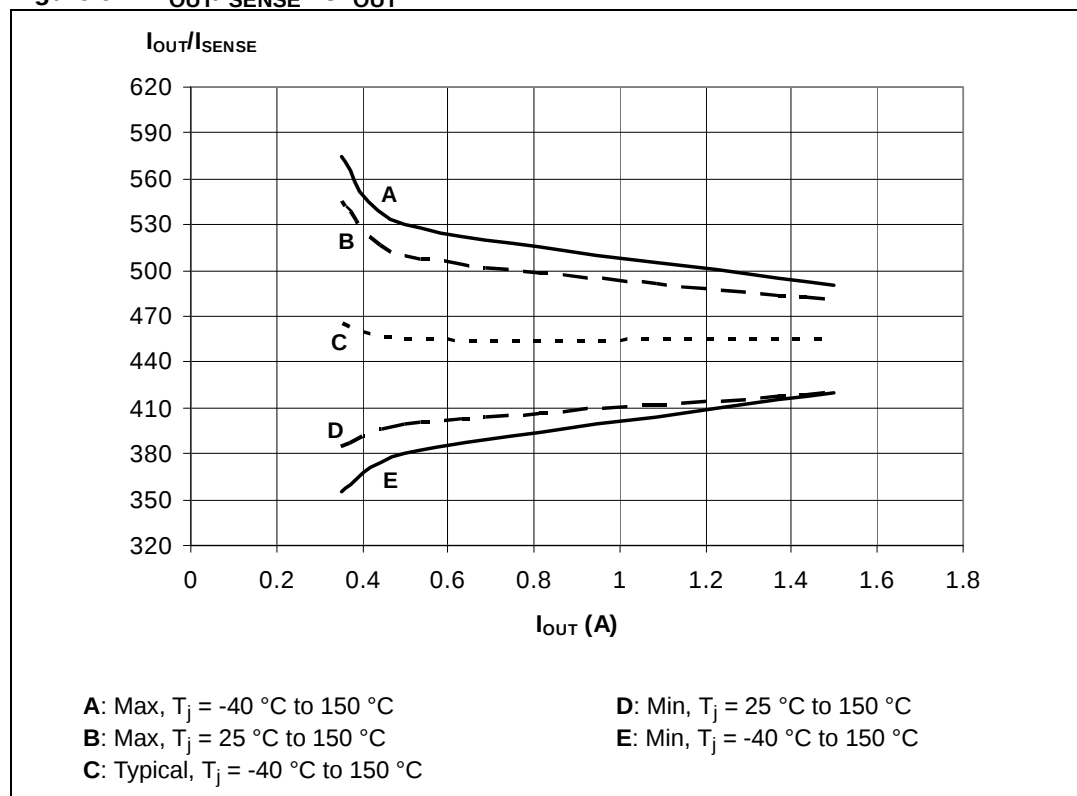
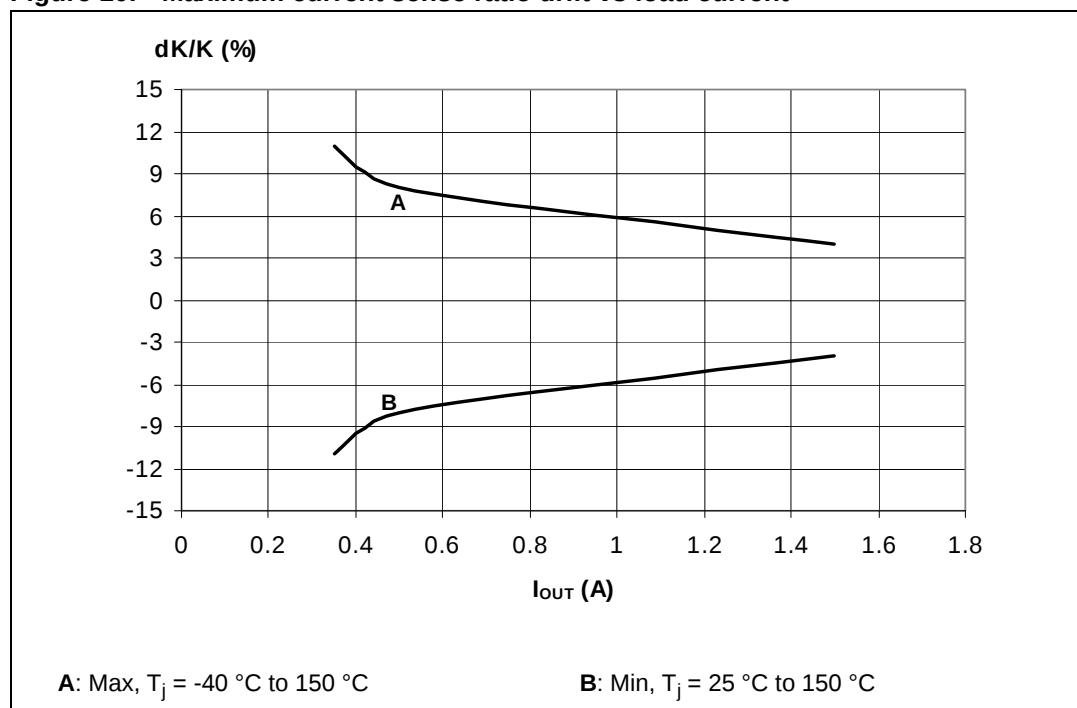


Figure 9. I_{OUT}/I_{SENSE} vs I_{OUT} Figure 10. Maximum current sense ratio drift vs load current⁽¹⁾

1. Parameter guaranteed by design; it is not tested.

Table 11. Truth table

Conditions	IN	OUT	SENSE ($V_{CSD} = 0\text{ V}$) ⁽¹⁾
Normal operation	L	L	0
	H	H	Nominal
Overtemperature	L	L	0
	H	L	V_{SENSEH}
Undervoltage	L	L	0
	H	L	0
Overload	H	X (no power limitation)	Nominal
	H	Cycling (power limitation)	V_{SENSEH}
Short circuit to GND (Power limitation)	L	L	0
	H	L	V_{SENSEH}
OFF-state open-load (with external pull-up)	L	H	V_{SENSEH}

1. If the V_{CSD} is high, the SENSE output is at a high impedance, its potential depends on leakage currents and external circuit.

Table 12. Electrical transient requirements (part 1)

ISO 7637-2: 2004(E) Test pulse	Test levels ⁽¹⁾		Number of pulses or test times	Burst cycle/pulse repetition time		Delays and Impedance
	III	IV				
1	-75 V	-100 V	5000 pulses	0.5 s	5 s	2 ms, 10 Ω
2a	+37 V	+50 V	5000 pulses	0.2 s	5 s	50 μ s, 2 Ω
3a	-100 V	-150 V	1h	90 ms	100 ms	0.1 μ s, 50 Ω
3b	+75 V	+100 V	1h	90 ms	100 ms	0.1 μ s, 50 Ω
4	-6 V	-7 V	1 pulse			100 ms, 0.01 Ω
5b ⁽²⁾	+65 V	+87 V	1 pulse			400 ms, 2 Ω

Table 13. Electrical transient requirements (part 2)

ISO 7637-2: 2004(E) Test pulse	Test level results ⁽¹⁾	
	III	IV
1	C	C
2a	C	C
3a	C	C
3b	C	C
4	C	C
5b ⁽²⁾	C	C

1. The above test levels must be considered referred to $V_{CC} = 13.5$ V except for pulse 5b

2. Valid in case of external load dump clamp: 40 V maximum referred to ground.

Table 14. Electrical transient requirements (part 3)

Class	Contents
C	All functions of the device are performed as designed after exposure to disturbance.
E	One or more functions of the device are not performed as designed after exposure to disturbance and cannot be returned to proper operation without replacing the device.

2.4 Waveforms

Figure 11. Normal operation

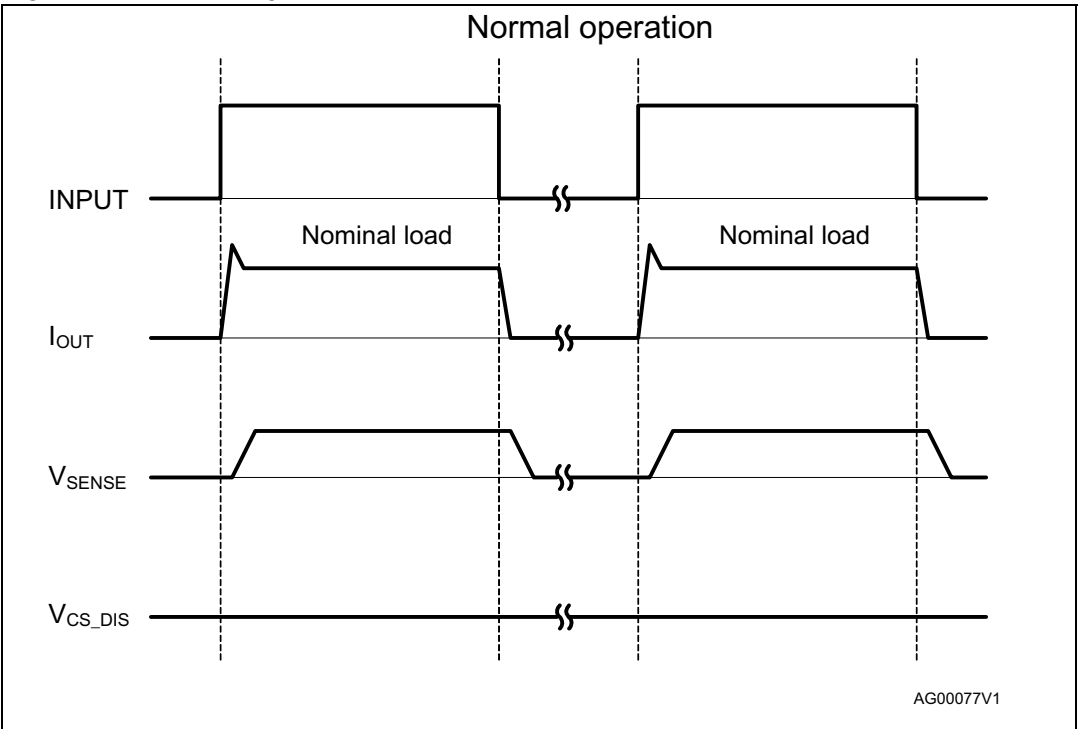


Figure 12. Overload or short to GND

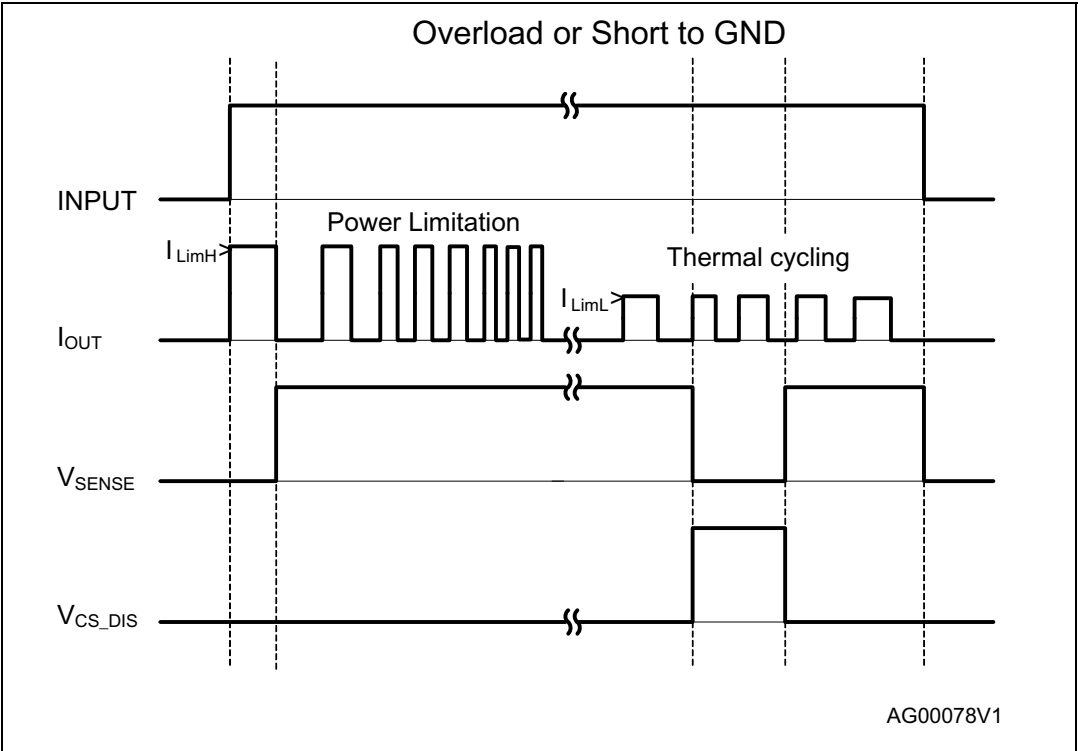


Figure 13. Intermittent overload

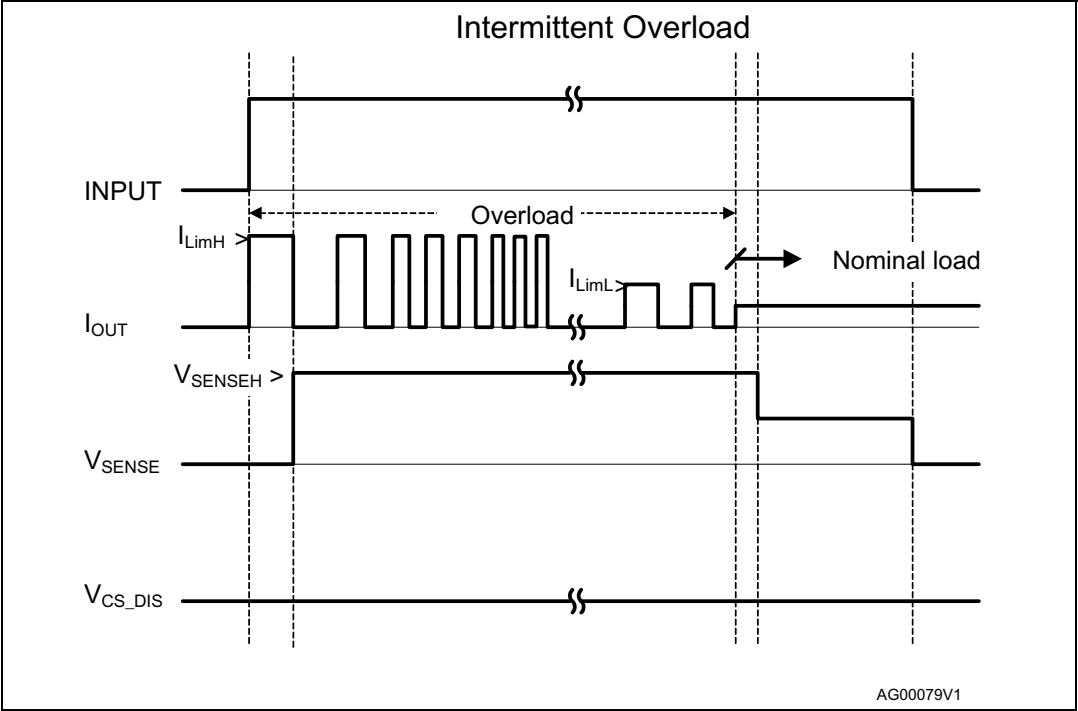


Figure 14. OFF-state open-load with external circuitry

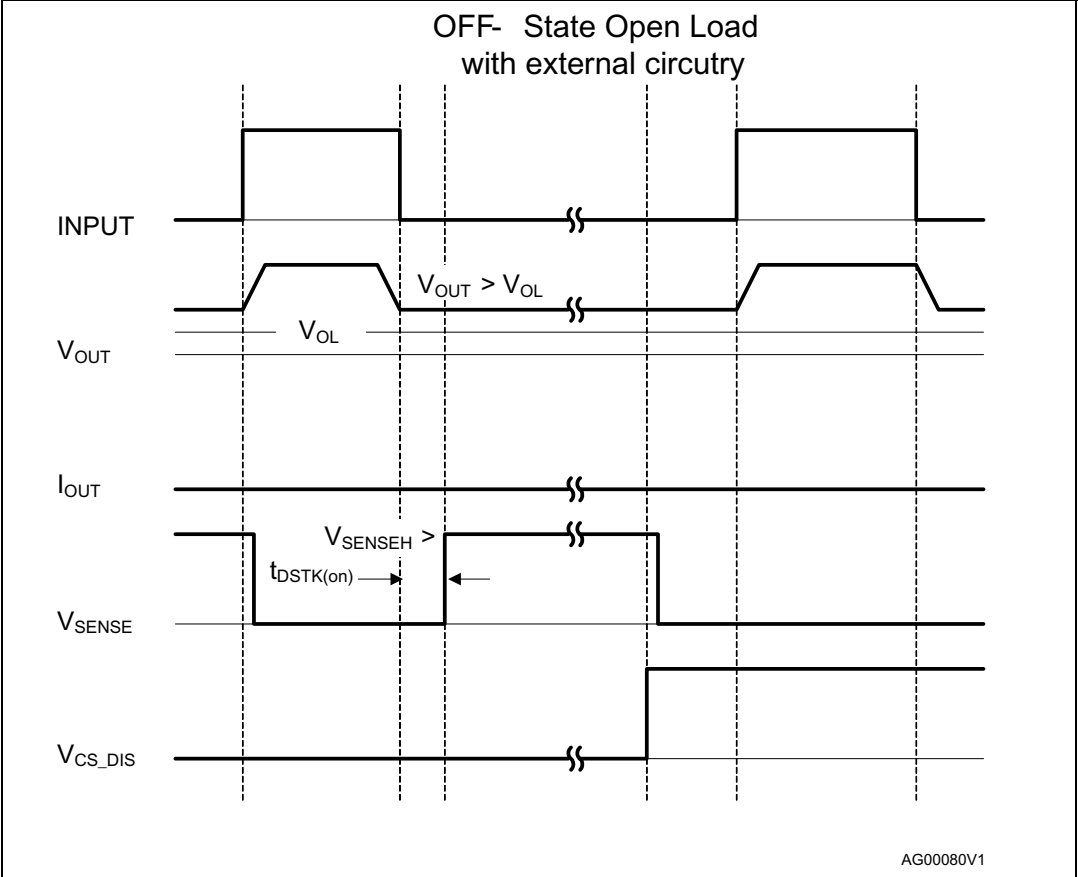


Figure 15. Short to V_{CC}

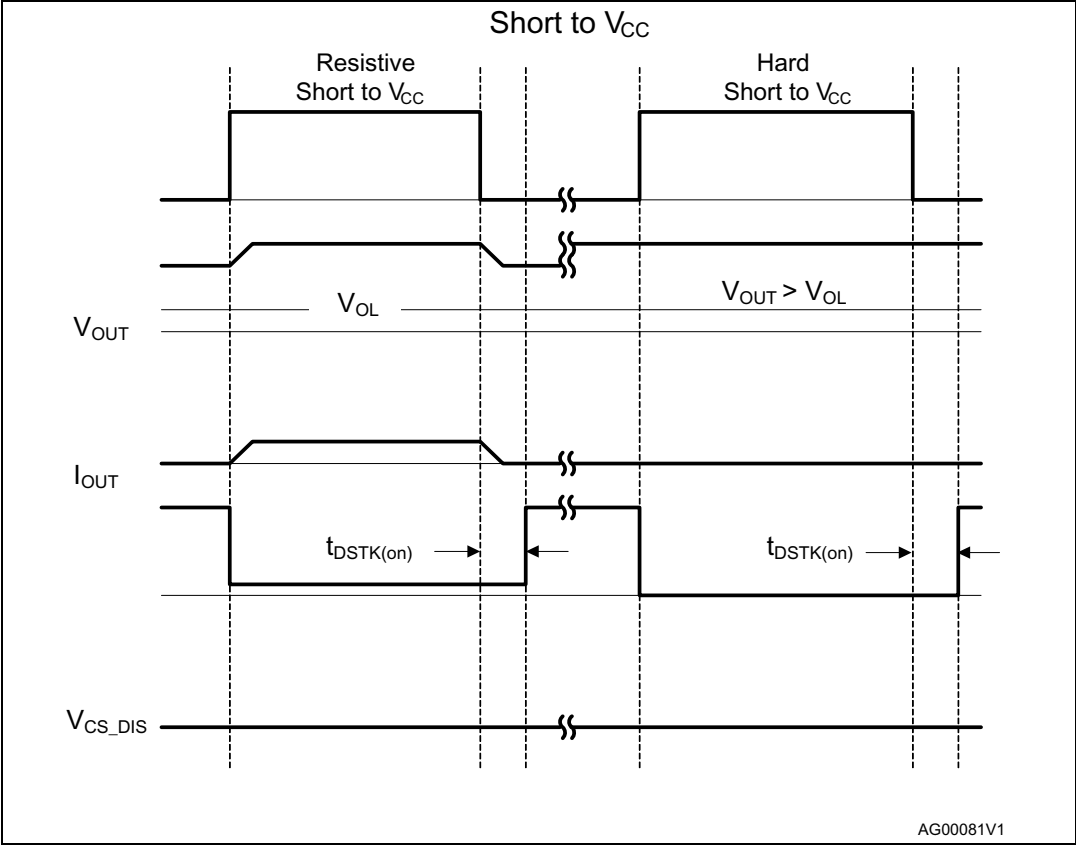
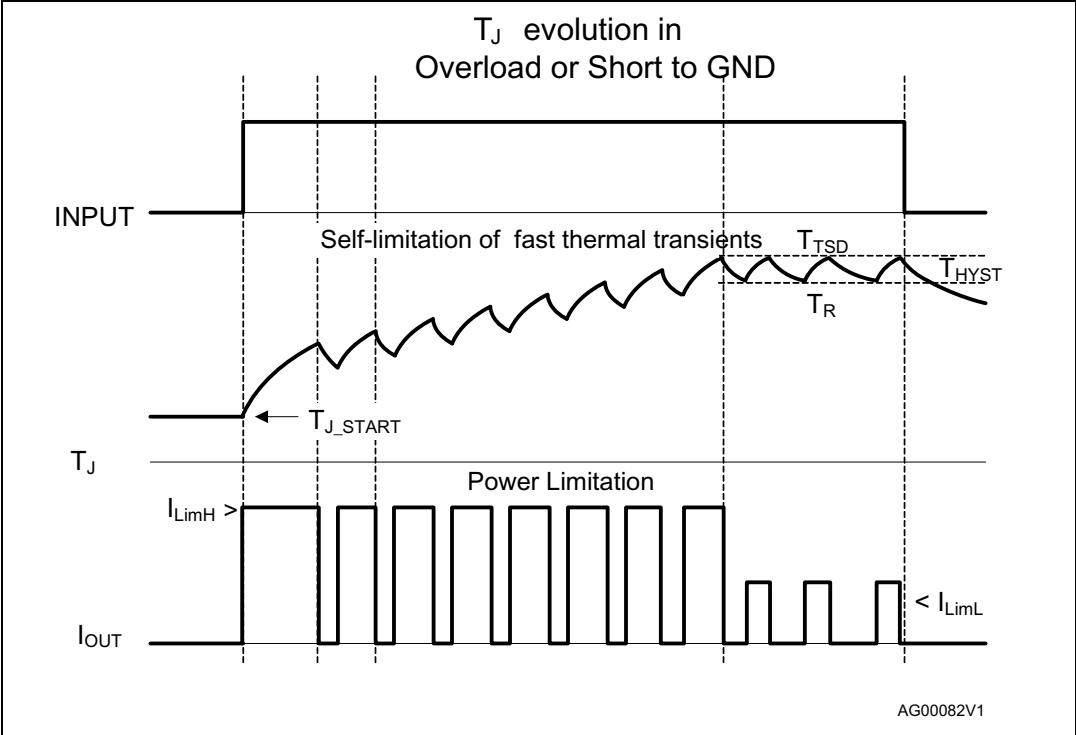


Figure 16. T_J evolution in overload or short to GND



2.5 Electrical characteristics curves

Figure 17. OFF-state output current

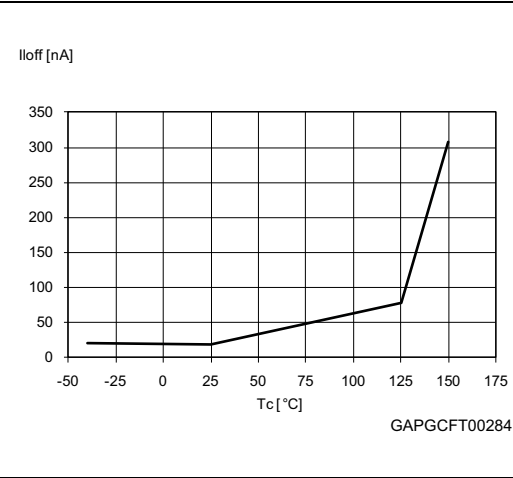


Figure 18. High-level input current

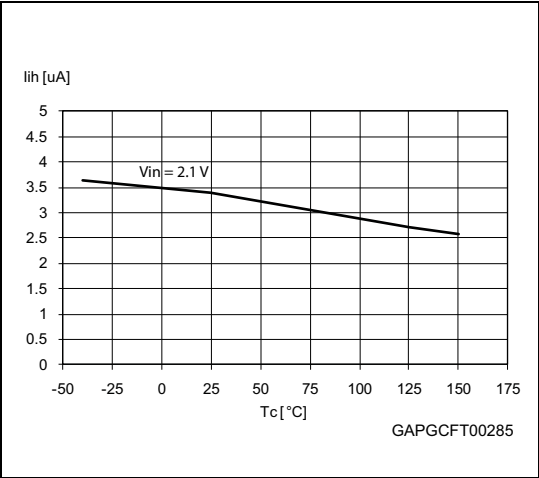


Figure 19. Input voltage clamp

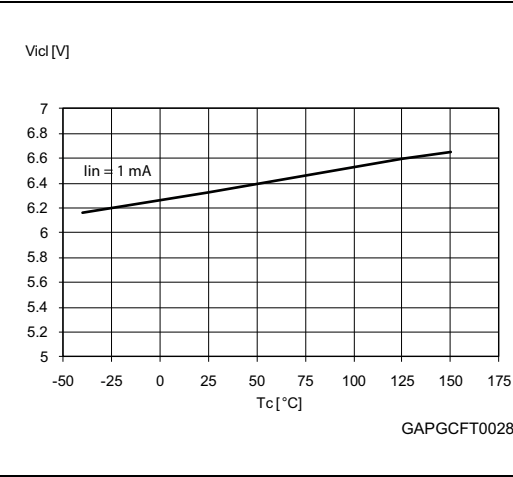


Figure 20. Low-level input voltage

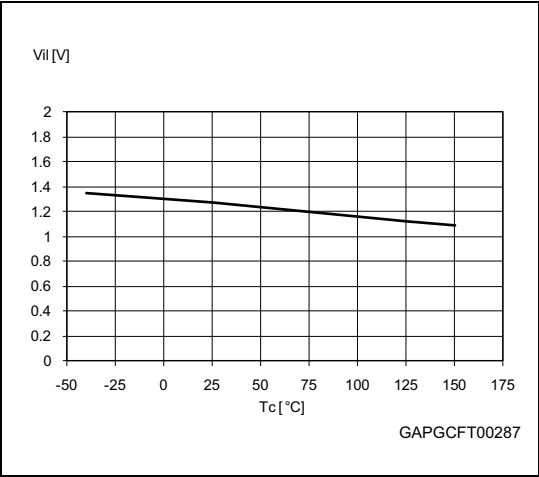


Figure 21. High-level input voltage

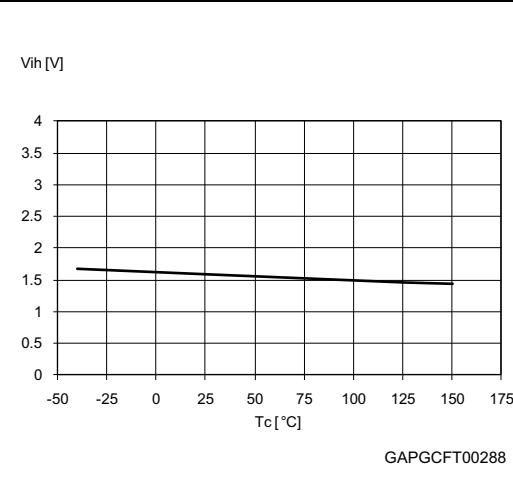


Figure 22. Hysteresis input voltage

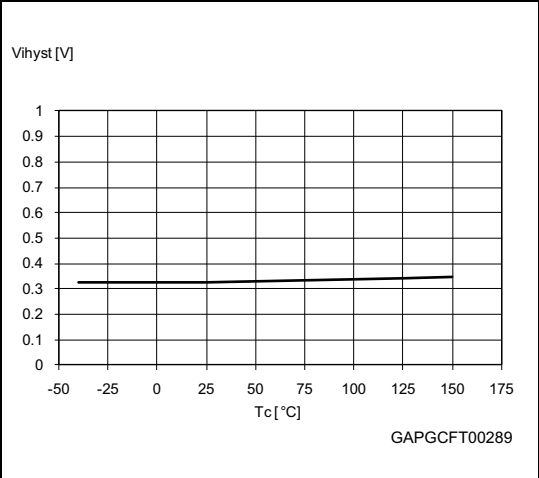


Figure 23. ON-state resistance vs. T_{case}

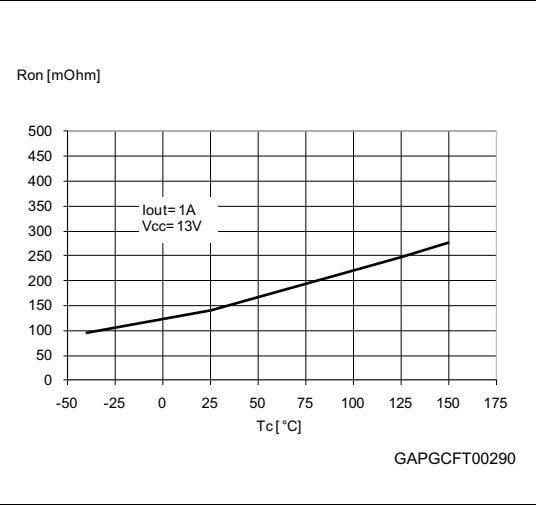


Figure 24. ON-state resistance vs. V_{CC}

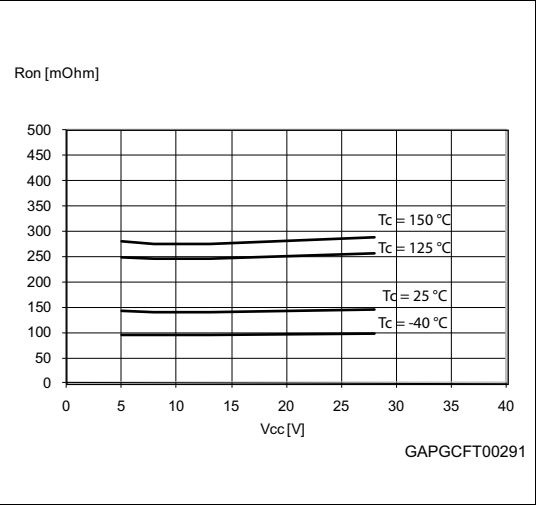


Figure 25. Undervoltage shutdown

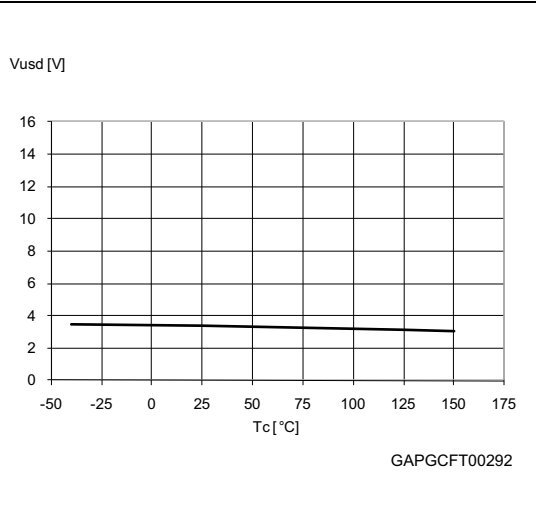


Figure 26. Turn-on voltage slope

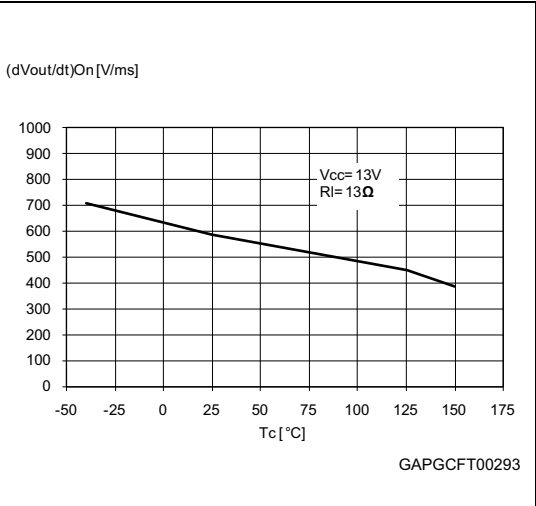


Figure 27. I_{LIMH} vs. T_{case}

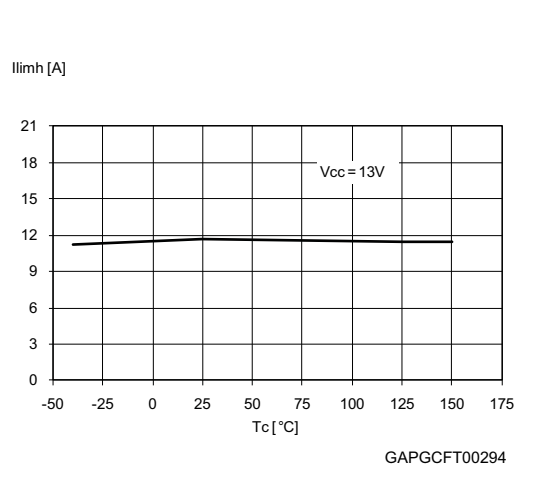


Figure 28. Turn-off voltage slope

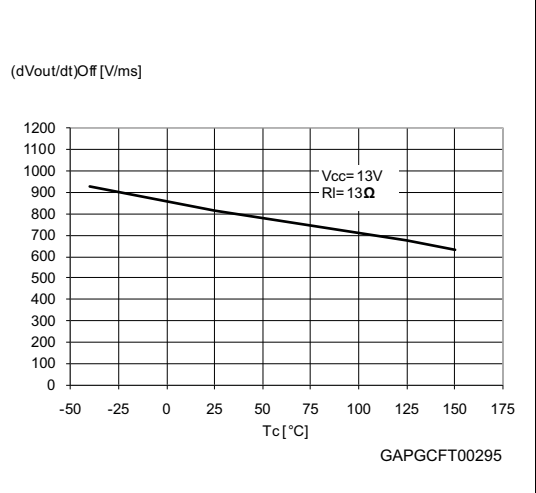


Figure 29. High-level CS_DIS voltage

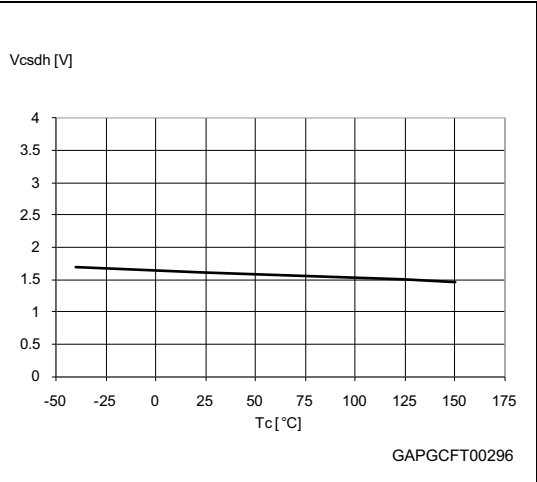


Figure 30. CS_DIS voltage clamp

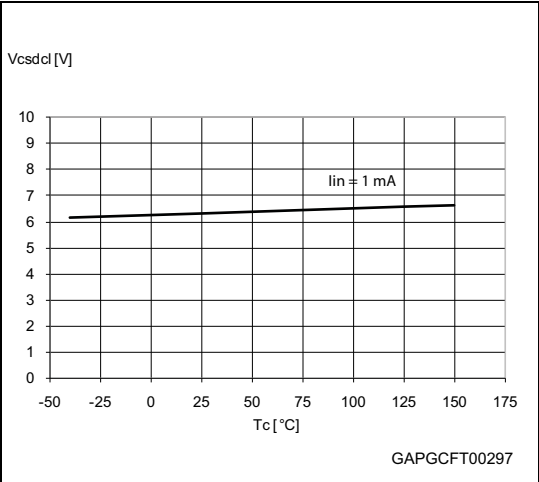
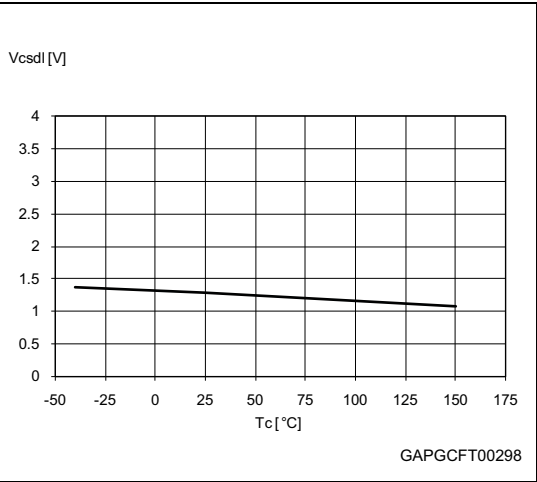
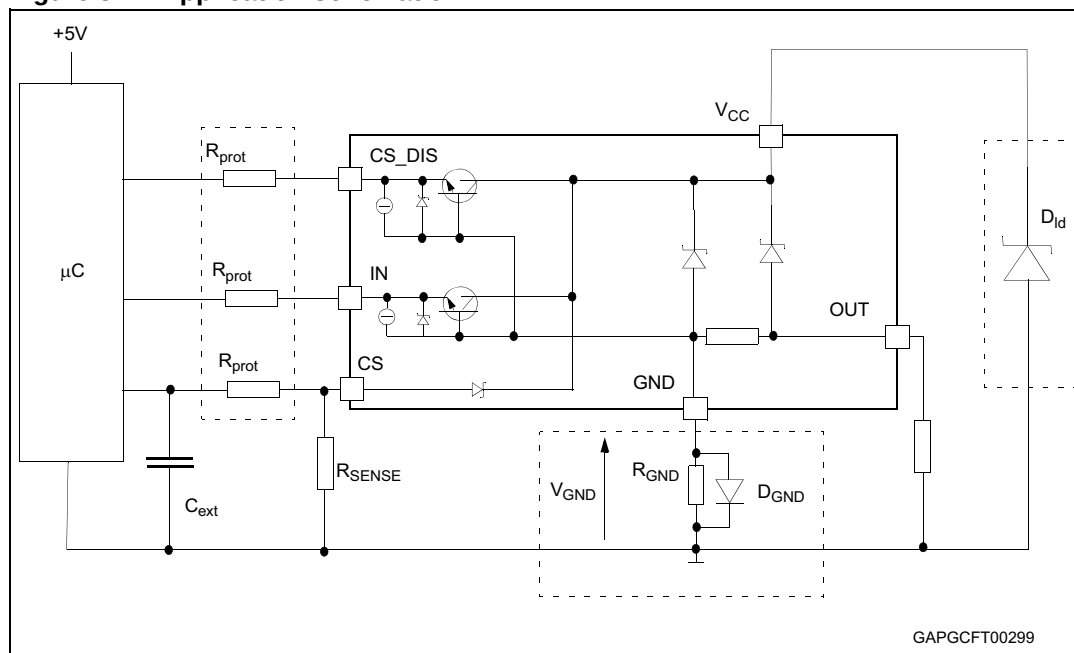


Figure 31. Low-level CS_DIS voltage



3 Application information

Figure 32. Application schematic



3.1 GND protection network against reverse battery

3.1.1 Solution 1: resistor in the ground line (R_{GND} only)

This can be used with any type of load.

The following is an indication on how to dimension the R_{GND} resistor.

1. $R_{GND} \leq 600 \text{ mV} / (I_{S(on)max})$.
2. $R_{GND} \geq (-V_{CC}) / (-I_{GND})$

where $-I_{GND}$ is the DC reverse ground pin current and can be found in the absolute maximum rating section of the device datasheet.

Power dissipation in R_{GND} (when $V_{CC} < 0$: during reverse battery situations) is:

Equation 1

$$P_D = (-V_{CC})^2 / R_{GND}$$

This resistor can be shared amongst several different HSDs. Please note that the value of this resistor should be calculated with formula (1) where $I_{S(on)max}$ becomes the sum of the maximum ON-state currents of the different devices.

Please note that if the microprocessor ground is not shared by the device ground then the R_{GND} produces a shift ($I_{S(on)max} * R_{GND}$) in the input thresholds and the status output

values. This shift varies depending on how many devices are ON in the case of several high-side drivers sharing the same R_{GND} .

If the calculated power dissipation leads to a large resistor or several devices have to share the same resistor then ST suggests to utilize Solution 2 (see [Section 3.1.2: Solution 2: a diode \(DGND\) in the ground line](#)).

3.1.2 Solution 2: a diode (D_{GND}) in the ground line

A resistor ($R_{GND} = 1\text{ k}\Omega$) should be inserted in parallel to D_{GND} if the device drives an inductive load.

This small signal diode can be safely shared amongst several different HSDs. Also in this case, the presence of the ground network produces a shift ($\approx 600\text{ mV}$) in the input threshold and in the status output values if the microprocessor ground is not common to the device ground. This shift not varies if more than one HSD shares the same diode/resistor network.

3.2 Load dump protection

D_{ld} is necessary (voltage transient suppressor) if the load dump peak voltage exceeds the V_{CC} max DC rating. The same applies if the device is subject to transients on the V_{CC} line that are greater than the ones shown in the ISO T/R 7637/1 table.

3.3 MCU I/Os protection

If a ground protection network is used and negative transients are present on the V_{CC} line, the control pins is pulled negative. ST suggests to insert a resistor (R_{prot}) in line to prevent the microcontroller I/O pins to latch-up.

The value of these resistors is a compromise between the leakage current of microcontroller and the current required by the HSD I/Os (input levels compatibility) with the latch-up limit of microcontroller I/Os.

Equation 2

$$-V_{CCpeak} / I_{latchup} \leq R_{prot} \leq (V_{OH\mu C} - V_{IH} - V_{GND}) / I_{IHmax}$$

Calculation example:

For $V_{CCpeak} = -100\text{ V}$, $I_{latchup} \geq 20\text{ mA}$, $V_{OH\mu C} \geq 4.5\text{ V}$

$$5\text{ k}\Omega \leq R_{prot} \leq 180\text{ k}\Omega.$$

Recommended values: $R_{prot} = 10\text{ k}\Omega$, $C_{EXT} = 10\text{ nF}$.

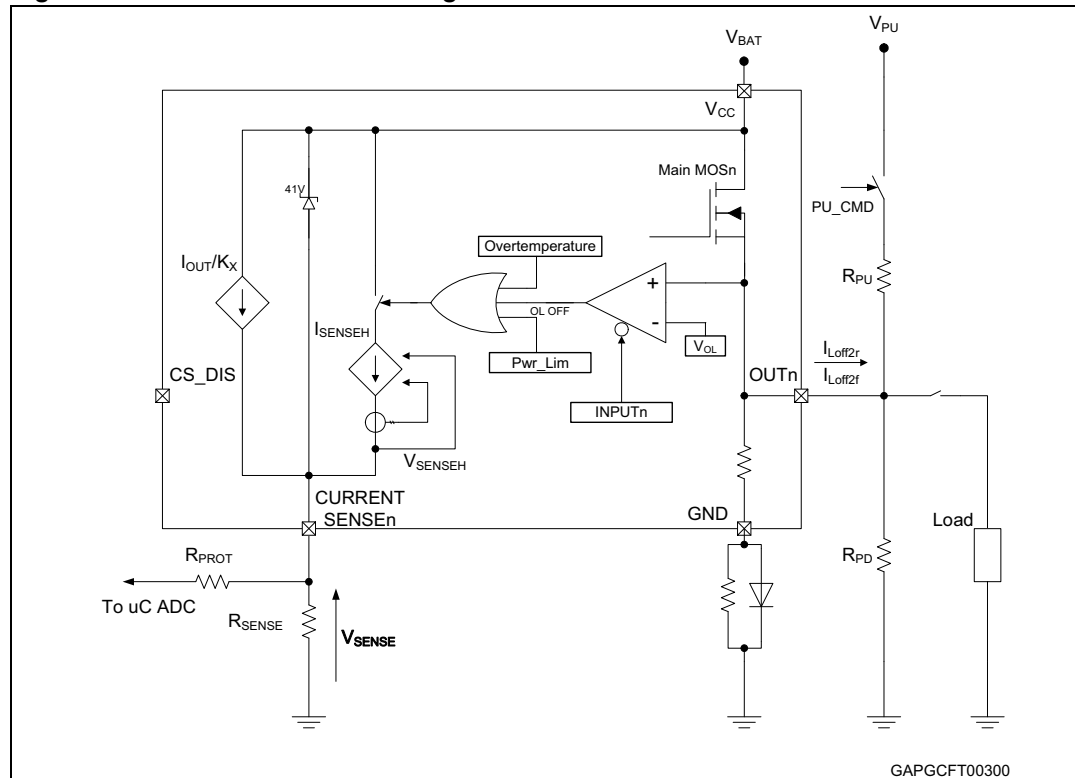
3.4 Current sense and diagnostic

The current sense pin performs a double function (see [Figure 33: Current sense and diagnostic](#)):

- **Current mirror of the load current in normal operation**, delivering a current proportional to the load one according to a known ratio K_X .
The current I_{SENSE} can be easily converted to a voltage V_{SENSE} by means of an external resistor R_{SENSE} . Linearity between I_{OUT} and V_{SENSE} is ensured up to 5 V minimum (see parameter V_{SENSE} in [Table 9: Current sense \(8 V < \$V_{CC}\$ < 18 V\)](#)). The current sense accuracy depends on the output current (refer to current sense electrical characteristics [Table 9: Current sense \(8 V < \$V_{CC}\$ < 18 V\)](#)).
- **Diagnostic flag in fault conditions**, delivering a fixed voltage V_{SENSEH} up to a maximum current I_{SENSEH} in case of the following fault conditions (refer to [Truth table](#)):
 - Power limitation activation
 - Overtemperature
 - Short to V_{CC} in OFF-state
 - Open-load in OFF-state with additional external components.

A logic high-level on CS_DIS pin sets at the same time all the current sense pins of the devices in a high-impedance-state, thus disabling the current monitoring and diagnostic detection. This feature allows multiplexing of the microcontroller analog inputs by sharing of sense resistance and ADC line among different devices.

Figure 33. Current sense and diagnostic



3.4.1 Short to V_{CC} and OFF-state open load detection

Short to V_{CC}

A short-circuit between V_{CC} and output is indicated by the relevant current sense pin set to V_{SENSEH} during the device OFF-state. Small or no current is delivered by the current sense during the ON-state depending on the nature of the short-circuit.

OFF-state open-load with external circuitry

Detection of an open-load in off-mode requires an external pull-up resistor R_{PU} connecting the output to a positive supply voltage V_{PU} .

It is preferable V_{PU} to be switched-off during the module standby-mode in order to avoid the overall standby current consumption to increase in normal conditions, i.e. when load is connected.

An external pull-down resistor R_{PD} connected between output and GND is mandatory to avoid misdetection in case of floating outputs in OFF-state (see [Figure 33: Current sense and diagnostic](#)).

R_{PD} must be selected in order to ensure $V_{OUT} < V_{OLmin}$ unless pulled up by the external circuitry:

Equation 3

$$V_{OUT|Pull-up_OFF} = R_{PD} \cdot I_{L(off2)f} < V_{OLmin} = 2\text{ V}$$

$R_{PD} \leq 22\text{ K}\Omega$ is recommended.

For proper open load detection in OFF-state, the external pull-up resistor must be selected according to the following formula:

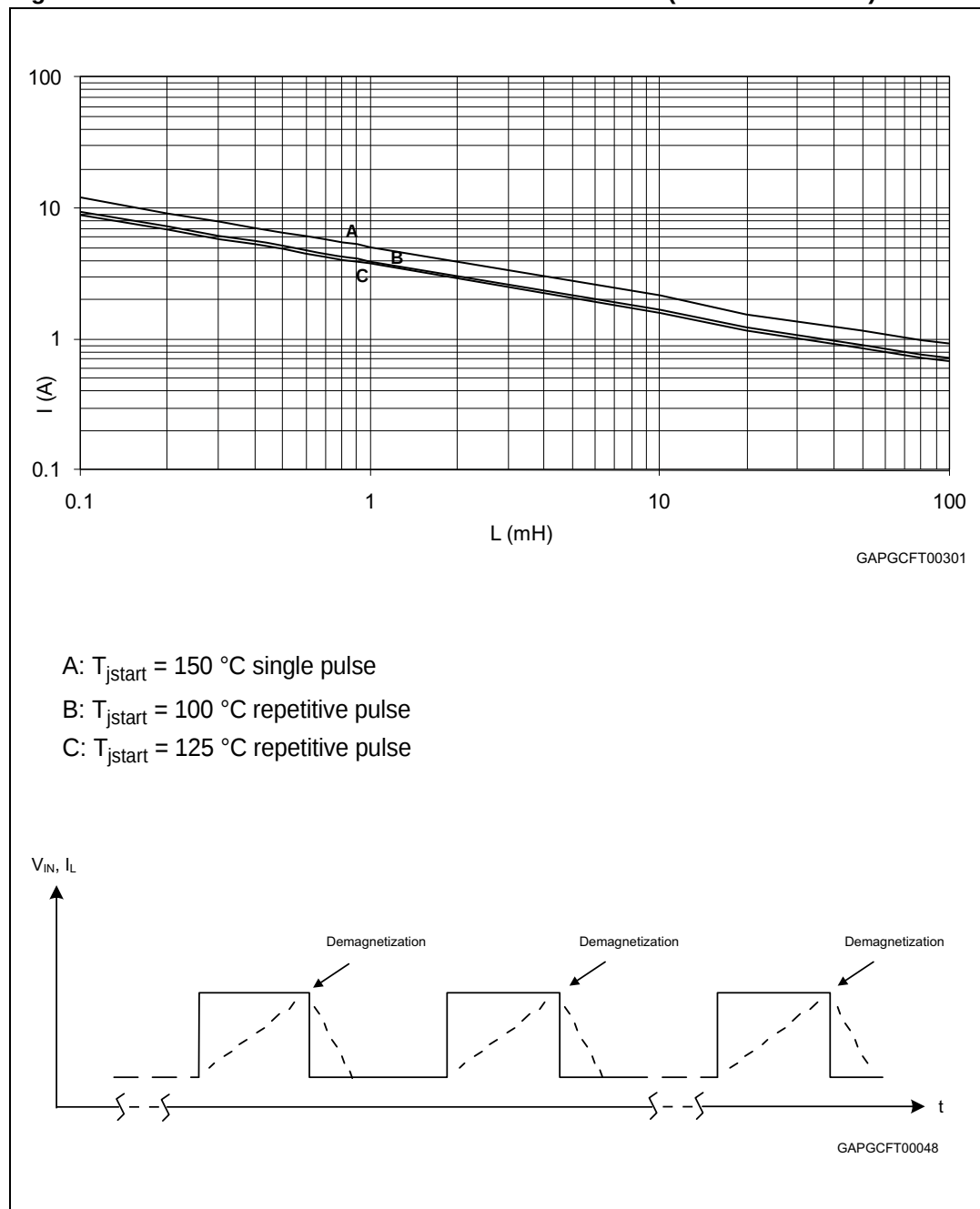
Equation 4

$$V_{OUT|Pull-up_ON} = \frac{(R_{PD} \cdot V_{PU}) - (R_{PU} \cdot R_{PD} \cdot I_{L(off2)r})}{(R_{PU} + R_{PD})} > V_{OLmax} = 4\text{ V}$$

For the values of V_{OLmin} , V_{OLmax} , $I_{L(off2)r}$ and $I_{L(off2)f}$ (see [Table 10: Openload detection \(8 V < \$V_{CC}\$ < 18 V\)](#)).

3.5 Maximum demagnetization energy ($V_{CC} = 13.5\text{ V}$)

Figure 34. Maximum turn-off current versus inductance (for each channel)⁽¹⁾



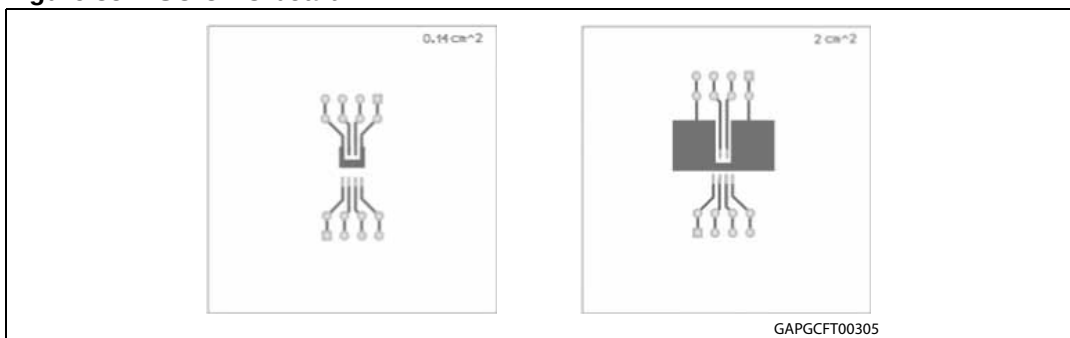
1. Values are generated with $R_L = 0\text{ }\Omega$.

In case of repetitive pulses, T_{jstart} (at beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves A and B.

4 Package and PCB thermal data

4.1 SO-8 thermal data

Figure 35. SO-8 PC board⁽¹⁾



1. Layout condition of R_{th} and Z_{th} measurements (PCB: FR4 area = 4.8 mm x 4.8 mm, PCB thickness = 2 mm, Cu thickness = 35 μ m, Copper areas: from minimum pad lay-out to 2 cm²).

Figure 36. $R_{thj-amb}$ vs PCB copper area in open box free air condition

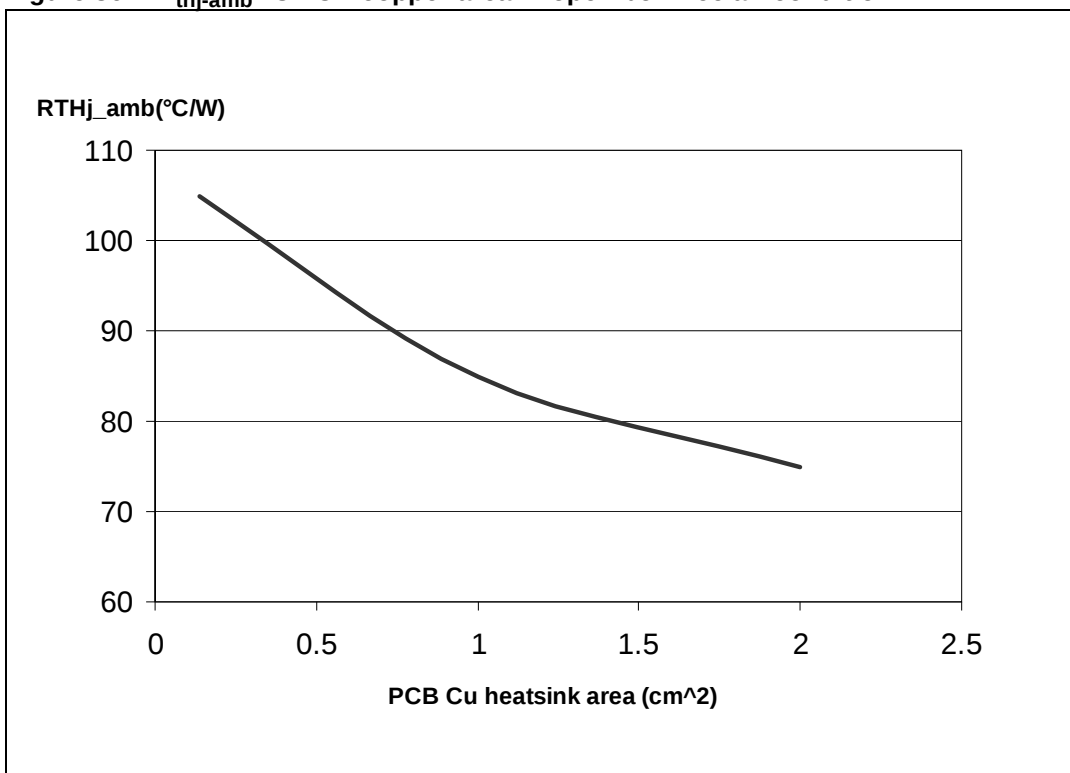
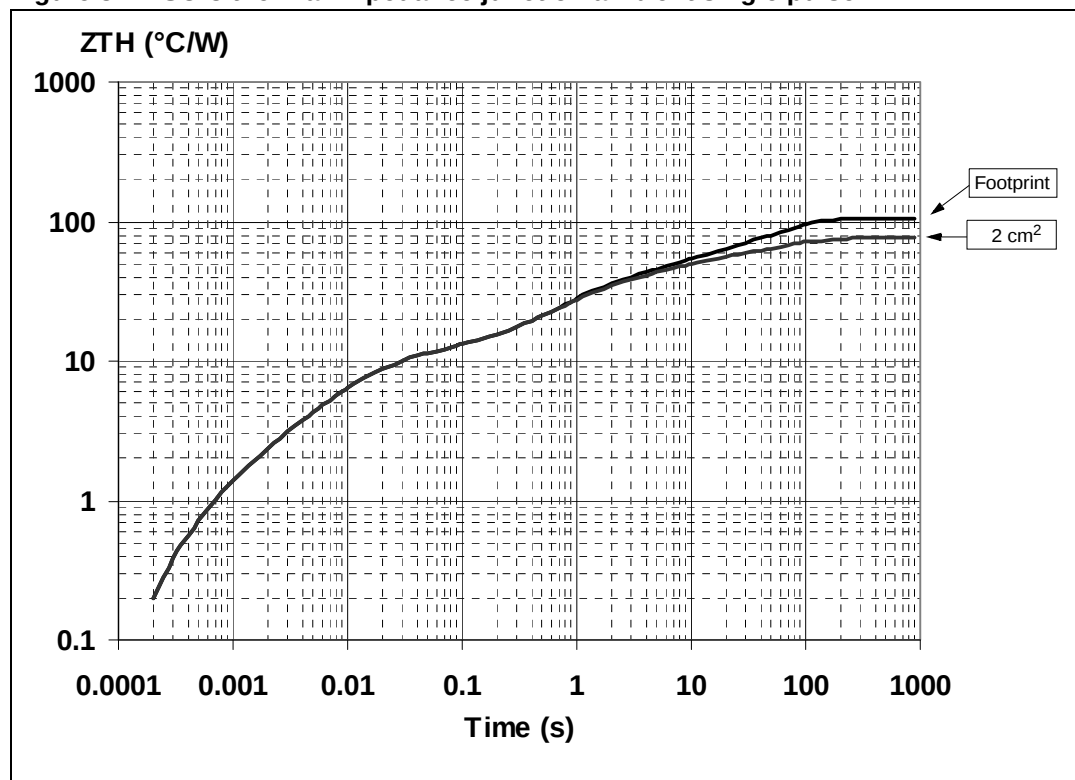


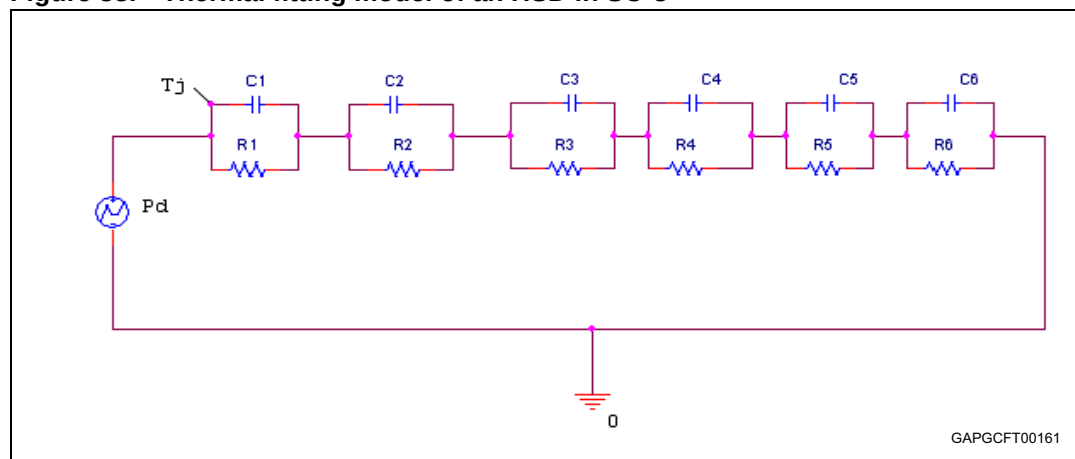
Figure 37. SO-8 thermal impedance junction ambient single pulse



Equation 5: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where $\delta = t_p/T$

Figure 38. Thermal fitting model of an HSD in SO-8⁽¹⁾

1. The fitting model is a simplified thermal tool and is valid for transient evolutions where the embedded protections (power limitation or thermal cycling during thermal shutdown) are not triggered.

Table 15. Thermal parameters

Arealisland (cm ²)	Footprint	2
R1 (°C/W)	1.2	
R2 (°C/W)	6	
R3 (°C/W)	3.5	
R4 (°C/W)	21	
R5 (°C/W)	16	
R6 (°C/W)	58	28
C1 (W.s/°C)	0.0008	
C2 (W.s/°C)	0.0016	
C3 (W.s/°C)	0.0075	
C4 (W.s/°C)	0.045	
C5 (W.s/°C)	0.35	
C6 (W.s/°C)	1.05	25

5 Package and packing information

5.1 ECOPACK®

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

5.2 Package mechanical data

Figure 39. SO-8 package dimensions

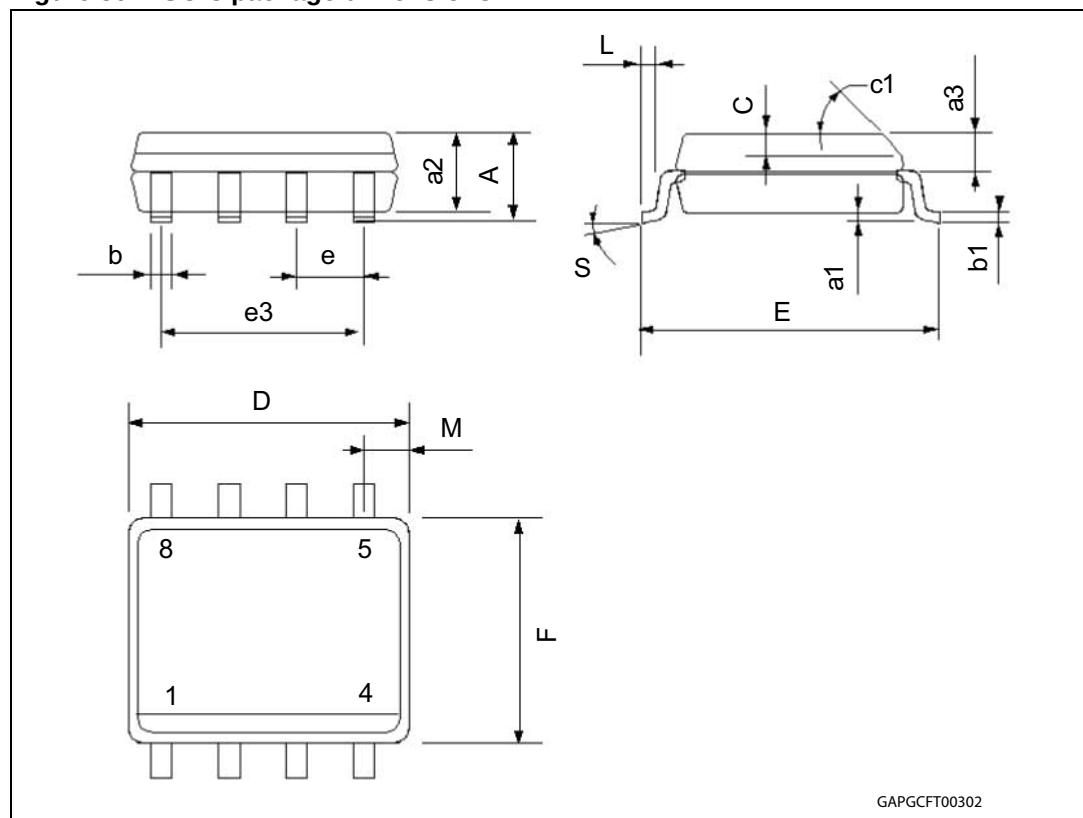


Table 16. SO-8 mechanical data

Dim.	mm.		
	Min.	Typ.	Max.
A			1.75
a1	0.1		0.25
a2			1.65
a3	0.65		0.85
b	0.35		0.48
b1	0.19		0.25
C	0.25		0.5
c1	45 (typ.)		
D	4.8		5
E	5.8		6.2
e		1.27	
e3		3.81	
F	3.8		4
L	0.4		1.27
M			0.6
S	8 (max.)		
L1	0.8		1.2

5.3 Packing information

Figure 40. SO-8 tube shipment (no suffix)

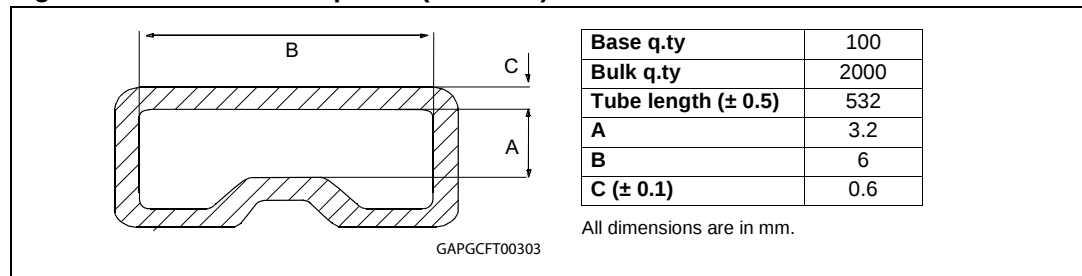
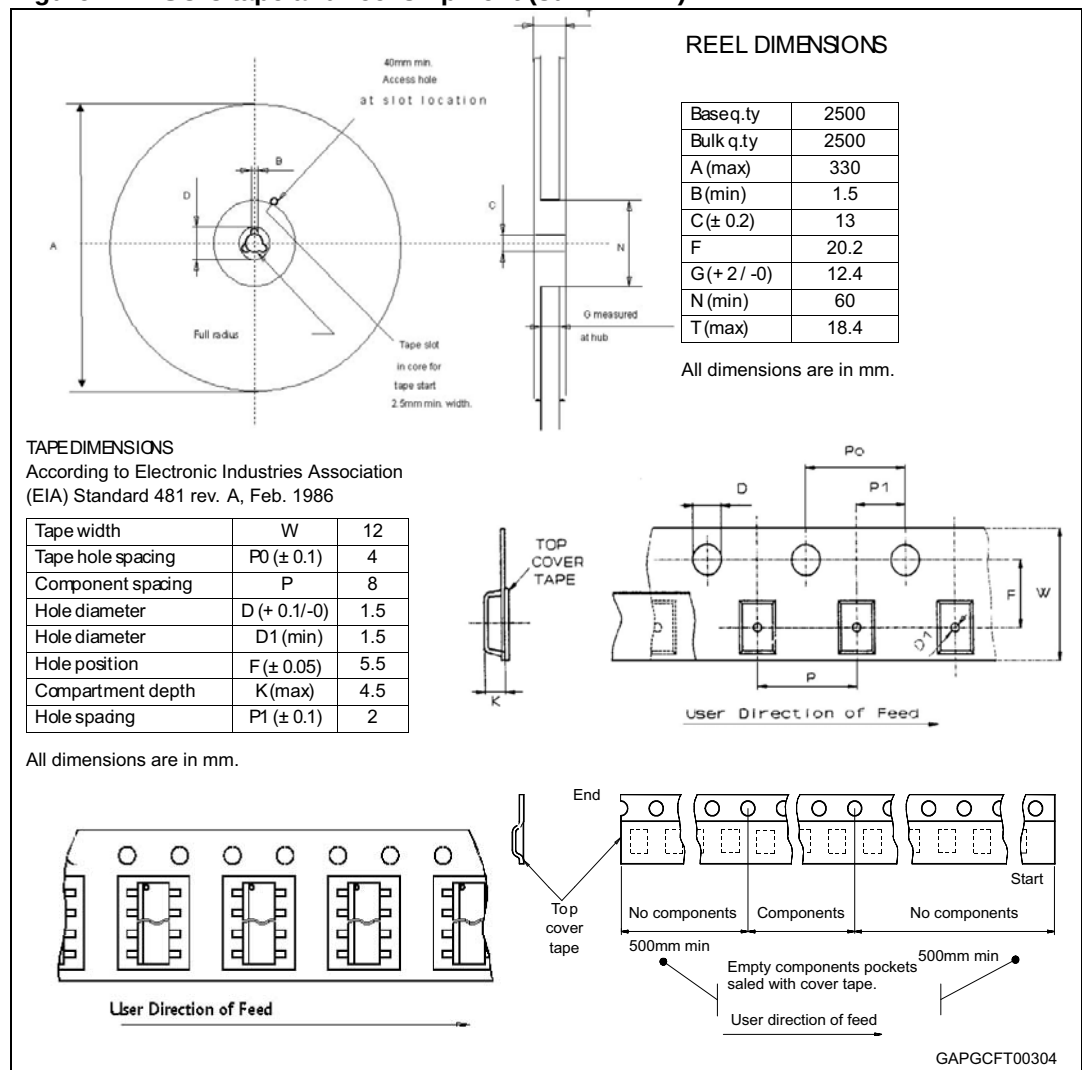


Figure 41. SO-8 tape and reel shipment (suffix "TR")



6 Order codes

Table 17. Device summary

Package	Order codes	
	Tube	Tape and reel
SO-8	VN5E160AS-E	VN5E160ASTR-E

7 Revision history

Table 18. Document revision history

Date	Revision	Changes
28-Apr-2009	1	Initial release.
25-Jan-2010	2	Updated Table 10: Openload detection ($8\text{ V} < V_{CC} < 18\text{ V}$) .
25-May-2011	3	Table 9: Current sense ($8\text{ V} < V_{CC} < 18\text{ V}$) : – t_{DSENSE2H} : updated typical and maximum values
18-Sep-2013	4	Updated Disclaimer.

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